TRANS-C5200/C5201
CompactPCI Rear Transition Modules

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

You must consider the possible negative effects of power, wiring, component, sensor, or software failure in the design of any type of control or monitoring system. This is very important where property loss or human life is involved. It is important that you perform satisfactory overall system design and it is agreed between you and Acromag, that this is your responsibility.

1.0 General Information

2.0 Preparation For Use

3.0 Service and Repair

4.0 Specifications

APPENDIX

1.0 GENERAL INFORMATION

The TRANS-C5200 and TRANS-C5201 are rear transition modules for Acromag's ACPC4620E/CC CompactPCI carrier cards. The modules are available for use in card cages which provide rear exit for I/O connections via 80 mm wide transition modules (transition modules can only be used in card cages specifically designed for them). They are double-height (6U), single-slot module and adheres to the CompactPCI mechanical dimensions and IEEE Standard (1101.11-1998), with a printed circuit board depth of 80mm, which is a standard transition module depth. These boards are designed to be used with the PMC-LX/SX and PMC-VLX/VSX/VFX Reprogrammable FPGA modules. The TRANS-C5200 converts the 2.5V Rear I/O signals to 64 5V/3.3V selectable Open-drain I/O. The TRANS-C5201 coverts the 2.5 Rear I/O signals to 32 RS485/RS422 I/O.

Table 1.1: *CompactPCI Rear I/O Transition modules.*

Board (Size)	Description
TRANS-4610 (3U)	Pass through
TRANS-4620 (6U)	Pass through
TRANS-C5200 (6U)	64 5V/3.3V selectable open-drain I/O
TRANS-C5201 (6U)	32 RS485/RS22 I/O

FIELD I/O CONNECTORS

The TRANS modules connections are made to Acromag ACPC4620E/CC carrier field I/O connections through the rear via J3 and J5 for two PMC mezzanine I/O module cards (Slot A & Slot B). Power is also provided through these connectors. Refer to the AcPC4620E/CC User's Manual for further information on the J3/J5 connectors.

The Field I/O Connections are made via two 68 pin SCSI connectors, one for each PMC module. Table 1.2 indicates the pin assignments for the Field I/O signal mapping of the TRANS-C5200 digital transition board. Table 1.3 indicates the pin assignments for the Field I/O signal mapping of the TRANS-C5201 differential transition board. The SCSI 68 Field I/O pin-out is the same for both PMC Slot A and PMC Slot B.

FIELD I/O CONNECTORS

***Table 1.2: TRANS-C5200 DIGITAL** Board Field I/O Pin Connections*

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	35
Digital Channel 0	2	Digital Channel 1	36
Digital Channel 2	3	Digital Channel 3	37
Digital Channel 4	4	Digital Channel 5	38
Digital Channel 6	5	Digital Channel 7	39
Digital Channel 8	6	Digital Channel 9	40
Digital Channel 10	7	Digital Channel 11	41
Digital Channel 12	8	Digital Channel 13	42
Digital Channel 14	9	Digital Channel 15	43
Digital Channel 16	10	Digital Channel 17	44
Digital Channel 18	11	Digital Channel 19	45
Digital Channel 20	12	Digital Channel 21	46
Digital Channel 22	13	Digital Channel 23	47
Digital Channel 24	14	Digital Channel 25	48
Digital Channel 26	15	Digital Channel 27	49
Digital Channel 28	16	Digital Channel 29	50
Digital Channel 30	17	Digital Channel 31	51
Digital Channel 32	18	Digital Channel 33	52
Digital Channel 34	19	Digital Channel 35	53
Digital Channel 36	20	Digital Channel 37	54
Digital Channel 38	21	Digital Channel 39	55
Digital Channel 40	22	Digital Channel 41	56
Digital Channel 42	23	Digital Channel 43	57
Digital Channel 44	24	Digital Channel 45	58
Digital Channel 46	25	Digital Channel 47	59
Digital Channel 48	26	Digital Channel 49	60
Digital Channel 50	27	Digital Channel 51	61
Digital Channel 52	28	Digital Channel 53	62
Digital Channel 54	29	Digital Channel 55	63
Digital Channel 56	30	Digital Channel 57	64
Digital Channel 58	31	Digital Channel 59	65
Digital Channel 60	32	Digital Channel 61	66
Digital Channel 62	33	Digital Channel 63	67
COMMON	34	COMMON	68

FIELD I/O CONNECTORS

SCSI-3 68-Pin Female Connector			
Pin Description	**Pin**	**Pin Description**	**Pin**
COMMON	1	COMMON	35
Differential Ch0+	2	Differential Ch0-	36
Differential Ch1+	3	Differential Ch1-	37
Differential Ch2+	4	Differential Ch2-	38
Differential Ch3+	5	Differential Ch3-	39
Differential Ch4+	6	Differential Ch4-	40
Differential Ch5+	7	Differential Ch5-	41
Differential Ch6+	8	Differential Ch6-	42
Differential Ch7+	9	Differential Ch7-	43
Differential Ch8+	10	Differential Ch8-	44
Differential Ch9+	11	Differential Ch9-	45
Differential Ch10+	12	Differential Ch10-	46
Differential Ch11+	13	Differential Ch11-	47
Differential Ch12+	14	Differential Ch12-	48
Differential Ch13+	15	Differential Ch13-	49
Differential Ch14+	16	Differential Ch14-	50
Differential Ch15+	17	Differential Ch15-	51
Differential Ch16+	18	Differential Ch16-	52
Differential Ch17+	19	Differential Ch17-	53
Differential Ch18+	20	Differential Ch18-	54
Differential Ch19+	21	Differential Ch19-	55
Differential Ch20+	22	Differential Ch20-	56
Differential Ch21+	23	Differential Ch21-	57
Differential Ch22+	24	Differential Ch22-	58
Differential Ch23+	25	Differential Ch23-	59
Differential Ch24+	26	Differential Ch24-	60
Differential Ch25+	27	Differential Ch25-	61
Differential Ch26+	28	Differential Ch26-	62
Differential Ch27+	29	Differential Ch27-	63
Differential Ch28+	30	Differential Ch28-	64
Differential Ch29+	31	Differential Ch29-	65
Differential Ch30+	32	Differential Ch30-	66
Differential Ch31+	33	Differential Ch31-	67
COMMON	34	COMMON	68

***Table 1.3: TRANS-C5201 DIFFERENTIAL** Board Field I/O Pin Connections*

RESISTOR/JUMPER CONFIGURATIONS

The TRANS-C5200 module has socketed resistors for the single ended open-drain pull-ups. There are also jumpers for selecting either 5V or 3.3V power supply for the pull-ups. The socketed resistors are 9 pin bussed SIP resistors (pin 1 common). When placed on the board, pin 1 of the SIP resistors must be orientated properly as noted by the pin 1 indicator on the board. Refer to table 1.4 to correlate the resistors and jumpers for each channel grouping.

Table 1.4: TRANS-C5200 Socketed 680 Ohm 5V/3.3V Selectable Pull-up Resistors/Jumpers.

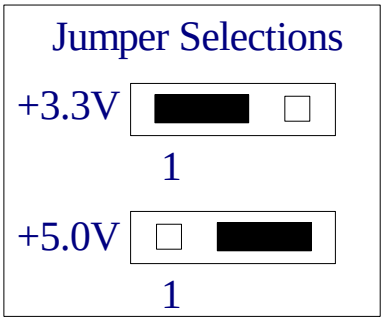
Resistor and Jumper locations are marked on the board.

TRANS-C5200	PMC SLOT A	PMC SLOT B
Ch. 0-7	R6/J6	R14/J14
Ch. 8-15	R7/J7	R15/J15
Ch. 16-23	R8/J8	R16/J16
Ch. 24-31	R9/J9	R17/J17
Ch. 32-39	R10/J10	R18/J18
Ch. 40-47	R11/J11	R19/J19
Ch. 48-55	R12/J12	R20/J20
Ch. 56-63	R13/J13	R21/J21

Figure 1.1 displays the jumper settings from the TRANS-C5200 modules. Pin 1 is indicated on the module. Note that a jumper MUST BE PRESESNT for each group of eight channels. If no jumper is present, then an external pull-up is required for the open drain I/O.

Figure 1.1: TRANS-C5200 Jumper Settings

All jumpers are set to 5V at the factory.



The TRANS-C5201 module has socketed resistors for the RS485/RS422 120 Ohm termination resistors. The socketed resistors are 8 pin isolated network SIP resistors. Since the SIP resistors contain 4 isolated resistors, the polarity indicators are not required. Refer to table 1.5 to correlate the resistors for each channel grouping. Acromag recommends that termination resistors are present for any Field input.

Table 1.5: TRANS-C5201 Socketed 120 Ohm Differential Termination Resistors.

Resistor locations are marked on the board.

TRANS-C5201	PMC SLOT A	PMC SLOT B
Ch. 0-3	R1	R9
Ch. 4-7	R2	R10
Ch. 8-11	R3	R11
Ch. 12-15	R4	R12
Ch. 16-19	R5	R13
Ch. 20-23	R6	R14
Ch. 24-27	R7	R15
Ch. 28-31	R8	R16

VHDL INTERFACE

The TRANS-C5200 and TRANS-C5201 boards are designed to be used in conjunction with Acromag's PMC-LX/SX & PMC-VLX/VSX/VFX models. The Engineering Design Kit (EDK) for each product does not support the proper interface for either the TRANS-C5200 or TRANS-C5201. The EDK currently defines the PMC Rear I/O as LVDS I/O. Both of these boards required that the Rear I/O on the PMC modules be redefined to 2.5V CMOS. The Pin-out table provided in the Appendix at the end of this manual links the FPGA connections to the functionality of both of these boards.

The TRANS-C5200 model requires a tri-state interface between the FPGA and the TRANS-C5200. This allows for bi-directional communication without the requirement for a direction control signal. Each I/O point can be either inferred using process statements or use the IOBUF Xilinx primitive. Note that the IOSTANDARD=LVCMOS25 must be assigned to every pin in the ucf file. An example 3-state process VHDL statement is below.

Example VHDL for TRANS-C5200

RIO_DATA0	Top level I/O point
RIO_DIR0	Direction control where output = 1
DATA0_OUT	Output from FPGA logic
DATA0_IN	Input to FPGA logic

```
process(DATA0_OUT, RIO_DIR0)  --3 state output
  begin
  if(RIO_DIR0  = '1' and DATA0_OUT = '0') then
    RIO_DATA0 <= '0';
   else
    RIO_DATA0 <=  'Z';
  end if;
end process;

DATA0_IN <= RIO_DATA0; --Input signal requires debounce
```

Note that due to the slow rising time of the signal (greater then 125nS), debounce is required for each input. Debounce will filter out any incidental transition caused by the slow rise time of the input signal. Example debounce VHDL is available upon request.

VHDL INTERFACE

Example VHDL for TRANS-C5201

The TRANS-C5201 interface uses one directional control signal and one I/O bit for each RS485/RS422 I/O signal. Each I/O point can be either inferred using process statements or use the OBUF Xilinx primitive for the direction lines and the IOBUF Xilinx primitive for I/O lines. Note that the IOSTANDARD=LVCMOS25 must be assigned to every pin in the ucf file. An example VHDL statement is below. A direction control output of logic high "1" will set the corresponding differential signal as an output. A direction control output of logic low "0" will set the corresponding differential signal as an input.

RIO_DATA0	Top level I/O point
DATA0_OUT	Output from FPGA logic
DATA0_IN	Input to FPGA logic
RIO_DIR0	Direction control where output = 1

```
process(DATA0_OUT, RIO_DIR0)  --3 state output
  begin
  if(RIO_DIR0  = '1') then
    RIO_DATA0 <= DATA0_OUT;
   else
    RIO_DATA0 <=  'Z';
  end if;
end process;

DATA0_IN  <= RIO_DATA0;
```

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

WARNING: This board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the system boards, plus the installed Acromag board, within the voltage tolerances specified.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

IMPORTANT: *Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.*

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the CompactPCI bus and PMC module grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 SERVICE AND REPAIR

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

SERVICE AND REPAIR ASSISTANCE

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier/CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

www.acromag.com

Choose the "Support" hyperlink in our website's top navigation row then select "Embedded Board Products Support" or go to http://www.acromag.com/subb_support.cfm to access:

- Application Notes
- Frequently Asked Questions (FAQ's)
- Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can be submitted from within the Knowledge Base or through the "Contact Us" hyperlink at the top of any web page.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed at the bottom of this page. When needed, complete repair services are also available.

4.0 SPECIFICATIONS

PHYSICAL

Physical Configuration	6U CompactPCI Rear Transition Board
Height	9.187 inches (233.35 mm)
Depth	3.150 inches (80.0 mm)
Board Thickness	0.063 inches (1.60 mm)
Unit Weight	
Model TRANS-C5200	TBD pounds (TBD Kg)
Model TRANS-C5201	TBD pounds (TBD Kg)

Connectors

J3, J5 (CompactPCI Rear I/O)	PMC on CompactPCI Specification PICMG 2.3 R1.0. Utilizes Type "B" right-angle female connector, 110 contacts with upper shield.
P1, P2 (Field I/O)	68-pin, SCSI-3, female receptacle header (AMP 787082-7 or equivalent)

ENVIRONMENTAL

Operating Temperature: -40 to 85°C
Relative Humidity: 5-95% Non-Condensing.
Storage Temperature: -55°C to 100°C.

Also, designed to meet the following environmental standards per ANSI/VITA47-2005(R2007).

- Environmental Class EAC6
- Operating Temperature: AC3 (-40 to 70°C)
- Vibration Class: V2
- Shock 20g

Non-Isolated: CompactPCI and field commons have a direct electrical connection.

POWER REQUIREMENTS

TRANS-C5200

3.3 VDC (±5%)[1]	Typical TBD mA	Max. TBD mA
5.0 VDC (±5%)[1]	Typical TBD mA	Max. TBD mA

TRANS-C5201

3.3 VDC (±5%)[1]	Typical TBD mA	Max. TBD mA
5.0 VDC (±5%)[1]	Not Used	

1. Note that all power is drawn from the AcPC4620CC/E Carrier board.

TRANS-C5200 DIGITAL I/O

OPEN DRAIN Channel Configuration: 2 PMC sites each with 64 Channels of open drain I/O. Note that the open drain architecture does not require direction control.

Reset/Power Up Condition: All Digital Channels Default to a high impedance state.

Pull-up Resistors: 680Ω Socketed bussed SIP pull-up resistors are installed in banks of 8. (Channels 0-7, 8-15, etc.) With SIP removed a nominal 47.5KΩ pull-up are always present. Each bank of eight can be selectively pulled up to either 3.3V or 5V via a jumper.

OPEN DRAIN Digital I/O DC Electrical Characteristics

- Digital I/O DC Electrical Characteristics w. 680Ω Pull-ups
- Input Voltage Range: -0.25V to 3.55V (3.3Vterm) or -0.25V to 5.25V (5.0Vterm)
- V_{IH}: 2.2V minimum
- V_{IL}: 0.8V maximum
- V_{OH}: 3.1V typical (3.3V pull-up)
- V_{OH}: 4.8V typical (5.0V pull-up)
- V_{OL}: 0.3V typical (0.4V max @ 12mA)
- Turn On Time (to logic low): 125nS Typical
- Turn Off Time (390Ω pull-ups) 500nS Typical

TRANS-C5201 DIFFERENTIAL I/O

Channel Configuration: 2 PMC sites each with 32 channels of Bi-directional EIA 485/422 I/O. Differential signals are independently direction controlled.

EIA 485/422 Differential I/O Electrical Characteristics

- 1.5 V Min., 3.3V Max.: Differential Driver Output Voltage with 54Ω load.
- 3 V Max.: Common Mode Output Voltage.
- -0.2 Min to -0.05 Max: Differential Input Threshold Voltage $-7V \le V_{CM} \le 12V$
- 15mV Typical: Input Hysteresis
- 96KΩ Minimum Input Resistance

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating) or shorted.

Differential Propagation Delay

- Driver Input to Output Delay = 27ns Typical, 40ns Maximum
- Receiver Input to Output Delay = 33ns Typical, 60ns Maximum

Termination Resistors

Termination Resistors: 120 Ohm socketed SIP termination resistors in groups of 4. (Channels 0-3, 4-7, etc.)

LX/SX & VLX/VSX/VFX Sch. Signal	V4 Pin #	V5 Pin #	TRANS-C5200 Schematic Signal	TRANS-C5201 Schematic Signal
RP_IO0	G18	L21	DATA00	DIR00
RN_IO1	G17	L20	DATA01	DIR01
RP_IO2	F20	J22	DATA02	DIR02
RN_IO3	E20	K21	DATA03	DIR03
RP_IO4	H24	K23	DATA04	DIR04
RN_IO5	H23	K22	DATA05	DIR05
RP_IO6	E21	G23	DATA06	DIR06
RN_IO7	D21	H23	DATA07	DIR07
RP_IO8	G24	AC28	DATA08	DIR08
RN_IO9	G23	AD27	DATA09	DIR09
RP_IO10	F24	AE27	DATA10	DIR10
RN_IO11	F23	AE26	DATA11	DIR11
RP_IO12	H22	AB28	DATA12	DIR12
RN_IO13	H21	AA28	DATA13	DIR13
RP_IO14	H20	AB25	DATA14	DIR14
RN_IO15	G20	AB26	DATA15	DIR15
RP_IO16	G26	AB27	DATA16	DIR16
RN_IO17	G25	AC27	DATA17	DIR17
RP_IO18	H26	AC25	DATA18	DIR18
RN_IO19	H25	AC24	DATA19	DIR19
RP_IO20	F26	AA25	DATA20	DIR20
RN_IO21	E26	AA26	DATA21	DIR21
RP_IO22	E25	AD24	DATA22	DIR22
RN_IO23	E24	AE24	DATA23	DIR23
RP_IO24	A22	Y24	DATA24	DIR24
RN_IO25	A21	AA24	DATA25	DIR25
RP_IO26	B24	AG18	DATA26	DIR26
RN_IO27	B23	AF19	DATA27	DIR27
RP_IO28	B18	AD26	DATA28	DIR28
RN_IO29	A18	AD25	DATA29	DIR29
RP_IO30	D26	AH14	DATA30	DIR30
RN_IO31	D25	AH13	DATA31	DIR31
RP_IO32	D22	AH12	DATA32	DATA00
RN_IO33	C22	AG13	DATA33	DATA01
RP_IO34	C19	AH17	DATA34	DATA02
RN_IO35	D18	AG16	DATA35	DATA03
RP_IO36	C21	AH15	DATA36	DATA04
RN_IO37	B21	AG15	DATA37	DATA05
RP_IO38	C26	AH18	DATA38	DATA06
RN_IO39	C25	AG17	DATA39	DATA07
RP_IO40	A20	AG22	DATA40	DATA08
RN_IO41	A19	AH22	DATA41	DATA09
RP_IO42	E23	AH20	DATA42	DATA10
RN_IO43	E22	AH19	DATA43	DATA11
RP_IO44	G19	AG27	DATA44	DATA12

APPENDIX

PMC LX/SX & PMC VLX/VSX/VFX Pin-out Table Continued

This table links the TRANS-C520x modules to the PMC-LX/SX & PMC-VLX/VSX/VFX.

The LX/SX & VLX/VSX/VFX Schematic Signal column corresponds to the signal name of that pin on the PMC-LX/SX schematic or PMC-VLX/VSX/VFX that was provided in the EDK.

The V4 Pin # column represents the pin number of the Virtex 4 FPGA that is routed to the Rear I/O. Note that to support these transitions modules the Rear I/O signals must be defined as 2.5V CMOS.

The V5 Pin # column represents the pin number of the Virtex 5 FPGA that is routed to the Rear I/O. Note that to support these transitions modules the Rear I/O signals must be defined as 2.5V CMOS.

The TRANS-C5200 Schematic signal column corresponds to the signal name of that pin on the TRANS-C5200 schematic. Note that the numerical value following DATA correlate directly to the Open Drain I/O on the 68-pin I/O connector.

The TRANS-C5201 Schematic signal column corresponds to the signal name of that pin on the TRANS-C5201 schematic. Note that the numerical value following DATA correlate directly to the RS485/RS422 channel number on the 68-pin I/O connector. A direction control value of 1 sets the channel as an output. A direction control value of 0 sets the channel as an input.

PMC LX/SX & PMC VLX/VSX/VFX Pin-out Table Continued

LX/SX & VLX/VSX/VFX Sch. Signal	V4 Pin #	V5 Pin #	TRANS-C5200 Schematic Signal	TRANS-C5201 Schematic Signal
RN_IO45	F19	AG26	DATA45	DATA13
RP_IO46	A24	AF24	DATA46	DATA14
RN_IO47	A23	AG25	DATA47	DATA15
RP_IO48	F18	AJ25	DATA48	DATA16
RN_IO49	E18	AH25	DATA49	DATA17
RP_IO50	D24	AF25	DATA50	DATA18
RN_IO51	C24	AF26	DATA51	DATA19
RP_IO52	C17	AH27	DATA52	DATA20
RN_IO53	D17	AJ26	DATA53	DATA21
RP_IO54	D23	AK26	DATA54	DATA22
RN_IO55	C23	AJ27	DATA55	DATA23
RP_IO56	E17	AK29	DATA56	DATA24
RN_IO57	F17	AJ29	DATA57	DATA25
RP_IO58	D20	AK28	DATA58	DATA26
RN_IO59	D19	AK27	DATA59	DATA27
RP_IO60	H4	AE28	DATA60	DATA28
RN_IO61	H3	AF28	DATA61	DATA29
RP_IO62	C20	AG28	DATA62	DATA30
RN_IO63	B20	AH28	DATA63	DATA31

Certificate of Volatility				
Acromag Model: TRANS-C5200 TRANS-C5201	Manufacturer: Acromag, Inc. 30765 Wixom Rd Wixom, MI 48393			
Volatile Memory				
Does this product contain Volatile memory (i.e. Memory of whose contents are lost when power is removed) □ Yes ■ No				
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type (SRAM, SDRAM, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Non-Volatile Memory				
Does this product contain Non-Volatile memory (i.e. Memory of whose contents is retained when power is removed) □ Yes ■ No				
Type(EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize:
Type(EEPROM, Flash, etc.)	Size:	User Modifiable □ Yes □ No	Function:	Process to Sanitize: