AMC335

Four-Port WAN Communications
AdvancedMC™ Module

Hardware Manual

Performance Technologies
205 Indigo Creek Drive
Rochester, NY 14626 USA
585.256.0248
support@pt.com

www.pt.com

PERFORMANCE TECHNOLOGIES

Document Revision History

Part Number	Date	Explanation of Changes
126p0694.10	October 21, 2008	Initial Release
126p0694.11	March 19, 2009	Added caution about product handling in Product Safety Information.
126p0694.12	June 17, 2009	Standardized Module Management Controller. Corrected board height specification on page 109.
126p0694.13	October 2, 2009	AMC335 has passed certifications testing; updated Chapter 9, "Agency Approvals" accordingly. Replaced Figure 2-2.
126p0694.15	November 20, 2009	Added note about FCLKA on page 36 and page 102.

Copyright Notice

Errors and Omissions

Although diligent efforts are made to supply accurate technical information to the user, occasionally errors and omissions occur in manuals of this type. Refer to the Performance Technologies, Inc. Web site to obtain manual revisions or current customer information:

http://www.pt.com.

Performance Technologies, Inc., reserves its right to change product specifications without notice.

Symbol Conventions

The following symbols appear in this document:

Caution:

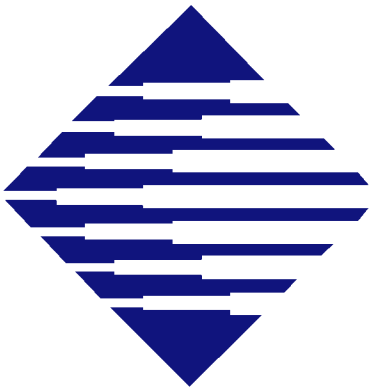
There is risk of equipment damage. Follow the instructions.

Warning:

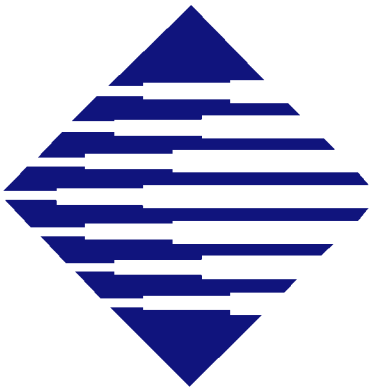
Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Caution:

Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. We recommended using anti-static groundig straps and anti-static mats when installing the board in a system to help prevent damage due to electrostatic discharge.



Contents



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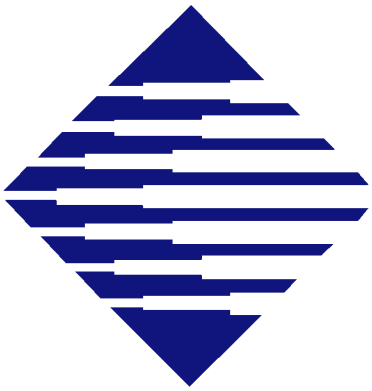
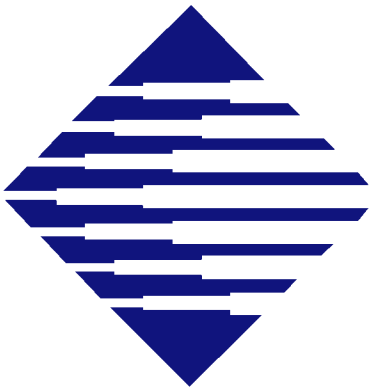


Figures



Chapter

1

About This Guide

Overview

This manual describes the hardware-specific functionality and usage of the Performance Technologies' AMC335 Four-Port WAN Communications AdvancedMC™ (AMC) module.

In these chapters you will find installation and configuration information, plus a functional block description intended for the application developer of this board. Here is a brief description of what you will find in this manual:

Chapter 1, "About This Guide," on page 13, this chapter, provides links to all chapters in this guide, plus text conventions, customer support and services, and product warranty information for the AMC335.

Chapter 2, "Introduction," on page 17 provides an overview of the AMC335 and includes information such as module features, front panel details, functional block diagram with a brief description of each block, and descriptions of software such as the supported operating systems and Intelligent Platform Management Interface (IPMI).

Chapter 3, "Getting Started," on page 35 provides setup information and includes information such as unpacking the AMC335, system requirements, configuration and installation.

Chapter 4, "System Monitoring and Alarms," on page 45 describes the commands supported by the on-board Module Management Controller (MMC), sensor thresholds, serial interface subsystem, and firmware upgrade process.

Chapter 5, "Connectors," on page 69 provides connector location, description, pinout, and cabling information for the AMC335.

Chapter 6, "MPC8270 Parallel I/O Ports," on page 95 provides information about the two general-purpose serial management controllers and the four general-purpose parallel I/O ports on the AMC335.

Chapter 7, “Reset,” on page 101 describes the AMC335 reset types with their respective sources.

Chapter 8, “Specifications,” on page 107 contains electrical, environmental, and mechanical specifications as well as reliability data.

Chapter 9, “Agency Approvals,” on page 111 presents agency approvals and certification information.

Chapter 10, “Data Sheet Reference,” on page 117 provides information on data sheets, devices, standards, specifications, and documentation for the technology designed into the AMC335.

An “Index,” on page 121 is also provided.

The AMC335 assembly should be used in conjunction with the Performance Technologies software package that you have chosen, for example NexusWare® Core.

The most current documentation to support the additional components that you purchased from Performance Technologies is available at http://www.pt.com under the product you are inquiring about.

Text Conventions

This guide uses the following text conventions:

Convention	Used For
`Monospace font`	Monospace font represents sample code
Bold font	Bold font represents: • Paths • File names • UNIX commands • User input
Italic font	Italic font represents: • Notes that supply useful advice • Supplemental information • Referenced documents

Customer Support and Services

Performance Technologies offers a variety of standard and custom support packages to ensure customers have access to the critical resources that they need to protect and maximize hardware and software investments throughout the development, integration, and deployment phases of the product life cycle.

If you encounter difficulty in using this Performance Technologies, Inc. product, you may contact our support personnel by:

1. **EMAIL** (Preferred Method) – Email us at the addresses listed below or use our online email support form. Outline your problem in detail. Please include your return email address and a telephone number.
2. **TELEPHONE** – Contact us via telephone at the number listed below, and request Technical Support. Our offices are open Monday to Friday, 8:00 a.m. to 8:00 p.m. (Eastern Time).

Performance Technologies Support Contact Information

	Embedded Systems and Software (Includes Platforms, Blades, and Servers)	SS7 Systems (Includes SEGway™)
Email	support@pt.com	ss7support@pt.com
Phone	+1 (585) 256-0248 (Monday to Friday, 8 a.m. to 8 p.m. Eastern Time)	+1 (585) 256-0248 (Monday to Friday, 8 a.m. to 8 p.m. Eastern Time)

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Other Web Support

Support for existing products including manuals, release notes, and drivers can be found on specific product pages at http://www.pt.com. Use the product search to locate the information you need.

Return Merchandise Authorization (RMA)

To submit a return merchandise authorization (RMA) request, complete the online RMA form available at http://pt.com/assets/lib/files/rma-request-form.doc and follow the instructions on the form. You will be notified with an RMA number once your return request is approved. Shipping information for returning the unit to Performance Technologies will be provided once the RMA is issued.

Product Warranty

Performance Technologies, Incorporated, warrants that its products sold hereunder will at the time of shipment be free from defects in material and workmanship and will conform to Performance Technologies' applicable specifications or, if appropriate, to Buyer's specifications accepted by Performance Technologies in writing. If products sold hereunder are not as warranted, Performance Technologies shall, at its option, refund the purchase price, repair, or replace the product provided proof of purchase and written notice of nonconformance are received by Performance Technologies within 12 months of shipment, or in the case of software and integrated circuits within ninety (90) days of shipment and provided said nonconforming products are returned F.O.B. to Performance Technologies's facility no later than thirty days after the warranty period expires. Products returned under warranty claims must be accompanied by an approved Return Material Authorization number issued by Performance Technologies and a statement of the reason for the return. Please contact Performance Technologies, or its agent, with the product serial number to obtain an RMA number. If Performance Technologies determines that the products are not defective, Buyer shall pay Performance Technologies all costs of handling and transportation. This warranty shall not apply to any products Performance Technologies determines to have been subject to testing for other than specified electrical characteristics or to operating and/or environmental conditions in excess of the maximum values established in applicable specifications, or have been subject to mishandling, misuse, static discharge, neglect, improper testing, repair, alteration, parts removal, damage, assembly or processing that alters the physical or electrical properties. This warranty excludes all cost of shipping, customs clearance and related charges outside the United States. Products containing batteries are warranted as above excluding batteries.

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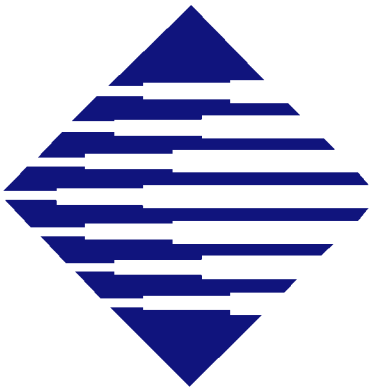


Chapter

2

Introduction

Overview

This chapter provides an introduction to the AMC335, a multipurpose, intelligent, four-port WAN communications module for AdvancedTCA® or MicroTCA™-based systems. Included here is a product definition, a list of product features, an AMC335 Front Panel figure, an AMC335 Functional Blocks figure, a description of each functional block, plus information about the software supported on the AMC335.

Information about unpacking, installing and other setup information for the AMC335 is provided in Chapter 3, “Getting Started,” on page 35.

Key topics in this chapter include:

Product Definition

The AMC335 Intelligent Synchronous WAN Communications Module provides four high-performance synchronous/serial channels for WAN connectivity in an AdvancedTCA or MicroTCA-based system. This module is ideally suited for use in creating flexible and efficient radar gateways, radar recorders, protocol convertors, serial gateways, and front-end I/O elements as well as many other high-speed communications devices that require RS232, RS422 (RS449/EIA530), and V.35 connectivity.

The architecture of the AMC335 capitalizes on the intelligence of the Freescale® MPC8270 PowerQUICC II™ Quad Integrated Communications Processor (referred to as the MPC8270 in this manual), which enables it to act as a specialized communications controller, and a Pericom® PI7C9X110 PCI-to- PCI Express reversible bridge.

Serial line electrical interfacing is available providing voltage-level adaptation to a recommended communication standard, such as RS232C, RS422 (and to RS449 or EIA530 with correct cabling), and ITU V.35 using a high-density dual VHDCI 136-pin receptacle containing the signals for all four ports. To provide an industry standard connection for each port, hydra adapter cables are offered.

Ethernet connectivity is provided via two 1000Base-X interfaces using the Broadcom® BCM5704S PCI MAC/PHY controller. Code storage and data buffering are provided by a 128 MB SDRAM array, which is available to both the MPC8270 and the PI7C9X110 PCI Express bridge devices. Additional on-board code space is available in the form of a 32 MB application flash device.

The AMC335 is capable of handling much of the low-level communications that typically burden the host processor, so most of the serial I/O communication-related processing can be relegated to the AMC335. In addition, the SDRAM eliminates the start-up delays associated with application download wait times by enabling the code to be executed directly onboard. The AMC335 supports the use of PCI Express or Ethernet for interconnecting to other subsystems used in an AdvancedTCA or MicroTCA-based environment.

The on-board Module Management Controller (MMC) monitors, controls, and performs remote diagnostics for many on- and off-board functions through the IPMI (Intelligent Platform Management Interface) compliant system management bus interface.

AMC335 I/O Configurations and Accessories

Three models of the AMC335 are available to support RS232, RS422, and V.35 standards. Other standards are supported through appropriate cabling. See “Cable Options,” on page 19. All four ports of connectivity are accessible through the high-density, dual-stacked VHDCI connector on the front panel of the AMC335.

- Model PT-AMC335-12289 (RS232C)
- Model PT-AMC335-12258 (RS422)
- Model PT-AMC335-12287 (V.35)

Note: *The instructions and information provided in this manual apply to all models. When values and options differ for any model, they are noted.*

Cable Options

Optional hydra cables allow the choice of RS232C, RS449, EIA530, or V.35 connections depending on the model of AMC335. The following four-position 6ft hydra cables, which must be ordered separately, are available for use with the AMC335:

- PT-ACC335-12233: Cable with Console, RS232C (male DB-25 connector)
- PT-ACC335-12234: Cable without Console, RS232C (male DB-25 connector)
- PT-ACC335-12203: Cable with Console, RS449 (male DB-37 connector)
- PT-ACC335-12205: Cable without Console, RS449 (male DB-37 connector)
- PT-ACC335-12256: Cable with Console, EIA530 (male DB-25 connector)
- PT-ACC335-12257: Cable without Console, EIA530 (male DB-25 connector)
- PT-ACC335-12290: Cable with Console, V.35 (male M34 connector)
- PT-ACC335-12291: Cable without Console, V.35 (male M34 connector)

The AMC335 ships with the appropriate hydra cable for the module model ordered. See “Serial Cable Connectors,” on page 88 for information about the various connectors and cable pinouts.

AMC335 Features

The AMC335 includes the following features:

- Single, mid-size PICMG® AMC.0 processor module (full-size option is available[1])
- PICMG AMC.0 R2.0, AMC.1 R1.0, and AMC.2 R1.0 compliant
- IPMI v1.5 specification compliant
- Four high-speed synchronous serial ports capable of sustaining 2 Mbps bi-directional per port
- Simultaneously sustained 8 Mbps maximum line speed
- Freescale MPC8270 PowerQUICC II Integrated Communications Processor (266 MHz)
- 128 MB dedicated processor SDRAM memory handles extensive on-board traffic and protocol requirements
- 32 MB of on-board application flash storage
- Full RS232C, RS422, RS449, EIA530 or V.35 physical interface support on all four ports
- Two 1000Base-X Ethernet ports (AMC.2, type E1 and E2)
- PCI Express x1 lane support at 2.5 Gbps (AMC.1)
- On-board RS232C debug port
- Full-board AMC card edge accessible JTAG scan chain
- System management bus
- On-board power regulation and control
- Power-on reset generator and push-button reset switch
- Application Status (APP), Out of Service (OOS), In Service (IS) and Hot Swap LED indicators
- Supports NexusWare Core CGL OS and development environment
- Supports NexusWare WAN Protocol communications software including Radar Receiver/SBSI, TADIL-B, HDLC, X.25, Frame Relay, ASYNC
- Supports Solaris™ 9/10, Windows® XP, and Linux® 64-bit operating systems
- RoHS compliant

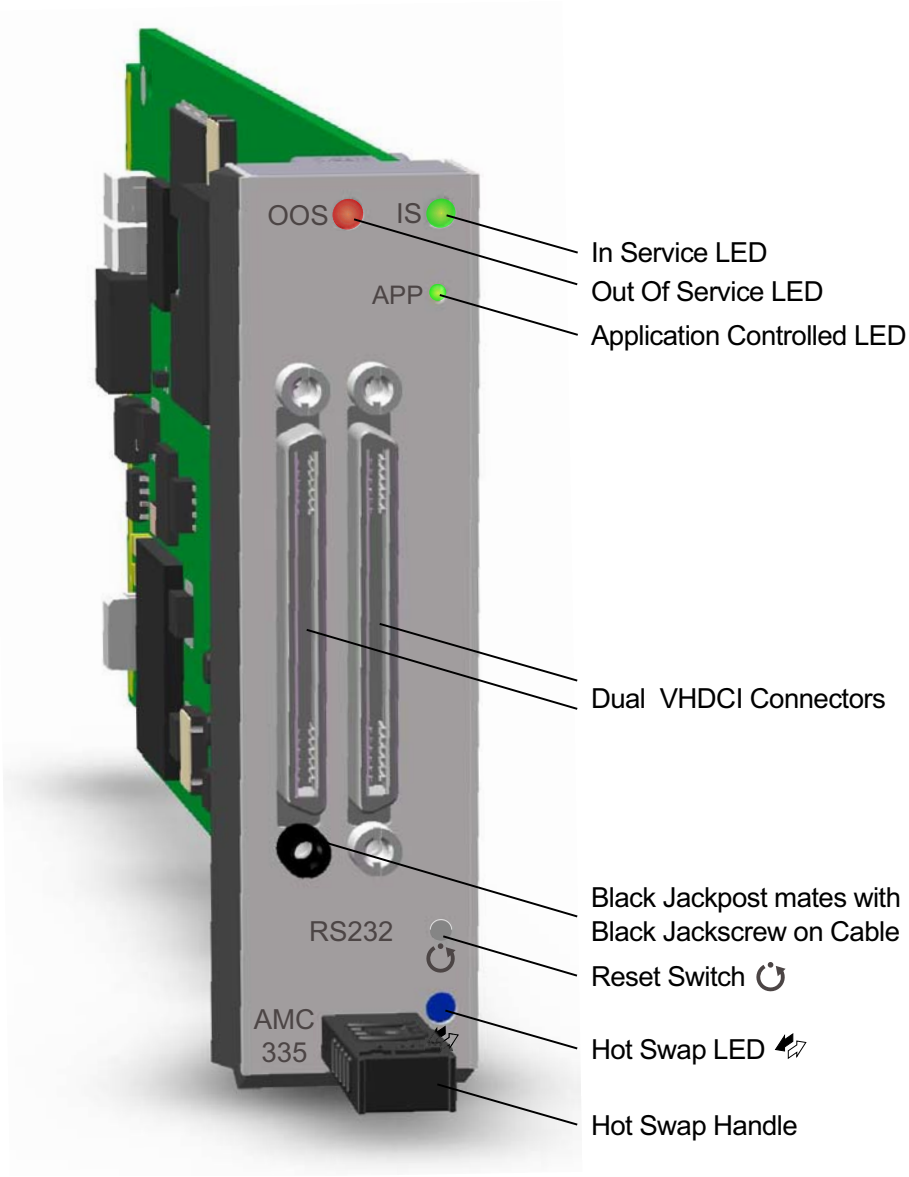
1. For a full-size option, contact the Performance Technologies’ Sales team, sales@pt.com for more information.

AMC335 Front Panel

The front panel of the AMC335, shown in Figure 2-1, “AMC335 Front Panel,” contains the following elements:

- A dual VHDCI connector carrying four independent serial I/O ports. See “Serial I/O Connector,” on page 73 for more information about this connector.
- One black jackpost and three silver jackposts. To properly connect the cable to the AMC335, align the black jackscrew on the cable with the black jackpost on the front panel. See “Connecting the Cable,” on page 43 for more information about connecting the cable.
- Four LED indicators: In Service (IS), Out of Service (OOS), Application (APP), and Hot Swap. See “LED Indicators,” on page 31.
- A push-button reset switch. See “Push-Button Reset Switch,” on page 42.
- An insert/extraction (hot swap) handle. See “Hot-Swap Handle Switch,” on page 42.

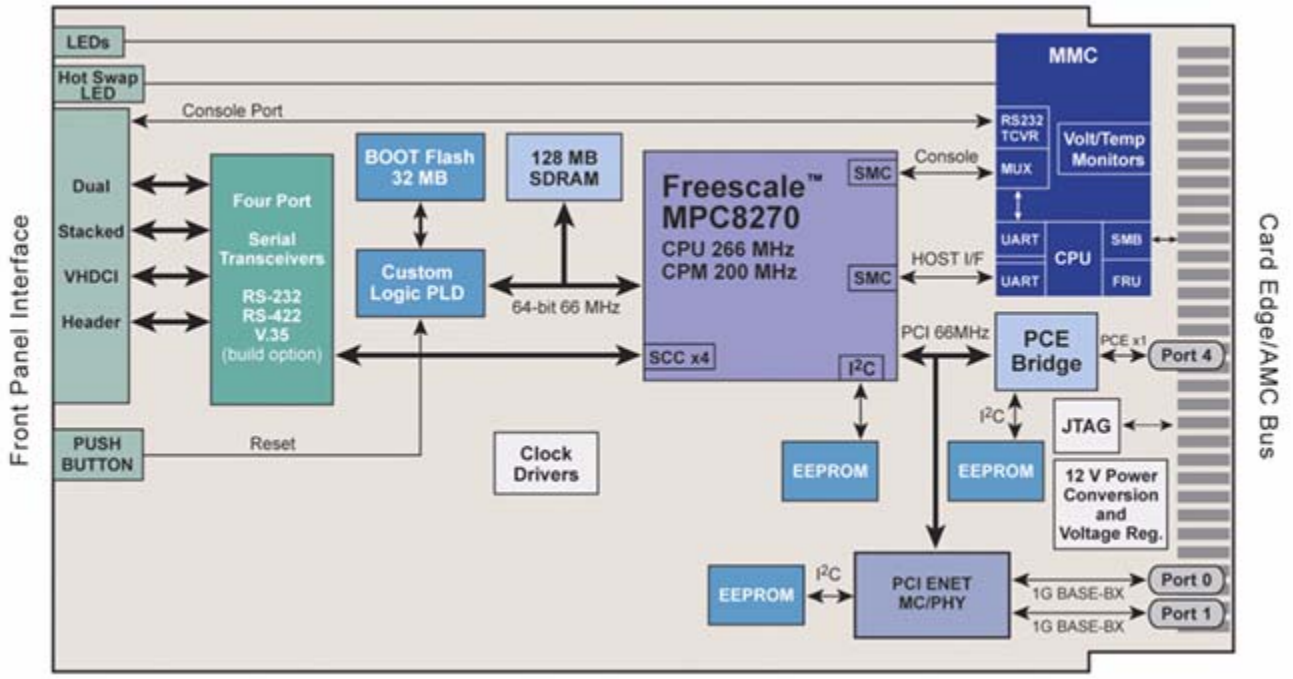
Figure 2-1: AMC335 Front Panel



AMC335 Functional Blocks

Figure 2-2, “AMC335 Functional Block Diagram,” presents a functional block diagram of the AMC335.

Figure 2-2: AMC335 Functional Block Diagram



The following topics provide overviews for each major block on the AMC335:

Freescale MPC8270 PowerQUICC II Processor

The AMC335 incorporates a Freescale MPC8270 PowerQUICC II integrated communications processor as the primary controller on the module. The processor supplies the 266 MHz PowerPC CPU core, the 200 MHz Communications Processor Module (CPM), and the 66 MHz external 60X single master bus. It has direct connections to, and is the controller for the Synchronous DRAM (SDRAM), and the PCI side of the PI7C9X110 PCI Express interface controller. It controls all of the on-board resources via a buffered data and address bus and a set of local control registers.

See "Freescale MPC8270 PowerQUICC II Processor," on page 117 for links to additional information and related documents for this device.

AMC Interface

The AMC335 is compliant with the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. It is designed to be hot swappable into a mid- or full-size bay on an AMC carrier board such as Performance Technologies' AMP507x MicroTCA platform, see Figure 2-3, "AMC335 in the AMP507x MicroTCA Platform," on page 22. The AMC335 can also function in a non-hot swap AMC system. Its AMC card edge connector provides rear I/O connectivity to the AMC bus in accordance with the *AMC Type 4 Specification*. The AMC335 AMC card edge connector supports the following PICMG subsidiary specifications:

- AMC.1 (PCIe), Type 1 — Port 4, x1 PCI Express at 2.5 Gbps
- AMC.2 (1GbE), Types E1 and E2 — Port 0 and Port 1, 1Gb Ethernet channels (1 & 2)

The PRESENT1# and PRESENT2# signals are connected together on the module for system presence detection. Primary module power is drawn through the AMC card edge connector as well.

Connector locations and pinouts are documented in "AdvancedMC Card Edge Connector," on page 70. See "PICMG Specifications," on page 118, which contains a link to the PICMG Web site, where the AMC specification may be obtained.

Figure 2-3: AMC335 in the AMP507x MicroTCA Platform

User I/O

The user I/O on the AMC335 consists of the serial I/O connector and a console port. Each is described below.

Serial I/O Connector

The serial I/O connection on the AMC335 is made through a dual VHDCI connector with 136 pins. Each port is configured to be a Data Terminal Equipment (DTE) connection and each port supports one set of the following signals:

RS232C

- EIA RS232C single-ended input connections conforming to the V.28 electrical characteristics for RXD, TXCI, RXC, DCD, DSR, CTS with built in 5K pulldowns
- Tri-state capable single ended output connections conforming to the V.28 electrical characteristics for TXD, DTR, RTS, TXC
- Signal Ground

See “RS232C Supported Signals,” on page 74 for supported signals and pinouts.

RS422

Note: *Supports RS449 and EIA530 with the correct breakout cable.*

- Differential input connections conforming to the V.35 electrical standards for RXD, TXCI, RXC. The RS422 configuration provides for an adjustable termination architecture. Four Single-Inline-Package (SIP) resistor pack connections are included to allow the user to remove or adjust the serial port termination if necessary. By default the AMC335 is populated with four 120 Ohm SIPs. One SIP is allocated for each port of the AMC335 so termination can be modified on a port-by-port basis if desired. Each input is terminated with 100 Ohms differentially: 120 Ohm SIP and 1K Ohm pullup and pulldown to ensure idle port condition if no external cable is present.
- Tri-state capable differential output connections conforming to the V.11 electrical standards for TXD, DTR, RTS, and TXC
- Signal Ground

See “RS422/RS449 Supported Signals,” on page 77 for supported signals and pinouts.

V.35

- Differential input connections conforming to the V.35 electrical standards for RXD, TXCI, and RXC. Each input is terminated with 100 Ohms differentially and has a 125 Ohm “T” connection to ground per the V.35 specification.
- RS232C single-ended input connections conforming to the V.28 electrical characteristics for DCD, DSR, CTS and RI with built in 5K pulldowns
- Tri-state capable differential output connections conforming to the V.35 electrical standards for TXD and TXC. Each input is terminated with 100 Ohms differentially and has a 125 Ohm “T” connection to ground per the V.35 specification.
- Tri-state capable RS232C single ended output connections conforming to the V.28 electrical characteristics for DTR, RTS, and LT
- Signal Ground

See “V.35 Supported Signals,” on page 83 for supported signals and pinouts.

Console Serial Port

The console serial port can be used with NexusWare to configure and control the module-level application software. It is implemented as a 9-pin D-sub female connector on each I/O cable. The port is an asynchronous RS232C serial I/O port that supports the following signals:

- RS232C single-ended input connection conforming to the V.28 electrical characteristics for RXD with built-in 5K pulldown
- RS232C single-ended output connection conforming to the V.28 electrical characteristics for TXD
- Signal Ground

See "Console Serial Port," on page 88 in for more information on the signals and pinouts for the serial console port. See also "Console Cable Option," on page 93.

Note: *A three-pin right angle header can be mounted on the bottom side of the card and used for debugging. Contact Performance Technologies' Customer Support and Services for more information.*

PCI Express Interface

The AMC335 uses a Pericom PI7C9X110 PCI-to-PCI Express bridge (referred to as the PI7C9X110 PCI Express bridge or the PI7C9X110 in this manual) to connect the AMC335's MPC8270 communications processor to the host PCI Express root complex. The PI7C9X110 PCI Express bridge is compliant with the following specifications:

- *PCI Express Base Specification, Revision 1.0a*
- *PCI Express Card Electromechanical Specification, Revision 1.0a*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *PCI Local Bus Specification, Revision 3.0*

The PI7C9X110 PCI Express bridge supports transparent and nontransparent modes of operation, as well as forward and reverse bridging. The application on the AMC335 is a forward bridging implementation, however if a PCI Express interface is not available or disabled the part needs to be configured in reverse mode and held in reset. In forward bridging mode, the PI7C9X110 has an x1 PCI Express upstream port and a 32-bit PCI/PCI-X downstream port running at 66 MHz. The PI7C9X110 PCI Express bridge configuration registers are backward compatible with existing PCI bridge software and firmware.

The PI7C9X110 PCI Express bridge's PCI Express connection to the root complex is made via the AMC card edge connector, per the AMC.1 and the *PCI Express Card Electromechanical Specification, Revision 1.0a*. The AMC335 utilizes an x1 lane configuration. RX,TX, RXCLK, and PERST# are the supported PCI Express signals.

See "PCI Express Bridge," on page 118 for links to additional information and related documents for this device.

Ethernet Interfaces

Two 1000Base-X interfaces for AMC.2 support are included on the AMC335. These ports use the Broadcom BCM5704S Dual MAC/PHY IC to connect the MPC8270 PCI bus to the host via the AMC.2 interface. The BCM5704S supports the 1000BASE-X interface through an integrated SerDes PHY whose control registers are specified in the MAC registers. An MDC and MDIO serial control interface is implemented inside the MAC/PHY via a bit banged register / an auto mode. Refer to the “MDI register access” section of the *BCM57XX Programmer’s Reference Guide* for additional information. The Ethernet port address mapping is defined in Table 2-1, “Ethernet Port Mapping,” below:

Table 2-1: Ethernet Port Mapping

Physical Port	AMC Port	Dual MAC Port	PHY MDIO Address (internal)
1	0	0	1
2	1	1	1

See “Ethernet Interfaces,” on page 118 for a link to additional information for this device.

Memory

Memory on the AMC335 consists of the following components:

- SDRAM
- Flash Memory
- EEPROM

The memory address map is discussed in “Memory Map,” on page 26.

SDRAM

Code storage and data buffering on the AMC335 are provided by a 128 MB Synchronous DRAM (SDRAM) array, which is available to both the MPC8270 and the PI7C9X110 PCI Express bridge. The SDRAM memory bank is comprised of individual chips mounted on both sides of the base board. The SDRAM architecture provides the ability to:

- Synchronously burst data at a high data rate with automatic column address generation
- Interleave between internal banks in order to hide PRECHARGE time
- Randomly change column addresses on each clock cycle during a burst access

The total SDRAM memory is 128 MB supported at 66 MHz bus speed. The data port size is 64 bits. The MPC8270 internal SDRAM controller takes care of all low-level SDRAM operations including row and column multiplexing, precharge times, and refresh.

Flash Memory

An on-board, non-volatile, programmable, Flash memory (32 MB x 8) device is provided for startup code and application storage. The device is accessed by the MPC8270 through the buffered data bus. The application Flash is a non-volatile memory that has the following general characteristics:

- Read accesses to the device are the same as any EPROM. The data appears on DQ0-DQ7 on the buffered data bus.
- For writing purposes, the device has 256 blocks of byte-wide data storage. The storage blocks have 128 KB of storage each.
- Selecting, writing and erasing the blocks are done by using a Common Flash Interface (CFI) and a Scalable Command Set (SCS)
- All read, erase, and program operations are accomplished using only a single power supply. Internally generated and regulated voltages are provided for the program and erase operations.

EEPROM

Three small Electrically Erasable Programmable Read-only Memory (EEPROM) devices are connected to components on the AMC335 to store initialization values and application code:

- A small EEPROM device is connected to the I^2C port (port A) on the MPC8270, which is used to store non-volatile information for the operating system or the application code. Reading and writing this device is currently under direct control of the operating system.
- A second EEPROM device is connected to the I^2C port on the PI7C9X110 PCI Express bridge, which handles power up/PCERST# configuration of the PI7C9X110 PCI Express bridge. This EEPROM device is configurable via a DIP switch selection. See “SW3-2 (EEPROM Write Protect),” on page 40 for more information about configuring this EEPROM device.
- A third EEPROM device is connected to the I^2C port on the BCM5704S Ethernet controller, which is used to store the BCM5704S initialization boot code. This EEPROM is programmed either by JTAG or over PCI through the BCM5704S. Refer to the *BCM57XX Programmer’s Reference Guide* for more information.

Memory Map

The address map is defined by the AMC335 address decode scheme. There are different levels of address decode built into the AMC335. The first level and primary decode is done by the MPC8270’s System Interface Unit (SIU). One of the SIU’s subsections is the memory controller, which is responsible for controlling a maximum of 12 memory banks shared by a high performance SDRAM machine, a general-purpose chip-select machine (GPCM), and three user-programmable machines (UPMs). It supports a glueless interface to synchronous DRAM, EPROM, Flash EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.

SDRAM Machine

The SDRAM machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve the highest performance.

GPCM

The GPCM provides interfacing for simpler, lower-performance memory resources and memory-mapped devices. The GPCM has inherently lower performance because it does not support bursting. For this reason, GPCM-controlled banks are used primarily for boot loading and access to low-performance memory-mapped peripherals.

UPM

The UPM supports address multiplexing of the external bus, refresh timers, and generation of programmable control signals for row address and column address strobes to allow for a glueless interface to DRAMs, burstable SRAMs, and almost any other kind of peripheral. The refresh timers allow refresh cycles to be initiated. The UPM can be used to generate different timing patterns for the control signals that govern a memory device. These patterns define how the external control signals behave during a read, write, burst-read, or burst- write access request. Refresh timers are also available to periodically generate user-defined refresh cycles.

The primary control of the devices served by the memory controller machines is through the MPC8270's external chip select lines.

Interrupt Sources

MPC8270 Interrupts

Several multifunction pins are used to supply the MPC8270 with the direct-connect interrupts from the various board peripherals. The !IRQ0 to !IRQ7 lines are used along with some of the 16 interrupt-capable pins on Port C of the MPC8270, see "I/O Ports," on page 95. The interrupt sources, for the most part, have multiple interrupt conditions. Refer to the component's user manual for the complete breakdown of interrupt causes. Table 2-2, "MPC8270 Interrupt Sources," shows the connections from these devices to the MPC8270:

Table 2-2: MPC8270 Interrupt Sources

IRQ Level	Pin	Controlled Device	Note
!IRQ0	T1	NMI Interrupt	
!IRQ1	A22	Not Used	
!IRQ2	E21	Not Used	
!IRQ3	D21	Not Used	
!IRQ4	C21	Not Used	PI7C9X110 general interrupt for INTA inbound interrupts to the MPC8270
!IRQ5	B21	Not Used	
!IRQ6	A21	Dual MAC/PHY Port 2	
!IRQ7	E20	Dual MAC/PHY Port 1	
PC0	AB26	WAKE4	On the RS232C build of the AMC335 this bit indicates that there is a valid electrical signal at port 4, on DCD or TXCI. It does not indicate a mark or space. This is typically used to indicate that a cable is plugged in and the transmitting element is active.
PC1	AD29	WAKE3	On the RS232C build of the AMC335 this bit indicates that there is a valid electrical signal at port 3, on DCD or TXCI. It does not indicate a mark or space. This is typically used to indicate that a cable is plugged in and the transmitting element is active.

Table 2-2: MPC8270 Interrupt Sources (Continued)

IRQ Level	Pin	Controlled Device	Note
PC2	AE29	WAKE1	On the RS232C build of the AMC335 this bit indicates that there is a valid electrical signal at port 2, on DCD or TXCI. It does not indicate a mark or space. This is typically used to indicate that a cable is plugged in and the transmitting element is active.
PC3	AE27	WAKE1	On the RS232C build of the AMC335 this bit indicates that there is a valid electrical signal at port 1, on DCD or TXCI. It does not indicate a mark or space. This is typically used to indicate that a cable is plugged in and the transmitting element is active.

PCI Express Interrupts

The PI7C9X110 PCI-to-PCI Express bridge chip can support both INT-x emulation of the legacy INT-x wires or the Message Signaled Interrupt (MSI) mode of interrupt passing on either side of the bridge. The AMC335 is designed to support both modes of operation. The selection of the mode of operation is up to the root complex software driver and is dependent on the hardware and software capabilities of the particular system in which the AMC335 is installed. The PI7C9X110 also imposes a limitation on modes by only allowing the same type of operation on either side (PCI or PCI Express) of itself, once one particular mode is chosen. This forces a change on how the interrupts are handled in the hardware and software so that a consistent interrupt method is used in either mode. The operating features are outlined in the following topics.

Outbound Interrupts

The method for creating an outbound interrupt is the same whether INT-x or MSI is chosen as the operating mode. The outbound interrupt is generated by the MPC8270 by using PI7C9X110's Primary IRQ register set to send an interrupt message to the host. Access to the registers is by the local PCI bus.

After writing the Primary IRQ, depending on the method chosen by the root complex OS and device driver, the PI7C9X110 generates either a legacy INT-x serial message to the host or an MSI message to the host. The interrupt message is mapped to the AMC335's root complex OS interrupt handler and the appropriate action can then be taken by the interrupt handler. The PI7C9X110 Primary IRQ register set is used to signal a particular interrupt event and the PI7C9X110 scratchpad registers can be used for argument and message passing.

Inbound Interrupts

The inbound interrupt is implemented by writing to the MPC8270's PCI inbound doorbell register directly by the root complex host. The register is exposed to the root complex through the PI7C9X110's BAR3 (Downstream Memory 2 BAR) memory space. The PI7C9X110's BAR3 (Downstream Memory 2 BAR) is initially mapped to 0xF0010000 with a size of 4 KB. The MPC8270's Inbound PCI doorbell is mapped to offset 0x468 from the initial BAR3

(Downstream Memory 2 BAR) base address. The initial secondary side mapping is not in the EEPROM for the PI7C9X110 but can be programmed by the MPC8270. Another value for this offset may be stored in the MPC8270's NVRAM. Care must be taken by the driver code not to alter registers outside of this PCI register set as they will change the operation of the MPC8270.

Since this setup works in either mode (INT-x or MSI) it will be used for both modes. Inbound messages and arguments are still going to be implemented in the PI7C9X110's scratchpad registers if their use is desired.

Ethernet Interrupts

The BCM5704S Ethernet controller provides an interrupt to indicate a change in status for each MAC/PHY. This interrupt is routed to the PLD, which adds a mask ability and status through a series of registers.

Module Management Controller

The AMC335 includes a Module Management Controller (MMC) based on the Atmel® ATMEGA128L-8MU, which interfaces to the local Intelligent Platform Management bus (IPMB-L). The MMC monitors and controls the module's payload per the PICMG AMC.0 specification.

See Chapter 4, "System Monitoring and Alarms," on page 45 for more information on MMC functionality, supported commands, AMC335 sensors, and the firmware upgrade process.

The AMC335 is compliant with standard *Intelligent Platform Management Interface v1.5 Specification* functionality. See "Module Management Controller," on page 118, for information about this specification.

Sensors

The following sensors are monitored on the AMC335:

- MMC voltage monitoring (3.3 V management power and 12 V power to the AMC slot)
- Air inlet temperature sensor
- Temperature sensor on the CPU, which measures the board's high temperatures. The sensor is located between the CPU and the voltage regulator.
- MMC hot-swap switch sensor

Other on-board voltages (3.3 V, 2.5 V, 1.8 V, 1.5 V. 1.2 V) are also measured. For more information on AMC335 sensors, see "Sensors," on page 50.

Reset

The AMC335 supports local power-on, hard and soft resets, as well as resets caused by the external PCI Express bus and the MMC. See Chapter 7, “Reset,” on page 101 for more information.

Push-Button Reset

The front-panel push button (see Figure 2-1, “AMC335 Front Panel,” on page 20) provides a hard reset if pressed. See “Push-Button Reset Switch,” on page 42 for more information.

Board Clocks and Frequencies

Table 2-3, “Locally Generated Frequencies and Sources,” shows the on-board generated frequencies and their sources on the AMC335.

Table 2-3: Locally Generated Frequencies and Sources

Frequency	Source	Use
1.250 GHz	Internal Multiplying PLL in the PI7C9X110 PCI Express bridge	PCI Express Serial Bit Rate
264 MHz	MPC8270 Internal Multiplying PLL	MPC8270 CPU Internal Use
198 MHz	MPC8270 Internal Multiplying PLL	MPC8270 CPM Internal Use
100 MHz	PCI Express Reference Clock	PI7C9X110 PCI Express Bridge Reference Clock Input
66 MHz	Crystal Controlled Clock Oscillator	CPU, SDRAM, and logic
66 MHz	MPC8270 Internal PLL	Local PCI Bus
25 MHz	BCM5704S Ethernet Clock	Dual PCI MAC/PHY 1000Base-X Ethernet
7.372 MHz	MMC CPU Clock	ATmega CPU Clock
Communications Baud Rate	MPC8270 Internal PLL	Various baud rates generated by the SCC Baud Rate Generator, typically <2.0 MHz
500 KHz	TPS5450 Switching Power Supply Oscillator	Internal Clock Source

Clock Steering

The AMC335 supports an optional crystal oscillator to provide custom synchronous clock speeds.

For synchronous serial applications, receive and transmit data signals may be accompanied by external receive and/or transmit clock signals. To manage the options for each clock line source and destination, a clock multiplexor is provided. The source and direction of the clocks are set up in a series of custom registers and controlled by local logic.

The Receive Clock of any serial channel can be sourced from the serial port receive clock signals (RXCLK_n) or can be sourced from an optional external clock (contact Performance Technologies’ Customer Support and Services for external oscillator OPTCLK support).

The Transmit Clock pin on the MPC8270 is bi-directional. The Transmit Clock of any serial channel may be sourced from the MPC8270's transmit clock signals (TXCn) or from the serial port's transmit clock in signal (TXCIn).

LED Indicators

The LEDs located on the AMC335 front panel are defined below. See Figure 2-1, "AMC335 Front Panel," on page 20 for the location of these LEDs.

Out of Service (OOS) and In Service (IS) LEDs

These LEDs are used to indicate an "out of service" condition or an "in service" status, per the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. Although these LEDs are managed by the MMC, a carrier manager or shelf manager can override the MMC's local LED settings.

The OOS LED is activated to indicate that the payload is known to be out of service (payload power is off, held in reset, or faulted in a way that precludes operation). Otherwise the OOS LED is off. The health of the board cannot be inferred solely from the state of this LED. The default local color of the OOS LED is determined by FRU data and is configurable as either red or amber. Contact Performance Technologies Customer Support for information about configuring this color.

The IS LED is activated when the OOS LED is turned off. It is never turned on when the OOS LED is on. The IS LED is green when all sensors are within the critical thresholds or amber when one or more sensors have exceeded a critical threshold.

Board Status (APP) LED

The front panel includes one application-controlled LED (controlled by application software, not the MMC) used to indicate the health of the module. The APP LED is a green/yellow/off LED that has the following states:

- Off = no power or booting
- Green = module is healthy
- Yellow = module has had an error
- Flashing = module is currently running (possible for both green and yellow colors)

Hot Swap LED

The blue Hot Swap LED indicates the module's state as it deactivates in preparation for extraction or reactivate after insertion. See"Hot-Swap Handle Switch," on page 42. Refer also to the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0* for more information (see "PICMG Specifications," on page 118).

Insertion Sequence

Off	Module handle open. Management power is not enabled.
Blue on	Module is fully seated in carrier. Module's management power is enabled. User may initiate activation by pushing in the handle on the module's front panel to close the hot swap switch.
Blue long blink	Module handle is closed; module is being activated.
Off	Module handle is closed. Module is in normal operational state.

Extraction Sequence

Off	Module is in normal operational state. User may initiate deactivation by pulling out the module handle to open the hot swap switch, sending a request via the MMC to the carrier for a hot swap extraction.
Blue short blink	Module handle open. Module is waiting to be deactivated. Not safe to extract module.
Blue on	Module is quiesced, module payload power is disabled. Safe to extract module.

Rear-Panel I/O

The AMC335 transitions the following I/O signals through the AMC card edge connector to the carrier board or MicroTCA system:

- 2x 1Gb 1000BASE-X Ethernet
- PCI Express x1
- Reset
- Power and Ground
- System Management Bus (SMB)
- JTAG

User-Configurable Switches

There are several user-configurable switches that may need to be configured. They may be used with the software package supplied for the module. See “Switches,” on page 37 for more information.

Software Support

NexusWare Software Support

The NexusWare software suite offers a CGL-registered and POSIX-compliant operating system and development environment. In addition, the suite includes an extensive list of installable protocols that can be leveraged to build robust solutions, such as media gateways, lawful intercept platforms, SS7 monitoring equipment for line usage/billing applications, radar gateways, and converged serial gateways.

The NexusWare family of products supported on the AMC335 includes:

NexusWare Core

At the very center of the NexusWare suite of software is NexusWare Core, which provides a comprehensive, highly integrated, Linux OS development, integration, and management environment. It is intended for system engineers who use Performance Technologies' embedded products to build packet-based systems, including next-generation wireless and IP-based systems.

NexusWare WAN

Performance Technologies' suite of NexusWare WAN protocols include, but are not limited to, HDLC, X.25, Frame Relay, and Radar Receiver. When combined with Performance Technologies' embedded products, these enhance the ability to create flexible and efficient product platforms such as radar gateways, converged serial gateways, and front-end I/O systems.

The WAN software products are offered as installable software packages for NexusWare Core or as turnkey packages for those developers interested in the protocol package by itself. Whether the installable or the turnkey solution is chosen, developers are provided with a well-documented and powerful API to assist in the development process.

Operating Systems

The AMC335 is enabled with the Linux-based NexusWare development environment. Due to the wide acceptance and extensive number of publicly available applications and protocols, system developers can bring sophisticated systems to market in a much shorter time.

With a well-defined API, the integrated protocol suite from Performance Technologies reduces time to market by eliminating unnecessary development time at the hardware/protocol level. The protocols for our standard WAN hardware products enable development engineers to proceed directly to integration and application development.

Performance Technologies suite of WAN communications protocols provides complete WAN connectivity solutions for MTP-2, Frame Relay, HDLC, LAPD, X.25, and Radar. OS support includes all OS that support TCP/IP such as Solaris, Linux and Windows.

For the Solaris environment, Performance Technologies' ComLink™ Communications Software provides both a transparent link to all SunLink™ protocols, as well as a documented set of driver primitives for developing applications.

Chapter

3

Getting Started

Overview

This chapter provides information about installing and configuring the AMC335. Key topics in this chapter include:

Unpacking

Inspect the packing container for any damage. If the container appears damaged, immediately contact the company responsible for the shipping and report the damage before opening and unpacking the container. It is recommended that you also notify Performance Technologies (see “Customer Support and Services,” on page 15 for assistance information).

Caution:

To reduce the risk of damage to the AMC335, the module must be protected from electrostatic discharge and physical shock. Never remove any of the socketed parts except in a static-free environment. Use the anti-static bag shipped with the product to handle the module.

Caution:
Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

System Requirements

The following topics provide information about the system requirements:

- Compatibility
- Electrical and Environmental Requirements

Compatibility

The AMC335 is offered with either a mid-size or full-size front panel. See “AMC335 Front Panel,” on page 20 for example of a mid-size front panel.

The AMC335 is compliant with the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. It is designed to be hot swappable into a mid-size or full-size bay in an AdvancedTCA or MicroTCA platform. The AMC335 also supports the following PICMG subsidiary specifications:

- AMC.1 (PCI Express) Type 1 for x1
- AMC.2 (1GbE) Types E1 and E2

FCLKA

The AMC335 requires the carrier to source FCLKA to the module. The AMC.1 R2.0 specification requires that FCLKA is e-keyed. The AMC335 is shipped from the factory configured for AMC.1 R2.0 e-keying of FCLKA. AMC.1 R1.0 carriers do not e-key FCLKA. If the AMC335 does not come out of reset when powered on, it is likely that FCLKA is not configured properly for the specific carrier.

For more information about configuring FCLKA on this AMC335, please contact Performance Technologies' Customer Support and Services.

Electrical and Environmental Requirements

Electrical specifications are presented in detail in “Electrical Specifications,” on page 108.

The AMC335 operates between 0 °C (32 °F) and 60 °C (140 °F) ambient temperature. It is the user’s responsibility to ensure that the AMC335 is installed in a chassis capable of supplying adequate airflow. External airflow must be provided at all times. See Chapter 8, “Specifications,” on page 107 for more details.

The maximum power dissipation is 3W peak generated by the MPC8270 and the linear regulator creating its core voltage. In a normal environment where the ambient temperature does not exceed the thermal operating range, a heat sink is not required by the AMC335. However, a heat sink may be employed to give the module a thermal margin beyond its normal operating range. Contact Performance Technologies’ Customer Support and Services for more information.

Warning:

Operating the AMC335 without adequate airflow may damage the processor.

The AMC335 may contain environmentally hazardous materials. You must make sure that you dispose of any such materials in accordance with your local rules and regulations. For disposal and recycling information, contact your local authorities or the Electronic Industries Alliance (EIA) at http://www.eiae.org/.

Performance Technologies' Compliance with RoHS and WEEE Directives statement is on page 115.

Connectivity

The AMC335 provides a dual VHDCI connector for interfacing with application-specific devices. Refer to Chapter 5, "Connectors," on page 69 for complete connector descriptions and pinouts.

Switches

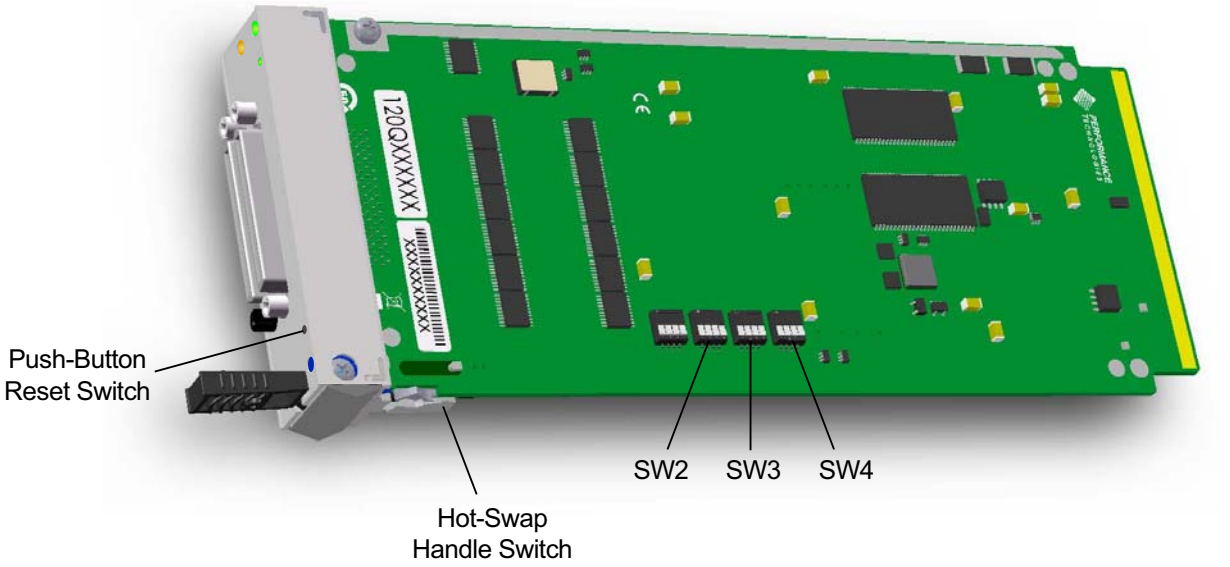
The AMC335 includes several options that tailor the operation of the module. Most of the options are selected through software. However, some options cannot be software controlled and are configured with DIP switches. Closing or opening the desired switch selects each switch's options. See Figure 3-1, "AMC335 Switch Locations," below.

Switch Locations

The AMC335 includes the following user-configurable switches:

- SW2 Switch Bank
- SW3 Switch Bank
- SW4 Switch Bank
- Push-Button Reset Switch
- Hot-Swap Handle Switch

Figure 3-1: AMC335 Switch Locations



Switch Descriptions

The following topics present the switches in numerical order and provide a description of each switch bank, switch number, and setting. Multiple-switch banks are identified in the form **SWx-N**, where **x** is the bank number and **N** is the switch number. For example, SW2-3 means “bank number 2, switch number 3."

Each switch is either ON (closed) or OFF (open). Each bank is labeled to indicate the switch number and the ON or OFF position.

Note: *The factory default switch settings are indicated below in* ***bold****.*

SW2 Switch Bank

There is a set of four general-purpose switches at position SW2 that can be configured for any purpose. They can be read by the software package supplied for the module in the General Purpose Switch and External Bus Reset Status Register. The default setting for all switches in the SW2 bank is OFF.

See Figure 3-1, “AMC335 Switch Locations,” on page 38 to see the location of the switch bank.

SW3 Switch Bank

SW3 allows the user to configure the following AMC335 functions:

- Reset Configuration
- EEPROM Write Protect
- Break Detect Enable
- Application Code Enable

See Figure 3-1, “AMC335 Switch Locations,” on page 38 for the location of this switch bank. The following topics describe the functionality of each switch in SW3.

SW3-1 (Reset Configuration)

SW3-1 (RSTCONF#) selects the hard reset configuration settings for the MPC8270. See Table 3-1 for switch settings. The default factory setting is **ON**.

Table 3-1: SW3-1 Settings

SW3-1	Description	Factory Setting
OFF (Open)	Sets the MPC8270 to the default HRESET# configuration settings. There will be no reset configuration cycles on the bus because the MPC8270 is set to be a reset slave.	
ON (Closed)	Sets the MPC8270 to use the HRESET# configuration settings from the boot flash. Sets the MPC8270 as the reset master.	**Default**

SW3-2 (EEPROM Write Protect)

SW3-2 (EEWP) selects the write-protect configuration for the P17C9X110 PCI Express bridge's boot EEPROM device. See Table 3-2 for switch settings. The default factory setting is **ON**.

Table 3-2: SW3-2 Settings

SW3-2	Description	Factory Setting
OFF (Open)	The PI7C9X110's boot EEPROM is write protected.	
ON (Closed)	The PI7C9X110's boot EEPROM can be written to by using the PI7C9X110's internal programming register.	**Default**

SW3-3 (Break Detect Enable)

SW3-3 (BRK_DET_EN#) is used to enable or disable a hard reset whenever a double break signal is sent to the AMC335 over the console serial port. See Table 3-3 for switch settings. The default factory setting is **OFF**.

Table 3-3: SW3-3 Settings

SW3-3	Description	Factory Setting
OFF (Open)	HRESET# is disabled.	**Default**
ON (Closed)	The control logic PLD enables a HRESET# whenever a double break signal is sent to the AMC335 over the console serial port. A break + character (enter or b for example) shifts the console focus from the MPC8270 to the MMC.	

SW3-4 (Application Code Enable)

SW3-4 (FACT_JMPR#) is used to configure the loading and execution of any application code that is present in the application flash. See Table 3-4 for switch settings. The default factory setting is **ON**.

Table 3-4: SW3-4 Settings

SW3-4	Description	Factory Setting
OFF (Open)	Disable the loading and execution of any application code that is present in the application flash.	
ON (Closed)	Enables the boot code to load and execute any application code that is present in the application flash.	**Default**

SW4 Switch Bank

SW4 allows the user to configure the following functions:

- PCI Express Configuration
- JTAG Enable

See Figure 3-1, “AMC335 Switch Locations,” on page 38 for the location of this switch bank. The following topics describe the functionality of each switch in SW4.

SW4-1 (PCI Express Configuration)

SW4-1 (CFGSW0) is used to enable or disable the PCI Express interface on the module. See Table 3-5 for switch settings. The default factory setting is **OFF**.

Table 3-5: SW4-1 Settings

SW4-1	Description	Factory Setting
OFF (Open)	Enables the PCI Express link on the AMC335.	**Default**
ON (Closed)	Disables PCI Express connectivity.	

SW4-2

SW4-2 (CFGSW1) is not used at this time. The default factory setting is **OFF.**

SW4-3

SW4-3 (CFGSW2) is not used at this time. The default factory setting is **OFF.**

SW4-4 (JTAG Enable)

SW4-4 (JTAG_EN_N) is used to enable the full JTAG scan chain. See Table 3-6 for switch settings. The default factory setting is **OFF**.

Table 3-6: SW4-4 Settings

SW4-4	Description	Factory Setting
OFF (Open)	Disables JTAG mode on the module. This switch is reserved for use by the factory and should not be modified.	**Default**
ON (Closed)	Grounds the JTAG_EN# signal enabling the full JTAG scan chain. This switch is reserved for use by the factory and should not be modified.	

Push-Button Reset Switch

The AMC335 provides a recessed, push-button reset switch on its front panel. When the system reset button is pressed, the AMC335 resets itself. Since the switch is recessed, a tool is necessary to reach through the front panel to reset the AMC335. An unfolded paper clip works well for this application. See “AMC335 Front Panel,” on page 20 for the location of this button.

Hot-Swap Handle Switch

The AMC335 provides a hot-swap handle on its front panel (see Figure 2-1, “AMC335 Front Panel,” on page 20). This handle is attached to a mechanical latching mechanism and to the hot-swap switch. When this switch opens or closes it sends a request via the MMC to the carrier for a hot-swap extraction or insertion. Its function and behavior is defined by the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. The hot-swap LED indicates the state of the module during extraction and insertion. See “LED Indicators,” on page 31 for more information.

Physical Installation

Before installing the AMC335, make sure the module is correctly configured for your application.

Installing the AMC335

The following instructions assume that chassis power is on and that the system supports hot-swap insertion. If the system does not support hot swap, power must be turned off prior to installation.

With a grounding strap connected to your wrist or ankle, perform the following steps to install the module:

1. Unlock the ejector handle by gently pulling it away from the front panel.
2. Select an appropriate AMC slot in the chassis and slide the AMC into the slot, aligning the module with the guides near the top of the slot. The module audibly snaps into place when properly inserted. When the AMC card edge connector makes proper contact with the backplane AMC connector, the blue hot-swap LED turns ON and the hardware connection process begins.
3. Press the handle toward the front panel to lock the module in the chassis. When the module is operational, the blue hot-swap LED turns OFF.
4. Connect any cables from peripheral devices.

Removing the AMC335

With a grounding strap connected to your wrist or ankle, perform the following steps to remove the module:

1. Disconnect any peripheral device cables from the module.
2. Gently press your thumb against the front panel of the module, while pulling the handle away from the front panel to unlock the module. The blue hot-swap LED blinks to indicate that the handle is open and the module is waiting to be deactivated. It is not yet safe to extract the module in this state.
3. Wait until the blue hot-swap LED stops blinking and remains illuminated to indicate that the module is ready for extraction.
4. When the blue hot-swap LED stops blinking and remains illuminated, the module is quiesced and module payload power is disabled. It is now safe to extract the module. Gently pull on the handle to remove the module from the system.
5. Carefully slide the module straight out of the chassis.

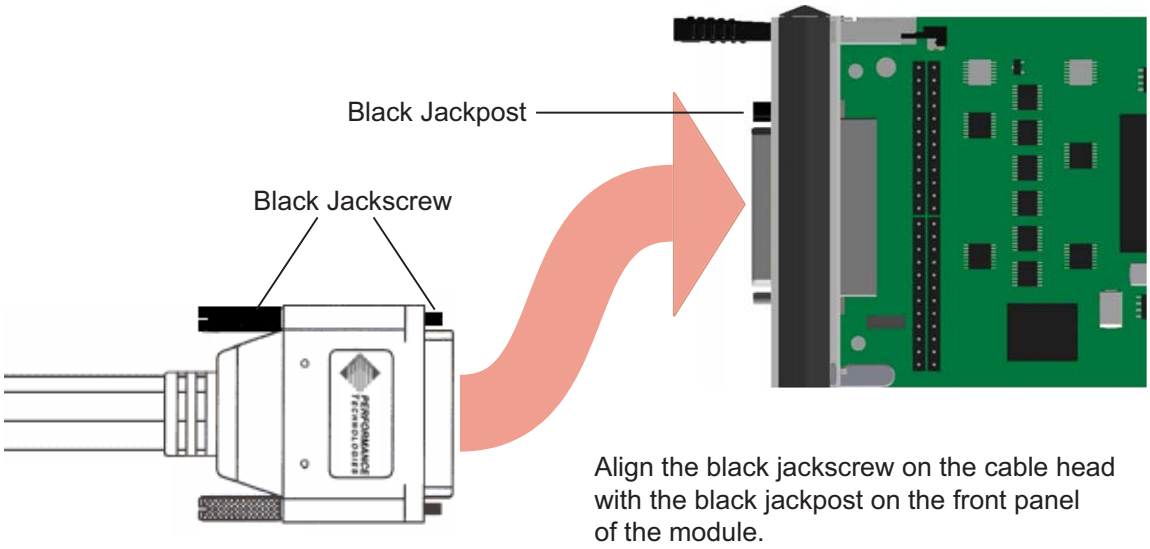
Note: *An extraction tool such as that manufactured by XTECH can aid in module removal.*

Connecting the Cable

See “AMC335 I/O Configurations and Accessories,” on page 18 for a list of the cables available for use with the AMC335. The AMC335 ships with the appropriate four-port hydra cable you have ordered. See “Serial Cable Connectors,” on page 88 for information about the various cable pinouts and connectors.

1. After installing the AMC335 in the host chassis, align the black jackscrew on the cable with the black jackpost on the front panel of the module (see Figure 3-2, “AMC335 Cable Alignment,” below).
2. Insert the cable into the dual VHDCI connector on the module.
3. Fasten the four jackscrews to secure the cable.

Figure 3-2: AMC335 Cable Alignment



Chapter

4

System Monitoring and Alarms

Overview

This chapter provides information about the Module Management Controller (MMC) device and how it uses the Intelligent Platform Management Interface (IPMI) to monitor the system and warn of problems with the AMC335.

Key topics in this chapter include:

MMC Functions

The MMC performs system monitoring and alarming functions using the flexible, industry standard, Intelligent Platform Management Interface (IPMI). The module comes equipped with an on-board MMC and IPMI v1.5 firmware already installed on the module. The MMC firmware is based on Pigeon Point System®'s (PPS) MMC firmware. Some of the functions available on the module through the IPMI interface include:

- Monitoring of the CPU and board temperatures with critical and non-critical alerting
- Monitoring of the voltage rails with critical and non-critical alerting
- Remote reset and shutdown of the module (hard and soft)

- Monitoring of ejector switches for hot-swap functionality (Performance Technologies' NexusWare IPMI driver and firmware provide additional payload features for hot swap)
- Monitoring and event reporting of critical errors
- Fabric and clock e-keying
- Interface to local IPMB (IPMB-L)

In order to take advantage of the features provided by the firmware, IPMI-aware applications must be developed. Information on IPMI v1.5 is provided at:

http://www.intel.com/design/servers/ipmi/spec.htm

Summary of Supported Commands

Table 4-1, "IPMI/PICMG Command Subset Supported by the MMC Firmware," lists all the commands supported by the MMC.

The **Spec Ref** column indicates where in the relevant specification a command is defined. IPMI references are to v1.5 unless indicated otherwise. The **MMC Req** column indicates if a particular command is required by the relevant specification (*AMC Specification* or *HPM.1 Specification*) or is optional.

See the various notes under the table for more information.

Table 4-1: IPMI/PICMG Command Subset Supported by the MMC Firmware

Command	Spec Ref	NetFn	CMD	MMC Req
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm Reset	17.3	App	03h	Optional
Broadcast "Get Device ID"[1]	17.9	App	01h	Mandatory
Messaging Commands				
Set BMC Global Enables	18.1	App	2Eh	Mandatory
Get BMC Global Enables	18.2	App	2Fh	Mandatory
Clear Message Flags	18.3	App	30h	Mandatory
Get Message Flags	18.4	App	31h	Mandatory
Get Message	18.6	App	33h	Mandatory
Send Message	18.7	App	34h	Mandatory
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory
Set Watchdog Timer	21.6	App	24h	Mandatory
Get Watchdog Timer	21.7	App	25h	Mandatory
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory
Get Event Receiver	23.2	S/E	01h	Mandatory
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory
Sensor Device Commands				

Table 4-1: IPMI/PICMG Command Subset Supported by the MMC Firmware (Continued)

Command	Spec Ref	NetFn	CMD	MMC Req
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Get Sensor Reading Factors	29.5	S/E	23h	Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU Data	28.2	Storage	11h	Mandatory
Write FRU Data	28.3	Storage	12h	Mandatory
AdvancedTCA Commands				
Get PICMG Properties	3-10	PICMG	00h	Mandatory
FRU Control	3-25	PICMG	04h	Mandatory
FRU Control Capabilities	3-24	PICMG	1Eh	Mandatory
Get FRU LED Properties	3-27	PICMG	05h	Mandatory
Get LED Color Capabilities	3-28	PICMG	06h	Mandatory
Set FRU LED State	3-29	PICMG	07h	Mandatory
Get FRU LED State	3-30	PICMG	08h	Mandatory
Get Device Locator Record ID[2]	3-35	PICMG	0Dh	Mandatory
AMC Commands				
Set AMC Port State	3-26	PICMG	19h	Optional/ Mandatory
Get AMC Port State	3-27	PICMG	1Ah	Optional/ Mandatory
Set Clock State	3-44	PICMG	2Ch	Optional/ Mandatory
Get Clock State	3-45	PICMG	2Dh	Optional/ Mandatory
HPM.1 Upgrade Commands (HPM.1)				
Get Target Upgrade Capabilities	3-3	PICMG	2Eh	Mandatory
Get Component Properties	3-5	PICMG	2Fh	Mandatory
Abort Firmware Upgrade	3-15	PICMG	30h	Optional
Initiate Upgrade Action[3]	3-8	PICMG	31h	Optional/ Mandatory
Upload Firmware Block	3-9	PICMG	32h	Mandatory
Finish Firmware Upload	3-10	PICMG	33h	Mandatory
Activate Firmware	3-11	PICMG	35h	Mandatory
Query Self-Test Results[4]	3-12	PICMG	36h	Optional/ Mandatory

Table 4-1: IPMI/PICMG Command Subset Supported by the MMC Firmware (Continued)

Command	Spec Ref	NetFn	CMD	MMC Req
Query Rollback Status[5]	3-13	PICMG	37h	Optional/ Mandatory
Initiate Manual Rollback[6]	3-14	PICMG	38h	Optional/ Mandatory

1. See "Device ID" below, for the device ID data retrieved in response to a **(Broadcast) Get Device ID** command for this module.
2. See "Device Locator Record" below, for the IPMB management controller device locator record retrieved in response to a **Get Device Locator Record ID** command for this module.
3. The HPM.1 **Initiate Upgrade Action** command is mandatory for an IPM Controller indicating that any of its implemented components supports preparation for Firmware Upgrade or comparison of the current firmware
4. The HPM.1 **Query Self-test Results** command is mandatory for IPM Controllers indicating self-test is supported in the Self-test capabilities field of the "Get target upgrade capabilities" response or the Self-test capabilities field of the Upgrade Image header.
5. The HPM.1 **Query Rollback Status** command is mandatory for IPM Controllers supporting automatic or manual Rollback.
6. The HPM.1 **Manual Firmware Rollback** command is mandatory for IPM Controllers indicating manual firmware Rollback is supported in the *Manual firmware Rollback* capabilities field of the "Get target upgrade capabilities" response.

Device Locator Record

The MMC firmware supports the **Get Device Locator Record ID** command for FRU device #0 (the only FRU device represented by an MMC). The MMC firmware obtains the ID of the IPMB management controller device locator record by scanning the Sensor Data Records (SDR) embedded into the firmware.

Table 4-2, "IPMB Management Controller Device Locator Record" shows an example of an IPMB management controller device locator record (SDR type 0x12) describing the properties of the MMC.

Table 4-2: IPMB Management Controller Device Locator Record

Parameter	Value
Power State Notification	
ACPI System Power State notification required	No
ACPI Device Power State notification required	No
Global Initialization	
Controller logs Initialization Agent errors	No
Log Initialization Agent errors accessing this controller	No
Event Generation	Enable event message generation from controller
Device Capabilities	
Chassis Device	No
Bridge	No
IPMB Event Generator	Yes
IPMB Event Receiver	No
FRU Inventory Device	Yes
SEL Device	No
SDR Repository Device	No
Sensor Device	Yes

Table 4-2: IPMB Management Controller Device Locator Record (Continued)

Parameter	Value
FRU Entity ID	0xC1
Entity Instance	(slot dependent)
OEM-specific	0
Device ID String Type/Length	8-bit ASCII with size of Device ID String *Note: See Table 4-3, "MMC Device ID" below.*
Device ID String	AMC335

Device ID

The MMC firmware provides the following device ID data in response to the (Broadcast) **Get Device ID** command, as shown in Table 4-3, "MMC Device ID" below.

Table 4-3: MMC Device ID

Parameter	Value
Device ID	0x00
Provides Device SDRs	Yes
Device Revision Number	0x00
Device Available	Yes
Firmware Revision	Changes with each release
IPMI Version	1.5
Additional Device Support	
Chassis Device	No
Bridge	No
IPMB Event Generator	Yes
IPMB Event Receiver	No
FRU Inventory Device	Yes
SEL Device	No
SDR Repository Device	No
Sensor Device	Yes
Manufacturer ID	0x000614
Product ID	0x000b
Auxiliary Firmware Revision Information	0x00000000

Sensors

Table 4-4, “MMC Sensors” lists the sensors and thresholds that are monitored by the MMC. Note that the sensor IDs are local to the MMC. The MMC's SDRs are inherited by the next level of management (MicroTCA MCMC or AMC carrier IPMC) and sensor IDs are reassigned.

Table 4-4: MMC Sensors

Sensor ID	Description	Lower Non-Recoverable Threshold	Lower Critical Threshold	Lower Non-Critical Threshold	Upper Non-Critical Threshold	Upper Critical Threshold	Upper Non-Recoverable Threshold
1	3.3 V MGMT	3 V	3.068 V	3.135 V	3.465 V	3.533 V	3.6 V
2	12 V	10 V	10.4 V	10.8 V	13.2 V	13.6 V	14 V
3	1.203 V	1.083 V	1.113 V	1.143 V	1.263 V	1.293 V	1.323 V
4	1.5 V	1.35 V	1.388 V	1.425 V	1.575 V	1.613 V	1.65 V
5	3.3 V	2.97 V	3.053 V	3.135 V	3.465 V	3.548 V	3.63 V
6	1.8 V	1.62 V	1.665 V	1.71 V	1.89 V	1.935 V	1.98 V
7	1.8 V CPLD	1.7 V	1.72 V	1.739 V	1.861 V	1.88 V	1.9 V
8	2.546 V	2.291 V	2.355 V	2.419 V	2.673 V	2.737 V	2.801 V
9	BMC Watchdog	NA	NA	NA	NA	NA	NA
10	Version Change	NA	NA	NA	NA	NA	NA
11	CPU Temp	-5 °C	0 °C	5 °C	65 °C	85 °C	95 °C
12	Inlet Temp	-5 °C	0 °C	5 °C	50 °C	70 °C	80 °C

Interpreting Sensor Events

The ATCA specification includes the following definitions for the sensor event severity levels:

- IPMI non-critical / PICMG 3.0 minor / telco minor – a warning that things are somewhat out of normal range, but not really a “problem” yet. See “Non-Critical Events” below.
- IPMI critical / PICMG 3.0 major / telco major – things are still in valid operating range, but are getting close to the edge; unit still operating within vendor-specified tolerances. See “Critical Events” below.
- IPMI non-recoverable / PICMG 3.0 critical / telco critical – unit no longer operating within vendor-specified tolerances. See “Non-Recoverable Events” below.

Non-Critical Events

Non-critical events are informative only. They do not indicate that the module is outside of its operating limits. In general, no action is required. However, in certain contexts, system or shelf management software may decide that preventive action should be taken. For example, if several modules in a shelf report upper non-critical temperature events, the shelf manager might decide to increase fan speed.

Critical Events

Critical events indicate that the module is still within its operating limits, but it is close to exceeding one of those limits. Possible action in this case is to closely monitor the alarming sensor and take more aggressive action if it approaches the non-recoverable threshold.

Non-Recoverable Events

Non-recoverable events indicate that the module may no longer be functioning because it is now outside of its operating limits. It is likely that action is required or has already been taken by the local hardware/firmware. For example, a processor may have shut itself down because its maximum die temperature was exceeded, or a shelf manager may decide to deactivate the module because the processor is too hot.

Serial Interface Subsystem

The MMC firmware implements a communication protocol over the payload and/or serial debug interfaces. The communication is in the form of formatted ASCII strings.

The Serial Interface Protocol Lite (SIPL) is based on the IPMI-defined Terminal Mode of the serial/modem interface. The following sections describe the SIPL:

- “Terminal Mode Messages and Commands,” on page 51
- “Terminal Mode Line Editing,” on page 52
- “Supported PPS Extension Commands,” on page 53

Terminal Mode Messages and Commands

Terminal Mode Message Format

Terminal Mode messages have the following format:

```
[<message data>]<newline>
```

The left bracket and the right bracket plus `<newline>` characters serve as START and STOP delimiters for a message. The MMC does not support multi-line IPMI messages.

Raw IPMI Messages

The SIPL supports raw IPMI messages that are entered as sequences of case-insensitive hex-ASCII pairs, each pair optionally separated from the previous one with a single `<space>` character. What follows are examples of raw IPMI request messages in Terminal Mode:

```
[18 00 22]<newline>
[180022]<newline>]
```

The MMC handles raw IPMI messages in the same way as it handles IPMI/PICMG/AMC messages coming from the IPMB-L bus and, with the exception that IPMI/PICMG/AMC replies are routed to the interfaces from which the respective requests have come (i.e. either the serial debug or payload interface of the MMC).

Terminal Mode Text Commands

The SIPL does not support Terminal Mode ASCII text commands defined by the *IPMI Specification (section 13.7.8)*.

Pigeon Point Systems (PPS) Extension Commands

The MMC firmware supports a set of PPS extension commands that are used to control and monitor the carrier Intelligent Platform Management Controller (IPMC) state over the serial debug interface. These commands are used to read the MMC status, implement graceful payload shutdown, etc.

The PPS extension commands are implemented as OEM IPMI commands with network function codes 2Eh/2Fh and message body transferred in the same manner as for raw IPMI messages (see "Raw IPMI Messages," on page 51). Figure 4-1, "PPS Extension Command Request," shows an example of a PPS extension command request:

Figure 4-1: PPS Extension Command Request

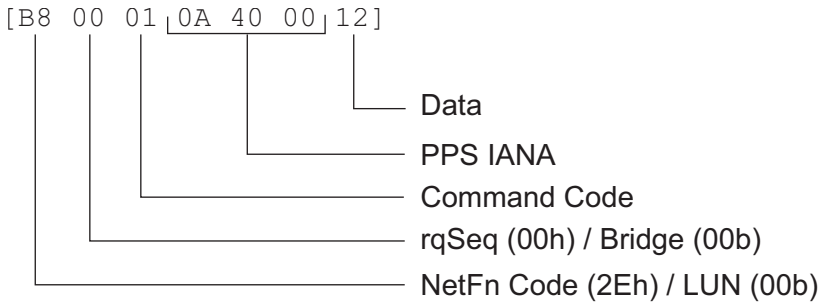
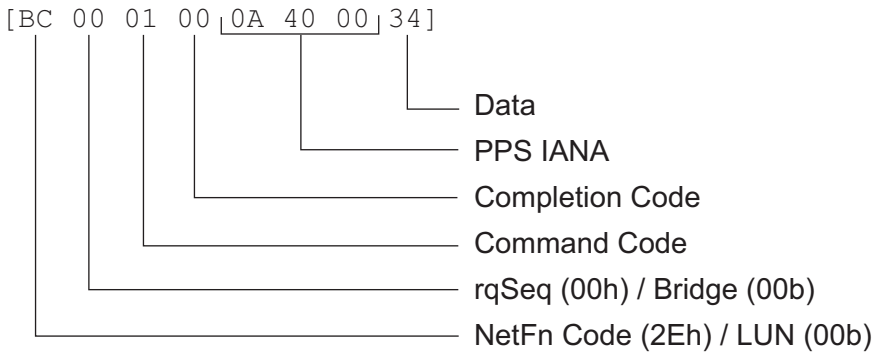


Figure 4-2, "PPS Extension Command Response," shows an example of a PPS extension command response:

Figure 4-2: PPS Extension Command Response



Terminal Mode Line Editing

The MMC does not support input line editing functionality defined as optional in the *IPMI Specification (section 13.8)*.

Supported PPS Extension Commands

The MMC firmware supports the following PPS extension commands (see “Pigeon Point Systems (PPS) Extension Commands,” on page 52):

Table 4-5: PPS Extension Commands Supported by the MMC

Command Request/Response	Code	Likely Command Source(s)	Description	See Also
Get Status	0x00	Serial debug and payload interfaces	Read the MMC status	Get Status Command
Get Serial Interface Properties	0x01	Serial debug and payload interfaces	Get the properties of a serial interface	Serial Line Properties Commands
Set Serial Interface Properties	0x02	Serial debug and payload interfaces	Set the properties of a serial interface	
Get Debug Level	0x03	Serial debug interface	Get debug/verbosity level	Debug/Verbosity Level
Set Debug Level	0x04	Serial debug interface	Set debug/verbosity level	
Get Payload Communication Timeout	0x09	Serial debug and payload interfaces	Get the timeout for payload communications	Payload Communication Timeout
Set Payload Communication Timeout	0x0A	Serial debug and payload interfaces	Set the timeout for payload communications	
Graceful Reset	0x11	Payload interface	The payload is ready to be shut down/reset	Graceful Payload Reset
Diagnostic Interrupt Results	0x12	Payload interface	Return diagnostic interrupt results	Payload Diagnostic Interrupt
Get Payload Shutdown Timeout	0x15	Serial debug and payload interfaces	Get the timeout for payload shutdown	Payload Shutdown Timeout
Set Payload Shutdown Timeout	0x16	Serial debug and payload interfaces	Set the timeout for payload shutdown	
Get Geographic Address	0x1F	Serial debug and payload interfaces	Get the geographic address	Get Geographic Address Command

The MMC accepts all PPS extension commands listed in Table 4-5 from both serial interfaces, as well as IPMB-L. This is done to achieve additional flexibility and extensibility in the MMC functionality.

The PPS extension commands listed in Table 4-5 are referred to as the SIPL commands throughout this document. The following sections discuss the SIPL commands in more detail.

Get Status Command

The MMC status is one byte describing the logical state of the MMC and the payload. Table 4-6, “MMC Status Bits,” provides a description of the MMC status bits:

Table 4-6: MMC Status Bits

Bit	Name	Description
0 (LSB)	Control	If set to 0, the MMC control over the payload is disabled.
1-2	NA	Reserved
3	Sensor Alert	If set to 1, indicates that at least one of the MMC sensors detects threshold crossing.
4	Reset Alert	If set to 1, indicates that the payload is going to be reset.
5	Shutdown Alert	If set to 1, indicates that the payload is going to be shut down.
6	Diagnostic Interrupt Request	If set to 1, indicates that a payload diagnostic interrupt request has arrived.
7 (MSB)	Graceful Reboot Request	If set to 1, indicates that the payload is requested to initiate the graceful reboot sequence.

The MMC firmware notifies the payload about changes of all status bits except for bits 0-2 by sending an unprintable character (ASCII 07, BELL) over the payload interface. The payload is expected to use the **Get Status** command to identify pending events and other SIPL commands to provide a response (if necessary). The event notification character is sent in a synchronous manner, and does not appear in the contents of SIPL messages sent to the payload.

The **Get Status** command has the following synopsis:

```
[B8 xx 00 0A 40 00]
```

The MMC responds to the **Get Status** command with the following reply:

```
[BC xx 00 00 0A 40 00 <status>]
```

Serial Line Properties Commands

The SIPL provides commands to get/set the properties of the MMC serial interfaces (the serial debug interface and the payload interface):

- "Get Serial Interface Properties Command," on page 55
- "Set Serial Interface Properties Command," on page 55

Get Serial Interface Properties Command

The **Get Serial Interface Properties** command is used to get the properties of a particular serial interface. This command has the following synopsis:

`[B8 xx 01 0A 40 00 <interface ID>]`

The `<interface ID>` parameter can have one of the values shown in Table 4-7, "The <interface ID> Parameter Values," below.

Table 4-7: The `<interface ID>` Parameter Values

Interface ID	Description
0	Serial debug interface
1	Payload interface

The MMC responds to the **Get Serial Interface Properties** command with the following reply:

`[BC xx 01 00 0A 40 00 <interface properties>]`

The `<interface properties>` parameter has the bit fields shown in Table 4-8, "The <interface properties> Parameter Bit Fields," below.

Table 4-8: The `<interface properties>` Parameter Bit Fields

Bits	Name	Description
0-3	Baud Rate ID	The baud rate ID defines the interface baud rate as follows: 0 – 9600 bps 1 – 19200 bps 2 – 38400 bps 3 – 57600 bps 4 – 115200 bps
4-6	NA	Reserved
7 (MSB)	Echo On	If this bit is set, the MMC enables echo for the given serial interface.

Set Serial Interface Properties Command

The **Set Serial Interface Properties** command is used to change the properties of a given interface:

`[B8 xx 02 0A 40 00 <interface ID> <interface properties>]`

Debug/Verbosity Level

The SIPL provides commands to enable and disable output of error/diagnostic messages to the serial debug interface at runtime:

- "Get Debug Level Command," on page 56
- "Set Debug Level Command," on page 56

Get Debug Level Command

To get the current debug level, the **Get Debug Level** command must be used. This command has the following synopsis:

```
[B8 xx 03 0A 40 00]
```

The MMC responds to the **Get Debug Level** command with the following reply:

```
[BC xx 03 00 0A 40 00 <debug level>]
```

The <debug level> parameter contains the bit fields shown in Table 4-9, "MMC Debug Levels," below.

Table 4-9: MMC Debug Levels

Bit	Name	Description
0 (LSB)	Error Logging Enable	If set to 1, the MMC outputs error/diagnostic messages onto the serial debug interface.
1	Low-level Error Logging Enable	If set to 1, the MMC outputs low-level error/diagnostic messages onto the serial debug interface.
2	Alert Logging Enable	If set to 1, the MMC outputs important alert messages onto the serial debug interface.
3	Payload Logging Enable	If set to 1, the MMC provides a trace of SIPL activity on the payload interface onto the serial debug interface.
4	IPMB Dump Enable	If set to 1, the MMC provides a trace of IPMB messages that are arriving to/going from the MMC via IPMB-L.
5-7	NA	Reserved

Set Debug Level Command

To change the current debug level, the **Set Debug Level** command must be used. This command has the following synopsis:

```
[B8 xx 04 0A 40 00 <debug level>]
```

Payload Communication Timeout

Some of the SIPL commands are subject to payload communication timeouts. If the payload does not respond with a correct reply within a definite period of time, the MMC assumes that a payload communication timeout occurred and acts accordingly. The SIPL timeout value also limits the period of time given to the payload to prepare for a payload reset.

- "Get Payload Communication Timeout Command," on page 57
- "Set Payload Communication Timeout Command," on page 57

Get Payload Communication Timeout Command

The MMC supports reading of the payload communication timeout using the **Get Payload Communication Timeout** command. This command has the following synopsis:

```
[B8 xx 09 0A 40 00]
```

The MMC responds to the **Get Payload Communication Timeout** command with the following reply:

```
[BC xx 09 00 0A 40 00 <payload timeout>]
```

The <payload timeout> parameter is the payload communication timeout measured in hundreds of milliseconds. Thus, the payload communication timeout may vary from 0.1 to 25.5 seconds. The default value of the payload communication timeout is specified by the CFG_APP_SIPL_PAYLOAD_TIMEOUT Configuration Parameter.

Set Payload Communication Timeout Command

To change the payload communication timeout, the **Set Payload Communication Timeout** command is used:

```
[B8 xx 0A 0A 40 00 <payload timeout>]
```

Graceful Payload Reset

The MMC supports the Graceful Reboot option of the **FRU Control** command. On receiving such a command, the MMC sets the Graceful Reboot Request bit of the MMC status, sends a status update notification to the payload, and waits for the **Graceful Reset** command from the payload. If the MMC receives such a command before the payload communication timeout time, it sends the 0x00 completion code (Success) to the carrier controller. Otherwise, the 0xC3 completion code (Timeout) is sent.

The **Graceful Reset** command has the following synopsis:

```
[B8 xx 11 0A 40 00]
```

Note that the MMC does not reset the payload on receiving the **Graceful Reset** command or timeout. If the MMC participation is necessary, the payload must request the MMC to perform a payload reset.

The **Graceful Reset** command is also used to notify the MMC about the completion of the payload shutdown sequence (refer to "Payload Shutdown Timeout," on page 58).

Payload Diagnostic Interrupt

The MMC supports the Issue Diagnostic Interrupt feature of the **FRU Control** command. The payload is notified about a diagnostic interrupt over the SIPL as described in “Get Status Command,” on page 54. The payload is expected to return diagnostic interrupt results before the payload communication timeout using the **Diagnostic Interrupt Results** command of the SIPL. This command has the following synopsis:

`[B8 xx 12 0A 40 00 <diagnostic interrupt return code>]`

If the payload responds before the payload communication timeout, the diagnostic interrupt return code is forwarded to the carrier controller as the completion code of the **FRU Control** command response. Otherwise, the 0xC3 completion code (Timeout) is returned.

Payload Shutdown Timeout

When the carrier controller commands the MMC to shut down the payload (i.e. sends the FRU Control (Quiesce) command), the MMC notifies the payload about it by asserting appropriate alert and sending an alert notification to the payload (refer to “Get Status Command,” on page 54). Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the **Graceful Reset** command (refer to “Graceful Payload Reset,” on page 57) to the MMC over the payload interface to notify the MMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the MMC provides a special timeout for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the MMC assumes that the payload shutdown sequence is finished, and sends a Module Quiesced hot-swap event to the carrier controller.

- “Get Payload Shutdown Timeout Command,” on page 58
- “Set Payload Shutdown Timeout Command,” on page 58

Get Payload Shutdown Timeout Command

The MMC supports reading of the payload shutdown timeout using the **Get Payload Shutdown Timeout** command. This command has the following synopsis:

`[B8 xx 15 0A 40 00]`

The MMC responds to the **Get Payload Shutdown Timeout** command with the following reply:

`[BC xx 15 00 0A 40 00 <LSB byte of timeout> <MSB byte of timeout>]`

The payload shutdown timeout is measured in hundreds of milliseconds and stored as a 2-byte integer. The default value of the payload shutdown timeout is specified by a dedicated Configuration Parameter.

Set Payload Shutdown Timeout Command

To change the payload shutdown timeout, the **Set Payload Shutdown Timeout** command is used:

`[B8 xx 16 0A 40 00 <LSB byte of timeout> <MSB byte of timeout>]`

Get Geographic Address Command

The MMC allows reading the geographic address of the module using the **Get Geographic Address** command, which has the following synopsis:

`[B8 xx 1F 0A 40 00]`

The MMC responds to the **Get IPMB Address** command with the following reply:

`[BC xx 1F 00 0A 40 00 <geographic address>]`

The `<geographic address>` parameter has the bit fields shown in Table 4-10, “The <geographic address> Parameter Bit Fields,” below.

Table 4-10: The <geographic address> Parameter Bit Fields

Bits	Name	Description
0-1	GA0 Signal	0 = GA0 is grounded 1 = GA0 is unconnected 3 = GA0 is pulled up
2-3	GA1 Signal	0 = GA1 is grounded 1 = GA1 is unconnected 3 = GA1 is pulled up
4-5	GA2 Signal	0 = GA2 is grounded 1 = GA2 is unconnected 3 = GA2 is pulled up
6-7	NA	Reserved

Firmware Upgrade Process

The MMC firmware supports a reliable field upgrade procedure compatible with the *HPM.1 Specification*. The key features of the firmware upgrade procedures are as follows:

- The upgrade can be performed over the serial debug/payload interface or over IPMB-L.
- The upgrade procedure is performed while the MMC firmware is online and operating normally.
- Upgrades of the firmware component are reliable. A failure in the download (error or interruption) does not disturb the MMC's ability to continue using the “old” firmware or its ability to restart the download process. Upgrades of the boot loader component are not reliable and may render the MMC non-functional in case of an incomplete upgrade.
- Upgrades of the firmware component are reversible. The MMC firmware automatically reverts back to the previous firmware if there is a problem when first running the new code and can be reverted manually using the HPM.1-defined **Manual Rollback** command. Upgrades of the boot loader component are not reversible.

HPM.1 Boot Loader

- The HPM.1 boot loader does not perform any upgrade actions
- The HPM.1 boot loader is able to boot either of two redundant copies of the MMC firmware in flash
- The HPM.1 boot loader is able to automatically rollback a failed copy of the MMC firmware and activate the backup one
- The HPM.1 boot loader can be upgraded in-field as an HPM.1-upgradeable component

HPM.1 Firmware Upgrade

The HPM.1 upgrade procedure is managed by a utility called the *upgrade agent*. The `ipmitool` utility is used as upgrade agent for upgrading the MMC firmware.

The upgrade agent communicates with the MMC firmware via serial interface or IPMB-L, and uses the ATCA commands that are described in the *HPM.1 Specification* for upgrading the firmware. Updated firmware is packed into a special image that has a format described in the *HPM.1 Specification*. That image is used by the upgrade agent to prepare and upgrade the MMC firmware. The HPM.1 upgrade procedure includes the following steps:

1. **Preparation step**. This step erases the region in the flash memory where a component will be written.
2. **Component upload step**. This step is designed to upload the component image via IPMB or a serial interface, and write it into the flash memory.
3. **Component activation step**. This step is designed to activate the previously upgraded component; for the firmware component, this step can be deferred until a later time.

The MMC firmware supports two upgradeable components: the firmware itself and the boot loader. In case of an unsuccessful firmware upgrade it is possible to roll back to the old firmware. This is not true for the boot loader.

Note: *Extreme caution should be exercised when upgrading the boot loader. There is no backup copy of the boot loader and if for any reason the boot loader upgrade procedure fails, the firmware becomes non-functional after reboot and must be reprogrammed over JTAG.*

Upgrade Utilities

The firmware upgrade procedure is performed using the upgrade agent utility, implementing the HPM.1 Upgrade Protocol and capable of programming custom firmware images into the flash memory of the MMC over a serial interface or IPMB-L. Any HPM.1-compatible Upgrade Agent can be used to upgrade the MMC firmware. It is recommended to use the `ipmitool` utility for these purposes. The `ipmitool` utility is available from Performance Technologies. Contact Performance Technologies Customer Support and Services for contact information.

The firmware image is supplied to the `ipmitool` utility in a single file called an HPM.1 upgrade image (for information about the format of HPM.1 upgrade images refer to the HPM.1 specification).

Detailed HPM.1 Upgrade Procedure

The following images are available from Performance Technologies:

- `hpm1fw.img` - this image contains the MMC firmware
- `hpm1boot.img` - this image contains the boot loader
- `hpm1all.img` - this image contains both the firmware and the boot loader

These images can be used to upgrade corresponding components of the IPMC: the firmware, the boot loader or both.

The following snapshot samples a command performing firmware upgrade from a Linux host over LAN/IPMB:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x7c -b 7 hpm
upgrade hpm1fw.img activate
PICMG HPM.1 Upgrade Agent 1.0:
Validating firmware image integrity...OK
Performing preparation stage...
    Services may be affected during upgrade. Do you with to continue?
y/n y...
OK
    Target Product ID : 15
    Target Manufacturer ID: 1556
Performing upgrade stage:
    Upgrading AVR-AMCm F/W
    with Version:   Major: 1
                    Minor: 70
                    Aux: 000 000 000 000
    Writing firmware: 100 % completed
Performing activation stage:
Firmware upgrade procedure successful
```

IPMI Communication Utility (ipmitool)

The `ipmitool` utility is a Linux application that can be used for a wide range of tasks involving IPMI-based communications. The following topics describe the installation process and provide information on specific applications of this utility.

Note: *Contact Performance Technologies Customer Support and Services for an enhanced version of `ipmitool`. Besides the standard functionality, it supports the following vendor-specific enhancements, which are not available in the official release (as of version 1.8.9):*

- *Support for the serial IPMI interface (Terminal Mode)*
- *Some improvements in HPM.1 upgrade protocol implementation.*
- *Support for double bridging via LAN for accessing MMCs through the Shelf Manager and carrier IPMC.*

The enhanced version is available in binary form for Windows and in source form for Linux.

Building the ipmitool Utility

Build and install the `ipmitool` utility on a Linux host system using the following procedure:

1. Unpack the source tarball obtained from the secure Web site and change to the `ipmitool` directory:

   `bash$ tar xzf <ipmitool_package_name>`

   `bash$ cd ipmitool`

2. Run the `configure` script to prepare for the build. The `--prefix=<dir>` option can be used to specify the directory where the resulting files are installed. If not specified, `/usr/local` is used (in this case, the installation requires root privileges).

   `bash$ ./configure --prefix=/home/user/ipmitool`

3. Run the **`make install`** command to build and install the `ipmitool` utility.

   `bash$ make install`

Accessing an MMC with ipmitool

The available access methods that can be used to communicate with the MMC depend on the MMC firmware configuration and overall system setup. The most frequently used access methods are the following:

- Via an Ethernet connection to a Shelf Manager that is able to access via IPMB-0 the carrier IPMC managing the MMC. See “Accessing an MMC via a Shelf Manager,” on page 62.

  This access method can be used from any Linux or Windows host that has an Ethernet connection to the Shelf Manager of the shelf in which the MMC is installed. In this access method, the `ipmitool` utility uses an Ethernet connection to the Shelf Manager to double bridge IPMI requests to the MMC over IPMB-0 and IPMB-L.
- Via the serial debug or serial payload interface of the MMC. See “Accessing an MMC via a Serial Interface,” on page 63.

  This access method can be used from any Linux or Windows host that has a serial connection with the MMC’s serial debug or serial payload interfaces. In this access method, the `ipmitool` utility uses a serial interface to directly access the MMC.

Accessing an MMC via a Shelf Manager

To access the MMC using an Ethernet connection to a Shelf Manager, the following parameters should be specified in the command line of the `ipmitool` utility:

`-I lan`

This command line parameter instructs the `ipmitool` utility to use Ethernet for communications with the MMC.

`-H <Shelf Manager IP>`

This command line parameter specifies the IP address of the Shelf Manager.

`-T <carrier IPMC address>`

This command line parameter specifies the remote transit address (IPMB-0 address of the carrier IPMC) to which requests should be bridged by the Shelf Manager.

`-B 0`

This command line parameter specifies the remote transit channel (with 0 designating IPMB-0) to which requests should be bridged by the Shelf Manager.

`-t <MMC address>`

This command line parameter specifies the remote target address (IPMB-L address of the MMC) to which requests should be bridged by the carrier IPMC.

`-b 7`

This command line parameter specifies the remote target channel (with 7 designating IPMB-L) to which requests should be bridged by the carrier IPMC.

`-A <authtype>`

This command line parameter forces the `ipmitool` to use a specific authentication type, which must, of course, be supported by the Shelf Manager.

For example, to fetch and print Sensor Device Records of an MMC at IPMB-L address `0x72` via a Shelf Manager with the IP address `192.168.0.2`, and a carrier IPMC at IPMB-0 address `0x82`, the following command line should be used:

```
# ipmitool –I lan –H 192.168.0.2 –T 0x82 –B 0 –t 0x72 –b 7 –A none sdr
```

Accessing an MMC via a Serial Interface

The following `ipmitool` command line parameters are used for communicating with the MMC via a serial interface:

```
-I serial-terminal
```

This command line parameter instructs the `ipmitool` utility to use the serial interface for communications with the MMC.

`-D <dev[:baudrate]>`

This command line parameter specifies the serial device and baud rate settings to use. For Linux hosts, the serial device is the system path to the device node (e.g. **/dev/ttyS0**). For the Cygwin-flavor of the `ipmitool` utility, Windows serial device names are translated as follows: the COM1 device name is mapped to **/dev/ttyS0**, COM2 is mapped to **/dev/ttyS1** and so on.

The supported baud rates are: 2400, 9600, 19200, 38400, 57600, and 115200.

For example, to fetch and print Sensor Device Records of an MMC via a serial interface connection with a baud rate of 9600, the following command line should be used:

```
# ipmitool –I serial-terminal –D /dev/ttyS0:9600 sdr
```

Using ipmitool for HPM.1 Upgrades

The `ipmitool` utility has built-in HPM.1 upgrade functionality and can be used as an upgrade agent. To be able to send HPM.1 commands to the MMC, the proper connection options should be specified in the `ipmitool` command line.

See “Accessing an MMC with ipmitool,” on page 62 for the list of available `ipmitool` command line connection options.

HPM.1 Commands

The `ipmitool` utility supports the following HPM.1 commands, which are described on the following pages:

targetcap

Get the target upgrade capabilities. This command can be used to find out the upgrade capabilities of an MMC.

```
ipmitool hpm targetcap
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
targetcap
PICMG HPM.1 Upgrade Agent 1.0:
TARGET UPGRADE CAPABILITIES
------------------------------
HPM.1 version.............0
Component 0 presence....[y]
Component 1 presence....[y]
Component 2 presence....[n]
Component 3 presence....[n]
Component 4 presence....[n]
Component 5 presence....[n]
Component 6 presence....[n]
Component 7 presence....[n]
Upgrade undesirable.....[n]
Aut rollback override...[n]
IPMC degraded...........[n]
Defered[1] activation......[y]
Service affected........[y]
Manual rollback.........[y]
Automatic rollback......[y]
Self test...............[n]
Upgrade timeout.........[100 sec]
Self test timeout.......[0 sec]
Rollback timeout........[5 sec]
Inaccessibility timeout.[5 sec]
```

1. “Defered” is misspelled in the `ipmitool` utility.

compprop

Get the specified component properties. This command can be used to find out component-specific properties.

```
ipmitool hpm compprop <id> <select>
```

The <id> parameter specifies the component whose properties are read; 0 corresponds to the firmware component and 1 corresponds to the boot loader component. The <select> parameter specifies the property that should be acquired. The properties are the following:

0	General properties
1	Current firmware version
2	Description string
3	Rollback firmware version
4	Deferred firmware version

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
compprop 0 0
PICMG HPM.1 Upgrade Agent 1.0:
GENERAL PROPERTIES
------------------------------
Payload cold reset req....[y]
Def. activation supported.[y]
Comparison supported......[n]
Preparation supported.....[y]
Rollback supported........[y]
```

upgrade

Upgrade the firmware with the specified image. This command can be used to upgrade the firmware using a valid HPM.1 image.

```
ipmitool hpm upgrade <file> [activate]
```

The `<file>` parameter specifies the name of the HPM.1 upgrade image. If the `[activate]` parameter is specified, the upgraded firmware is activated just after the upgrade procedure. In the other case, an additional command should be issued to activate the firmware.

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
upgrade hpm1fw.img
Validating firmware image integrity...OK
Performing preparation stage...
    Services may be affected during upgrade. Do you wish to continue?
y/n y
OK
    Target Product ID     : 15
    Target Manufacturer ID: 1556
Performing upgrade stage:
    Upgrading AVR-AMCm F/W
    with Version: Major: 0
                  Minor: 5
                  Aux  : 000 000 000 000
    Writing firmware: 100 % completed
```

activate

Activate the newly uploaded firmware. This command can be used for activating the newly uploaded firmware if there was no activate parameter passed to the upgrade command.

```
ipmitool hpm activate
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
activate
PICMG HPM.1 Upgrade Agent 1.0:
```

rollback

Perform a manual rollback on the IPM controller. This command can be used to roll back from the newly uploaded firmware to the old one.

```
ipmitool hpm rollback
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
rollback
PICMG HPM.1 Upgrade Agent 1.0:
```

rollbackstatus

Query the rollback status. This command can be used to query the firmware on the IPMC about whether a rollback event has occurred.

```
ipmitool hpm rollbackstatus
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm
rollbackstatus
PICMG HPM.1 Upgrade Agent 1.0:
Rollback occured[2] on component mask: 0x01
```

2. “occured” is misspelled in the `ipmitool` utility.

Chapter

5

Connectors

Overview

The AMC335 includes several connectors to interface with application-specific devices. The connectors discussed in this chapter are shown in Table 5-1, “AMC335 Connector Assignments,” below.

Table 5-1: AMC335 Connector Assignments

Connector	Location
“AdvancedMC Card Edge Connector,” on page 70	Card Edge
“Serial I/O Connector,” on page 73 • “RS232C Supported Signals,” on page 74 • “RS422/RS449 Supported Signals,” on page 77 • “V.35 Supported Signals,” on page 83	Front Panel
“Console Serial Port,” on page 88	Bottom Side
“Serial Cable Connectors,” on page 88 • “RS232C Hydra Cable Connector,” on page 89 • “RS449 (RS422) Hydra Cable Connector,” on page 90 • “EIA530 Hydra Cable Connector,” on page 91 • “V.35 Hydra Cable Connector,” on page 92 • “Console Cable Option,” on page 93	Cables

A detailed description and pinout for each connector is given in the topics that follow.

AdvancedMC Card Edge Connector

The AMC connector provides the electrical interface between the AMC335 and the MicroTCA enclosure or ATCA carrier board. The AMC connector is fixed to the enclosure or carrier board and the card edge interface at the back of the AMC335 plugs into it. There are different styles of connectors for the different types of AMC bays and for different levels of connectivity. The card edge interface on the AMC335 is compatible with the extended, 170 pin B+ style connector found on Performance Technologies' AMP507x MicroTCA platform.

Besides power and ground, the AMC335 card edge interface routes two SerDes 1Gb Ethernet channels, PCI Express x1 bus, and System Management Bus (SMB) to the AMC connector.

See Table 5-2, "AMC Connector Pinout," on page 70 for pin definitions.

Table 5-2: AMC Connector Pinout

Pin	Signal	Driven By	Mating	Pin Function on Module	Pin	Signal	Driven By	Mating	Pin Function on Module
1	GND		First	Logic Ground	170	GND		First	Logic Ground
2	PWR	Carrier	First	Payload Pwr	169	TDI	Carrier	Second	JTAG Test Data Input
3	PS1#	Module	Last	Presence 1	168	TDO	Module	Second	JTAG Test Data Output
4	MP	Carrier	First	Mgmt Power	167	TRST#	Carrier	Second	JTAG Test Reset Input
5	GA0	Carrier	Second	Geo. Addr. 0	166	TMS	Carrier	Second	JTAG Test Mode Select In
6	RSRVD6		Second	Reserved, n/a	165	TCK	Carrier	Second	JTAG Test Clock Input
7	GND		First	Logic Ground	164	GND		First	Logic Ground
8	RSRVD8		Second	Reserved, n/a	163	TX20+		Third	Port 20 TX +
9	PWR	Carrier	First	Payload Pwr	162	TX20-		Third	Port 20 TX -
10	GND		First	Logic Ground	161	GND		First	Logic Ground
11	TX0+		Third	Port 0 TX +	160	RX20+		Third	Port 20 RX +
12	TX0-		Third	Port 0 TX -	159	RX20-		Third	Port 20 RX -
13	GND		First	Logic Ground	158	GND		First	Logic Ground
14	RX0+		Third	Port 0 RX +	157	TX19+		Third	Port 19 TX +
15	RX0-		Third	Port 0 RX -	156	TX19-		Third	Port 19 TX -
16	GND		First	Logic Ground	155	GND		First	Logic Ground
17	GA1	Carrier	Second	Geo. Addr. 1	154	RX19+		Third	Port 19 RX +
18	PWR	Carrier	First	Payload Pwr	153	RX19-		Third	Port 19 RX -
19	GND		First	Logic Ground	152	GND		First	Logic Ground
20	TX1+		Third	Port 1 TX +	151	TX18+		Third	Port 18 TX +
21	TX1-		Third	Port 1 TX -	150	TX18-		Third	Port 18 TX -
22	GND		First	Logic Ground	149	GND		First	Logic Ground
23	RX1+		Third	Port 1 RX +	148	RX18+		Third	Port 18 RX +
24	RX1-		Third	Port 1 RX -	147	RX18-		Third	Port 18 RX -
25	GND		First	Logic Ground	146	GND		First	Logic Ground
26	GA2	Carrier	Second	Geo. Addr. 2	145	TX17+		Third	Port 17 TX +
27	PWR	Carrier	First	Payload Pwr	144	TX17-		Third	Port 17 TX -
28	GND		First	Logic Ground	143	GND		First	Logic Ground
29	TX2+		Third	Port 2 TX +	142	RX17+		Third	Port 17 RX +
30	TX2-		Third	Port 2 TX -	141	RX17-		Third	Port 17 RX -

Table 5-2: AMC Connector Pinout (Continued)

Pin	Signal	Driven By	Mating	Pin Function on Module	Pin	Signal	Driven By	Mating	Pin Function on Module
31	GND		First	Logic Ground	140	GND		First	Logic Ground
32	RX2+		Third	Port 2 RX +	139	TCLKD+		Third	Port 16 TX +
33	RX2-		Third	Port 2 RX -	138	TCLKD-		Third	Port 16 TX -
34	GND		First	Logic Ground	137	GND		First	Logic Ground
35	TX3+		Third	Port 3 TX +	136	TCLKC+		Third	Port 16 RX +
36	TX3-		Third	Port 3 TX -	135	TCLKC-		Third	Port 16 RX -
37	GND		First	Logic Ground	134	GND		First	Logic Ground
38	RX3+		Third	Port 3 RX +	133	TX15+		Third	Port 15 TX +
39	RX3-		Third	Port 3 RX -	132	TX15-		Third	Port 15 TX -
40	GND		First	Logic Ground	131	GND		First	Logic Ground
41	ENABLE#	Carrier	Second	AMC Enable	130	RX15+		Third	Port 15 RX +
42	PWR	Carrier	First	Payload Pwr	129	RX15-		Third	Port 15 RX -
43	GND		First	Logic Ground	128	GND		First	Logic Ground
44	TX4+		Third	Port 4 TX +	127	TX14+		Third	Port 14 TX +
45	TX4-		Third	Port 4 TX -	126	TX14-		Third	Port 14 TX -
46	GND		First	Logic Ground	125	GND		First	Logic Ground
47	RX4+		Third	Port 4 RX +	124	RX14+		Third	Port 14 RX +
48	RX4-		Third	Port 4 RX -	123	RX14-		Third	Port 14 RX -
49	GND		First	Logic Ground	122	GND		First	Logic Ground
50	TX5+		Third	Port 5 TX +	121	TX13+		Third	Port 13 TX +
51	TX5-		Third	Port 5 TX -	120	TX13-		Third	Port 13 TX -
52	GND		First	Logic Ground	119	GND		First	Logic Ground
53	RX5+		Third	Port 5 RX +	118	RX13+		Third	Port 13 RX +
54	RX5-		Third	Port 5 RX -	117	RX13-		Third	Port 13 RX -
55	GND		First	Logic Ground	116	GND		First	Logic Ground
56	SCL_L IPMI Agent		Second	IPMB-L Clock	115	TX12+		Third	Port 12 TX +
57	PWR	Carrier	First	Payload Pwr	114	TX12-		Third	Port 12 TX -
58	GND		First	Logic Ground	113	GND		First	Logic Ground
59	TX6+		Third	Port 6 TX +	112	RX12+		Third	Port 12 RX +
60	TX6-		Third	Port 6 TX -	111	RX12-		Third	Port 12 RX -
61	GND		First	Logic Ground	110	GND		First	Logic Ground
62	RX6+		Third	Port 6 RX +	109	TX11+		Third	Port 11 TX +
63	RX6-		Third	Port 6 RX -	108	TX11-		Third	Port 11 TX -
64	GND		First	Logic Ground	107	GND		First	Logic Ground
65	TX7+		Third	Port 7 TX +	106	RX11+		Third	Port 11 RX +
66	TX7-		Third	Port 7 TX -	105	RX11-		Third	Port 11 RX -
67	GND		First	Logic Ground	104	GND		First	Logic Ground
68	RX7+		Third	Port 7 RX +	103	TX10+		Third	Port 10 TX +
69	RX7-		Third	Port 7 RX -	102	TX10-		Third	Port 10 TX -
70	GND		First	Logic Ground	101	GND		First	Logic Ground
71	SDA_L IPMI Agent		Second	IPMB-L Data	100	RX10+		Third	Port 10 RX +

Table 5-2: AMC Connector Pinout (Continued)

Pin	Signal	Driven By	Mating	Pin Function on Module	Pin	Signal	Driven By	Mating	Pin Function on Module
72	PWR	Carrier	First	Payload Pwr	99	RX10-		Third	Port 10 RX -
73	GND		First	Logic Ground	98	GND		First	Logic Ground
74	TCLKA+		Third	Sync Clock 1+	97	TX9+		Third	Port 9 TX +
75	TCLKA-		Third	Sync Clock 1-	96	TX9-		Third	Port 9 TX -
76	GND		First	Logic Ground	95	GND		First	Logic Ground
77	TCLKB+		Third	Sync Clock 2+	94	RX9+		Third	Port 9 RX +
78	TCLKB-		Third	Sync Clock 2-	93	RX9-		Third	Port 9 RX -
79	GND		First	Logic Ground	92	GND		First	Logic Ground
80	FCLKA+		Third	Sync Clock 3+	91	TX8+		Third	Port 8 TX +
81	FCLKA-		Third	Sync Clock 3-	90	TX8-		Third	Port 8 TX -
82	GND		First	Logic Ground	89	GND		First	Logic Ground
83	PS0#	Carrier	Last	Presence 0	88	RX8+		Third	
84	PWR	Carrier	First	Payload Pwr	87	RX8-		Third	Port 8 RX +
85	GND		First	Logic Ground	86	GND		First	Port 8 RX -

Note: *Shaded areas in table denote unused pins.*

Serial I/O Connector

The dual VHDCI connector assumes different configurations depending on which communication standard is employed. The following communications standards are supported on the AMC335:

- “RS232C Supported Signals,” on page 74
- “RS422/RS449 Supported Signals,” on page 77
- “V.35 Supported Signals,” on page 83

See Chapter 6, “MPC8270 Parallel I/O Ports,” on page 95 for information about the two general-purpose serial management controllers and the pin assignments for the four general-purpose parallel I/O ports on the MPC8270.

Cable Type Indicator Pins

There are four pins on the dual VHDCI connector that indicate what type of cable is plugged into the I/O port. The decode of these pins can be read by the software package supplied for the module in the Flash Sector Protect, BUSY/RDY and Cable Type register.

Table 5-3, “Cable Type Indicator Pins,” describes the cable type mappings.

Table 5-3: Cable Type Indicator Pins

PIN T51 Cabtyp3	PIN T52 Cabtyp2	PIN B51 Cabtyp1	PIN B52 Cabtyp0	Cable Type
1	1	1	1	Cable Unplugged
1	0	0	0	RS422 DTE
0	1	0	0	RS232C DTE
1	1	0	0	V.35 DTE
1	0	0	0	EIA530

RS232C Supported Signals

This configuration supports the RS232C standard in a DTE format. Table 5-4, “RS232C Signals and Pins,” shows the supported signals and their positions on the dual VHDCI connector.

Note: *Some of the pins on the connector are not included in the table. For each electrical standard, the pins that are not included in the table for that standard MUST BE LEFT UNCONNECTED.*

Table 5-4: RS232C Signals and Pins

Pin	Signal Name	Direction	Termination	Description
B3, B6, B9, B12, B15, B16, B19, B20, B23, B26, B29, B32, B37, B40,B46, B49, B50, B53, B54, B60, B63, B66, T3, T6, T12, T15, T16, T19, T20, T26, T29, T32, T37, T40, T43, T46, T49, T50, T53, T54, T57, T60, T63, T66			Signal Ground	
B64	RXD1	Input	5K to Ground	RS232C Receive Data port 1 RS232 BB
B55	DTR1	Output	NA	RS232C Data Terminal Ready port 1 RS232 CD
B58	TXD1	Output	NA	RS232C Transmit Data port 1 RS232 BA
B24	RTS1	Output	NA	RS232C Request to Send port 1 RS232 CA
B21	TXC1	Output	NA	RS232C Transmit Data Clock port 1 RS232 DA
B27	TXCI1	Input	5K to Ground	RS232C Transmit Signal Element Timing 1 RS232 DB
B30	DCD1	Input	5K to Ground	RS232C Data Carrier Detect port 1 RS232 CF
B67	DSR1	Input	5K to Ground	RS232C Data Set Ready port 1 RS232 CC
B61	CTS1	Input	5K to Ground	RS232C Clear to Send port 1 RS232 CB
B57	GND			Signal Ground for I/O connector RS232 AB
B33	RXC1	Input	5K to Ground	RS232C Receive Data Clock port 1 RS232 DD

Table 5-4: RS232C Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B39	RXD2	Input	5K to Ground	RS232C Receive Data port 2 RS232 BB
B48	DTR2	Output	NA	RS232C Data Terminal Ready port 2 RS232 CD
B45	TXD2	Output	NA	RS232C Transmit Data port 2 RS232 BA
B11	RTS2	Output	NA	RS232C Request to Send port 2 RS232 CA
B14	TXC2	Output	NA	RS232C Transmit Data Clock port 2 RS232 DA
B8	TXCI2	Input	5K to Ground	RS232C Transmit Signal Element Timing 2 RS232 DB
B5	DCD2	Input	5K to Ground	RS232C Data Carrier Detect port 2 RS232 CF
B36	DSR2	Input	5K to Ground	RS232C Data Set Ready port 2 RS232 CC
B42	CTS2	Input	5K to Ground	RS232C Clear to Send port 2 RS232 CB
B43	GND			Signal Ground for I/O connector RS232 AB
B2	RXC2	Input	5K to Ground	RS232C Receive Data Clock port 2 RS232 DD
T5	RXD3	Input	5K to Ground	RS232C Receive Data port 3 RS232 BB
T14	DTR3	Output	NA	RS232C Data Terminal Ready port 3 RS232 CD
T11	TXD3	Output	NA	RS232C Transmit Data port 3 RS232 BA
T45	RTS3	Output	NA	RS232C Request to Send port 3 RS232 CA
T48	TXC3	Output	NA	RS232C Transmit Data Clock port 3 RS232 DA
T42	TXCI3	Input	5K to Ground	RS232C Transmit Signal Element Timing 3 RS232 DB
T39	DCD3	Input	5K to Ground	RS232C Data Carrier Detect port 31 RS232 CF
T2	DSR3	Input	5K to Ground	RS232C Data Set Ready port 3 RS232 CC
T8	CTS3	Input	5K to Ground	RS232C Clear to Send port 3 RS232 CB
T9	GND			Signal Ground for I/O connector RS232AB
T36	RXC3	Input	5K to Ground	RS232C Receive Data Clock port 3 RS232 DD
T30	RXD4	Input	5K to Ground	RS232C Receive Data port 4 RS232 BB

Table 5-4: RS232C Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
T21	DTR4	Output	NA	RS232C Data Terminal Ready port 4 RS232 CD
T24	TXD4	Output	NA	RS232C Transmit Data port 4 RS232 BA
T58	RTS4	Output	NA	RS232C Request to Send port 4 RS232CA
T55	TXC4	Output	NA	RS232C Transmit Data Clock port 4 RS232 DA
T61	TXCI4	Input	5K to Ground	RS232C Transmit Signal Element Timing 4 RS232 DB
T64	DCD4	Input	5K to Ground	RS232C Data Carrier Detect port 4 RS232 CF
T33	DSR4	Input	5K to Ground	RS232C Data Set Ready port 4 RS232 CC
T27	CTS4	Input	5K to Ground	RS232C Clear to Send port 4 RS232 CB
T23	GND			Signal Ground for I/O connector RS232AB
T67	RXC4	Input	5K to Ground	RS232C Receive Data Clock port 4 RS232 DD

RS422/RS449 Supported Signals

This configuration supports the RS422/RS449 standard in a DTE format. The EIA530 standard is also supported through a hydra cabling option. Table 5-5, “RS422/RS449/EIA530 Signals and Pins,” shows the supported signals and their positions on the dual VHDCI connector.

Note: *Some of the pins on the connector may not be included in the table. For each electrical standard, the pins that are not included in the table for that standard MUST BE LEFT UNCONNECTED.*

Table 5-5: RS422/RS449/EIA530 Signals and Pins

Pin	Signal Name	Direction	Termination	Description
B3, B6, B9, B12, B15, B16, B19, B20, B23, B26, B29, B32, B37, B40, B46, B49, B50, B53, B54, B60, B63, B66, T3, T6, T12, T15, T16, T19, T20, T26, T29, T32, T37, T40, T43, T46, T49, T50, T53, T54, T57, T60, T63, T66			Signal Ground	
B57	GND			Signal Ground for I/O connector
B64	RXD(A)1	Input	100 Ohms differential	RS422 Receive Data- port 1 RS449 RD(A) RSEIA530 BB(A)
B65	RXD(B)1	Input	100 Ohms differential	RS422 Receive Data+ port 1 RS449 RD(B) EIA530 BB(B)
B55	DTR(A)1	Output	NA	RS422 DTR- port 1 RS449 TR(A) EIA530 CD(A)
B56	DTR(B)1	Output	NA	RS422 DTR+ port 1 RS449 TR(B) EIA530 CD(B)
B58	TXD(A)1	Output	NA	RS422 Transmit Data- port 1 RS449 SD(A) EIA530 BA(A)
B59	TXD(B)1	Output	NA	RS422 Transmit Data+ port 1 RS449 SD(B) EIA530 BA(B)
B24	RTS(A)1	Output	NA	RS422 RTS- port 1 RS449 RS(A) EIA530 CA(A)
B25	RTS(B)1	Output	NA	RS422 RTS+ port 1 RS449 RS(B) EIA530 CA(B)

Table 5-5: RS422/RS449/EIA530 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B21	TXC(A)1	Output	NA	RS422 TXC- port 1 RS449 TT(A) EIA530 DA(A)
B22	TXC(B)1	Output	NA	RS422 TXC+ port 1 RS449 TT(B) EIA530 DA(B)
B27	TXCI(A)1	Input	100 Ohms differential	RS422 SCTE- port 1 RS449 ST(A) EIA530 DB(A)
B28	TXCI(B)1	Input	100 Ohms differential	RS422 SCTE + port 1 RS449 ST(B) EIA530 DB(B)
B30	DCD(A)1	Input	100 Ohms differential	RS422 DCD- port 1 RS449 RR(A) EIA530 CF(A)
B31	DCD(B)1	Input	100 Ohms differential	RS422 DCD+ port 1 RS449 RR(B) EIA530 CF(B)
B67	DSR(A)1	Input	100 Ohms differential	RS422 DSR- port 1 RS449 DM(A) EIA530 CC(A)
B68	DSR(B)1	Input	100 Ohms differential	RS422 DSR+ port 1 RS449 DM(B) EIA530 CC(B)
B61	CTS(A)1	Input	100 Ohms differential	RS422 CTS- port 1 RS449 CS(A) EIA530 CB(A)
B62	CTS(B)1	Input	100 Ohms differential	RS422 CTS+ port 1 RS449 CS(B) EIA530 CB(B)
B33	RXC(A)1	Input	100 Ohms differential	RS422 RXC- port 1 RS449 RT(A) EIA530 DD(A)
B34	RXC(B)1	Input	100 Ohms differential	RS422 RXC+ port 1 RS449 RT(B) EIA530 DD(B)
B43	GND			Signal Ground for I/O connector
B39	RXD(A)2	Input	100 Ohms differential	RS422 Receive Data- port 2 RS449 RD(A) EIA530 BB(A)
B38	RXD(B) 2	Input	100 Ohms differential	RS422 Receive Data+ port 2 RS449 RD(B) EIA530 BB(B)
B48	DTR(A) 2	Output	NA	RS422 DTR- port 2 RS449 TR(A) EIA530 CD(A)

Table 5-5: RS422/RS449/EIA530 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B47	DTR(B) 2	Output	NA	RS422 DTR+ port 2 RS449 TR(B) EIA530 CD(B)
B45	TXD(A) 2	Output	NA	RS422 Transmit Data- port 2 RS449 SD(A) EIA530 BA(A)
B44	TXD(B) 2	Output	NA	RS422 Transmit Data+ port 2 RS449 SD(B) EIA530 BA(B)
B11	RTS(A) 2	Output	NA	RS422 RTS- port 2 RS449 RS(A) EIA530 CA(A)
B10	RTS(B) 2	Output	NA	RS422 RTS+ port 2 RS449 RS(B) EIA530 CA(B)
B14	TXC(A) 2	Output	NA	RS422 TXC- port 2 RS449 TT(A) EIA530 DA(A)
B13	TXC(B) 2	Output	NA	RS422 TXC+ port 2 RS449 TT(B) EIA530 DA(B)
B8	TXCI(A) 2	Input	100 Ohms differential	RS422 SCTE- port 2 RS449 ST(A) EIA530 DB(A)
B7	TXCI(B) 2	Input	100 Ohms differential	RS422 SCTE + port 2 RS449 ST(B) EIA530 DB(B)
B5	DCD(A) 2	Input	100 Ohms differential	RS422 DCD- port 2 RS449 RR(A) EIA530 CF(A)
B4	DCD(B) 2	Input	100 Ohms differential	RS422 DCD+ port 2 RS449 RR(B) EIA530 CF(B)
B36	DSR(A) 2	Input	100 Ohms differential	RS422 DSR- port 2 RS449 DM(A) EIA530 CC(A)
B35	DSR(B) 2	Input	100 Ohms differential	RS422 DSR+ port 2 RS449 DM(B) EIA530 CC(B)
B42	CTS(A) 2	Input	100 Ohms differential	RS422 CTS- port 2 RS449 CS(A) EIA530 CB(A)
B41	CTS(B) 2	Input	100 Ohms differential	RS422 CTS+ port 2 RS449 CS(B) EIA530 CB(B)
B2	RXC(A) 2	Input	100 Ohms differential	RS422 RXC- port 2 RS449 RT(A) EIA530 DD(A)

Table 5-5: RS422/RS449/EIA530 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B1	RXC(B) 2	Input	100 Ohms differential	RS422 RXC+ port 2 RS449 RT(B) EIA530 DD(B)
T9	GND			Signal Ground for I/O connector
T5	RXD(A) 3	Input	100 Ohms differential	RS422 Receive Data- port 3 RS449 RD(A) EIA530 BB(A)
T4	RXD(B) 3	Input	100 Ohms differential	RS422 Receive Data+ port 3 RS449 RD(B) EIA530 BB(B)
T14	DTR(A) 3	Output	NA	RS422 DTR- port 3 RS449 TR(A) EIA530 CD(A)
T13	DTR(B) 3	Output	NA	RS422 DTR+ port 3 RS449 TR(B) EIA530 CD(B)
T11	TXD(A) 3	Output	NA	RS422 Transmit Data- port 3 RS449 SD(A) EIA530 BA(A)
T10	TXD(B) 3	Output	NA	RS422 Transmit Data+ port 3 RS449 SD(B) EIA530 BA(B)
T45	RTS(A) 3	Output	NA	RS422 RTS- port 3 RS449 RS(A) EIA530 CA(A)
T44	RTS(B) 3	Output	NA	RS422 RTS+ port 3 RS449 RS(B) EIA530 CA(B)
T48	TXC(A) 3	Output	NA	RS422 TXC- port 3 RS449 TT(A) EIA530 DA(A)
T47	TXC(B) 3	Output	NA	RS422 TXC+ port 3 RS449 TT(B) EIA530 DA(B)
T42	TXCI(A) 3	Input	100 Ohms differential	RS422 SCTE- port 3 RS449 ST(A) EIA530 DB(A)
T41	TXCI(B) 3	Input	100 Ohms differential	RS422 SCTE + port 3 RS449 ST(B) EIA530 DB(B)
T39	DCD(A) 3	Input	100 Ohms differential	RS422 DCD- port 3 RS449 RR(A) EIA530 CF(A)
T38	DCD(B) 3	Input	100 Ohms differential	RS422 DCD+ port 3 RS449 RR(B) EIA530 CF(B)

Table 5-5: RS422/RS449/EIA530 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
T2	DSR(A) 3	Input	100 Ohms differential	RS422 DSR- port 3 RS449 DM(A) EIA530 CC(A)
T1	DSR(B) 3	Input	100 Ohms differential	RS422 DSR+ port 3 RS449 DM(B) EIA530 CC(B)
T8	CTS(A) 3	Input	100 Ohms differential	RS422 CTS- port 3 RS449 CS(A) EIA530 CB(A)
T7	CTS(B) 3	Input	100 Ohms differential	RS422 CTS+ port 3 RS449 CS(B) EIA530 CB(B)
T36	RXC(A) 3	Input	100 Ohms differential	RS422 RXC- port 3 RS449 RT(A) EIA530 DD(A)
T35	RXC(B) 3	Input	100 Ohms differential	RS422 RXC+ port 3 RS449 RT(B) EIA530 DD(B)
T23	GND			Signal Ground for I/O connector
T30	RXD(A) 4	Input	100 Ohms differential	RS422 Receive Data- port 4 RS449 RD(A) EIA530 BB(A)
T31	RXD(B) 4	Input	100 Ohms differential	RS422 Receive Data+ port 4 RS449 RD(B) EIA530 BB(B)
T21	DTR(A) 4	Output	NA	RS422 DTR- port 4 RS449 TR(A) EIA530 CD(A)
T22	DTR(B) 4	Output	NA	RS422 DTR+ port 4 RS449 TR(B) EIA530 CD(B)
T24	TXD(A) 4	Output	NA	RS422 Transmit Data- port 4 RS449 SD(A) EIA530 BA(A)
T25	TXD(B) 4	Output	NA	RS422 Transmit Data+ port 4 RS449 SD(B) EIA530 BA(B)
T58	RTS(A) 4	Output	NA	RS422 RTS- port 4 RS449 RS(A) EIA530 CA(A)
T59	RTS(B) 4	Output	NA	RS422 RTS+ port 4 RS449 RS(B) EIA530 CA(B)
T55	TXC(A) 4	Output	NA	RS422 TXC- port 4 RS449 TT(A) EIA530 DA(A)

Table 5-5: RS422/RS449/EIA530 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
T56	TXC(B) 4	Output	NA	RS422 TXC+ port 4 RS449 TT(B) EIA530 DA(B)
T61	TXCI(A) 4	Input	100 Ohms differential	RS422 SCTE- port 4 RS449 ST(A) EIA530 DB(A)
T62	TXCI(B) 4	Input	100 Ohms differential	RS422 SCTE + port 4 RS449 ST(B) EIA530 DB(B)
T64	DCD(A) 4	Input	100 Ohms differential	RS422 DCD- port 4 RS449 RR(A) EIA530 CF(A)
T65	DCD(B) 4	Input	100 Ohms differential	RS422 DCD+ port 4 RS449 RR(B) EIA530 CF(B)
T33	DSR(A) 4	Input	100 Ohms differential	RS422 DSR- port 4 RS449 DM(A) EIA530 CC(A)
T34	DSR(B) 4	Input	100 Ohms differential	RS422 DSR+ port 4 RS449 DM(B) EIA530 CC(B)
T27	CTS(A) 4	Input	100 Ohms differential	RS422 CTS- port 4 RS449 CS(A) EIA530 CB(A)
T28	CTS(B) 4	Input	100 Ohms differential	RS422 CTS+ port 4 RS449 CS(B) EIA530 CB(B)
T67	RXC(A) 4	Input	100 Ohms differential	RS422 RXC- port 4 RS449 RT(A) EIA530 DD(A)
T68	RXC(B) 4	Input	100 Ohms differential	RS422 RXC+ port 4 RS449 RT(B) EIA530 DD(B)

V.35 Supported Signals

This configuration supports the V.35 standard in a DTE format. The V.35 standard is also supported through a hydra cabling option. Table 5-6, “V.35 Signals and Pins,” shows the supported signals and their positions on the dual VHDCI connector.

Note: *Some of the pins on the connector may not be included in the table. For each electrical standard, the pins that are not included in the table for that standard MUST BE LEFT UNCONNECTED.*

Table 5-6: V.35 Signals and Pins

Pin	Signal Name	Direction	Termination	Description
B3, B6, B9, B12, B15, B16, B19, B20, B23, B26, B29, B32, B37, B40, B46, B49, B50, B53, B54, B60, B63, B66, T3, T6, T12, T15, T16, T19, T20, T26, T29, T32, T37, T40, T43, T46, T49, T50, T53, T54, T57, T60, T63, T66			Signal Ground	
B64	RXD(A)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data- port 1 .V.35 104, M-34 R
B65	RXD(B)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data+ port 1 .V.35 104, M-34 T
B55	DTR1	Output	NA	V.35 Data Terminal Ready port 1 .V.35 108, M-34 H
B58	TXD(A)1	Output	NA	V.35 Transmit Data- port 1 .V.35 103, M-34 P
B59	TXD(B)1	Output	NA	V.35 Transmit Data+ port 1 .V.35 103, M-34 S
B24	RTS1	Output	NA	V.35 Request To Send port 1 .V.35 105, M-34 C
B57	GND1	-	NA	V.35 port 1 Signal Ground .V.35 102, M-34 B
B21	TXC(A)1	Output	NA	V.35 Transmit Clock- port 1 .V.35 113, M-34 U
B22	TXC(B)1	Output	NA	V.35 Transmit Clock+ port 1 .V.35 113, M-34 W

Table 5-6: V.35 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B27	TXCI(A)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In- port 1 .V.35 114, M-34 Y
B28	TXCI(B)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In+ port 1 .V.35 114, M-34 AA
B30	DCD1	Input	5K Ohms to ground	V.35 Data Carrier Detect port 1 .V.35 109, M-34 F
B31	RI1	Input	5K Ohms to ground	V.35 Ring Indicator port 1 .V.35 125, M-34 J
B67	DSR1	Input	5K Ohms to ground	V.35 Data Set Ready port 1 .V.35 107, M-34 E
B56	LT1	Output	NA	V.35 Line Test port 1 .V.35 ---, M-34 K
B61	CTS1	Input	5K Ohms to ground	V.35 Clear To Send port 1 .V.35 106, M-34 D
B33	RXC(A)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock- port 1 .V.35 115, M-34 V
B34	RXC(B)1	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock+ port 1 .V.35 115, M-34 X
B39	RXD(A)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data- port 2 .V.35 104, M-34 R
B38	RXD(B)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data+ port 2 .V.35 104, M-34 T
B48	DTR2	Output	NA	V.35 Data Terminal Ready port 2 .V.35 108, M-34 H
B45	TXD(A)2	Output	NA	V.35 Transmit Data- port 2 .V.35 103, M-34 P
B44	TXD(B)2	Output	NA	V.35 Transmit Data+ port 2 .V.35 103, M-34 S
B11	RTS2	Output	NA	V.35 Request To Send port 2 .V.35 105, M-34 C
B43	GND2	-	NA	V.35 port 2 Signal Ground .V.35 102, M-34 B
B14	TXC(A)2	Output	NA	V.35 Transmit Clock- port 2 .V.35 113, M-34 U
B13	TXC(B)2	Output	NA	V.35 Transmit Clock+ port 2 .V.35 113, M-34 W

Table 5-6: V.35 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
B8	TXCI(A)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In- port 2 .V.35 114, M-34 Y
B7	TXCI(B)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In+ port 2 .V.35 114, M-34 AA
B5	DCD2	Input	5K Ohms to ground	V.35 Data Carrier Detect port 2 .V.35 109, M-34 F
B4	RI2	Input	5K Ohms to ground	V.35 Ring Indicator port 2 .V.35 125, M-34 J
B36	DSR2	Input	5K Ohms to ground	V.35 Data Set Ready port 2 .V.35 107, M-34 E
B47	LT2	Output	NA	V.35 Line Test port 2 .V.35 ---, M-34 K
B42	CTS2	Input	5K Ohms to ground	V.35 Clear To Send port 2 .V.35 106, M-34 D
B2	RXC(A)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock- port 2 .V.35 115, M-34 V
B1	RXC(B)2	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock+ port 2 .V.35 115, M-34 X
T5	RXD(A)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data- port 3 .V.35 104, M-34 R
T4	RXD(B)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data+ port 3 .V.35 104, M-34 T
T14	DTR3	Output	NA	V.35 Data Terminal Ready port 3 .V.35 108, M-34 H
T11	TXD(A)3	Output	NA	V.35 Transmit Data- port 3 .V.35 103, M-34 P
T10	TXD(B)3	Output	NA	V.35 Transmit Data+ port 3 .V.35 103, M-34 S
T45	RTS3	Output	NA	V.35 Request To Send port 3 .V.35 105, M-34 C
T9	GND3	-	NA	V.35 port 3 Signal Ground .V.35 102, M-34 B
T48	TXC(A)3	Output	NA	V.35 Transmit Clock- port 3 .V.35 113, M-34 U
T47	TXC(B)3	Output	NA	V.35 Transmit Clock+ port 3 .V.35 113, M-34 W

Table 5-6: V.35 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
T42	TXCI(A)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In- port 3 .V.35 114, M-34 Y
T41	TXCI(B)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In+ port 3 .V.35 114, M-34 AA
T39	DCD3	Input	5K Ohms to ground	V.35 Data Carrier Detect port 3 .V.35 109, M-34 F
T38	RI3	Input	5K Ohms to ground	V.35 Ring Indicator port 3 .V.35 125, M-34 J
T2	DSR3	Input	5K Ohms to ground	V.35 Data Set Ready port 3 .V.35 107, M-34 E
T13	LT3	Output	NA	V.35 Line Test port 3 .V.35 ---, M-34 K
T8	CTS3	Input	5K Ohms to ground	V.35 Clear To Send port 3 .V.35 106, M-34 D
T36	RXC(A)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock- port 3 .V.35 115, M-34 V
T35	RXC(B)3	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock+ port 3 .V.35 115, M-34 X
T30	RXD(A)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data- port 4 .V.35 104, M-34 R
T31	RXD(B)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Data+ port 4 .V.35 104, M-34 T
T21	DTR4	Output	NA	V.35 Data Terminal Ready port 4 .V.35 108, M-34 H
T24	TXD(A)4	Output	NA	V.35 Transmit Data- port 4 .V.35 103, M-34 P
T25	TXD(B)4	Output	NA	V.35 Transmit Data+ port 4 .V.35 103, M-34 S
T58	RTS4	Output	NA	V.35 Request To Send port 4 .V.35 105, M-34 C
T23	GND4	-	NA	V.35 port 4 Signal Ground .V.35 102, M-34 B
T55	TXC(A)4	Output	NA	V.35 Transmit Clock- port 4 .V.35 113, M-34 U
T56	TXC(B)4	Output	NA	V.35 Transmit Clock+ port 4 .V.35 113, M-34 W

Table 5-6: V.35 Signals and Pins (Continued)

Pin	Signal Name	Direction	Termination	Description
T61	TXCI(A)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In- port 4 .V.35 114, M-34 Y
T62	TXCI(B)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Transmit Clock In+ port 4 .V.35 114, M-34 AA
T64	DCD4	Input	5K Ohms to ground	V.35 Data Carrier Detect port 4 .V.35 109, M-34 F
T65	RI4	Input	5K Ohms to ground	V.35 Ring Indicator port 4 .V.35 125, M-34 J
T33	DSR4	Input	5K Ohms to ground	V.35 Data Set Ready port 4 .V.35 107, M-34 E
T22	LT4	Output	NA	V.35 Line Test port 4 .V.35 ---, M-34 K
T27	CTS4	Input	5K Ohms to ground	V.35 Clear To Send port 4 .V.35 106, M-34 D
T67	RXC(A)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock- port 4 .V.35 115, M-34 V
T68	RXC(B)4	Input	100 Ohms differential/ 125 Ohms to ground	V.35 Receive Clock+ port 4 .V.35 115, M-34 X

Console Serial Port

Table 5-7, “Console Serial Port Pinout,” shows the pinout for the internal header used for the console serial port and the console serial port connections on the dual VHDCI I/O connector.

Table 5-7: Console Serial Port Pinout

Internal Header Pin	Dual VHDCI Connector Pin	Signal Name
1	T17	Asynchronous RS232C TXD conforming to the V.28 electrical standard
2	T18	Asynchronous RS232C RXD conforming to the V.28 electrical standard and terminated with 5K to ground
3	T19	Signal Ground

Note: *A three-pin right angle internal header can be mounted on the bottom side of the card and used for debugging. Contact Performance Technologies’ Customer Support and Services for more information.*

Serial Cable Connectors

The serial connections are brought out from the dual VHDCI connector to standard connectors through a set of shielded, hydra-style breakout cables. See “AMC335 I/O Configurations and Accessories,” on page 18 for a list of the hydra cables available for the AMC335. The standard cable pinouts of the hydra cables are shown in the following tables:

- Table 5-8, “RS232C Hydra Cable Connector Pinout,” on page 89
- Table 5-9, “RS449 (RS422) Hydra Cable Connector Pinout,” on page 90
- Table 5-10, “EIA530 Hydra Cable Connector Pinout,” on page 91
- Table 5-11, “V.35 Hydra Cable Connector Pinout,” on page 92
- Table 5-12, “RS232C/RS422/RS449/EIA530/V.35 Console Cable Option Pinout,” on page 93

RS232C Hydra Cable Connector

A hydra cable providing four 25-pin, D-shell (DB-25) DTE with male connectors (pins) is available for the AMC335 (RS232C) model. The pin assignments for the RS232C hydra cable are shown in Table 5-8, “RS232C Hydra Cable Connector Pinout,” below. Duplicate each pin four times to create the hydra cable for ports 1-4.

Table 5-8: RS232C Hydra Cable Connector Pinout

Pin	Signal Name	Description
1	CGND	Cable Shield
2	TXD	Transmit Data
3	RXD	Receive Data
4	RTS	Request To Send
5	CTS	Clear To Send
6	DSR	Data Set Ready
7	GND	Signal Ground
8	DCD	Data Carrier Detect
9	-	No connection
10	-	No connection
11	-	No connection
12	-	No connection
13	-	No connection
14	-	No connection
15	TXCI	Transmit Clock In
16	-	No connection
17	RXC	Receive Clock
18	-	No connection
19	-	No connection
20	DTR	Data Terminal Ready
21	-	No connection
22	-	No connection
23	-	No connection
24	TXC	Transmit Clock
25	-	No connection

RS449 (RS422) Hydra Cable Connector

A hydra cable providing four 37-pin, D-shell (DB-37) DTE with female connectors (pins) is available for the AMC335 (RS449 (RS422)) model. The pin assignments for the RS422/RS449 hydra cable are shown in Table 5-9, “RS449 (RS422) Hydra Cable Connector Pinout,” below. Duplicate each pin four times to create the hydra cable for ports 1-4.

Table 5-9: RS449 (RS422) Hydra Cable Connector Pinout

Pin	Signal Name	Description
1	CGND	Cable Shield
2	-	No connection
3	-	No connection
4	TXD-	Transmit Data
5	TXCI-	Transmit Clock In
6	RXD-	Receive Data
7	RTS-	Request To Send
8	RXC-	Receive Clock
9	CTS-	Clear To Send
10	-	No connection
11	DSR-	Data Set Ready
12	DTR-	Data Terminal Ready
13	DCD-	Data Carrier Detect
14	-	No connection
15	-	No connection
16	-	No connection
17	TXC-	Transmit Clock
18	-	No connection
19	GND	Signal Ground
20	-	No connection
21	-	No connection
22	TXD+	Transmit Data
23	TXCI+	Transmit Clock In
24	RXD+	Receive Data
25	RTS+	Request To Send
26	-	No connection
27	CTS+	Clear To Send
28	-	No connection
29	DSR+	Data Set Ready
30	DTR+	Data Terminal Ready
31	DCD+	Data Carrier Detect
32	-	No connection
33	-	No connection
34	RXC+	Receive Clock
35	TXC+	Transmit Clock
36	-	No connection
37	-	No connection

EIA530 Hydra Cable Connector

A hydra cable providing four 25-pin, D-shell (DB-25) DTE with male connectors (pins) is available for the AMC335 (EIA530) model. The pin assignments for the EIA530 hydra cable are shown in Table 5-10, “EIA530 Hydra Cable Connector Pinout,” below. Duplicate each pin four times to create the hydra cable for ports 1-4.

Table 5-10: EIA530 Hydra Cable Connector Pinout

Pin	Signal Name	Description
1	CGND	Cable Shield
2	TXD-	Transmit Data
3	RXD-	Receive Data
4	RTS-	Request To Send
5	CTS-	Clear To Send
6	DSR-	Data Set Ready
7	GND	Signal Ground
8	DCD-	Data Carrier Detect
9	RXC+	Receive Clock
10	DCD+	Data Carrier Detect
11	TXC+	Transmit Clock
12	TXCI+	Transmit Clock In
13	CTS+	Clear To Send
14	TXD+	Transmit Data
15	TXCI-	Transmit Clock In
16	RXD+	Receive Data
17	RXC-	Receive Clock
18	-	No connection
19	RTS+	Request To Send
20	DTR-	Data Terminal Ready
21	-	No connection
22	DSR+	Data Set Ready
23	DTR+	Data Terminal Ready
24	TXC-	Transmit Clock
25	-	No connection

V.35 Hydra Cable Connector

A hydra cable providing four 34-pin DTE with male connectors (pins) is available for the AMC335 (V.35) model. The pin assignments for the V.35 hydra cable are shown in Table 5-11, “V.35 Hydra Cable Connector Pinout,” below. Duplicate each pin four times to create the hydra cable for ports 1-4.

Table 5-11: V.35 Hydra Cable Connector Pinout

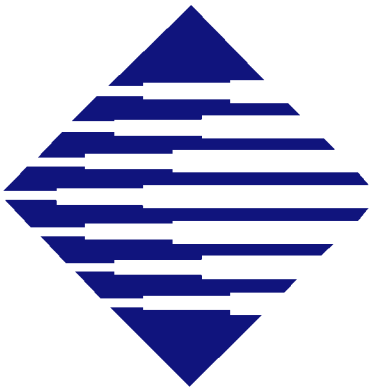
Pin	Signal Name	Description
R	RXD-	Receive Data
T	RXD+	Receive Data
H	DTR-	Data Terminal Ready
P	TXD-	Transmit Data
S	TXD+	Transmit Data
C	RTS-	Request To Send
B	GND	Signal Ground
U	TXC-	Transmit Clock
W	TXC+	Transmit Clock
Y	TXCI-	Transmit Clock In
AA	TXCI+	Transmit Clock In
F	DCD-	Data Carrier Detect
J	RI-	Ring Indicator
E	DSR-	Data Set Ready
K	LT-	Local Test
D	CTS-	Clear To Send
V	RXC-	Receive Clock
X	RXC+	Receive Clock
A	CGND	Chassis Ground

Console Cable Option

A console cable providing an RD Series DSUB nine-position female connector is available for each communication standard. The pin assignments for the console cable, which are identical for each standard, are shown in Table 5-12, “RS232C/RS422/RS449/EIA530/V.35 Console Cable Option Pinout,” below.

Table 5-12: RS232C/RS422/RS449/EIA530/V.35 Console Cable Option Pinout

Pin	Signal Name
1	Connected to Pins 4 and 6
2	TXD
3	RXD
4	Connected to Pins 1 and 6
5	GND
6	Connected to Pins 1 and 4
7	Connected to Pin 8
8	Connected to Pin 7
9	-



Chapter

6

MPC8270 Parallel I/O Ports

Overview

The Communications Processor Module (CPM) on the MPC8270 supports four general-purpose parallel I/O ports: A, B, C, and D. The following topics describe the I/O ports, the Serial Management Controllers (SMCs) and the pinouts for the four parallel I/O ports.

Key topics in this chapter include:

I/O Ports

Each pin in the I/O ports can be configured as a general-purpose I/O signal or as a dedicated peripheral interface signal. Port C is unique in that 16 of its pins can generate interrupts to the internal interrupt controller. See Table 2-2, "MPC8270 Interrupt Sources," on page 27 for more information.

Each pin can be configured as an input or an output and has a latch for data output, read or written at any time, and configured as general-purpose I/O or a dedicated peripheral pin. Some of the pins can be configured as open-drain (the pin can be configured in a wired-OR configuration on the module). The pin drives a zero voltage but three-states when driving a high voltage. Note that port pins do not have internal pull-up resistors. Due to the MPC8270's

significant flexibility, many dedicated peripheral functions are multiplexed onto the ports. The functions are grouped to maximize the pin's usefulness in the greatest number of MPC8270 applications. Refer to the *MPC8270 PowerQUICC II User's Manual* for more information on the various peripheral setups. See "Freescale MPC8270 PowerQUICC II Processor," on page 117 for a link to this manual.

Any port pins that do not have a dedicated function in the AMC335 configuration should be configured as an output and set to either a high or low. This eliminates the potential for an unterminated input that could create severe current draw and electrical noise within the part if it were floating.

Serial Management Controllers

The MPC8270 features two general-purpose serial management controllers (SMC1 and SMC2) that may be used as general-purpose RS232C communications interfaces. The two SMCs are full-duplex ports that can be configured independently to support one of three operating or modes:

- Universal Asynchronous Receiver/Transmitter (UART)
- Transparent
- General Circuit Interface (GCI)

The AMC335 is designed to support UART operation on two ports (one console and one MMC). The default point for console access is through the dual VHDCI connector when the module is installed in a system. An additional connection is available through a three-pin header, located on the top side of the AMC335, providing connectivity to the SMC, which is configured as the console serial port.

The console serial port can be used to provide a debug, monitor, or download function. The console serial port also has the ability to generate a PQ_HRESET_N if it receives two RS232 break signals that each lasts for longer than 13 ms. If a break and a character is received the console focus shifts from the MCP8270 to the MMC. The logic that watches the console receive line is located in the control logic PLD. The reset-on-break detect can be enabled by setting the Break Detect Enable Switch (SW3-3) to ON. Setting the switch to OFF disables the feature. See "SW3-3 (Break Detect Enable)," on page 40 for more information.

Note: *The reset-on-break detect can still be enabled with a software settable PAL register bit.*

The secondary Serial I/O channel is used to communicate with the MMC.

MPC8270 Parallel Port Pin Assignments

The MPC8270 parallel ports are configured to support serial I/O, modem control, interrupts, and other module-required functions. The program settings for the parallel port pins can be found in the files **init.inc** and **hardware.c**. Individual pin assignments for each port are shown in the following tables:

- Table 6-1, "MPC8270 Port A Pin Assignments," on page 97
- Table 6-2, "MPC8270 Port B Pin Assignments," on page 98
- Table 6-3, "MPC8270 Port C Pin Assignments," on page 99
- Table 6-4, "MPC8270 Port D Pin Assignments," on page 100

MPC8270 Port A Pin Assignments

Table 6-1: MPC8270 Port A Pin Assignments

Pin	Pin Function					
	PPARA = 1				PPARA = 0	
	PSORA = 0		PSORA = 1			
	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In
PA31	Default = Unassigned					
PA30	Default = Unassigned					
PA29	Default = Unassigned					
PA28	Default = Unassigned					
PA27	Default = Unassigned					
PA26	Default = Unassigned					
PA25	Default = Unassigned					
PA24	Default = Unassigned					
PA23	Default = Unassigned					
PA22	Default = Unassigned					
PA21	Default = Unassigned					
PA20	Default = Unassigned					
PA19	Default = Unassigned					
PA18	Default = Unassigned					
PA17	Default = Unassigned					
PA16	Default = Unassigned					
PA15	Default = Unassigned					
PA14	Default = Unassigned					
PA13	Default = Unassigned					
PA12	Default = Unassigned					
PA11	Default = Unassigned					
PA10	Default = Unassigned					
PA9	SMTXD2					
PA8		SMRXD2				
PA7	Default = Unassigned					
PA6					MACPHY_SMB_CLK	
PA5						MACPHY_SMB_DAT
PA4						
PA3					EE_CS	
PA2					EE_SCL	
PA1					EE_DI	
PA0						EE_DO

MPC8270 Port B Pin Assignments

Table 6-2: MPC8270 Port B Pin Assignments

Pin	Pin Function					
	PPARB = 1				PPARB = 0	
	PSORB = 0		PSORB = 1			
	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In
PB31	Default = Unassigned					
PB30	Default = Unassigned					
PB29	Default = Unassigned					
PB28	Default = Unassigned					
PB27	Default = Unassigned					
PB26	Default = Unassigned					
PB25	Default = Unassigned					
PB24	Default = Unassigned					
PB23	Default = Unassigned					
PB22	Default = Unassigned					
PB21	Default = Unassigned					
PB20	Default = Unassigned					
PB19	Default = Unassigned					
PB18	Default = Unassigned					
PB17	Default = Unassigned					
PB16	Default = Unassigned					
PB15		SCC2 RXD				
PB14		SCC3 RXD				
PB13	Default = Unassigned					
PB12			SCC2 TXD			
PB11	Default = Unassigned					
PB10	Default = Unassigned					
PB9	Default = Unassigned					
PB8			SCC3 TXD			
PB7						DSR PORT 1
PB6						DSR PORT 2
PB5						DSR PORT 3
PB4						DSR PORT 4

MPC8270 Port C Pin Assignments

Table 6-3: MPC8270 Port C Pin Assignments

Pin	Pin Function					
	PPARC = 1				PPARC = 0	
	PSORC = 0		PSORC = 1			
	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In
PC31	BRG1 BRGO					
PC30	Default = Unassigned					
PC29	BRG2 BRGO	SCC1 TXCLK				
PC28		SCC1 RXCLK				
PC27		SCC3 TXCLK	BRG3 BRGO			
PC26		SCC3 RXCLK				
PC25		SCC4 TXCLK	BRG4 BRGO			
PC24		SCC4 RXCLK				
PC23	Default = Unassigned					
PC22	Default = Unassigned					
PC21		SCC2 TXCLK				
PC20		SCC2 RXCLK				
PC19	Default = Unassigned					
PC18	Default = Unassigned					
PC17					JTAG_SDRAM_CLK	
PC16	Default = Unassigned					
PC15		SCC1 CTS				
PC14		SCC1 CD				
PC13		SCC2 CTS				
PC12		SCC2 CD				
PC11		SCC3 CTS				
PC10		SCC3 CD				
PC9		SCC4 CTS				
PC8		SCC4 CD				
PC7	Default = Unassigned					
PC6	Default = Unassigned					
PC5	Default = Unassigned					
PC4	Default = Unassigned					
PC3						WAKE1
PC2						WAKE2
PC1						WAKE3
PC0						WAKE4

MPC8270 Port D Pin Assignments

Table 6-4: MPC8270 Port D Pin Assignments

Pin	Pin Function					
	PPARD = 1				PPARD = 0	
	PSORD = 0		PSORD = 1			
	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In
PD31		SCC1 RXD				
PD30			SCC1 TXD			
PD29	SCC1 RTS					
PD28	Default = Unassigned					
PD27	Default = Unassigned					
PD26	SCC2 RTS					
PD25	Default = Unassigned					
PD24	Default = Unassigned					
PD23	SCC3 RTS					
PD22		SCC4 RXD				
PD21	SCC4 TXD					
PD20	SCC4 RTS					
PD19					SCC1 DTR	
PD18					SCC2 DTR	
PD17					SCC3 DTR	
PD16					SCC4 DTR	
PD15	Default = Unassigned					
PD14	Default = Unassigned					
PD13					LT PORT 1 (V.35)	
PD12					LT PORT 2 (V.35)	
PD11					LT PORT 3 (V.35)	
PD10					LT PORT 4 (V.35)	
PD9	SMC1 SMTXD					
PD8		SMC1 SMRXD				
PD7						RI PORT 1 (V.35)
PD6						RI PORT 2 (V.35)
PD5						RI PORT 3 (V.35)
PD4						RI PORT 4 (V.35)

Chapter

7

Reset

Overview

This chapter discusses the various reset types and sources supported by the AMC335. Because many embedded systems have different requirements for module reset functions, the incorporation of this sub-system on the AMC335 has been designed to provide maximum flexibility.

Key topics in this chapter include:

Reset Types and Sources

The AMC335 supports the following reset types that affect the entire module:

- Power-On Reset
- Hard Reset
- Soft Reset

Limited resets that do not affect the entire module are also supported.

Power-On Reset

An on-board reset controller initiates the power-on reset sequence for the AMC335. The controller provides a 20 ms reset pulse after the 3.3 V power returns from an “intolerance” condition or a brownout condition. This signal excludes the MMC block and the PI7C9X110 PCI Express interface. The control logic PLD on the module receives this signal and issues a PORESET# to the MPC8270, resets internal logic, and then supplies resets to the module peripheral devices.

The power-on reset signal (PORESET#) is also asserted by the control logic PLD in response to a PCI Express reset (PCE_PERST#). The control logic PLD logic pulses the PORESET# signal once upon detecting the PCI Express reset assertion, when PCI Express is enabled in the system.

MMC Reset

The MMC has the ability to remove power from the module by turning off the 12 V to 3.3 V regulator. The MMC also has the ability to reset the module, which includes a reset to the PI7C9X110 PCI Express bridge.

FCLKA

The AMC335 requires the carrier to source FCLKA to the module. The AMC.1 R2.0 specification requires that FCLKA is e-keyed. The AMC335 is shipped from the factory configured for AMC.1 R2.0 e-keying of FCLKA. AMC.1 R1.0 carriers do not e-key FCLKA. If the AMC335 does not come out of reset when powered on, it is likely that FCLKA is not configured properly for the specific carrier.

For more information about configuring FCLKA on this AMC335, please contact Performance Technologies' Customer Support and Services.

Hard Reset

The hard-reset signal (PQ_HRESET#) is generated by the MPC8270 or the control logic PLD. The MPC8270 generates the hard-reset signal in response to the following triggers:

- Power-on reset
- Push-button reset
- Software watchdog reset (if enabled)
- Bus monitor reset (if enabled)
- Checkstop reset (if enabled)

The effect of a hard reset on the processor is different to a power-on reset. For more information, refer to the “Reset” chapter in the *MPC8270 PowerQUICC II Family User’s Manual,* from http://www.freescale.com/. The signal runs between the MPC8270 and the control logic PLD.

The MPC8270 normally read its HRESET# configuration settings from the boot Flash. To force the MPC8270 to take the default settings (no reset configuration cycles on the bus because the CPU is set to be a RESET slave) change the RSTCONF# Switch (SW3-1) to OFF. See “SW3-1 (Reset Configuration),” on page 39 for more information about this switch setting.

The control logic PLD generates a PQ_HRESET# signal in response to a system module reset from the local PCI reset issued by the PI7C9X110 PCI Express interface. This happens only if the host system is not generating a PCI Express reset at the same time and the PCI Express link is enabled.

The control logic PLD also asserts a PQ_HRESET# signal in response to the reception of an RS232C double BREAK signal on the console serial port. This happens if the Break Detect Enable Switch (SW3-3) is ON. When the hard-reset signal is asserted because of an RS232C double BREAK signal, it remains asserted until the break signal is removed. See “SW3-3 (Break Detect Enable),” on page 40 for more information about this switch setting.

Soft Reset

The soft reset for the module is accomplished by asserting the PQ_SRESET# signal. The signal is connected to the MPC8270 and the control logic PLD. The signal source for soft-reset signal is the MPC8270.

The MPC8270 asserts this signal in response to any power-on reset or hard-reset condition. The effect of soft reset on the processor is different to a power-on reset or a hard-reset. Refer to the “Reset” chapter in the *MPC8270 PowerQUICC II Family User’s Manual,* from http://www.freescale.com/.

PCI Express Interface Resets

The PI7C9X110 PCI Express bridge has more than one reset condition; each is described in the following topics.

Primary PCI Express Reset

The PI7C9X110 receives primary resets from the PCI Express root complex on the PCI Express bus via the PCE_PERST# signal. It resets all of the PI7C9X110’s internal logic as well as initializing the rest of the AMC335’s logic to the power-on reset condition. Refer to the *Pericom PI7C9X110 PCI Express-to-PCI Reversible Bridge Data Sheet* at the Pericom Web site for a complete description of this reset: http://www.pericom.com/.

The MPC8270 PORESET# signal is held true as long as the PCI Express reset is held true and the PCI Express link is enabled.

PCI Express Reset Levels

There are two further PCI Express reset levels supported in the AMC335 configuration (forward nontransparent): Hot Reset, Level 1 and Secondary Bus Reset.

Hot Reset, Level 1

Hot Reset, Level 1 is received by the PI7C9X110 in the form of a PCI Express in-band message. It causes the reset of internal registers and state machines, but does not cause the reset of sticky bits in the internal registers. It also propagates across the PI7C9X110 and is output on the local PCI reset signal as PERI_PCIRST#. This signal is connected to the control logic PLD and causes a hard reset to the MPC8270.

Refer to the *Pericom PI7C9X110 PCI Express-to-PCI Reversible Bridge Data Sheet* at the Pericom Web site for a complete description of this reset: http://www.pericom.com/.

Secondary Bus Reset

The Secondary Bus Reset is invoked by setting the internal Bridge Control and Status register by software. This reset takes the bridge state machines to a known state but does not reset internal registers. It also causes the propagation of the Local PCI reset signal as PERI_PCIRST#. This signal is connected to the control logic PLD and causes a hard reset to MPC8270 when the PCI Express link is enabled. The PCI bus reset condition is sustained until the bit in the control register is reset. This is the preferred method to cause a “Software Reset” of the AMC335. If the PCI Express link is not enabled a “Software Reset” can be caused by writing to the SRST bit in the PLD to send a soft reset to the MPC8270 only.

Refer to the *Pericom PI7C9X110 PCI Express-to-PCI Reversible Bridge Data Sheet* at the Pericom Web site for a complete description of this reset: http://www.pericom.com/

Chapter

8

Specifications

Overview

This chapter describes the electrical, environmental, and mechanical specifications of the AMC335. Reliability information is also provided in this chapter.

Key topics in this chapter include:

Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the AMC335 at these maximums. See “Power Requirements,” on page 108 for actual operating conditions.

Supply Voltage, Vcc12 (+12 V):	10 - 14 V
Supply Voltage, Vcc3 (+3.3 V):	3.0 - 3.6 V
Storage Temperature:	-20 °C to +80 °C (-4 °F to 176 °F)
Non-Condensing Relative Humidity:	5 to 90% RH

Electrical Specifications

This section describes the electrical requirements for the AMC335.

Power Requirements

The power distribution network on the AMC335 starts with the AMC card edge interface connecting to an AdvancedTCA or MicroTCA-based platform. The power pins are connected per the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. The voltages supplied are +3.30 V management and +12 V. Maximum and typical operating power requirements are shown in Table 8-1, “Power Consumption with 266 MHz Processor,” below.

Table 8-1: Power Consumption with 266 MHz Processor

			Typical Power		Maximum Power	
Voltage	Source	Tolerance	Required Current	Power	Required Current	Power
+12 V	AMC B+ connector	+/- 25%	0.875 A	10.5 W	1.1 A	13.2 W
+3.30 V MGNT	AMC B+ connector	+/- 5%	0.05 A	0.165 W	0.0525 A	0.173 W
Total Power				10.665 W		13.373 W

Caution:

Use anti-static grounding straps and anti-static mats when you are handling the AMC335 to help prevent damage due to electrostatic discharge. Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment.

Environmental Specifications

This section describes the environmental requirements for the AMC335.

Operating Temperature

The module operating range is 0 to 60 °C (32 °F to 140 °F). The maximum power dissipation by any part is the 3 W peak generated by the MPC8270 and the linear regulator creating its core voltage. In a normal environment where the ambient temperature doesn’t exceed the thermal operating range a heatsink is not required for any of the module level components. However, one may be employed to give the assembly a thermal margin beyond its normal operating range.

Contact Performance Technologies’ Customer Support and Services for more information if additional thermal margin is desired.

Caution:

External airflow must be provided at all times during operation to avoid damaging the CPU.

Temperature Monitoring

Because reliable long-term operation of the AMC335 depends on maintaining proper temperature, Performance Technologies strongly recommends that you verify the operating temperature of the CPU. The MMC monitors the temperature of the device and reports any temperature violations that may occur via the IPMB interface.

Mechanical Specifications

The AMC335 is compliant with the *PICMG AMC.0 R 2.0* specification for all mechanical parameters. Mechanical dimensions are outlined below and shown in Figure 8-1, “AMC335 Dimensions,” below.

Length: 180.6 mm (7.11 in)

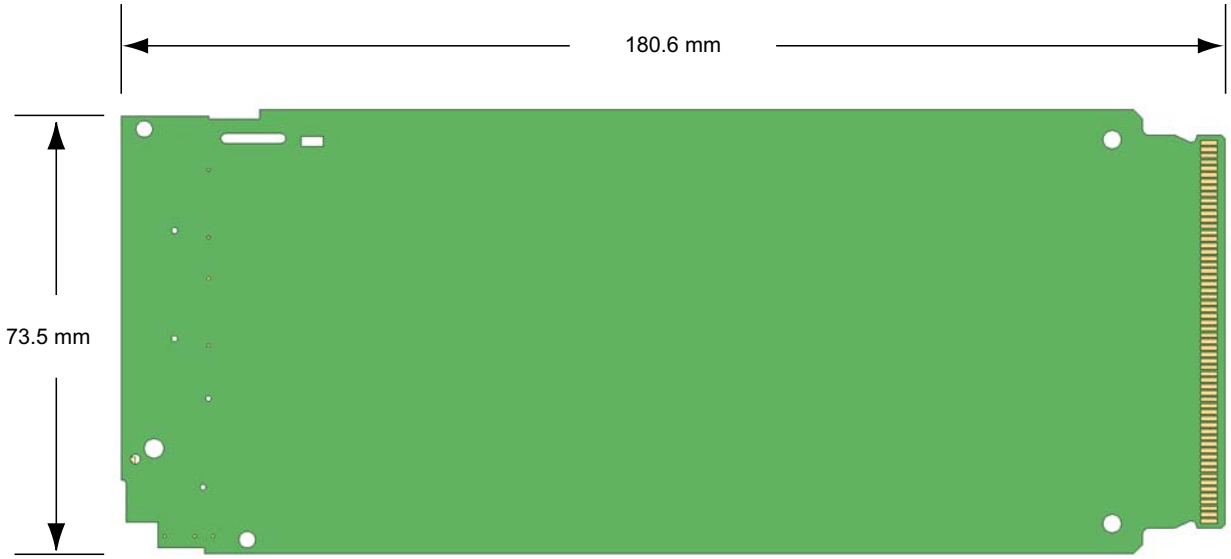
Width: 73.5 mm (2.89 in)

Height: 19.05 mm (0.75 in) (mid-sized front panel)

Weight: 0.11 kg (0.25 lbs)

Front Panel Bracket: Mid and full-size AMC.0 bracket with opening for a dual VHDCI I/O connector.

Figure 8-1: AMC335 Dimensions



Reliability

Table 8-2, “Reliability Data,” shows reliability data for the models of the AMC335.

Table 8-2: Reliability Data

AMC335 Model	MTBF[1]	MTTR
PT-AMC335-12289 (RS232C)	383,371 hours	3 minutes
PT-AMC335-12258 (RS422)	383,371 hours	3 minutes
PT-AMC335-12287 (V.35)	383,371 hours	3 minutes

1. MTBF calculated using Bellcore SR-332 Issue 2.

Chapter

9

Agency Approvals

Overview

This chapter presents agency approval and certification information for the AMC335 Four-Port WAN Communications AMC module.

Key topics in this chapter include:

Network Equipment-Building System (NEBS) and European Telecommunications Standards Institute (ETSI)

The product described in this manual is designed to meet NEBS Level 3 and ETSI Environmental Criteria:

- GR-63-CORE - *Network Equipment-Building System Requirements: Physical Protection*
- GR-1089-CORE - *Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment*

CE Certification

The product described in this manual meets the intent of the following European Union Directives:

- *EU 89/336/EEC Electromagnetic Compatibility Directive*, amended by 92/31/EEC, 93/68/EEC, 98/13/EEC, and 2004/108/EC
- *EU 72/23/EEC Low Voltage Directive*, amended by 93/68/EEC and 2006/95/EC

by meeting the applicable EU standards as outlined in the *Declaration of Conformance*. The *Declaration of Conformance* is available from Performance Technologies, or from your authorized distributor. Compliance will be demonstrated to the following specifications as listed in the *Official Journal of the European Communities*.

EN55022 Radiated and Conducted Emissions

EN300 386 Electromagnetic Compatibility (EMC)

EN55024 Immunity

EN61000-4-2	Electro-Static Discharge (ESD)
EN61000-4-3	Radiated Susceptibility
EN61000-4-4	Electrical Fast Transient Burst
EN61000-4-5	Surge Immunity
EN61000-4-6	Frequency Magnetic Fields
EN61000-4-11	Voltage Dips, Variations, and Short Interruptions

Safety

The product described in this manual meets the following safety regulations:

EN/IEC 60950	Safety Requirements for Information Technology Equipment
CB Scheme	CB Scheme Certificate and Report
UL60950	UL Recognized

FCC (USA) Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: *Modifications made to this device that are not approved by Performance Technologies, Inc. may void the authority granted to the user by the FCC to operate this equipment.*

Industry Canada Class A Notice

This Class A digital apparatus complies with Industry Canada’s Equipment Standard for Digital Equipment (ICES-003).

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

Product Safety Information

Safety Precautions

Review the following precautions to avoid injury and prevent damage to this product, or any products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information provided in the component product user manuals and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit. Save this document for future reference.

Caution:

To Avoid Burns: *If there is a heat sink on this module, it can get very hot during normal operation. To avoid burns, take extra care when removing the module from the chassis soon after shutdown. Wait a few minutes to allow the heat sink to cool down.*

Caution:

Handling the Module: *It is important to hold the module only by the front panel or PCB edges. Avoid touching any components unless necessary to service the product. Do not handle the heat sink, as this can adversely affect the thermal connection between the heat sink and the processor, and cause the processor to overheat under normal operating conditions.*

Caution:

To Avoid Electric Overload: *To avoid electrical hazards (heat, shock and/or fire hazard), do not make connections to terminals outside the range specified for that terminal. Refer to the product user manual for correct connections.*

Caution:

To Avoid the Risk of Electric Shock: *When supplying power to the system, always make connections to a grounded main. Always use a power cable with a grounded plug (third grounding pin). Do not operate in wet, damp, or condensing conditions.*

Caution:

System Airflow Requirements: *Platform components such as processor boards, Ethernet switches, etc., are designed to operate with external airflow. Components can be destroyed if they are operated without external airflow. Chassis fans normally provide external airflow when components are installed in compatible chassis. Filler panels must be installed over unused chassis slots so that airflow requirements are met. Please refer to the product data sheet for airflow requirements if you are installing components in custom chassis.*

Caution:

Do Not Operate Without Covers: *To avoid electric shock or fire hazard, do not operate this product with any removed enclosure covers or panels.*

Caution:

To Avoid the Risk of Electric Shock: *Do not operate in wet, damp, or condensing conditions.*

Caution:

Do Not Operate in an Explosive Atmosphere: *To avoid injury, fire hazard, or explosion, do not operate this product in an explosive atmosphere.*

Caution:

If Your System Has Multiple Power Supply Sources: *Disconnect all external power connections before servicing.*

Warning:

System power supplies must be replaced by qualified service personnel only.

Compliance with RoHS and WEEE Directives

In February 2003, the European Union issued *Directive 2002/95/EC* regarding the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS) and *Directive 2002/96/EC* on Waste Electrical and Electronic Equipment (WEEE).

This product is compliant with *Directive 2002/95/EC*. It may also fall under the *Directive 2002/96/EC*.

Performance Technologies' complete position statements on the RoHS and WEEE Directives can be viewed on the Web at: http://pt.com/page/about-us/ehsms/.

Chapter

10

Data Sheet Reference

Overview

This chapter provides information on data sheets, devices, standards, specifications, and documentation for the technology designed into the AMC335.

Key topics in this chapter include:

Freescale MPC8270 PowerQUICC II Processor

The AMC335 uses a Freescale MPC8270 PowerQUICC II CPU, which is discussed in the documentation for the MPC8280 family. For more information about the Freescale MPC8270 PowerQUICC II integrated communications processor, refer to the following documents at the Freescale Web site:

http://www.freescale.com/

- *Freescale MPC603e RISC Microprocessor User's Manual*
- *Freescale MPC8280 PowerQUICC II Family User's Manual*
- *Freescale MPC8280 PowerQUICC II Family Reference Manual*

- *Freescale MPC8280 PowerQUICC II Family Hardware Specifications*
- *Freescale MPC8280 PowerQUICC II Family Device Errata*
- *Freescale MPC8280 PowerQUICC II Family Technical Summary*

PCI Express Bridge

The AMC335 incorporates a PCI-to-PCI Express bridge (PI7C9X110) to connect the CPU to the host PCI Express root complex. For more information refer to the *Pericom PI7C9X110 PCI Express-to-PCI Reversible Bridge Data Sheet* at the Pericom Web site:

http://www.pericom.com/products/pci/PI7C9X110/

Ethernet Interfaces

Ethernet is implemented on the AMC335 via the Broadcom BCM5704S 1000BaseX Dual MAC/PHY Ethernet controller. For more information about this device, refer to the Broadcom Web site:

http://www.broadcom.com/products/Enterprise-Networking/Gigabit-Ethernet-Controllers/BCM5704S

Module Management Controller

The MMC is implemented with Atmel's 8-bit microcontroller with 128 KB in-system programmable flash. For more information refer to the Atmel Web site:

http://www.atmel.com/dyn/resources/prod_documents/doc2467.pdf

Refer to the Intel IPMI home page for information concerning the Intelligent Platform Management Interface, including the *Intelligent Platform Management Interface v1.5 Specification* and the *Intelligent Platform Management Interface Implementer's Guide*:

http://developer.intel.com/design/servers/ipmi/spec.htm

PICMG Specifications

The AMC335 is compliant with the following PICMG specifications:

- *PICMG AMC.0, R 2.0 Specification*
- *IPMI v1.5 Specification*

These specifications can be purchased from PICMG (PCI Industrial Computers Manufacturers Group). A short-form specification is also available at PICMG's Web site:

https://www.picmg.org

PCI Express Specifications

The following PCI Express specifications can be purchased from the PCI-SIG. Short form specifications in Adobe Acrobat format (PDF) are also available at the PCI-SIG Web site:

http://www.pcisig.com/specifications/

- *PCI Local Bus Specification, Revision 2.2*, 1998. PCI Special Interest Group.
- *PCI Express Base Specification Revision 1.0*. PCI Special Interest Group
- *PCI Express Card Electromechanical Specification Revision 1.0*. PCI Special Interest Group

Electronic Industries Alliance Specifications

The following Electronic Industries Alliance (EIA) specifications for the communication standards provided on the different models of the AMC335 may be useful.

- EIA RS232C Specification
- EIA RS422 Specification
- EIA EIA530 Specification
- ITU V.35 Specification

Consult the following Web sites for more information:

- http://www.eia.org/
- http://www.tiaonline.org/index.cfm
- http://www.itu.int/net/home/index.aspx

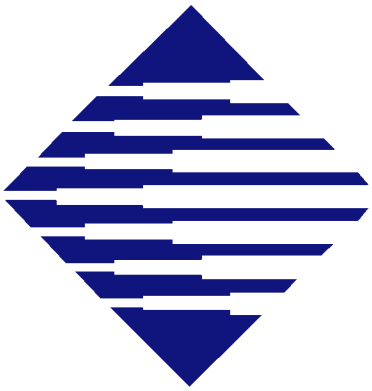
User Documentation

The latest product information and user manuals are available at the Performance Technologies Web site:

http://www.pt.com

Information specific to the AMC335 is available at this Web page:

http://go.pt.com/amc335



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