# LS27B Hardware User's Manual

**Dual channel Multi-Band RF Downconverter**
**with AM and FM Demodulation**

| | |
|---|---|
| Document: | U027B101 |
| Author: | B. Graber |
| Date: | 03/01/10 |
| Release: | Initial |


## Lumistar Inc

**5870 El Camino Real**

**Carlsbad, California 92008**

**(760) 431-2181**

**www.lumi-star.com**

Lumistar Inc
5870 El Camino Real
Carlsbad, CA 92008
(760) 431-2181
(760) 431-2665 Fax
www.lumi-star.com

# TABLE OF CONTENTS

# 1 Introduction

## 1.1 General

This document is the Hardware User's Manual for the Lumistar LS27B Dual Channel Multi-band RF Downconverter. This product represents Lumistar's 3rd generation of the LS27 Series of Dual Channel RF Downconverters. In addition to the functionalities of the Lumistar LS27P3 PCI downconverter, this product also provides and optional FM demodulation stage for each input channel. Figure 1-1 contains detailed model number construction. This document applies to all model combinations indicated by this figure.

The intent of this document is to provide physical, functional, and operational information for the end user including hardware configuration, interconnection and software interfaces for the device.

The design implements a Digital Signal Processor Engine (DSPE) controlled superhetrodyne downconverter with AM demodulation and optional FM demodulation. This receiver is in the physical format and size similar to a standard 5 3/4" CD or DVD drive format. The product provides two independent and autonomous multi-band downconversion stages. Each channel provides the conversion of up to four RF pass-bands to a 70MHz Intermediate Frequency (IF) output while providing AM demodulation of the input signal. The product's standard configuration provides eight software selectable IF bandwidth filters, roughly placed at octave intervals (or as ordered by the customer), to reduce channel noise bandwidth and improve adjacent channel rejection. The product line can optionally be equipped with an FM demodulation stage and eight video filters.

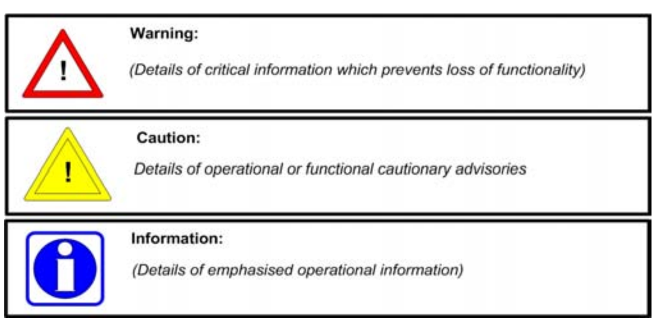
Table 1-1 provides specifications for electrical, mechanical, and operational characteristics of the LS27B product. A block diagram of the product design is shown in Figure 1-2.

## 1.2 Manual Format and Conventions

This manual contains the following sections:

- Chapter 1 provides a brief product overview and technical specifications
- Chapter 2 provides receiver theory of operation
- Chapter 3 provides installation and configuration instructions
- Chapter 4 provides programming information

Throughout this document, several document flags will be utilized to emphasis warnings or other important data. These flags come in three different formats: Warnings, Cautions, and Information. Examples of these flags appear below.



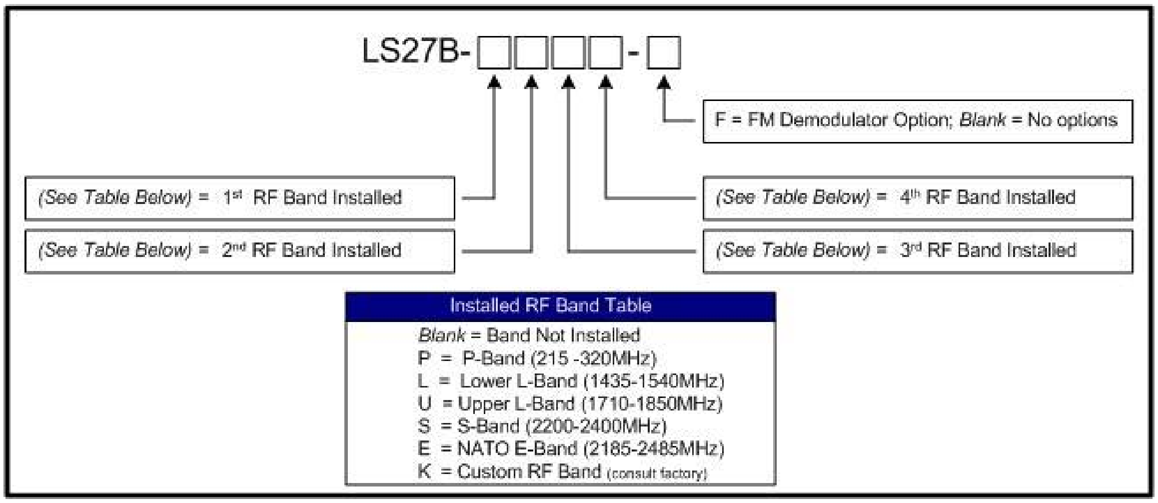



**Figure 1-1** LS27B Model Number Construction Details

| Category: | Specifications: | Details: |
|---|---|---|
| ***Mechanical*** | | |
| | Envelope Dimensions | 7.00"(L) x 5.75"(W) x 1.625" (H) |
| | Form Factor | 5 3/4" CD/DVD Drive Size |
| | Weight | ~ 30oz. |
| ***Electrical*** | | |
| | Individual power requirements | +12VDC @ 2A (nominal); 11-36VDC input |
| | Total Power (both Channels) | ~ 22Watts (nominal), ~26Watts (max.) |
| ***Performance*** | | |
| RF Tuner | RF Input Bands | 2185.5 - 2485.5 MHz (E-Band) |
| | | 2200.5 - 2399.5 MHz (S-Band) |
| | | 1710.5 - 1849.5 MHz (Upper L-Band) |
| | | 1435.5 - 1539.5 MHz (Lower L-Band) |
| | | 215.5 - 319.5 MHz (P-Band) |
| | | Custom (Consult Factory) |
| | Tuner Resolution | 50kHz (Typical) |
| | Frequency Accuracy | 0.002% (Max.) 0.001% (Typical) |
| | RF Input AGC Range | +10dBm to –100dBm |
| | Input Level without Damage | +28dBm |
| | Receiver Input $P_{1dB}$ | +10dBm (typical) |
| | Receiver Noise Figure | 5dB (typical @ threshold) |
| | 70MHz Phase Noise @ 100kHz | Less than -110dBc (typical) |
| | Receiver $OIP_3$ | > +15dBm (typical) |
| | 70MHz Output Level | -20dBm (+/- 1dBm) |
| | $2^{nd}$ IF 3dB Bandwidths Available (typical) | 250kHz, 500kHz, 1MHz, 2MHz, 5MHz, 10MHz, 20MHz, 40MHz |
| Demodulation | Types | AM, FM (optional) |
| | AM -3dB Frequency Response | 50kHz (AM Low-pass Bypass Mode) |
| | AM Low-pass Filters | 32 Software Selectable |
| | AM -3dB Bandwidths | 50, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1K, 1.1K, 1.2K, 1.3K, 1.4K, 1.5K, 1.6K, 1.7K, 1.8K, 1.9K, 2K, 3K, 4K, 5K, 6K, 7K, 8K, 9K, 10K, 15K, 20K, 50K Hz |
| | FM Video Filters (typical) | 125kHz, 250kHz, 500kHz, 1MHz, 2.5MHz, 4.6MHz, 10MHz, 15MHz. |
| ***Connectors*** | | |
| | External Reference Input/Output | (1) SMA Jack, Female |
| | RF Signal Input | (2) SMA Jack, Female |
| | IF Signal Output | (2) SMA Jack, Female |
| | Output Connector | (1) 2x8 0.100 Shrouded Header, keyed |
| | DC Power Connector | (1) 1x4 0.200 Shrouded Header, keyed |
| | Serial Interface, DI Connector | (1) 2x10 0.100 Shrouded Header, keyed |
| ***Environmental*** | | |
| | Temperature, Operational | -40° to 85° C (Industrial) |
| | Temperature, Storage | -20° to 90° C |
| | Humidity, non-condensing | <40° C 0-90%, >40° C 0-75% |

**Table 1-1** Specifications for the LS27B

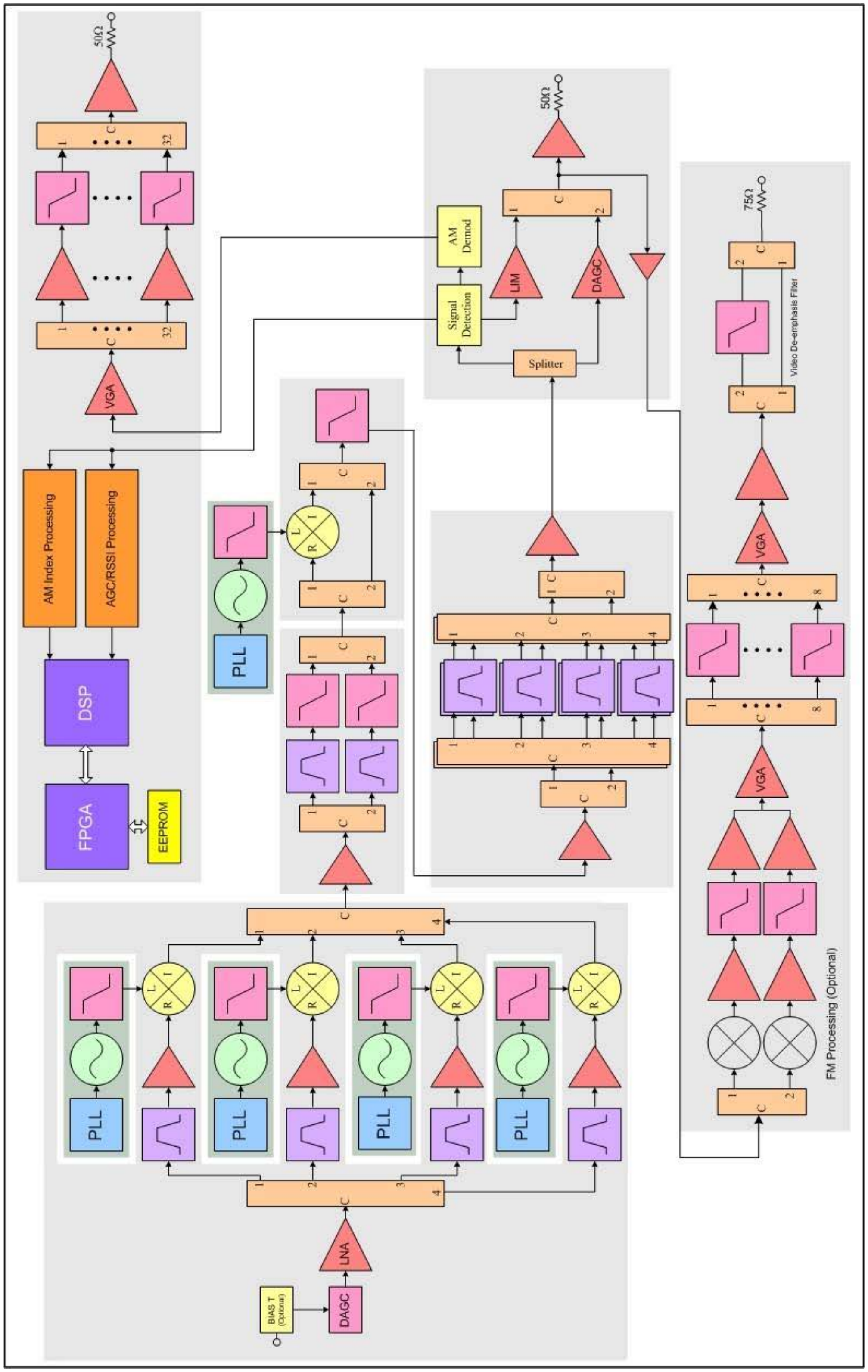



**Figure 1-2** Block Diagram of LS27B Series Multi-band Receiver

# 2 Theory of Operation

In order to more clearly understand the operation of the receiver, this section will detail the various stages of the receiver design. These stages are as follows:

- 1st Downconversion
- 1st IF Band-pass Filter
- 1st Local Oscillator
- 2nd Downconversion
- 2nd Local Oscillator
- 2nd IF Filter
- Limiting Amplifier/AM Demodulation/Digital AGC (DAGC)
- Digital Signal Processing Engine (DSPE)
- FM Demodulation Stage (Optional)

With the exception of the DSPE, each of these sections are physically shielded and isolated from one another to facilitate the greatest EMI/RFI ingress and egress protection allowing the receiver exceptional performance.

For the following sections, refer to the block diagram of Figure 1-2.

## *2.1 1st Downconversion*

The RF input is applied to the 1st Downconversion stage. The stage may optionally contain a bias-T which can be used to power an external LNA through the RF interface port. (Contact the factory for further details on this option.) A DAGC section is next in the signal chain for very high level signal protection and compression compensation. This is followed by a low-noise amplifier (LNA) to provide a large amount of gain while maintaining a very low noise figure enhancing the receiver's overall sensitivity. Selectable RF band-pass filters follow the LNA. The RF signal is then mixed with the first local oscillator (LO) which converted to the 1st IF frequency.

## *2.2 1st IF Band-pass Filter*

The output of the 1st Downconversion stage is send through one of two1st IF filter paths based on the selection of high-side or low side conversion. To eliminate images and limit the overall noise bandwidth to the remaining receiver sections, a 50MHz band-pass filter is switched into the signal path.

## *2.3 1st Local Oscillator*

In a superhetrodyne design, local oscillators (LOs) are utilized to convert high frequencies to lower, "intermediate" frequencies. The first LO is injected into the mixer of the first Downconversion stage to accomplish this task. Mixers can either utilize a sum or difference frequency component to produce IF frequencies. For example, if an RF frequency of 2,200 MHz was to be converted to an intermediate frequency of 250MHz, a difference component of 1,950MHz could injected to the mixer or a sum frequency component of 2,450MHz could be applied. The difference component LO application is referred to a "low-side" conversion. The sum component application is referred to as "high-side" conversion. Both methods are equally valid and each has its own benefits. The LS27B design has the ability to utilize either approach and actually switch between the methods when necessary for performance reasons.

## 2.4 2nd Downconversion

The receiver designs contain a switchable 2nd Downconversion stage. Similar to the 1st Downconversion stage, it contains a mixer to convert the 1st IF frequency to a second IF frequency of 70MHz. If the RF frequency band is relatively low, as is the case for P-Band inputs, the on-board processor can bypass the 2nd Downconversion stage switching to a single superhetrodyne process. In either case, a low-pass filter is applied to the signal path at the output of this stage to reduce harmonics and low frequency noise from being applied to subsequent stages.

## 2.5 2nd Local Oscillator

The second LO is injected into the mixer of the 2nd Downconversion stage to provide the second IF frequency of 70MHz. Like the first conversion stage, the second LO utilizes low-side injection for this conversion. A low-pass filter is applied to the LO output to minimize spurious and harmonic signals from being converted in the 2nd Downconversion stage. The 2nd LO is automatically disabled for RF bands that employ a single super heterodyne process.

## 2.6 2nd IF Filter

From the output of the 2nd conversion stage, the resulting intermediate frequency is then applied to a group of bandpass filters to minimize noise bandwidth and improve adjacent channel rejection. The 2nd IF stage contains eight IF (SAW) filters centered at 70MHz and varying in bandwidth from 250kHz to 40MHz in approximately octave steps.

## 2.7 Digital AGC/Limiting Amplification/AM Demodulation

Outputs from the 2nd IF Filter Stage are routed to the final signal detection, AM demodulation, and gain stage in the receiver. The output stage combines both a limiting amplifier and digital AGC (DACG) section. Included in the design is an AM demodulation stage for antenna tracking applications. The main system gain element provides for 90 to 110dB of signal gain. Signal level detection is utilized in DAGC controls.

## 2.8 Digital Signal Processing Engine (DSPE)

The LS27B design contains a highly integrated digital signal processing engine (DSPE) which is utilized for linearization, filtering and control applications. This engine is composed of a digital signal processor, FPGA resources, ADCs, DACs and localized memory used to process the signal path parameters. Each of the channels is controlled and statused as an autonomous receiver. The engine performs "real-time" tasks as well as user software interfaces.

## 2.9 FM Demodulation Stage (Optional)

The LS27B design may optionally contain an FM demodulation stage for each channel. The stage is split between a narrow-band and wide-band demodulator to optimize processing of each signal characteristic. The output of the FM demodulation is software switched between one of eight video filters. The output can also be switched, in addition to the video filter, thru a video de-emphasis network for true analog video signals. The unit is comes standard with NTSC de-emphasis but other formats are available. The demodulation stage has a software adjustable output level.

# 3 Installation and Configuration

Chapter 3 provides installation and configuration information. This chapter will familiarize the user with the layout of the device, and provide information on the proper installation and interconnection of the hardware.

## 3.1 Product Outline Diagrams

Figure 3-1 contains an outline diagram of the top and bottom sides of the product. Connector locations and switch positions are indicated. The model number, serial number, revision information and product options are denoted on the RF enclosure label.

## 3.2 Hardware Configuration

The receiver design contains configuration switches to control various functions. Figure 3-2 contains a diagram of the configuration switches along with the default factory positions for these switches.

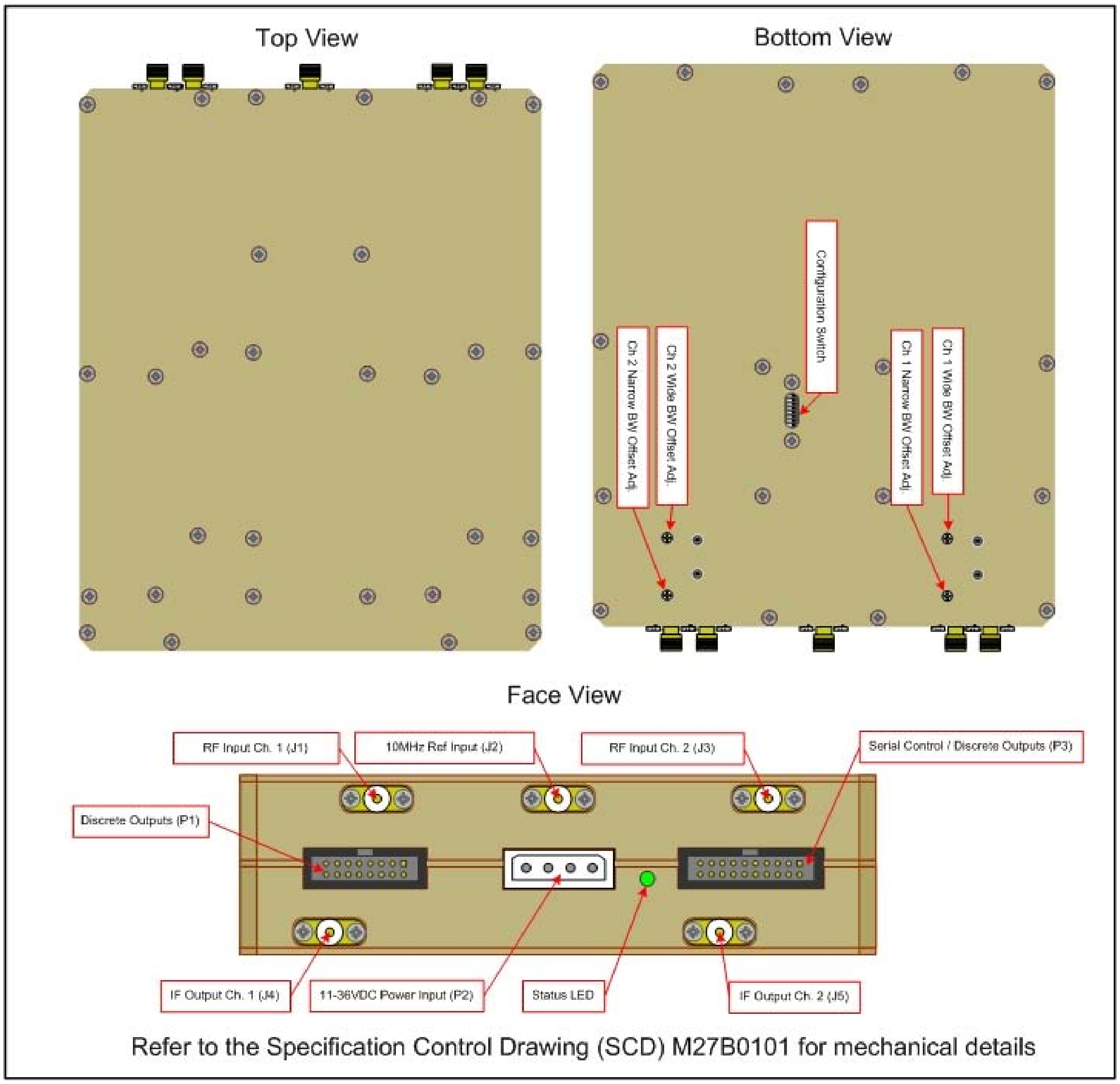



**Figure 3-1** LS27B Mechanical Outline Drawing

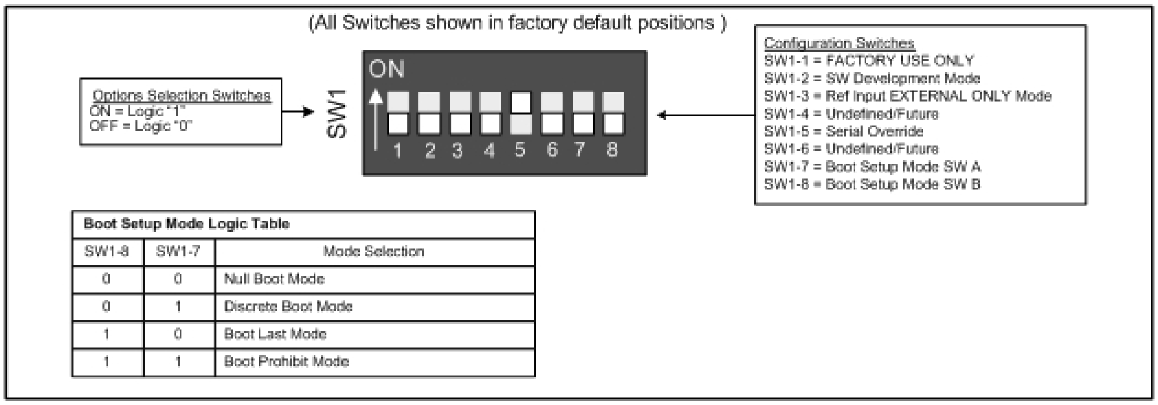



**Figure 3-2** Receiver Configuration Switch SW1

The configuration switches in Figure 3-2 have the following functions:

1.) The SW1-1 is defined as FACTORY USE and should remain in the OFF state as shown.

> **Warning:**
> SW1-1 is defined as FACTORY USE ONLY. In order to facilitate proper operation this switch MUST remain in the OFF position.

2.) The SW1-2 switch sets the LS27B to SW Development mode. When the switch is in the ON position, the serial status messages will contain dynamic data. The intent of this switch is to aid the development of user software without the necessity of having any inputs to the unit.

> **Warning:**
> If SW1-2 is in the ON position, the serial status will not reflect the actual input conditions. During normal operations, this switch MUST be in the OFF position.

3.) J2 allows for either an external reference source to be supplied to the receiver for synchronization to external RF hardware, or for the output of an on-board 10MHz reference to synchronize other external items to the unit's synthesizer reference source. SW1-3 controls the operation of the synthesizer reference clock distribution and PLL at boot-time. When SW1-3 is in the OFF position, the J2 connection is in an automatic sense mode. In this mode, at boot-time, the clock distribution system monitors for the presence of an external reference at port J2 (see Figures 3-1). If there is no external reference present at J2 (10MHz @ +4dBm) within 250msecs of boot-time, the unit will automatically switch the J2 input port to an output mode, enable on on-board 10MHz TCXO (+/- 3ppm stability minimum), and the route the 10MHz TCXO source to both the J2 output (at +2 to -2dBm @ 50 ohms) and use it to synchronize the internal synthesizers. When SW1-3 is in the ON position, the internal LS27B 10MHz reference clock will be disabled and the J2 connector will be switched to be a dedicated input. In this mode, the unit will presume the presence of an external 10MHz reference source.

> **Warning:**
> SW1-3 switch is set to ON, the reference input is in the "EXTERNAL ONLY" mode. If no external reference is supplied (10MHz @ >=4dBm), the unit will lack synthesizer synchronization which will affect the overall performance of the unit.

4.) Switch SW1-5 initiates the serial override mode. When in the ON position, the serial interface is automatically set to 57.6K BAUD for each serial communications channel. When in the OFF position, commands to alter the serial data rate can be issued.

5.) Switches SW1-7 and SW1-8 define the LS27B power-up boot configuration selection. This combination of switches allows the user to select pre-stored configuration setups by various methods. The description of these methods follows:

  **a.** **NULL Boot Mode** – In this mode, the LS27B receivers will not tune to any stored setups that may have been previously stored in the unit's internal non-volatile memory. When commanded via one of the appropriate serial interfaces, it will tune the receiver as commanded. In this mode, storage of setup parameters are stored in internal non-volatile memory.

  **b.** **Discrete Boot Mode –** In this mode, the LS27B receiver will be setups will be selected via the state of the external discrete lines on P3-7 thru P3-10. These discrete lines will determine a four bit number from zero to fifteen. At boot time, the LS27B will tune both receivers to the setup whose number is defined by the values of the discrete lines. Note that each receiver may still be tuned to a different frequency and setup, since each receiver has a separate list of 16 setups. Subsequent serial setup commands will override the boot setup and save that setup in non-volatile memory.

  **c.** **Boot Last Mode –** In this mode LS27B will program the receivers with the last valid setup. Subsequent setup commands will override the boot setup and replace the setup as directed by the user.

  **d.** **Boot Prohibit Mode** - This mode is designed for security conscious requirements. In this state the LS27B will not tune to any setup at power-up. Any serial commands will setup the receivers as usual, but no information will be retained internally in non-volatile memory. In addition, at boot time any existing setup information in any of the sixteen possible setup locations in non-volatile memory will be deleated.

6.) Switches defined as "Undefined/Future" have no implementation and thus their state is irrelevant.

## 3.3 Physical Installation

To install the receiver in the target computer system, the following procedure should be followed:

1. Perform a normal system shutdown of the target host system and remove the primary power plug.

2. Install the receiver in an unobstructed DVD/CD drive bay or in mounting rails. PCs vary in their mechanical configurations so it may be necessary to remove additional PC hardware to properly install the unit.

3. For mounting hardware locations, reference the Specification Control Drawing for the product (Doc. Number: M27B0101).

4. It is recommended that at least four 4-40UNC mounting screws (provided) be used in the mounting of the unit. This accommodates higher vibration and shock environments. Ensure that the installation provides room for the RF and I/O connections.

5. Airflow across the unit is strongly recommended to prevent long-term heat related damage. Multiple sets of mounting holes have been provided to allow for some rear fan clearances.

6. Connect the serial control interface to an available RS/EIA-232 interface via the P3 connector.

7. Connect the user I/O as desired via the P1 connector (refer to Figure 3-3).

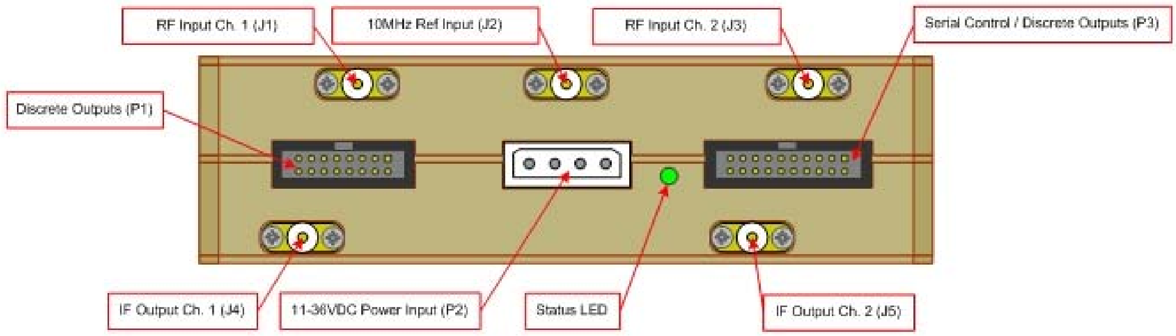
8. Connect the required RF and IF connections via the J-numbered connectors (refer to Figure 3-3).

9. Re-apply power to the unit and initiate the user software to communicate via the serial interface.

## 3.4 Interconnection

The receiver platforms provide multiple interface connectors. Figure 3-3 provides interface pin-outs and mating connector information for all connectors. Lumistar can provide an optional BNC style interface panel as shown in Figure 3-4 to ease the facilitation of user interfaces. Consult the factory for further details.

A communication harness is provided with the delivered unit. This harness is shown in Figure 3-5.




| J1 Connector | |
|---|---|
| RF Signal Input Ch. 1 | SMA Female |

| J2 Connector | |
|---|---|
| 10MHz Reference Input | SMA Female |

| J3 Connector | |
|---|---|
| RF Signal Input Ch. 2 | SMA Female |

| J4 Connector | |
|---|---|
| IF Signal Output Ch. 1 | SMA Female |

| J5 Connector | |
|---|---|
| IF Signal Output Ch. 2 | SMA Female |

| P1 Connector | Tyco PN:5103310-3 |
|---|---|
| Pin 1 | Ch. 2 AGC Output |
| Pin 2 | Ground |
| Pin 3 | Ch. 2 AM Output |
| Pin 4 | Ground |
| Pin 5 | Ch. 2 PCM Output #1 |
| Pin 6 | Ground |
| Pin 7 | Ch. 2 Optional Bias-T Vin |
| Pin 8 | Ground |
| Pin 9 | Ch. 1 AGC Output |
| Pin 10 | Ground |
| Pin 11 | Ch. 1 AM Output |
| Pin 12 | Ground |
| Pin 13 | Ch. 1 PCM Output #1 |
| Pin 14 | Ground |
| Pin 15 | Ch. 1 Optional Bias-T Vin |
| Pin 16 | Ground |

| P2 Connector | Molex PN:53109-0410 |
|---|---|
| Pin 1 | +11-36VDC Power |
| Pin 2 | Power Return |
| Pin 3 | Power Return |
| Pin 4 | (Unused) |

| P3 Connector | Tyco PN:5103310-5 |
|---|---|
| Pin 1 | SERIAL RDXA |
| Pin 2 | SERIAL TXDA |
| Pin 3 | SERIAL RTNC |
| Pin 4 | ------ |
| Pin 5 | ------ |
| Pin 6 | ------ |
| Pin 7 | DIO1 |
| Pin 8 | DIO2 |
| Pin 9 | DIO3 |
| Pin 10 | DIO4 |
| Pin 11 | DIO5 |
| Pin 12 | DIO RTN |
| Pin 13 | ------- |
| Pin 14 | SERIAL RXDB |
| Pin 15 | SERIAL TXDB |
| Pin 16 | SERIAL RTNB |
| Pin 17 | ------ |
| Pin 18 | SERIAL RXDC |
| Pin 19 | SERIAL TXDC |
| Pin 20 | SERIAL RTNC |

**Figure 3-3** LS27B Pin-outs and Connector Identification

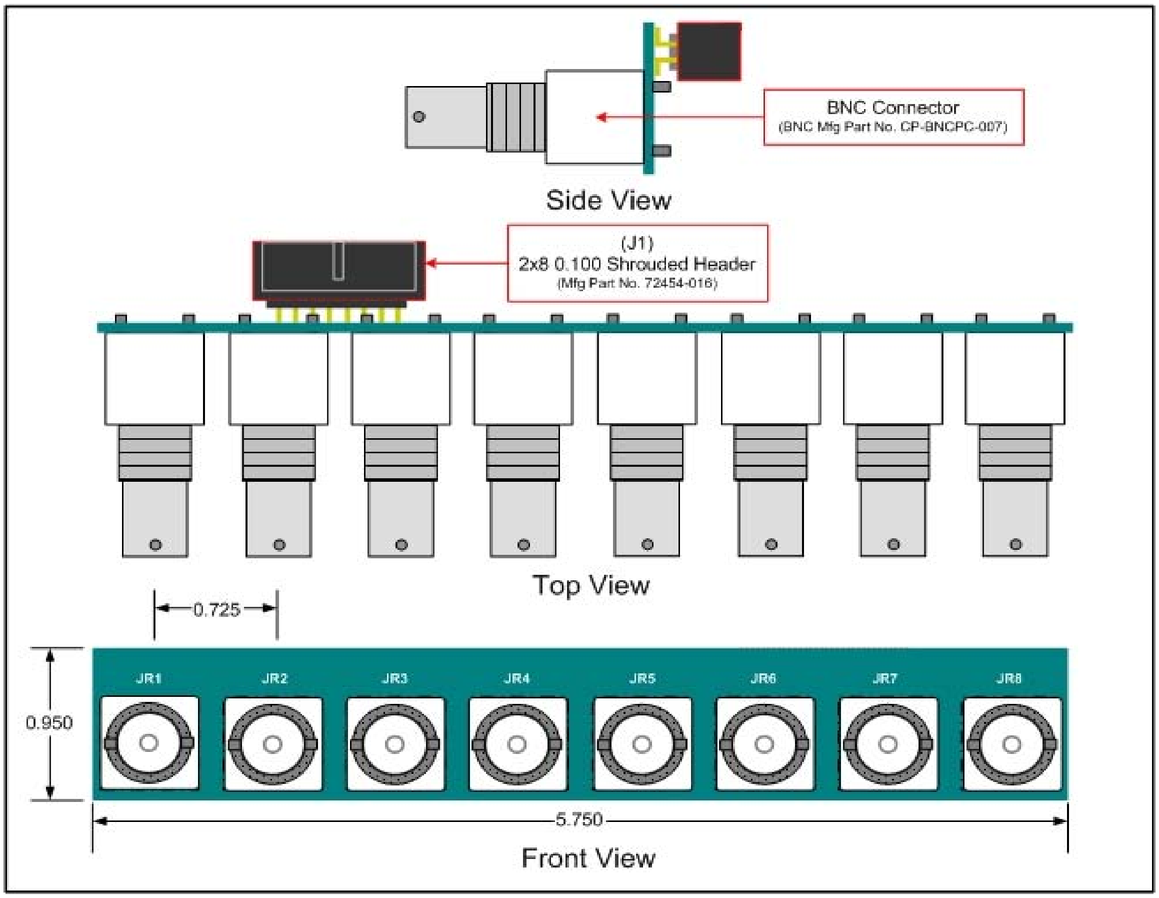



**Figure 3-4** LS27B Optional User Interface Panel

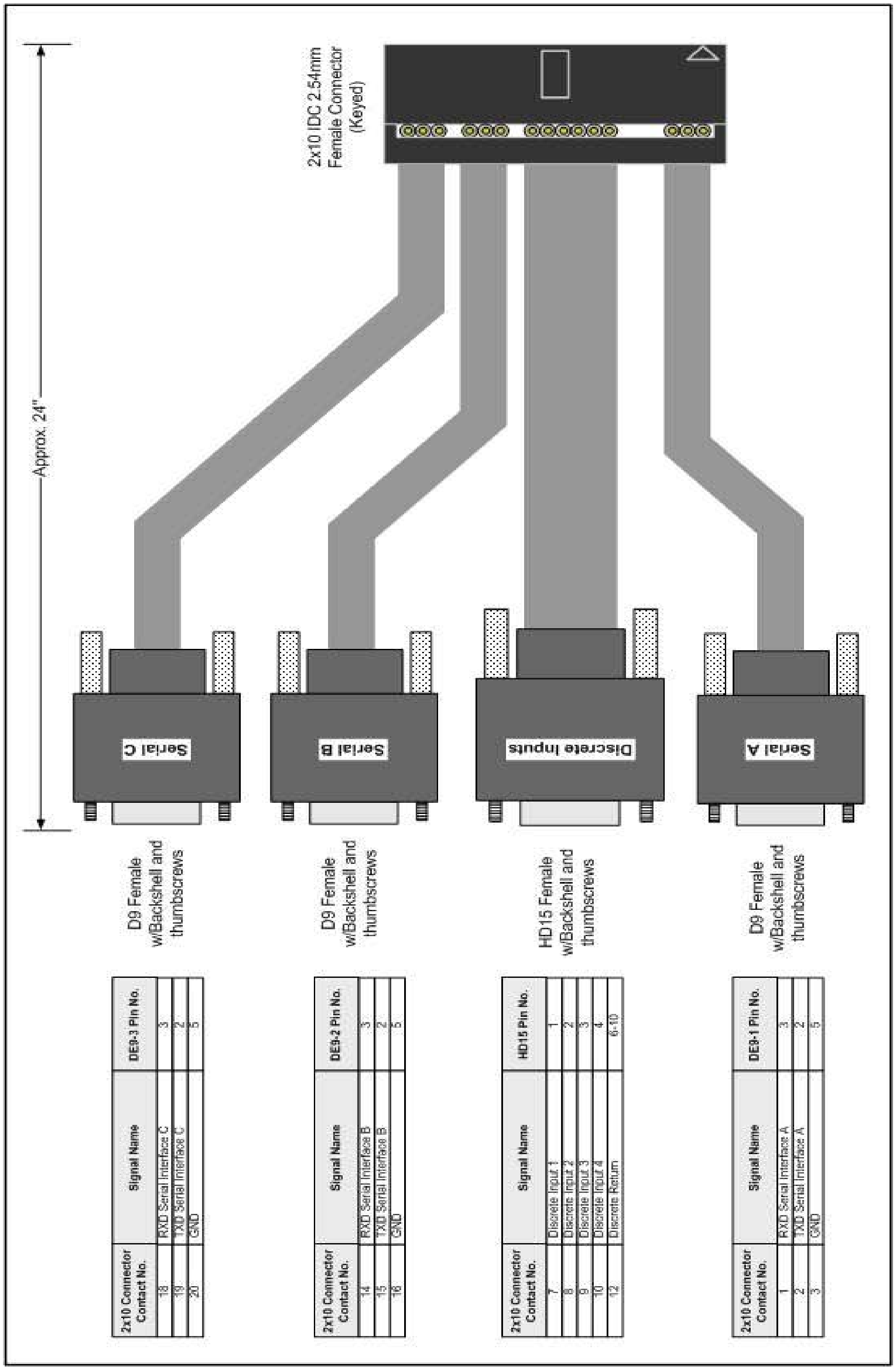



**Figure 3-5** LS27B Communication Interface Cable (C27B0001)

### 3.5 External Setup Discretes

As shown in Figure 3-3, connector P3 contains five discrete selection inputs (four of which are active). These bits are used to select previously stored user setups for the LS27B without the use of a serial host interface.

Each of the LS27B input channels allows the storage of up to sixteen (16) receiver setups. Using the serial interface, the user can program particular configurations for the receiver channels, and then select a corresponding storage number. The operation of these discretes is based on the boot-time mode selection switches of SW1-7 and SW1-8. (Refer to section 3.2 for the proper setting of the configuration switches to enable the use of the external setup discretes.)

The discrete inputs will function as the main controls until serial communications to the unit takes place. At that point, the discrete interfaces are ignored and control of the unit is switched to the serial interface.

Selection of the discrete (logic 1) is made by connecting the desired discrete input to P3-13 pin. If the discrete input is left disconnected, the input will be considered logic 0.

| DIO 4-0 Setting | Format Selected |
|---|---|
| $0000_b$ | Programmed Setup 0 |
| $0001_b$ | Programmed Setup 1 |
| $0010_b$ | Programmed Setup 2 |
| $0011_b$ | Programmed Setup 3 |
| $0100_b$ | Programmed Setup 4 |
| $0101_b$ | Programmed Setup 5 |
| $0110_b$ | Programmed Setup 6 |
| $0111_b$ | Programmed Setup 7 |
| $1000_b$ | Programmed Setup 8 |
| $1001_b$ | Programmed Setup 9 |
| $1010_b$ | Programmed Setup 10 |
| $1011_b$ | Programmed Setup 11 |
| $1100_b$ | Programmed Setup 12 |
| $1101_b$ | Programmed Setup 13 |
| $1110_b$ | Programmed Setup 14 |
| $1111_b$ | Programmed Setup 15 |

**Table 3-1** LS27B External Discrete Setup Selection Table

# 4 Communications

This chapter provides communications interface information pertaining to the LS27B drive bay dual receiver.

## 4.1 Serial Bus Interface

The LS27B is controlled and statused via a standard RS/EIA-232 asynchronous, 3-wire, serial interface method. The interface is capable of being run at rates between 9.6k BAUD and 115.2k BAUD with a default rate of 57.6k BAUD. The unit is shipped with SW1-5 position in the ON position. In this position, the unit will only communicate at 57.6k BAUD. (See programming section for details on how to alter the serial communication BAUD rate.)

The host communication channel should be setup in the following configuration:

| | |
|---|---|
| Number of bits: | 8 |
| Parity: | None |
| Stop Bits: | 1 |
| Flow Control: | None |

The design contains three serial interface channels, operating via two different protocols: "single receiver protocol" and "dual receiver protocol". Refer to Figure 3-3 for pin-out assignments.

### 4.1.1 Serial Bus Interface – Dual Receiver Interface Protocol

The Serial "A" bus, contained on P3 pins 1 thru 3, communicates via the "Dual Receiver Interface Protocol" defined in chapter 5. This protocol is "enhanced" from the existing "LS25B" protocol and provides for controls for both receiver channels via a single physical interface.

**Information:**
The "dual receiver" interface protocol provides some expanded functional capabilities that are not available via the previous LS25B "single receiver" interface protocol.

### 4.1.2 Serial Bus Interface – Single Receiver Interface Protocol

The Serial "B" bus, contained on P3 pins 14 thru 16, and Serial "C" bus, contained on P3 pins 18 thru 20, communicates via the existing LS25B Single Receiver Interface Protocol defined in chapter 5. The Serial "B" control/status interface is dedicated to the Channel 1 receiver. The Serial "C" bus control/status interface is dedicated to Channel 2 receiver.

**Warning:**
Only utilize one interface protocol at a time. Do not communicate on all three interfaces simulatenously.

# 5 Communications

This chapter provides interface protocol information for the LS27B drive bay dual receiver.

The LS27B product provides a dual protocol interface method. It supports a "single receiver protocol" which is operational compatible with the previous Lumistar generation of LS25B drive-bay receiver. It also supports an enhanced "dual receiver protocol" which provides some additional functional capabilities.

## *5.1 Single Receiver Protocol*

Single receiver protocol is active on serial interface B which controls receiver number one of the device, and serial interface C, which controls receiver number two. The two receiver interfaces can be operated simultaneously and autonomously. All command/status information contained in the following sections relates to single channel operation but the format is identical between channels.

### *5.1.1 Single Receiver Protocol - Command and Status Messaging*

Interface using the single receiver protocol is via command-response messaging. For every command sent from the host, the receiver will respond to indicate that the command was received. Commands from the host are grouped in two categories: primary commands and secondary commands. Primary commands are used to control the basic tuning and setup of the receiver. Secondary commands are used to set various "lower-priority" operational modes and to obtain secondary status. Secondary host commands occasionally require that the host send two commands: a first command followed by a status request message.

All host messages require a message header of six (6) bytes. If the host command requires additional data be transferred to the host, the data will immediately follow the command header. Figure 5-1 contains a diagram of the message header for the single receiver protocol.

The first byte of the message header contains a device identification flag of 0x25. The second byte indicates the module address being commanded. For RS-232 communications, this should always be set to 0x00. Bytes 3 and 4 contain the message identification. Message identification informs the type and format of data that will follow the header, if any. Bytes 5 and 6 of the message header indicate the number of command related bytes that follow the message header.

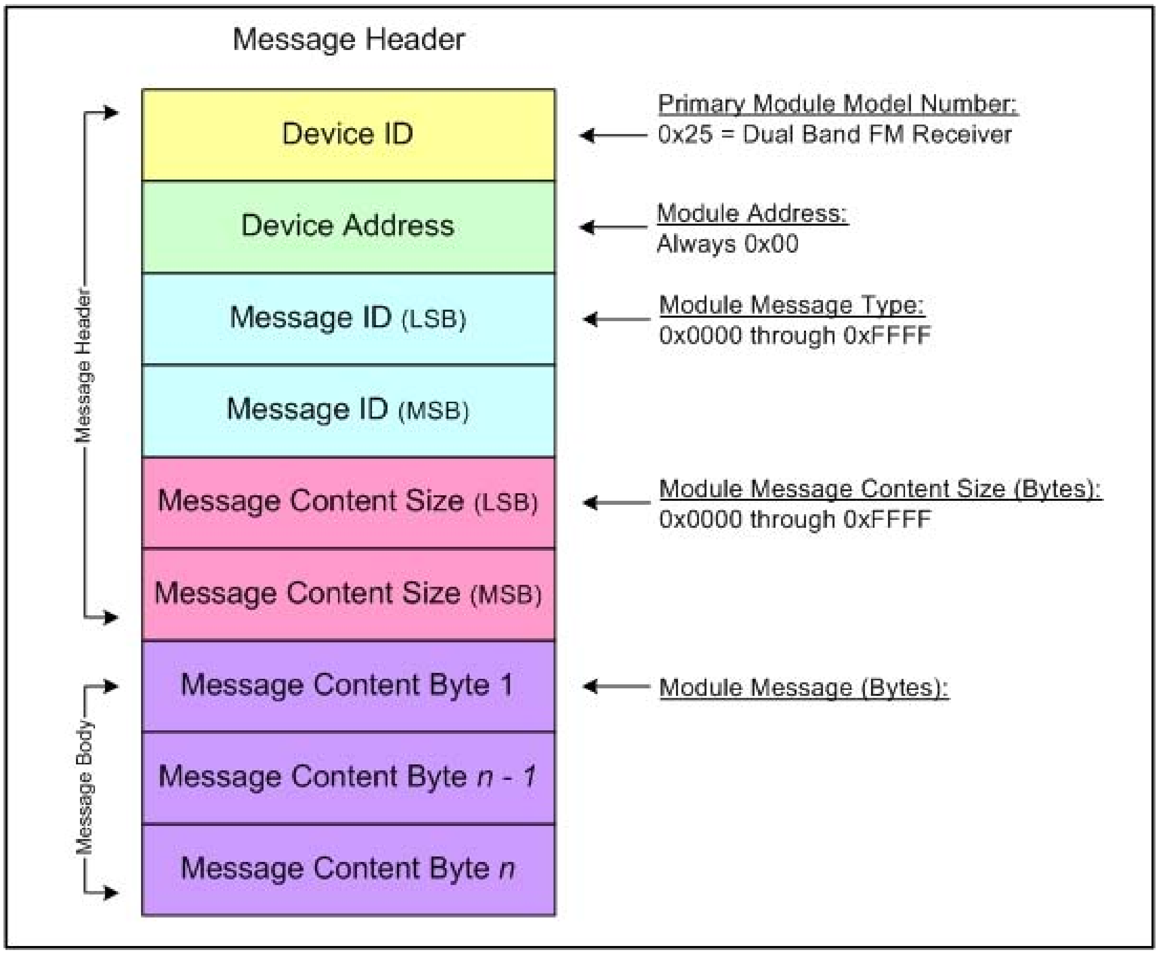



Figure 5-1 **Single Receiver Protocol Message Format**

In response to any host command, the protocol will respond with a minimum of an echoed message header. If additional information is to be conveyed to the host, the data will immediately follow the echoed header. Figure 5-2 indicates the general configuration of the host and terminal responses.

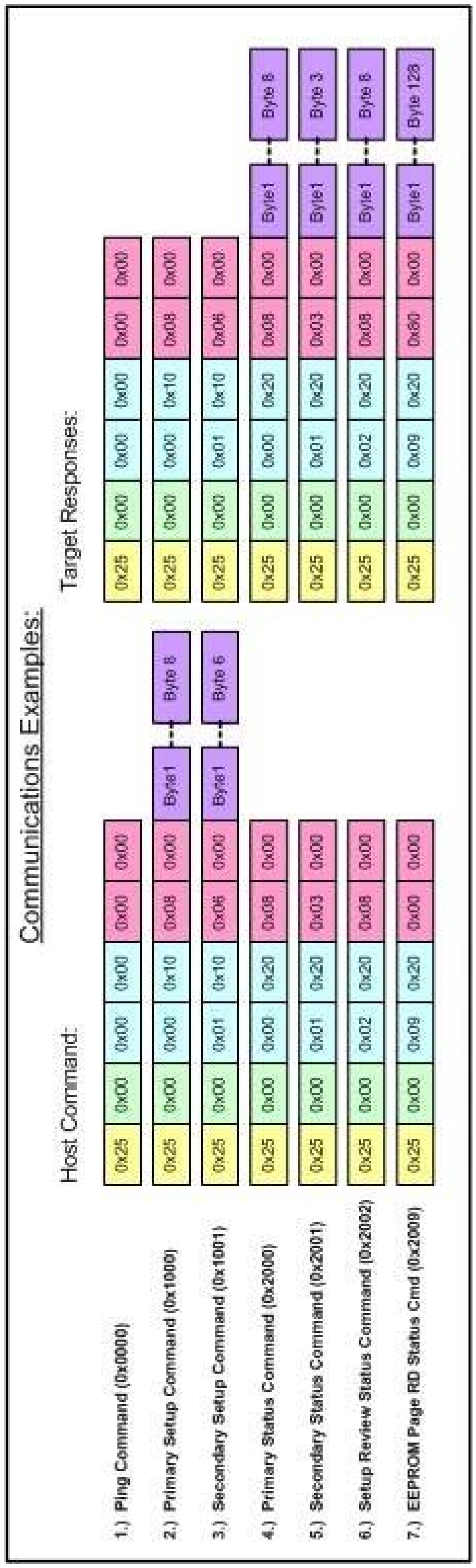



Figure 5-2 **Single Receiver Protocol Messaging Configurations**

### *5.1.1.1 Single Receiver Protocol - Command Messaging*

There are three command message types: a "Ping" command, a "Primary Setup" command, and a "Secondary Setup" command.

#### *5.1.1.1.1 Single Receiver Protocol - PING Command*

The "Ping" command is used as to determine the health/presence of the communications channel between the host and the receiver. In response to the "Ping" command, the receiver will echo the received message header back to the host.

#### *5.1.1.1.2 Single Receiver Protocol - Primary Setup Command*

The "Primary Setup" command is provides fundamental control information to the receiver channel. The message header is followed by eight (8) data bytes as defined in Figure 5-3.

**Primary Command Message Content (Message ID = 0x1000)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TLM2DEMP | POLARITY | AMINV | REF | - | LINEAR | TCONST | | |
| 2 | DO3 | DO2 | DO1 | DO0 | - | - | - | - | |
| 3 | VFILT | | | | IFFILT | | | | |
| 4 | - | - | - | - | AMFILT | | - | RFBAND | |
| 5 | TUNE1 (Fc /256MHz) | | | | | | | | |
| 6 | TUNE2 (Fc *mod* 256MHz/1MHz) | | | | | | | | |
| 7 | TUNE3 (Fc *mod* 1MHz/10kHz) | | | | | | | | |
| 8 | SNUM | | | | | | | | |

Figure 5-3 **Single Receiver Protocol Primary Message Command Structure**

**Caution:**

Only 8 IF Filter bandwidths and 8 Video Filter bandwidths are available in the LS27B configuration. Selections of bandwidths are above this number will be ignored.

#### *5.1.1.1.3 Single Receiver Protocol - Secondary Setup Command*

The "Secondary Setup" command is provides non-critical control information to the receiver channel and requests that internal status from the controlled channel. The message header is followed by six (6) data bytes as defined in Figure 5-4.

**Secondary Command Message Content (Message ID = 0x1001)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | MODE | | | | | | | | |
| 2 | CMD1 | | | | | | | | |
| 3 | CMD2 | | | | | | | | |
| 4 | CMD3 | | | | | | | | |
| 5 | CMD4 | | | | | | | | |
| 6 | CMD5 | | | | | | | | |

Figure 5-4 **Single Receiver Protocol Secondary Message Command Structure**

### *5.1.1.2 Single Receiver Protocol - Command Bit/Byte Definitions*

Figure 5-5 contains the bit and bit pairing definitions for the primary and the secondary messages. Figure 5-6 contains the definition for the secondary message mode byte.

| Command Mnemonic | Description/Definition | Logic State/Explanation |
|---|---|---|
| TLM2DEMP | TLM2 Out De-emphasis video filter selection | 0 = Disabled; 1 = Enabled |
| POLARITY | Demodulator Polarity Invert | 0 = Normal Polarity; 1 = Inverted Polarity |
| AMINV | AM Output Inversion | 0 = Normal Polarity; 1 = Inverted Polarity |
| REF | Reference Source Select | 0 = Internal 10MHz Reference Osc. Select; 1 = External Reference Osc. Select |
| LINEAR | Linear Output Select | 0 = Linear Output Disabled; 1 = Linear Output Enabled |
| TCONST | AGC Time Constant Select | 00 = Shortest Time Constant 01 = Next to Longest Time Constant<br>10 = Next to Shortest Time Constant 11 = Longest Time Constant |
| VFILT | Video Filter Select | 0000 = Video Filt.0 0100 = Video Filt.4 1000 = Video Filt.8 11xx = (Unused)<br>0001 = Video Filt.1 0101 = Video Filt.5 1001 = Video Filt.9<br>0010 = Video Filt.2 0110 = Video Filt.6 1010 = Video Filt.10<br>0011 = Video Filt.3 0111 = Video Filt.7 1011 = Video Filt.11 |
| IFFILT | IF Filter Select | 0000 = IF Filt.0 0100 = IF Filt.4 1000 = IF Filt.8 11xx = (Unused)<br>0001 = IF Filt.1 0101 = IF Filt.5 1001 = IF Filt.9<br>0010 = IF Filt.2 0110 = IF Filt.6 1010 = IF Filt.10<br>0011 = IF Filt.3 0111 = IF Filt.7 1011 = IF Filt.11 |
| RFBAND | RF Band Select | 0 = Highest Frequency Band Enabled; 1 = Lowest Frequency Band Enabled |
| AMFILT | AM Low-Pass Filter Cutoff Select | 00 = EEPROM Contents 39 01 = EEPROM Contents 40<br>10 = EEPROM Contents 41 11 = EEPROM Contents 42 |
| TUNE1 | Receiver Tune Center Frequency Wd 1 | Wd1 Receive Center Frequency (MHz) Fc/256MHz |
| TUNE2 | Receiver Tune Center Frequency Wd 2 | Wd2 Receiver Center Frequency (MHz) (Fc mod 256MHz)/1MHz |
| TUNE3 | Receiver Tune Center Frequency Wd 3 | Wd3 Receiver Center Frequency (MHz) (Fc mod 1MHz)/10kHz |
| SNUM | Setup storage Number | Value between 0 and 15 |
| MODE | Secondary Operations Mode Command | [See Operational Mode Table] |
| CMD1 | Secondary Command Wd 1 | [See Operational Mode Table] |
| CMD2 | Secondary Command Wd 2 | [See Operational Mode Table] |
| CMD3 | Secondary Command Wd 3 | [See Operational Mode Table] |
| CMD4 | Secondary Command Wd 4 | [See Operational Mode Table] |
| CMD5 | Secondary Command Wd 5 | [See Operational Mode Table] |

Figure 5-5 **Single Receiver Protocol Command Bit Grouping Definitions**

| Mode | Definition | CMD5 | CMD 4 | CMD3 | CMD2 | CMD1 |
|---|---|---|---|---|---|---|
| 0x02 | Digipot Mode | (Unused) | (Unused) | *Digipot Select:*<br>0x01 = AGC Slope<br>0x02 = AM Gain<br>0x04 = LOG Level | *Digipot Preset Value:*<br>0-99 Digipot Setting | *Digipot Instruction:*<br>0x01 = Decrement Digitpot<br>0x02 = Increment Digipot<br>0x03 = Set Digipot to Preset Value<br>0x04 = Query Digipot Setting |
| 0x03 | DAC Mode | (Unused) | (Unused) | *DAC Data:*<br>6 MSBs of DAC Setting | *DAC Data:*<br>8 LSBs of DAC Setting | *DAC Selection:*<br>0x01 = TLM Gain<br>0x02 = RF Attn Control |
| 0x04 | Ext. Ref. Mode | (Unused) | (Unused) | (Unused) | (Unused) | Ext. Reference Freq. (MHz) |
| 0x05 | Stored Setup Review | (Unused) | (Unused) | (Unused) | (Unused) | *Stored setup number:*<br>Value between 0-15 |
| 0x07 | EEPROM Mode | *PROM Write Data:*<br>8MSBs of Write Data | *PROM Write Data:*<br>8LSBs of Write Data | *PROM Line:*<br>Value Between 0-63 or 255 For page response (see information below) | *PROM Page:*<br>Value Between 0-15 | *Mode:*<br>0x00 = RD PROM 0 (Primary)<br>0x01 = WR PROM 0 (Primary)<br>0x10 = RD PROM 1 (Secondary)<br>0x11 = WR PROM 1 (Secondary) |
| 0x1F | Serial Channel Control Mode | (Unused) | (Unused) | 3 MSBits of (BAUD Rate/100). | 8 LSBits of (BAUD Rate/100). | 0x00 = Serial Baudrate Select Submode. |

Figure 5-6 **Single Receiver Protocol Secondary Command Mode Definitions**

### 5.1.1.3 Single Receiver Protocol - Status Messaging

There are four (4) status message types: primary status response, secondary status response, stored setup status response, and the EEPROM Page read status response.

#### 5.1.1.3.1 Single Receiver Protocol - Primary Status Response

The primary status response provides the host with fundamental receiver status such as the received signal strength, FM deviation measurement, AM index value, and the detected AM frequency. Figure 5-7 depicts the primary status message content.

**Primary Status Response Content (Message ID = 0x2000)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | - | - | - | - | MODID | | | | |
| 2 | RSSI7 | RSSII6 | RSSI5 | RSSI4 | RSSI3 | RSSI2 | RSSI1 | RSSI0 | |
| 3 | - | - | - | - | - | - | RSSI9 | RSSI8 | |
| 4 | DEV | | | | | | | | |
| 5 | AMI | | | | | | | | |
| 6 | AMFREQ1 | | | | | | | | |
| 7 | AMFREQ2 | | | | | | | | |
| 8 | SNUM | | | | | | | | |

Figure 5-7 **Single Receiver Protocol Primary Status Message Structure**

#### 5.1.1.3.2 Single Receiver Protocol - Secondary Status Response

The secondary status response provides the receiver with configuration information and provides information relates to mode commands. Figure 5-8 depicts the secondary status message content.

**Secondary Status Response Content (Message ID = 0x2001)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | MODE | | | | | | | | |
| 2 | RTN1 | | | | | | | | |
| 3 | RTN2 | | | | | | | | |

Figure 5-8 **Single Receiver Protocol Secondary Status Message Structure**

### 5.1.1.4 Single Receiver Protocol - Stored Setup Status Response

A total of sixteen (16) receiver setups can be stored in the receiver's internal memory and then be recalled by simply providing an index value. (Future provisions will allow these setups to be activated via discrete interaction.) These configurations can be reviewed using secondary mode commands. The stored setup status response message structure is shown in Figure 5-9.

**Stored Setup Status Response Content (Message ID = 0x2002)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | TLM2DEMP | POLARITY | AMINV | REF | - | LINEAR | TCONST | | |
| 2 | - | - | - | - | MODID | | | | |
| 3 | VFILT | | | | IFFILT | | | | |
| 4 | - | - | - | - | AMFILT | | - | RFBAND | |
| 5 | TUNE1 (Fc /256MHz) | | | | | | | | |
| 6 | TUNE2 (Fc *mod* 256MHz/1MHz) | | | | | | | | |
| 7 | TUNE3 (Fc *mod* 1MHz/10kHz) | | | | | | | | |
| 8 | SNUM | | | | | | | | |

Figure 5-9 **Single Receiver Protocol Stored Setup Status Message Structure**

### *5.1.1.5 Single Receiver Protocol - EEPROM Page Read Status Response*

The primary receiver configuration information, used to drive software controls, is found in the first page (indexed from 0) of the receivers primary internal EEPROM. Information contained in this EEPROM includes the bandwidths installed in the receiver, associated IF and video filter bandwidths, along with various other configuration information. This information can be accessed via an EEPROM read mode command. The resulting status message contents are shown in the Figure 5-10. An example of the EEPROM contents is shown in Figure 5-12.

**EEPROM Page Read Response Content (Message ID = 0x2009)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | LOC0_LSB | | | | | | | | |
| 2 | LOC0_MSB | | | | | | | | |
| … | … | | | | | | | | More bytes |
| 127 | LOC63_LSB | | | | | | | | |
| 128 | LOC63_MSB | | | | | | | | |

Figure 5-10 **Single Receiver Protocol EEPROM Page Read Status Message Structure**

### *5.1.1.6 Single Receiver Protocol - Status Bit/Byte Definitions*

Figure 5-11 contains the bit and bit pairing definitions for the status messages.

| Status Mnemonic | Description/Definition | Logic State/Explanation |
|---|---|---|
| MODID | Module Serial ID | Value between 0 and 15; RS232 indicated by address 0 |
| RSSI0-9 | RSSI Signal Strength | Value between 0 and 1024 (Linear dBm = ( 0.0782 x Value) - 100.0; Limited dBm = (0.1075 x Value) - 100.0) |
| DEV | FM Deviation Estimate | Value between 0 and 120 |
| AMI | AM Index Estimate | Value between 0 and 100 |
| AMFREQ1 | AM Frequency Wd 1 | 8 MSBs of the AM Frequency Counter |
| AMFREQ2 | AM Frequency Wd 2 | 8 LSBs of the AM Frequency Counter |
| TLM2DEMP | TLM2 Out De-emphasis video filter selection | 0 = Disabled; 1 = Enabled |
| POLARITY | Demodulator Polarity Invert | 0 = Normal Polarity; 1 = Inverted Polarity |
| AMINV | AM Output Inversion | 0 = Normal Polarity, 1 = Inverted Polarity |
| REF | Reference Source Select | 0 = Internal 10MHz Reference Osc. Select; 1 = External Reference Osc. Select |
| LINEAR | Linear Output Select | 0 = Linear Output Disabled; 1 = Linear Output Enabled |
| TCONST | AGC Time Constant Select | 00 = Shortest Time Constant 01= Next to Longest Time Constant<br>10 = Next to Shortest Time Constant 11= Longest Time Constant |
| VFILT | Video Filter Select | 0000 = Video Filt.0 0100 = Video Filt.4 1xxx = (Unused)<br>0001 = Video Filt.1 0101 = Video Filt.5<br>0010 = Video Filt.2 0110 = Video Filt.6<br>0011 = Video Filt.3 0111 = Video Filt.7 |
| IFFILT | IF Filter Select | 0000 = IF Filt.0 0100 = IF Filt.4 1xxx = (Unused)<br>0001 = IF Filt.1 0101 = IF Filt.5<br>0010 = IF Filt.2 0110 = IF Filt.6<br>0011 = IF Filt.3 0111 = IF Filt.7 |
| RFBAND | RF Band Select | 0 = Highest Frequency Band Enabled; 1 = Lowest Frequency Band Enabled |
| AMFILT | AM Low-Pass Filter Select | 00 = Lowest Fcutoff 01 = Next to Lowest Fcutoff<br>10 = Next to highest Fcutoff 11 = Highest Fcutoff |
| TUNE1 | Receiver Tune Center Frequency Wd 1 | Wd1 Receive Center Frequency (MHz) Fc/256MHz |
| TUNE2 | Receiver Tune Center Frequency Wd 2 | Wd2 Receiver Center Frequency (MHz) (Fc mod 256MHz)/1MHz |
| TUNE3 | Receiver Tune Center Frequency Wd 3 | Wd3 Receiver Center Frequency (MHz) (Fc mod 1MHz)/10kHz |
| SNUM | Setup storage Number | Value between 0 and 15 |
| MODE | Secondary Operations Mode Command | [See Operational Mode Table] |
| RTN1 | Secondary Status Wd 1 | [See Operational Mode Table] |
| RTN2 | Secondary Status Wd 2 | [See Operational Mode Table] |
| LOC0 LSB | EEPROM Contents – LSB | EEPROM Page Content Data Byte |
| LOC0 MSB | EEPROM Contents – MSB | EEPROM Page Content Data Byte |
| LOC63 LSB | EEPROM Contents – LSB | EEPROM Page Content Data Byte |
| LOC63 MSB | EEPROM Contents – MSB | EEPROM Page Content Data Byte |

Figure 5-11 **Single Receiver Protocol Status Response Bit Grouping Definitions**

| EEPROM Map | | |
|---|---|---|
| **Offset** | **Contents** | **Description/ Information** |
| 0 | Signal Bandwidth IF Filter 0 (kHz) | IF Filter Bandwidth (Hz) = Value x1000 Hz |
| 1 | Signal Bandwidth IF Filter 1 (kHz) | |
| 2 | Signal Bandwidth IF Filter 2 (kHz) | |
| 3 | Signal Bandwidth IF Filter 3 (kHz) | |
| 4 | Signal Bandwidth IF Filter 4 (kHz) | |
| 5 | Signal Bandwidth IF Filter 5 (kHz) | |
| 6 | Signal Bandwidth IF Filter 6 (kHz) | |
| 7 | Signal Bandwidth IF Filter 7 (kHz) | |
| 8 | *(Unused / Spare)* | |
| 9 | *(Unused / Spare)* | |
| 10 | *(Unused / Spare)* | |
| 11 | *(Unused / Spare)* | |
| 12 | Signal Bandwidth Video Filter 0 (kHz) | Video Filter Bandwidth (Hz) = Value x1000 Hz |
| 13 | Signal Bandwidth Video Filter 1 (kHz) | |
| 14 | Signal Bandwidth Video Filter 2 (kHz) | |
| 15 | Signal Bandwidth Video Filter 3 (kHz) | |
| 16 | Signal Bandwidth Video Filter 4 (kHz) | |
| 17 | Signal Bandwidth Video Filter 5 (kHz) | |
| 18 | Signal Bandwidth Video Filter 6 (kHz) | |
| 19 | Signal Bandwidth Video Filter 7 (kHz) | |
| 20 | *(Unused / Spare)* | |
| 21 | *(Unused / Spare)* | |
| 22 | *(Unused / Spare)* | |
| 23 | *(Unused / Spare)* | |
| 24 | RF Input Attenuator Set Point | |
| 25 | *(Unused / Spare)* | |
| 26 | RF Band 0 Start Frequency (MHz) | RF Band Edge = Value x 1MHz |
| 27 | RF Band 0 Stop Frequency (MHz) | |
| 28 | RF Band 1 Start Frequency (MHz) | |
| 29 | RF Band 1 Stop Frequency (MHz) | |
| 30 | RF Band 0 Linear Output Compression | Linear Output Compression Point (RSSI Count) |
| 31 | RF Band 1 Linear Output Compression | |
| 32 | AGC Time Constant Count #0 | AGC Time Constant (msec) = Constant Count x 0.1msec |
| 33 | AGC Time Constant Count #1 | |
| 34 | AGC Time Constant Count #2 | |
| 35 | AGC Time Constant Count #3 | |
| 36 | *(Unused / Spare)* | |
| 37 | *(Unused / Spare)* | |
| 38 | AM LPF Filter #0 | AM Low-pass filter Bandwidth = Value x 1Hz |
| 39 | AM LPF Filter #1 | |
| 40 | AM LPF Filter #2 | |
| 41 | AM LPF Filter #3 | |
| 42 | De-emphasis Filter Line Count | Video Line Count: 525 = NTSC |
| 43 | *(Unused / Spare)* | |
| 44 | Max Preset Value | Maximum number of User Presets (Indexed from 0) |
| 45 | Active Setup Value | Preset Number at Boot-time |
| 46 | *(Unused / Spare)* | |
| 47 | *(Unused / Spare)* | |
| 48 | FPGA Firmware ID | FPGA Firmware Number |
| 49 | DSP Firmware ID1 | DSP Firmware Date: MSB = Month in Hex, LSB = Day in Hex |
| 50 | DSP Firmware ID2 | DSP Firmware Date: Two Bytes = Year in Hex |
| 51 | Board Serial Number MSW | Device Serial Number in Hex. |
| 52 | Board Serial Number LSW | |
| 53 | Primary Configuration ID | ASCII Representation Of Device ID (Always 0x25) |
| 54 | Options #1 | ASCII Representation Of Device Options (Future Use) |
| 55 | Options #2 | |
| 56 | *(Unused / Spare)* | |
| 57 | Serial Channel Baud Rate | Serial Channel BAUD/100 |
| 58 | Serial Channel Format | Serial Channel Signaling Level = 232 |
| 59 | *(Unused / Spare)* | |
| 60 | *(Unused / Spare)* | |
| 61 | Ext. Ref. Input Freq. Multiplier | External Reference Input Frequency = Multiplier x 1MHz |
| 62 | *(Unused / Spare)* | |
| 63 | *(Unused / Spare)* | |

Figure 5-12 **Single Receiver Protocol - EEPROM Contents**

## *5.2 Dual Receiver Protocol*

Dual receiver protocol is active on serial interface A only. This interface controls both internal receivers using the same serial interface channel. Each receivers operations are autonomous.

### *5.2.1 Dual Receiver Protocol - Command and Status Messaging*

Interface using the dual receiver protocol is via command-response messaging. For every command sent from the host, the receiver will respond to indicate that the command was received. Commands from the host are grouped in two categories: primary commands and secondary commands. Primary commands are used to control the basic tuning and setup of the receiver. Secondary commands are used to set various “lower-priority” operational modes and to obtain secondary status. Secondary host commands occasionally require that the host send two commands: a first command followed by a status request message.

All host messages require a message header of six (6) bytes. If the host command requires additional data be transferred to the host, the data will immediately follow the command header. Figure 5-13 contains a diagram of the message header for the dual receiver protocol.

The first byte of the message header contains a device identification flag of 0x27. The second byte indicates the module address being commanded which should always be set to 0x00. Bytes 3 and 4 contain the message identification. Message identification informs the type and format of data that will follow the header, if any. Bytes 5 and 6 of the message header indicate the number of command related bytes that follow the message header.

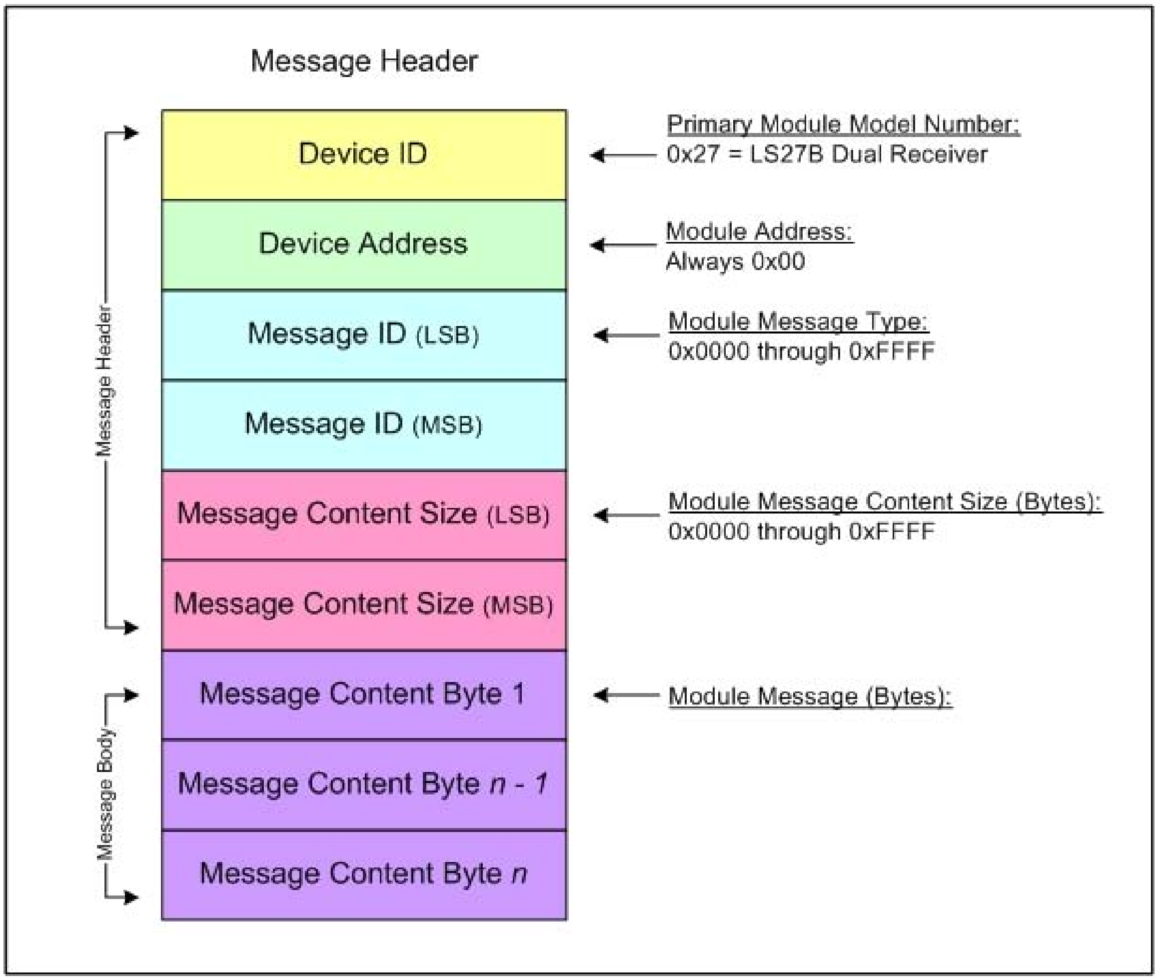



Figure 5-13 **Dual Receiver Protocol Message Format**

In response to any host command, the protocol will respond with a minimum of an echoed message header. If additional information is to be conveyed to the host, the data will immediately follow the echoed header. Figure 5-14 indicates the general configuration of the host and terminal responses.

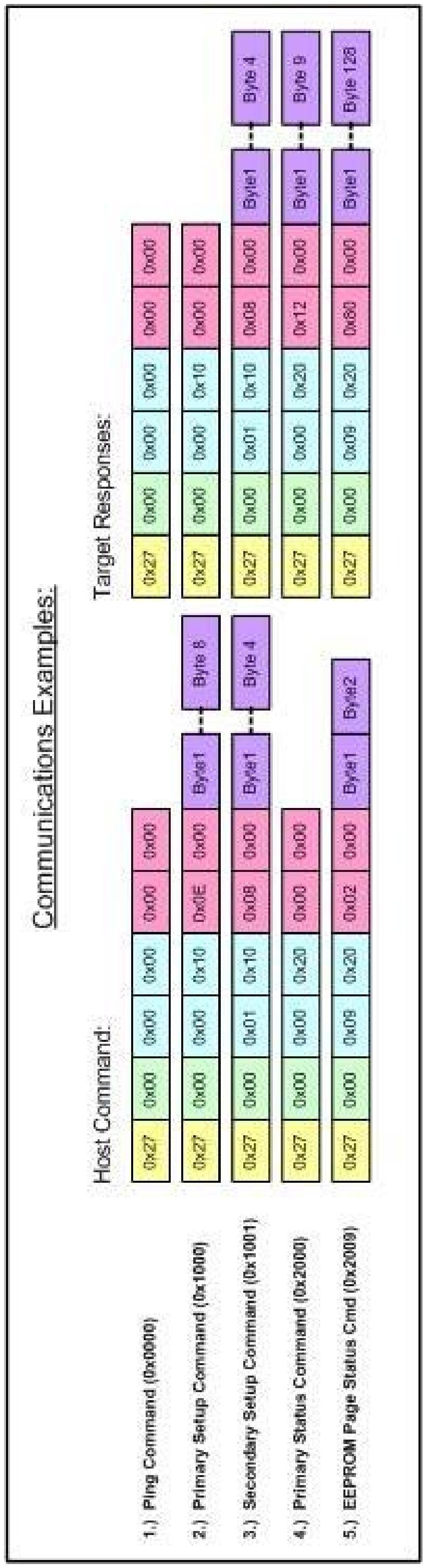



Figure 5-14 **Dual Receiver Protocol Messaging Configurations**

### *5.2.1.1 Dual Receiver Protocol - Command Messaging*

There are three command message types: a "Ping" command, a "Primary Setup" command, and a "Secondary Setup" command.

#### *5.2.1.1.1 Dual Receiver Protocol - PING Command*

The "Ping" command is used as to determine the health/presence of the communications channel between the host and the receiver. In response to the "Ping" command, the receiver will echo the received message header back to the host.

#### *5.2.1.1.2 Dual Receiver Protocol - Primary Setup Command*

The "Primary Setup" command is provides fundamental control information to the receiver channel. The message header is followed by eight (8) data bytes as defined in Figure 5-3.

**Primary Command Message Content (Message ID = 0x1000)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | - | - | POLARITY | SNUM | | | | CHx | |
| 2 | INTREF | - | - | - | - | - | - | - | |
| 3 | LIM | | | | FRZ | AGCTC | | | |
| 4 | - | IFBW | | | DEMP | VFILT | | | |
| 5 | AMINV | | | AMFIL | | | | | |
| 6 | TUNE1 (Fc /256MHz) | | | | | | | | |
| 7 | TUNE2 (Fc *mod* 256MHz/1MHz) | | | | | | | | |
| 8 | TUNE3 (Fc *mod* 1MHz/10kHz) | | | | | | | | |

Figure 5-15 **Dual Receiver Primary Protocol Message Command Structure**

#### *5.2.1.1.3 Dual Receiver Protocol - Secondary Setup Command*

The "Secondary Setup" command is provides control information to the receiver channel commanded and requests that internal status from the controlled channel. The message header is followed by four (4) data bytes as defined in Figure 5-15.

**Secondary Command Message Content (Message ID = 0x1001)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | MODE | | | | | | | CHx | |
| 2 | CMD1 | | | | | | | | |
| 3 | CMD2 | | | | | | | | |
| 4 | CMD3 | | | | | | | | |

Figure 5-15 **Dual Receiver Protocol Secondary Message Command Structure**

### 5.2.1.2 Dual Receiver Protocol - Command Bit/Byte Definitions

Figure 5-16 contains the bit and bit pairing definitions for the primary and the secondary messages. Figure 5-17 contains the definition for the secondary message mode byte. Figure 5-18 contains the definitions for the secondary message mode responses.

| Command Mnemonic | Description/Definition | Logic State/Explanation |
|---|---|---|
| CHx | Radio Selection Number | 0=Radio 1 or Down Converter 1, 1=Radio 2 or Down Converter 2 |
| INTREF | Internal/External Reference Clock Selection | 0=Select External Reference Clock, 1=Select Internal Reference Clock |
| POLARITY | FM Demodulator Output Polarity | 0=Normal Polarity, 1=Inverse Polarity |
| LIM | Hardware Limited Mode | 0=LIM mode is off, 1=LIM mode is on. |
| FRZ | AGC Freeze | 0=Freeze AGC (infinite AGCTC), 1=Use selected AGCTC. |
| AGCTC | AGC Time Constant Selection | 0=0.1 msec, 1=1 msec, 2=10 msec, 3=100 msec, 4=1 sec, 5=CustomTC1, 6=CustomTC2, 7=CustomTC3 |
| IFBW | IFBW Filter Selection | 0=Filter 1, 1=Filter 2, 2=Filter 3, 3=Filter 4, 4=Filter 5, 5=Filter 6, 6=Filter 7, 7=Filter 8 |
| VFLT | Video Filter Selection | 0=Filter 1, 1=Filter 2, 2=Filter 3, 3=Filter 4, 4=Filter 5, 5=Filter 6, 6=Filter 7, 7=Filter 8 |
| DEMP | DeEmphasis Filter Selection | 0=Don't use DeEmphasis Filter, 1=Use DeEmphasis Filter. |
| AMINV | AM Inverse | 0=AM is normal, 1=AM is inverted. |
| AMFIL | AM Filter Selection | 0=50, 1=100, 2=200, 3=300, 4=400, 5=500, 6=600, 7=700, 8=800, 9=900, 10=1000, 11=1100, 12=1200, 13=1300, 14=1400, 15=1500, 16=1600, 17=1700, 18=1800, 19=1900, 20=2000, 21=3000, 22=4000, 23=5000, 24=6000, 25=7000, 26=8000, 27=9000, 28=10000, 29=15000, 30=20000, 31=50000 |
| TUNE1 | Receiver Tune Center Frequency Wd 1 | Wd1 Receiver Center Frequency (MHz) Fc/256MHz |
| TUNE2 | Receiver Tune Center Frequency Wd 2 | Wd2 Receiver Center Frequency (MHz) (Fc mod 256MHz)/1MHz |
| TUNE3 | Receiver Tune Center Frequency Wd 3 | Wd3 Receiver Center Frequency (MHz) (Fc mod 1MHz)/10kHz |
| SNUM | Setup Number | Save the current setup to one of 16 possible storage locations. |

Figure 5-16 **Dual Receiver Protocol Command Bit Grouping Definitions**

| Mode | Definition | CMD1 | CMD2 | CMD3 |
|---|---|---|---|---|
| 0x02 | EEPROM Mode | EEPROM Sub Mode:<br>000ppppppb = PROM Page No.<br>01aaaaaab = RD Offset Pg Address<br>(LSB is returned on STAT2, MSB is returned on STAT3). | (Unused)<br>(Unused) | (Unused)<br>(Unused) |
| 0x03 | Tune Mode | Fc Mod 1MHz/10Khz | Fc MOD 256MHz/1MHz | Fc/256MHz |
| 0x04 | DAGC Control Mode | 0x00 = PROFILE A<br>0x01 = LIMITED<br>0x02 = COMBINER (Not implemented)<br>0x03 = RESERVED (Not implemented) | (Unused) | (Unused) |
| 0x06 | Read AM LPF Table | (Unused) | Table Index (0 to 31) | (Unused) |
| 0x07 | Read AM Freq Value | (Unused) | (Unused) | (Unused) |
| 0x08 | Program Ext Ref Freq | (Unused) | Allowable: 5, 10, 20, 25 MHz | (Unused) |
| 0x09 | Read SW1 Mode Cmd | (Unused) | (Unused) | (Unused) |
| 0x0A | Program Custom Time Constants | Custom Time Constant Number (Values between 1 and 3) | 8 LSBs of 100uSec TConstant Multiple | 8 MSBs of 100uSec TConstant Multiple |
| 0x0B | Select AGC Out Range | (Unused) | 0x00 = -4V to 0V, 0x08 = 0V to -4V,<br>0x01 = -2V to 0V, 0x09 = 0V to -2V,<br>0x02 = 0V to +2V, 0x0A = 2V to 0V,<br>0x03 = 0V to +4V, 0x0B = 4V to 0V,<br>0x04 = -2V to +2V, 0x0C = 2V to -2V,<br>0x05 = -4V to +4V, 0x0D = 4V to -4V,<br>All others undefined. | (Unused) |
| 0x0D | Program Digipot Mode | Digipot Instruction:<br>0x01 = Decrement Digipot<br>0x02 = Increment Digipot<br>0x03 = Set Digipot to Preset Value<br>0x04 = Query Digipot Setting | Digipot Preset Value:<br>0-99 Digipot Setting | Digipot Select:<br>0x00 = AM Gain<br>0x01 = TLM Gain |
| 0x1F | Serial Channel Control Mode | 0x00 = Serial Baudrate Select Submode. | 8 LSBits of (BAUD Rate/100). | 3 MSBits of (BAUD Rate/100). |

Figure 5-17 **Dual Receiver Protocol Secondary Command Mode Definitions**

| Mode | Functional Mode | STAT1 | STAT2 | STAT3 |
|---|---|---|---|---|
| 0x02 | EEPROM Mode: Read | Page Offset | 8 LSBs of EEPROM Read Value | 8 MSBs of EEPROM Read Value |
| 0x02 | EEPROM Mode: Pg Set | Page Number | (Unused = 0) | (Unused = 0) |
| 0x04 | DAGC Control Mode | DAGC Control Mode Commanded | (Unused = 0) | (Unused = 0) |
| 0x06 | Read AM LPF Table | Index Value | 8 LSBs of AM LPF Fc Frequency | 8 MSBs of AM LPF Fc Frequency |
| 0x07 | Read AM Freq Counter | 8 LSBs of AM Counter Frequency | 8 Mid-SBs of AM Counter Frequency | 1 MSB of AM Counter Frequency |
| 0x08 | Program Ext Ref Freq | (Unused = 0) | Ext Ref Frequency in MHz (5,10,20,25) | (Unused = 0) |
| 0x09 | Read SW1 | (Unused = 0) | SW1 Value (0x0 to 0xF) | (Unused = 0) |
| 0x0A | Program Custom Time Constants | Custom Time Constant Number (Values between 1 and 3) | 8 LSBs of 100uSec TConstant Multiple | 8 MSBs of 100uSec Tconstant Multiple |
| 0x0B | Select AGC Output Range | (Unused = 0) | 0x00 = -4V to 0V, 0x08 = 0V to -4V,<br>0x01 = -2V to 0V, 0x09 = 0V to -2V,<br>0x02 = 0V to +2V, 0x0A = 2V to 0V,<br>0x03 = 0V to +4V, 0x0B = 4V to 0V,<br>0x04 = -2V to +2V, 0x0C = 2V to -2V,<br>0x05 = -4V to +4V, 0x0D = 4V to -4V,<br>All others undefined. | (Unused = 0) |
| 0x0D | Program Digipot Mode | | Current Digipot Setting (0 – 99) | |
| 0x10 | DAC Adjust Mode | DAC Selection Value | 8 LSBs of the DAC Setting | 6 MSBs of the DAC Setting |
| 0x1F | Serial Channel Control Mode | (Unused = 0) | (Unused = 0) | (Unused = 0) |

Figure 5-18 Dual Receiver Protocol Secondary Command Mode Responses

### *5.2.1.3 Dual Receiver Protocol - Status Messaging*

There are two (2) status message types: primary status response, and the EEPROM Page read status response.

#### *5.2.1.3.1 Dual Receiver Protocol - Primary Status Response*

The primary status response provides the host with fundamental receiver status such as the received signal strength, FM deviation measurement, AM index value, and the detected AM frequency. Figure 5-19 depicts the primary status message content.

**Primary Status Response Content (Message ID = 0x2000)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | REF | PLL | - | - | - | - | - | - | |
| 2 | CH1RSSIL | | | | | | | | |
| 3 | CH1COMP | - | CH1LO2 | CH1LO1 | CH1RSSIH | | | | |
| 4 | - | CH1AMINDX | | | | | | | |
| 5 | - | CH1FMDEV | | | | | | | |
| 6 | CH2RSSIL | | | | | | | | |
| 7 | CH2COMP | - | CH2LO2 | CH2LO1 | CH2RSSIH | | | | |
| 8 | - | CH2AMINDX | | | | | | | |
| 9 | - | CH2FMDEV | | | | | | | |

Figure 5-19 **Dual Receiver Protocol Primary Status Message Structure**

#### *5.2.1.3.2 Dual Receiver Protocol - EEPROM Page Read Status Response*

The primary receiver configuration information, used to drive software controls, is found in the first page (indexed from 0) of the receivers primary internal EEPROM. Information contained in this EEPROM includes the bandwidths installed in the receiver, associated IF and video filter bandwidths, along with various other configuration information. This information can be accessed via an EEPROM read mode command. The EEPROM read status command structure is shown in Figure 5-20. The resulting status message contents are shown in the Figure 5-21. An example of the EEPROM contents is shown in Figure 5-22.

**EEPROM Page Read Command Content (Message ID = 0x2009)**

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | - | - | - | - | - | - | - | CHx | |
| 2 | - | - | - | PAGE | | | | | |

Figure 5-20 **Dual Receiver Protocol EEPROM Page Read Status Command Structure**

### EEPROM Page Read Response Content (Message ID = 0x2009)

| Content Byte | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Notes: |
|---|---|---|---|---|---|---|---|---|---|
| 1 | LOC0_LSB | | | | | | | | |
| 2 | LOC0_MSB | | | | | | | | |
| … | … | | | | | | | | More bytes |
| 127 | LOC63_LSB | | | | | | | | |
| 128 | LOC63_MSB | | | | | | | | |

Figure 5-21 **Dual Receiver Protocol EEPROM Page Read Status Message Structure**

| EEPROM Map | | | |
|---|---|---|---|
| **Offset** | **CH1** | **CH2** | **Description/ Information** |
| 0 | Signal Bandwidth Filter 0 (kHz) | Signal Bandwidth Filter 0 (kHz) | IF Filter Bandwidth (Hz) = Value x1000 Hz |
| 1 | Signal Bandwidth Filter 1 (kHz) | Signal Bandwidth Filter 1 (kHz) | |
| 2 | Signal Bandwidth Filter 2 (kHz) | Signal Bandwidth Filter 2 (kHz) | |
| 3 | Signal Bandwidth Filter 3 (kHz) | Signal Bandwidth Filter 3 (kHz) | |
| 4 | Signal Bandwidth Filter 4 (kHz) | Signal Bandwidth Filter 4 (kHz) | |
| 5 | Signal Bandwidth Filter 5 (kHz) | Signal Bandwidth Filter 5 (kHz) | |
| 6 | Signal Bandwidth Filter 6 (kHz) | Signal Bandwidth Filter 6 (kHz) | |
| 7 | Signal Bandwidth Filter 7 (kHz) | Signal Bandwidth Filter 7 (kHz) | |
| 8 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 9 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 10 | AGC Time Constant Count #0 | AGC Time Constant Count #0 | AGC Time Constant (msec) = Constant Count x 0.1msec |
| 11 | AGC Time Constant Count #1 | AGC Time Constant Count #1 | |
| 12 | AGC Time Constant Count #2 | AGC Time Constant Count #2 | |
| 13 | AGC Time Constant Count #3 | AGC Time Constant Count #3 | |
| 14 | AGC Time Constant Count #4 | AGC Time Constant Count #4 | |
| 15 | User AGC Time Constant Count #5 | User AGC Time Constant Count #5 | |
| 16 | User AGC Time Constant Count #6 | User AGC Time Constant Count #6 | |
| 17 | User AGC Time Constant Count #7 | User AGC Time Constant Count #7 | |
| 18 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 19 | RF Band 1 Start Frequency (MHz) | RF Band 1 Start Frequency (MHz) | RF Band Edge = Value x 1MHz |
| 20 | RF Band 1 Stop Frequency (MHz) | RF Band 1 Stop Frequency (MHz) | |
| 21 | RF Band 2 Start Frequency (MHz) | RF Band 2 Start Frequency (MHz) | |
| 22 | RF Band 2 Stop Frequency (MHz) | RF Band 2 Stop Frequency (MHz) | |
| 23 | RF Band 3 Start Frequency (MHz) | RF Band 3 Start Frequency (MHz) | |
| 24 | RF Band 3 Stop Frequency (MHz) | RF Band 3 Stop Frequency (MHz) | |
| 25 | RF Band 4 Start Frequency (MHz) | RF Band 4 Start Frequency (MHz) | |
| 26 | RF Band 4 Stop Frequency (MHz) | RF Band 4 Stop Frequency (MHz) | |
| 27 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 28 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 29 | RF Band 1 RSSI M Scale Factor | RF Band 1 RSSI M Scale Factor | RSSI (dBm) = ((RSSI Reg Value) x (M/10000)) + (B/10) |
| 30 | RF Band 1 RSSI B Scale Factor | RF Band 1 RSSI B Scale Factor | |
| 31 | RF Band 2 RSSI M Scale Factor | RF Band 2 RSSI M Scale Factor | |
| 32 | RF Band 2 RSSI B Scale Factor | RF Band 2 RSSI B Scale Factor | |
| 33 | RF Band 3 RSSI M Scale Factor | RF Band 3 RSSI M Scale Factor | |
| 34 | RF Band 3 RSSI B Scale Factor | RF Band 3 RSSI B Scale Factor | |
| 35 | RF Band 4 RSSI M Scale Factor | RF Band 4 RSSI M Scale Factor | |
| 36 | RF Band 4 RSSI B Scale Factor | RF Band 4 RSSI B Scale Factor | |
| 37 | Signal Bandwidth Video Filter 0 (kHz) | Signal Bandwidth Video Filter 0 (kHz) | Video Filter Bandwidth (Hz) = Value x1000 Hz |
| 38 | Signal Bandwidth Video Filter 1 (kHz) | Signal Bandwidth Video Filter 1 (kHz) | |
| 39 | Signal Bandwidth Video Filter 2 (kHz) | Signal Bandwidth Video Filter 2 (kHz) | |
| 40 | Signal Bandwidth Video Filter 3 (kHz) | Signal Bandwidth Video Filter 3 (kHz) | |
| 41 | Signal Bandwidth Video Filter 4 (kHz) | Signal Bandwidth Video Filter 4 (kHz) | |
| 42 | Signal Bandwidth Video Filter 5 (kHz) | Signal Bandwidth Video Filter 5 (kHz) | |
| 43 | Signal Bandwidth Video Filter 6 (kHz) | Signal Bandwidth Video Filter 6 (kHz) | |
| 44 | Signal Bandwidth Video Filter 7 (kHz) | Signal Bandwidth Video Filter 7 (kHz) | |
| 45 | Serial Channel Baud Rate | *(Future Use)* | Serial Channel BAUD/100 |
| 46 | Serial Channel Format | *(Future Use)* | No. Bits/PE/Parity/Stop Bits |
| 47 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 48 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 49 | DSP Firmware ID MSW | *(Unused / Spare)* | DSP Firmware Date: MSB = Month in Hex, LSB = Day in Hex |
| 50 | DSP Firmware ID LSW | *(Unused / Spare)* | DSP Firmware Date: Two Bytes = Year in Hex |
| 51 | RF/IF Hardware Port Configuration | RF/IF Hardware Port Configuration | (Future Use) |
| 52 | Board Serial Number MSW | *(Unused / Spare)* | Device Serial Number in Hex. |
| 53 | Board Serial Number LSW | *(Unused / Spare)* | |
| 54 | Ext. Ref. Input Freq. Multiplier (MHz) | *(Unused / Spare)* | External Reference Input Frequency = Multiplier x 1MHz |
| 55 | *(Unused / Spare)* | *(Unused / Spare)* | |
| 56 | Board ID ASCII Character 1 | *(Unused / Spare)* | ASCII Representation Of Device ID |
| 57 | Board ID ASCII Character 2 | *(Unused / Spare)* | |
| 58 | Board ID ASCII Character 3 | *(Unused / Spare)* | |
| 59 | Board ID ASCII Character 4 | *(Unused / Spare)* | |
| 60 | Board ID ASCII Character 5 | *(Unused / Spare)* | |
| 61 | Board ID ASCII Character 6 | *(Unused / Spare)* | |
| 62 | Board ID ASCII Character 7 | *(Unused / Spare)* | |
| 63 | Board ID ASCII Character 8 | *(Unused / Spare)* | |

Figure 5-22 **Dual Receiver Protocol EEPROM Contents**

### *5.2.1.4 Dual Receiver Protocol - Status Bit/Byte Definitions*

Figure 5-23 contains the bit and bit pairing definitions for the status messages.

| Response Mnemonic | Description/Definition | Logic State/Explanation |
|---|---|---|
| REF | Present state of the Internal/External Reference Select | 1 = Internal Reference Selected, 0 = External Reference Selected |
| PLL | Internal Synthesizer Reference Synchronization Status | 1 = PLL Synchronized, 0 = PLL Unsynchronized |
| CHxRSSIL | CHx Received Signal Strength (8 LSBs) | Lower 8 bits of RSSI level |
| CHxRSSIH | CHx Received Signal Strength (4 MSBs) | Upper 4 bits of RSSI level |
| CHxCOMP | CHx Compression Warning | 0 = Not in compression, 1 = May be in compression. |
| CHxAMINDX | CHx Measured AM Index | AM Index Measurement (Range 0-127) |
| CHxLO1STAT | CHx LO1 Status | 1 = Locked, 0 = Unlocked |
| CHxLO2STAT | CHx LO2 Status | 1 = Locked, 0 = Unlocked |
| CHxFMDEV | CHx FM Deviation in Percent | Valid range is from 0% – 127%. |

| Command Mnemonic | Description/Definition | Logic State/Explanation |
|---|---|---|
| DCX | Radio Selection Number | 0=Radio 1 or Down Converter 1, 1=Radio 2 or Down Converter 2 |
| PAGE | EEPROM Page Number Selection | 0 – 31 are valid page numbers. |

Figure 5-23 **Dual Receiver Protocol Status Cmd/Response Bit Grouping Definitions**