SEED International Ltd.

SEED-DEC138

Hardware User Manual

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Preface

Read This Frist

About This Manual

This document describes the board level operations of the OMAP-L138. The SEED-DEC138 is based on the Texas Instruments OMAP processor. The SEED-DEC138 allows engineers and software developers to evaluate certain characteristics of the OMAP processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Warranty

The warranty period for all hardware and software products manufactured by SEED Electronic Technology Ltd is one year after shipment. SEED Electronic Technology Ltd guarantees free of charge repair or replacement for the manufacturer caused damaged products during warranty period. Software updates will be sent free of charge to the customer during warranty period.

Information about Cautions

The Boards contains Electro-static Discharge (ESD) sensitive devices. Take proper precautions to ground yourself before handling the board.

This Document may contain cautions. A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

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Related Documents, Application Notes and User Guides

Information regarding the OMAP-L138 Processor can be found at the following Texas Instruments website: http://www.ti.com
Information about this production if you need assistance can be found at the following Seed International website: http://www.seeddap.com

Contents

Figure List

Table List

Chapter 1

Functional Overview

1. Functional Overview

Chapter 1 provides a description of the SEED-DEC138 along with the key features and a block diagram of the circuit board.

1.1 Key Features

The SEED-DEC138 uses OMAP-L138 high performance processor from Texas Instruments. The OMAP-L138 is a dual-core device: a 300-MHz ARM926EJ-S MPU core and a 300-MHz C6748 VLIW DSP core. The SEED-DEC138 board provides rich peripheral interfaces. The SEED-DEC138 adopts the SEED standard DEC serial board structure that suit a wide variety of application environments.

The SEED-DEC138 operates from +5V and +/-15V external power supply. The +5V input is converted into core voltage, +1.2V, +1.8V and +3.3V. The +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.2V is the DSP core voltage. The +1.8V voltage is used for the USB and DDR2. CPU power rails are sequenced on the module.

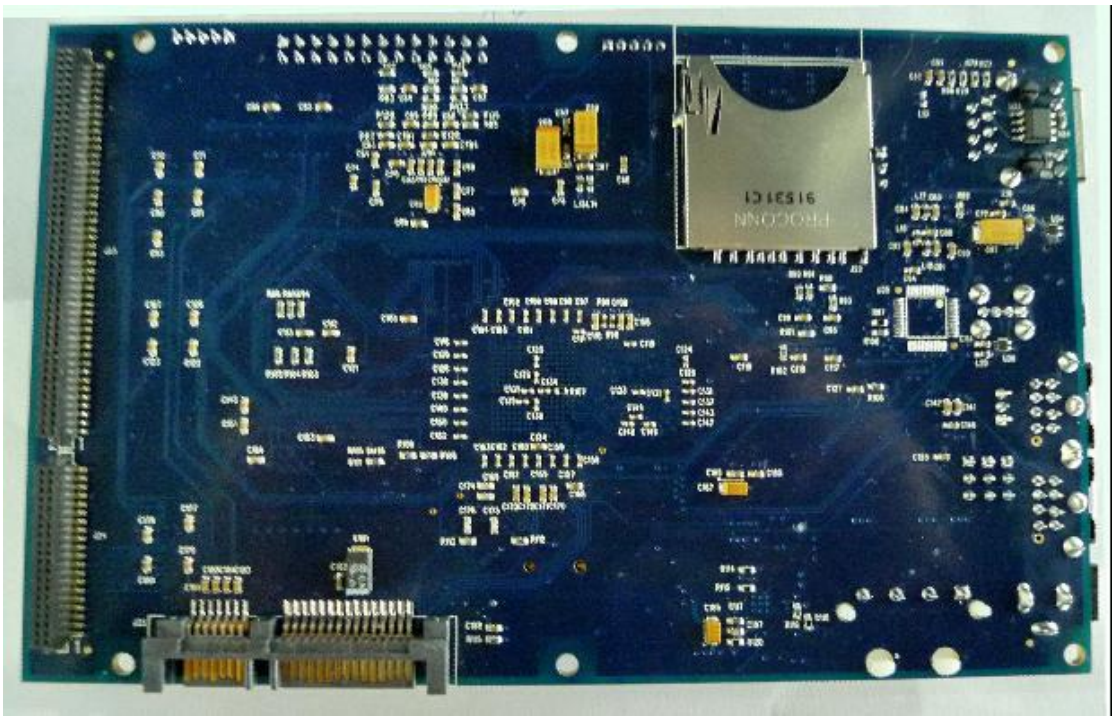

Figure 1. SEED-DEC138

The SEED-DEC138 hardware key features include:

- OMAP-L138 from Texas Instruments: a 300-MHz ARM926EJ-S MPU and a 300-MHz C6748 VLIW DSP.
- 512Mb DDR2: K4T51163QG-HCF7
- 4Gb NAND FLASH: K9F4G08U0A-PCB0
- 2 UART: RS232 and RS485/RS232 (jumper selection)
- 2 USB port: OTG2.0 and HOST
- MMC/SD
- SATA
- 10/100 Mbps Port Ethernet Phy
- Motor port: 2 group eHRPWM
- AD: 6 channel 16 bit AD converter, input voltage range: -12V~ +12V
- DA: 4 channel 12 bit DA converter, output voltage range: -10V~ +10V or 0V~ +10V
- EXT_BUS: data bus, address bus, control signals, status signals, chip select signal, McBSP0，McBSP1 and etc. Interface voltage level +3.3V/ +5V
- LCD: TFT565

1.2 Block Diagram:

The block diagram of the SEED-DEC138 is shown as below:

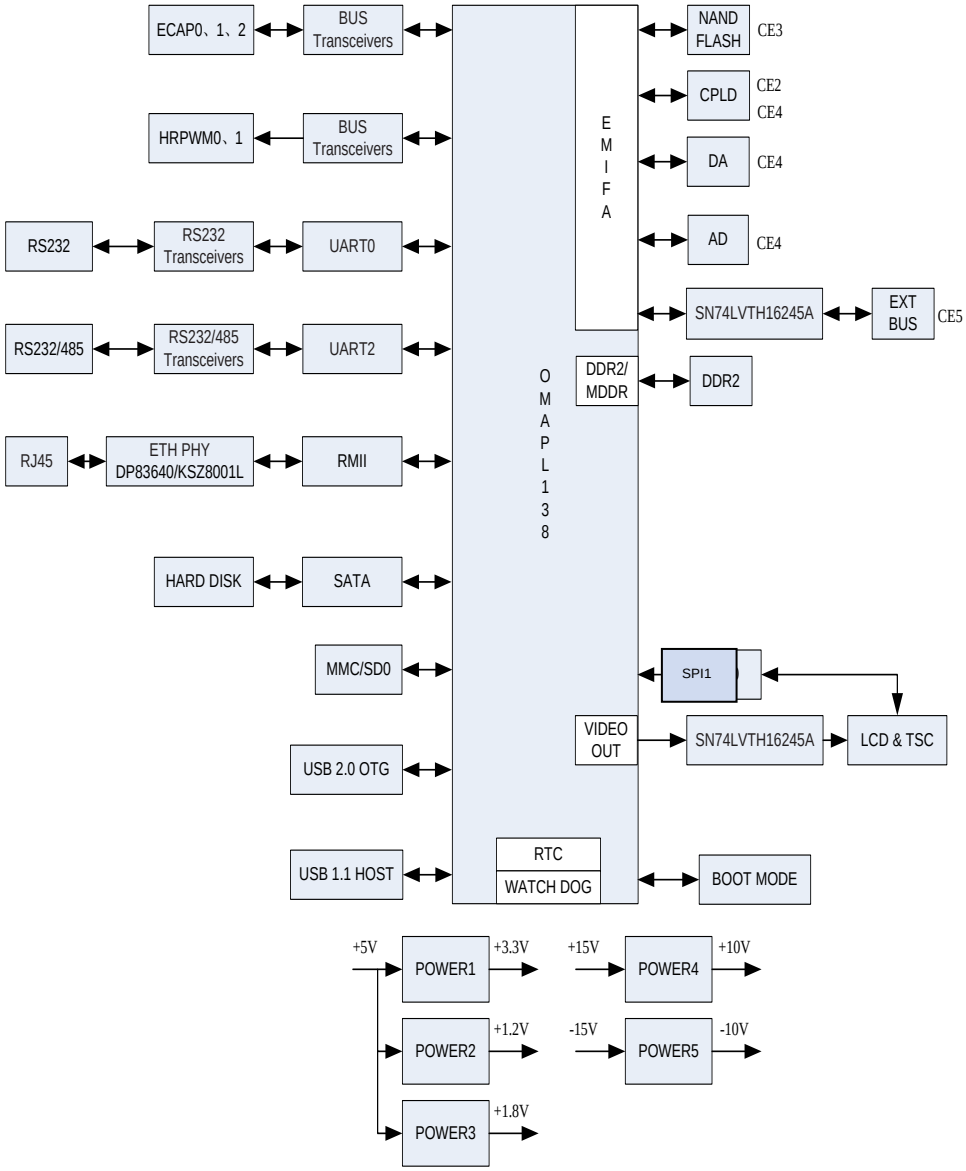

Figure 2: Block Diagram of the SEED-DEC138

Chapter 2

Board Components

2. Board Components

This chapter describes the operation of the major board components on the SEED-DEC138. It includes processors module, interfaces module and power management module.

2.1 OMAP-L138 Processors Module

2.1.1 OMAP-L138 Processor

The SEED-DEC138 uses OMAP-L138 high performance processor from Texas Instruments. The OMAP-L138 is a dual-core device: a 300-MHz ARM926EJ-S MPU core and a 300-MHz C6748 VLIW DSP core. The OMAP-L138 sits at the U25 on the board.

2.1.2 DDR2

The SEED-DEC138 provides 512M DDR2 (K4T51163QG-HCF7). It is connected to the on-chip DDR2 space and sits at the U21 on the board.

2.1.3 NAND FLASH

The SEED-DEC138 provides 512Mb x8 bit NAND FLASH (K9F4G08U0A-PCB0). It is connected to the on-chip EMIFA space and sits at the U22 on the board.

2.1.4 CPLD

The CPLD is connected to the EMIFA space. The CPLD is used to control peripherals, allocate interrupts sources and multiplex with logical controllers. The CS2, CS4, CS5, they are the chip select signals from the EMIFA. They are connected to the CPLD and control the external devices by selecting the address. The CPLD also controls the enable signal for some other devices. The CPLD also processes the interrupts between processor and peripherals.

The CPLD controls the peripheral logics of the SEED-DEC138.

The CPLD logics include:

- Interrupts, status and handshaking signals are via CPLD connected to the OMAP-L138.
- Address coding
- Enable or select some signals

2.2 SEED-DEC138 Peripherals and Interfaces

2.2.1 LCD

The SEED-DEC138 is equipped with one LCD. The signals from the OMAP-L138 LCD controller are interfaced through the expansion connectors. The SEED-DEC138 uses 16bit digital mode TFT565 to control LCD.

To improve the signals' driving power, the signals from the OMAP are connected to the LCD via SN74LVTH16245A first.

The touch screen controller (TSC) on the SEED-DEC138 is controlled by the TSC2046. This TSC2046 is used to support standard 4-wire resistive touch panels. The TSC2046 is connected to the OMAP-L138 by the SPI1 interface.

2.2.2 AD Data Acquisition

The SEED-DEC138 is integrated with one 3 channel AD data acquisition module (ADS8556). It sits at the U11 on the board.

2.2.3 DA Converter Module

The SEED-DEC138 is integrated with one 4 channel DA converter module (DAC7724). Its features include:

- 4 channel analogue output
- 12 bit resolution
- +/-15V power supply
- +/-10V signal range

The high reference voltage of the DA converter module is +10V. The low reference voltage can be selected at either 0V or -10V.

Note:

0V: L14 is connected, L15 is empty.

-10V: L14 is empty, L15 is connected.

The default voltage of the SEED-DEC138 board is -10V.

2.2.4 Ethernet Interface

The SEED-DEC138 incorporates an 10M/100M Ethernet interface, KSZ8001/DP83640 multiplex, RMII interface. The RJ-45 jacks have 2 LEDs integrated into their connector. The LEDs are green and yellow and provide link and transmit status from the ethernet controller.

2.2.5 MMC/SD Media Card Interfaces

The SEED-DEC138 supports a group of MMC/SD interface, four groups data line mode and +3.3V operating voltage.

2.2.6 USB Interface

The SEED-DEC138 incorporates two on chip USB controllers: USB0 OTG interface; USB1 HOST interface. OTG power mode is realized by TPS2065D. Each of the two USB interfaces are protected by the TPDE0001RSE_0.

2.2.7 UART

The OMAP-L138 supports 3 UARTs. Since the pins are multiplexed, the SEED-DEC138 supports 2 UARTs, UART0 and UART2.

The UART0 is driven to J9 to realize the RS232. The UART2 is driven to J14 to realize the RS232 or RS485. The selection is through the jumper J11-J13.

2.2.8 SATA

The OMAP-L138 supports 1 SATA interface, +5V power supply.

2.2.9 JTAG Debugger Interface

The SEED-DEC138 supports the JTAG debugger interface. The J17 is the JTAG debugger of the OMAP-L138, and the debugging environment is CCStudio from Texas Instruments. The SEED-XDS560PLUS is used for debugging.

The JTAG debugger interface can be used for test, debug, program run, trace and download.

2.2.10 Expansion Bus

Memory Bus

Memory bus includes:

- Memory interfaces (16-bit data bus, 19-bit address bus, 4 register space)
- System interface (1 reset output, 4 maskable interrupt input)
- Main power supply (+3.3V, +5V and GND)

The memory bus is realized through 90-pin 1.27mm x 1.27mm high density shield socket.

Peripheral Bus

The peripheral bus includes:

- On-chip peripheral interfaces (2 McBSP)
- Handshake interfaces (2 controller output, 2 status input)
- Supportive power supply (+3.3V, +5V and GND)

The peripheral bus is realized through 40-pin 1.27mm x 1.27mm high density shield socket.

2.2.11 Clock and LED

The clock of the SEED-DEC138 contains crystal and 1 clocking processor CY22831. The input of the CY22381 is 10M, outputs are 50M, 31.5M and 100M.

The SEED-DEC138 provides the following clocks:

- Y1:10M crystal uses as the clock signal source for clock processor
- Y2: 32.768K crystal uses as the clock signal for RTC
- Y3: 24M crystal uses as the clock signal for CPU
- 31.5M clock for CPLD, frequency division for AD
- 50M clock for the Ethernet interface
- 100M for the SATA

The SEED-DEC138 provides 3 LED:

- D3 is the indicator for the +3.3V power supply
- D1 and D2 are the indicator for the program debugging

2.3 Power Management Module

2.3.1 Power Management Layout and Application

The SEED-DEC138 provides two sources of power supply: external power supply, the electrical power being supplied from the external; and the internal power supply, it is generated from the on-board power processor.

- External power input: +15V，-15V，+5V
- On board power supply: +1.2V， +1.2V_RTC,+1.8V， +3.3V,+3.3VA， +3.3V_RTC,+5VA， +5V_LCD,+5V_USB， +10VA， -10VA， +15VA， -15VA，+EMAC_1.8V，+EMAC_1.8VA，+EMAC_1.8VALL

The applications of these power supply include:

- +3.3V: DSP and external devices
- +5V: SATA,LCD,USB and interfaces
- +1.2V: DSP core
- +1.8V: USB and DDR2
- +1.2V_RTC, +3.3V_RTC: RTC
- +10V, -10V, +15VA, -15VA: DA
- +EMAC_1.8V,+3.3VA,+EMAC_1.8VA,+EMAC_1.8VALL:
- Ethernet interface

2.3.2 Power Supply

The SEED-DEC138 incorporates three power processors: TPS65053, TPS77001 and LM4040A10. The TPS65053 is powered by +5V input, it converts to +1.8V, +1.2V, +3.3V and the +3.3V_RTC. The TPS77001 coverts the +3.3V_RTC to +1.2V_RTC. The LM4040A10 generates the +/-10VA for the analogue module.

Chapter 3

Physical Description

3. Physical Description

3.1 PCB Layout

The top side of the SEED-DEC138 is shown as below:

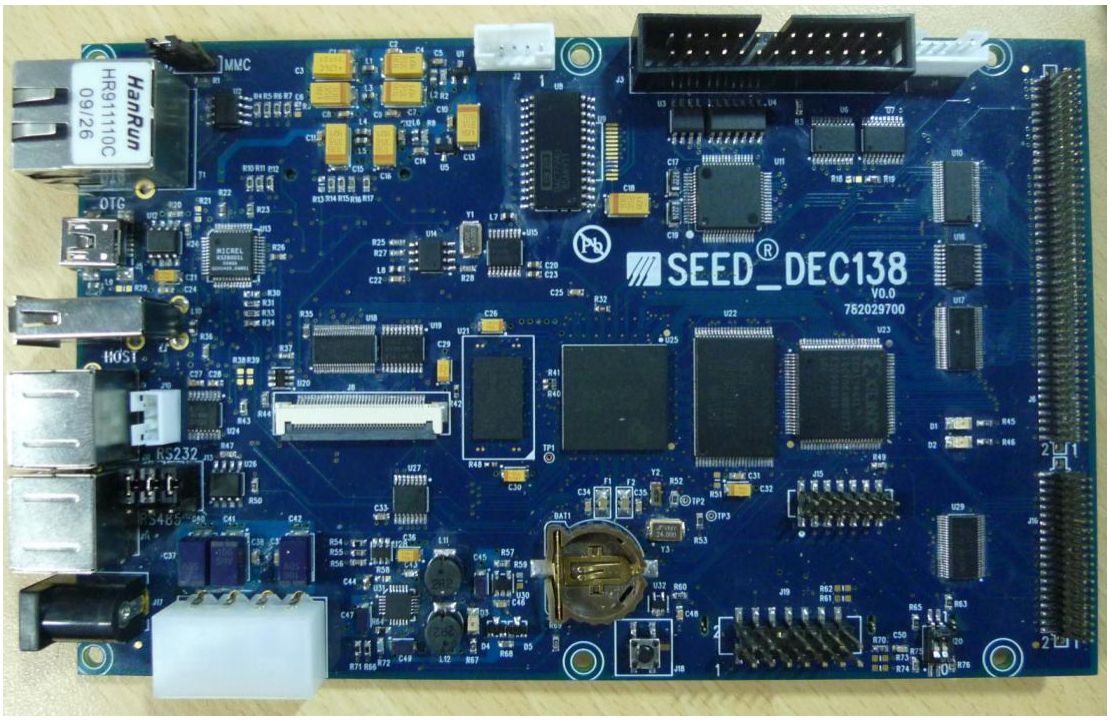

Figure 3: SEED-DEC138 Top Side

The bottom side of the SEED-DEC138 is shown as below:

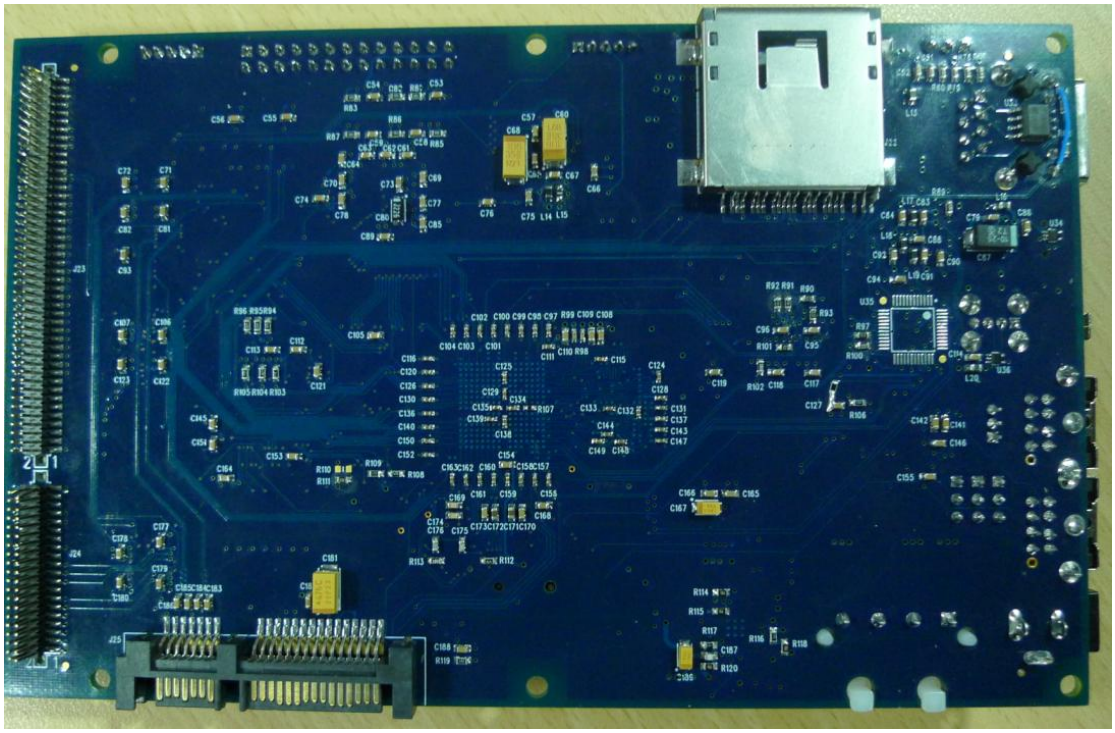

Figure 4: SEED-DEC138 Bottom Side

3.2 Connector

Pin	Type	Size	Location	Function
J1	Jumper	3	Top	MMC/SD Select
J2	Connector	5	Top	DA Output
J3	Connector	26	Top	Electrical Motor Interface and AD Input
J4	Connector	5	Top	Capture Interface
J5	Connector	9	Top	USB Interface (OTG)
J6	Connector	90	Top	Expansion Bus
J7	Connector	8	Top	USB Interface (HOST)

J8	Connector	42	Top	LCD Interface
J9	Connector	9	Top	RS232
J10	Jumper	3	Top	Testing
J11	Jumper	3	Top	RS232/RS485 Select
J12	Jumper	3	Top	RS232/RS485 Select
J13	Jumper	3	Top	RS232/RS485 Select
J14	Connector	9	Top	RS232/RS485
J15	Connector	14	Top	CPLD-JTAG
J16	Connector	40	Top	Expansion Bus
J17	Connector	3	Top	|+5V Power Cord
J18	Button	5	Top	Reset
J19	Connector	14	Top	JTAG
J20	DIP Switch	4	Top	BOOT
J21	Connector	4	Top	+/- 15V,+5VPo wer Cord
J22	SD Connector	28	Bottom	SD Connector
J23	Connector	90	Bottom	Expansion Bus
J24	Connector	40	Bottom	Expansion Bus
J25	Connector	22	Bottom	SATA Interface

Table 1: Connector

3.2.1 J2 DA Output

Signal	Pin
VOUTA	1
VOUTB	2
VOUTC	3
VOUTD	4
AGND	5

Table 2: J2 Definition

3.2.2 J3 Electrical Motor Interface and AD Input Interface

Pin	Signal
1	PWM0A
2	PWM0B
3	PWM1A
4	PWM1B
5	PWM1TZ
6	PWM0TZ
7	CPLD0
8	CPLD1
9	CPLD2
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	AGND
17	AGND
18	AGND
19	AGND
20	AGND
21	C0
22	C1
23	B0
24	B1
25	A0
26	A1

Table 3: J3 Definition

3.2.3 J4 Capture Interface

Signal	Pin
+5V	1
CAP0	2
CAP1	3
CAP2	4
GND	5

Table 4: J4 Definition

3.2.4 Expansion Bus

Signal	Pin	Pin	Signal
+5V	1	2	+5V
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
GND	19	20	GND
E_D15	21	22	E_D14
E_D13	23	24	E_D12
E_D11	25	26	E_D10
E_D9	27	28	E_D8
E_D7	29	30	E_D6
E_D5	31	32	E_D4
E_D3	33	34	E_D2
E_D1	35	36	E_D0
+3.3V	37	38	+3.3V
NC	39	40	E_A18
E_A17	41	42	E_A16
E_A15	43	44	E_A14
E_A13	45	46	E_A12
E_A11	47	48	E_A10
E_A9	49	50	E_A8
E_A7	51	52	E_A6
E_A5	53	54	E_A4
GND	55	56	GND
E_A3	57	58	E_A2
E_A1	59	60	E_A0
+3.3V	61	62	+3.3V
GND	63	64	GND
\RD	65	66	\OE
\WE	67	68	NC
NC	69	70	NC
NC	71	72	NC

GND	73	74	GND
\CE3	75	76	\CE2
\CE1	77	78	\CE0
NC	79	80	NC
NC	81	82	NC
\RESET	83	84	NC
INT3	85	86	INT2
INT1	87	88	INT0
GND	89	90	GND

Table 5: J6 Definition

Expansion bus J23 definition:

Signal	Pin	Signal	Pin
+5V	1	2	+5V
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
GND	19	20	GND
E_D14	21	22	E_D15
E_D12	23	24	E_D13
E_D10	25	26	E_D11
E_D8	27	28	E_D9
E_D6	29	30	E_D7
E_D4	31	32	E_D5
E_D2	33	34	E_D3
E_D0	35	36	E_D1
+3.3V	37	38	+3.3V
E_A18	39	40	NC
E_A16	41	42	E_A17
E_A14	43	44	E_A15
E_A12	45	46	E_A13
E_A10	47	48	E_A11
E_A8	49	50	E_A9
E_A6	51	52	E_A7
E_A4	53	54	E_A5
GND	55	56	GND
E_A2	57	58	E_A3
E_A0	59	60	E_A1
+3.3V	61	62	+3.3V
GND	63	64	GND
\OE	65	66	\RD
NC	67	68	\WE
NC	69	70	NC
NC	71	72	NC

GND	73	74	GND
\CE2	75	76	\CE3
\CE0	77	78	\CE1
NC	79	80	NC
NC	81	82	NC
NC	83	84	\RESET
INT2	85	86	INT3
INT0	87	88	INT1
GND	89	90	GND

Table 6: J23 Definition

Expansion J16 definition:

Signal	Pin	Pin	Signal
-15V	1	2	-15V
GND	3	4	GND
+15V	5	6	+15V
+5V	7	8	+5V
E_CLKX0	9	10	E_CLKR0
E_FSX0	11	12	E_FSR0
E_DX0	13	14	E_DR0
NC	15	16	NC
E_CLKX1	17	18	E_CLKR1
E_FSX1	19	20	E_FSR1
E_DX1	21	22	E_DR1
NC	23	24	NC
GND	25	26	GND
NC	27	28	NC
NC	29	30	NC
CNTL1	31	32	CNTL0
STAT1	33	34	STAT0
NC	35	36	NC
NC	37	38	NC
+3.3V	39	40	+3.3V

Table 7: J16 Definition

Expansion bus J24 definition:

Signal	Pin	Signal	Pin
-15V	1	2	-15V
GND	3	4	GND
+15V	5	6	+15V
+5V	7	8	+5V
E_CLKR0	9	10	E_CLKX0
E_FSR0	11	12	E_FSX0
E_DR0	13	14	E_DX0
NC	15	16	NC
E_CLKR1	17	18	E_CLKX1
E_FSR1	19	20	E_FSX1
E_DR1	21	22	E_DX1
NC	23	24	NC

GND	25	26	GND
NC	27	28	NC
NC	29	30	NC
CNTL0	31	32	CNTL1
STAT0	33	34	STAT1
NC	35	36	NC
NC	37	38	NC
+3.3V	39	40	+3.3V

Table 8: J24 Definition

3.2.5 J8 LCD Interface

J8 Definition:

Signal	Pin	Pin	Signal
GND	1	2	+5V_LCD
GND	3	4	+3.3V
I_LCD_D11	5	6	I_LCD_D11
I_LCD_D11	7	8	I_LCD_D11
I_LCD_D12	9	10	I_LCD_D13
I_LCD_D14	11	12	I_LCD_D15
I_LCD_D5	13	14	I_LCD_D5
I_LCD_D5	15	16	I_LCD_D6
I_LCD_D7	17	18	I_LCD_D8
I_LCD_D9	19	20	I_LCD_D10
I_LCD_D0	21	22	I_LCD_D0
I_LCD_D0	23	24	I_LCD_D0
I_LCD_D1	25	26	I_LCD_D2
I_LCD_D3	27	28	I_LCD_D4
GND	29	30	I_LCD_DCLK
NC	31	32	I_LCD_HSYNC
I_LCD_VSYNC	33	34	I_\LCD_ENB
NC	35	36	GND
X1	37	38	Y1
X2	39	40	Y2
NC	41	42	NC

Table 9: LCD Definition

3.2.6 Power Cord

Power cord J17 definition:

Signal	Pin
+5V	1
GND	2
NC	3

Table 10: J17 Definition

Power cord J21 definition:

Signal	Pin
+15V	1
-15V	2
GND	3
+5V	4

Table 11: J21 Definition

3.2.7 JTAG Pin Definition and DIP Switch

JTAG J19 pin definition:

Signal	Pin
TMS	1
\TRST	2
TDI	3
GND	4
+3.3V	5
NC	6
TDO	7
GND	8
RTCK	9
GND	10
TCK	11
GND	12
EMU0	13
EMU1	14

Table 12: DA Output Definition

J20 BOOT mode selection:

Mode	Switch 1	Switch 2
Emulation Debug	ON(1)	ON(1)
NAND8	ON(0)	OFF(1)(Default)
UART0	OFF(0)	ON(1)

Table 13: J20 Definition

3.2.8 J25 SATA Interface

SATA J25 pin definition:

Signal	Pin
GND	1
SATA_TX	2
\SATA_TX	3
GND	4
\SATA_RX	5
SATA_RX	6
GND	7
NC	8
NC	9
NC	10
GND	11
GND	12
GND	13
+5V	14
+5V	15
+5V	16
GND	17
NC	18
GND	19
NC	20
NC	21
NC	22

Table 14: J25 Definition