



D. Reference Manual (Electrical)

The SNAPS Reference Manual is a “what is” guide enumerating the specifications of SNAPS PCBs. For each revision of each item, related files are listed. **Please ensure that you are viewing files for the correct version!** Oldest revisions come first so readers can easily follow the design decisions and changes made to each revision of an item.

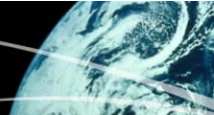
For convenience, here is a [link to the root of the SNAPS Files Distribution](#).

D1 C&DH PCB Evolution	3
D1.1 C&DH v0.1	3
D1.1.1 v0.1: About.....	3
D1.1.2 v0.1: Specifications	4
D1.1.3 v0.1: Files.....	4
D1.2 C&DH v1.1	4
D1.2.1 v1.1: About.....	4
D1.2.2 v1.1: Specifications	5
D1.1.3 v1.1: Files.....	5
D2 Switch PCB Evolution	6
D2.1 Switch v0.1	6
D2.1.1 v0.1: About.....	6
D2.1.2 v0.1: Specifications	6
D2.1.3 v0.1: Bill of Materials.....	6
D3 Solar PCB Evolution.....	6
D3.1 Solar v0.1	6
D3.1.1 v0.1: About.....	6
D3.1.2 v0.1: Specifications	7
D3.1.3 v0.1: Bill of Materials.....	7
D4 Other Items	7



Changelog

Rev.	Date	Author	Comments
A	20130517	MCP	Initial Revision
B	20130520	MCP	Updated style of project links
C	20130607	MCP	Project files link updates and TOC

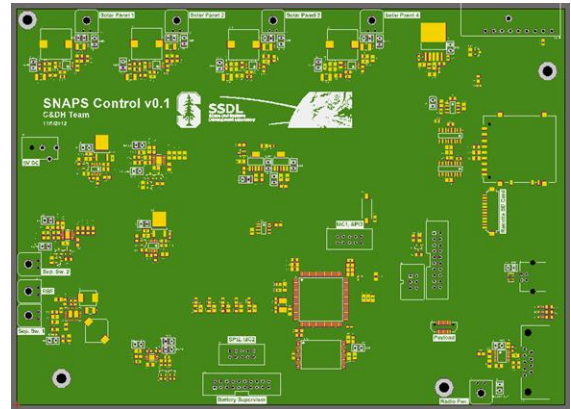


D1 C&DH PCB Evolution

D1.1 C&DH v0.1

D1.1.1 v0.1: About

The C&DH v0.1 “Flat-Sat” PCB is the first implementation of the initial SNAPS architecture. The board was designed with the following in mind: no space constraints, ease of debugging, and fast bring-up. (System design, schematic capture, layout, fabrication, assembly and some debugging were accomplished over the course of a 10 week quarter). MPPT circuitry is included on this PCB – however, multiple footprint and schematic errors are present. While the majority of the functionality (most useful is the SD card dual-port interface), it is not recommended that this PCB be used as an analog for a flight-ready SNAPS implementation.



Below follows a discussion of the design decisions made in each sub-circuit of v0.1:

- **Processor** – the STM32F40x processor was chosen because of the familiarity of the board designers with this processor, the attractive performance and peripheral specifications, and the built-in parallel memory interface that would enable large image processing programs to run.
- **Overall Power Topology** – we chose to use two 18650 cells (that have space heritage) in parallel to avoid the need to balance batteries. Some circuitry requires less than battery voltage (i.e. 3.3V for the microcontroller) and some requires more than battery voltage (i.e. 5-9V for the Lithium Radio and 5V for the HackHD). Also, the system must run off of a 5V input from an external power source. This external power source is ORed with the battery to provide a local power bus. The LTC4415 was chosen for its efficiency in ORing power supplies and its current limit abilities.

To accommodate the range of devices, the digital logic is powered by linear regulator from the ORed bus. The LDO that we chose lowered the output voltage if the input fell too low due to the battery’s falling state-of-charge. To provide power to the radio and camera, we implemented a high-efficiency boost converter to 8.5V (using the LT3959). Because the camera is not expected to run for a significant amount of time, we chose to use a linear regulator from 8.5V to 5V to provide camera power.

- **Radio Protection** –extra precautions were taken to protect it against a malfunction of the LT3959 boost converter. While a Zener diode and fuse were considered, the LTC4363 was used to provide OV/UV/OC protection for the radio. The IC will retry powering the device after a fault has occurred. The extra complexity of this circuit was deemed necessary for protecting the most expensive component of the satellite.
- **Solar MPPT** – the SPV1040 maximum power point tracking battery charger was chosen as the interface between the solar array and the battery bus in order to collect the most energy possible from SNAPS’ relatively small solar array. Concerns about the SPV1040’s ability to track the MPP of a triple-junction solar cell (due to a



perturb and observe strategy) arose. More testing is required to determine the interaction of triple-junction cells with terrestrial sunlight and the SPV1040.

- **Memory Architecture** – in addition to the memory space natively available to the STM32F40x processors, the MCU may access the SD card using a SPI interface. The MCU may also access a 2Mb FRAM storage IC (over SPI) to store non-volatile memory. The MCU also may use its built-in FSMC interface to communicate with the 4MB onboard SRAM. Using macros explained in the source code, a variable may be placed in the memory space residing externally when it is declared.
- **Dual-Port SD Interface** – because the HackHD only exposes control signals via a 9-pin header, we chose to host its SD storage on the C&DH board, using an interface board and wiring harness to simulate the microSD card of the HackHD. In order to take files off of the SD card, the MCU must be able to ensure that the HackHD is not in possession of the SD card.

The ADG711BRZ switch was selected for switching the HackHD’s access to the onboard SD card. By enabling the switch, signals from the HackHD’s microSD adapter board may pass through to the card. In order to prevent the HackHD from driving against the MCU’s pins during communication, care must be taken to place the MCU SPI pins in a high-impedance mode.

- **RS-232 Interface** – in order to test with a less expensive radio module, hardware was included for communicating over RS-232 with an AstroDev Helium radio that SSDL already owned.
- **Safety Interlocks** – the safety switches on v0.1 of the SNAPS C&DH board are explicit switches, requiring current to flow through the switch to activate a function.

D1.1.2 v0.1: Specifications

Dimensions	__x__x__
Weight	___ g
Processing Capabilities (STM32F405ZGT6)	See STM32F405xx/STM32F407xx full datasheet for specifications
Power Consumption (idle)	___ W
Power Consumption (processing video)	___ W
Video Processing Speed	___ seconds (video) / second (execution time)

D1.1.3 v0.1: Files

- [C&DH v0.1 Bill of Materials](#)
- [C&DH v0.1 CAD \(Altium\)](#)
- [C&DH v0.1 Gerber Files](#) (Advanced Circuits \$33/ea is recommended)
- SD card correction PCB

D1.2 C&DH v1.1

D1.2.1 v1.1: About

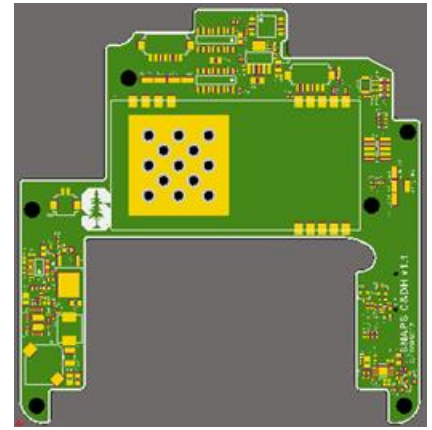
SNAPS C&DH v1.1 fixes the schematic and footprint layers present in v0.1, while also designing within the constraints of the mechanical structure. C&DH v1.1 not only is compatible with STRUCT v[#], but addresses the interconnectivity of PCB’s through



wiring harnesses and a Samtec FSI-110-03-G-D-AD connector to interface with the Battery Supervisor PCB.

Below follows a discussion of the upgrades from v0.1 to v1.1 and new features in each sub-circuit:

- **Overall Power Topology** – The overall power architecture becomes more streamlined between v0.1 and v1.1: USB power and external DC power are combined into a USB 3.0 connector sitting on the battery supervisor (that can provide 900 mA nominally, or 1500 mA while charging a battery. Through the board-to-board connector, only two power nets are received: VBATT (2.7-4.2V nominal) and VBUS (5.0V nominal). VBATT and VBUS are combined with an ideal diode controller in order to provide power to the radio, camera, 3.3V logic, etc.
- **Radio Protection** – the radio is prevented from receiving power until SNAPS has exited the CSD by manipulating the \SHDN pin of the protection IC.
- **Solar MPPT** –the solar PCB does not provide power directly to the C&DH board; rather, the battery supervisor lets the MPPT “see” a battery and subsequently distributes the battery voltage to the C&DH PCB through a Samtec TMM-102-06-S-D-SM connector
- **Safety Interlocks** – we chose DF13 connectors to interface with a switch PCB, controlling on-board P-FETs in the power path because finding connectors that were small and could handle the required current became difficult
- **Inter-PCB Connector** – the Samtec FSI series board-to-board connector was chosen because of the desired spacing between boards (3mm). The connector is soldered to one board, and the other has pads to receive spring pins.
- **Wiring Harness Connectors** – the Hirose DF13 series of connectors is used because of its low profile and acceptance as a space-worthy connector. As of v1.1, separation switches control gates of MOSFETs, so negligible current is required to operate the interlocks.



D1.2.2 v1.1: Specifications

Dimensions ___x___x___
Weight ___ g

Processing Capabilities (STM32F405ZGT6) See [STM32F405xx/STM32F407xx full datasheet](#) for specifications

Power Consumption (idle) ___ W
Power Consumption (processing video) ___ W

Video Processing Speed ___ seconds (video) / second (execution time)

D1.1.3 v1.1: Files



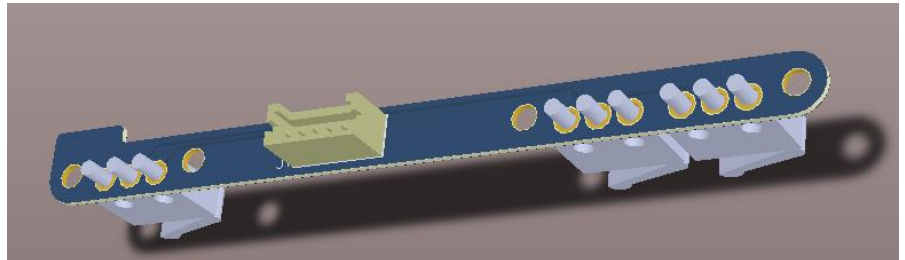
- [C&DH v1.1 Bill of Materials](#)
- [C&DH v1.1 CAD \(Altium\)](#)
- [C&DH v1.1 Gerber Files](#) (Sierra Proto Express No-Touch is recommended)
- [AstroDev Lithium Radio](#)

D2 Switch PCB Evolution

D2.1 Switch v0.1

D2.1.1 v0.1: About

The SNAPS Switch PCB is a board designed for attaching flight control switches to the body of the spacecraft. It breaks



out three MDS6500AL02PS switches to a Hirose DF13-5 connector. A wiring harness splits the connections between the Battery Supervisor PCB (3 wires) and the C&DH board (2 wires).

Two switches are used to detect SNAPS' exit from the CSD, while the other is used to prevent the Lithium Radio from turning on before exiting the parent spacecraft. These switches do not need to handle significant amounts of current, as they are used to control the gates of MOSFETs on the C&DH and Battery Supervisor PCB.

v0.1 of the Switch PCB was designed in conjunction with and is compatible with the C&DH v1.1 and the Battery Supervisor v0.2 PCB's. The PCB design rules are set for low cost manufacturing.

D2.1.2 v0.1: Specifications

Dimensions __x__x__
Weight __ g

D2.1.3 v0.1: Bill of Materials

- [Switch v0.1 Bill of Materials](#)
- [Switch v0.1 CAD \(Altium\)](#)
- [Switch v0.1 Gerber Files](#) (\$2.50/ea at BatchPCB)

D3 Solar PCB Evolution

D3.1 Solar v0.1

D3.1.1 v0.1: About

The SNAPS Solar PCB performs multiple functions:

- Fastening two Spectrolab UTJ solar cells onto the structure
- Boosting solar cell voltage to battery voltage with the SPV1040 MPPT IC
- Attachment of the Bodipole antenna, along with tuning circuit

Two Solar PCBs cover the large faces of either side of SNAPS in order to both maximize solar array space and cover SNAPS internal elements. Power is transferred from the MPPT circuit to the Battery Supervisor PCB using Samtec TMM-102-06-S-D-SM connectors (which tolerate large amounts of vertical misalignment). The Solar PCB is designed to be



symmetrical, allowing for one design to cover both sides of the spacecraft.

The onboard SPV1040 maximum power point tracking (MPPT) IC uses a boost topology to convert the lower solar cell input voltage to the higher Li-Ion battery voltage. Significantly higher solar array efficiency may be achieved using an MPPT.

D3.1.2 v0.1: Specifications

Dimensions	__x__x__
Weight	__ g
Input Voltage Range	__ V
Input Current (Max)	__ A
Maximum Power	__ W
Maximum Output Voltage	__ V

D3.1.3 v0.1: Bill of Materials

- [Solar v0.1 Bill of Materials](#)
- [Solar v0.1 CAD \(Altium\)](#)
- [Solar v0.1 Gerber Files](#) (Sierra Proto Express No-Touch is recommended)
- Spectrolab UTJ Cells

D4 Other Items

- SNAPS Battery Supervisor PCB (Pumpkin)
 - Full documentation on the Pumpkin-built SNAPS Battery Supervisor PCB can be found [[link](#)]
- HackHD
 - The HackHD can be purchased from Sparkfun Electronics. The user manual is available on [this](#) page.
- AstroDev Lithium Radio
 - AstroDev provides documentation on its Lithium Radio [here](#).