DIGITAL PULSE WIDTH MODULATION TECHNIQUES FOR POWER CONVERTERS

by

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A THESIS

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ABSTRACT

Recently, digital controls are becoming dominant in almost every power electronic application because of the advantage when compared to analog control. This includes the ability of digital controllers to perform more advanced and sophisticated functions that potentially result in improving power conversion efficiency and/or the dynamic performance of the power converter, the ease of digital control function and loop upgradeability (or revision), and reduced sensitivity to component variations. However, there are also some challenges in digital control such as control loop delays that impact the dynamic performance of the power converters and the additional controller power consumption in some digital control implementations.

Digital Pulse Width Modulation (DPWM) is one of the most important parts in digital control systems which control the power switch of the power converters. Modulation technique plays a vital role in causing control delays. There are several implementation schemes of digital pulse width modulation such as counter based DPWM, delay line based DPWM, and hybrid based DPWM. The output voltage is required to have little deviation from the reference voltage and fast settling times under transient events. Therefore, in order to maintain a well regulated output voltage, the control signal must instruct the power converter to either turn on (when there is undershoot in output voltage) or turn off (when there is overshoot in output voltage), as fast as possible.

The work presented in this thesis suggests a modulation technique that reduces the turn on delay caused by trailing-edge digital modulation and turn off delay caused by leading-edge digital modulation. Reducing the digital pulse width modulation delay reduces the overshoot and undershoot in the output voltage in power converters with digital closed loop control. The proposed modified digital pulse width modulation scheme is verified using computer simulations and experimental results.

LIST OF ABBREVIATIONS AND SYMBOLS

PWM	Pulse Width Modulation
APWM	Analog Pulse Width Modulation
DPWM	Digital Pulse Width Modulation
FPGA	Field-Programmable Gate Array
MSB	Most significant bit
LSB	Least significant bit
V	volts: Unit of voltage.
A	amperes: Unit of Current.
µF	micro Farad: Unit of capacitance.
nH	nano Henry: Unit of inductance.
KHz	kilo (10^3) Hertz. Unit of frequency.
MHz	mega (10^6) Hertz. Unit of frequency.
<	Less than
>	Greater than
=	Equal to

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CHAPTER 1

INTRODUCTION

1.1 Overview

Years ago, the linear regulator was used in supplying partial power to devices such as electric stoves, lamp dimmers, and audio amplifiers, by controlling the amount of current flowing to a motor. The linear regulator is an electrical component that acts like a variable resistor. By using a linear regulator much power is wasted in the resistor element, and therefore this method is inefficient. There are other methods, such as variable auto transformers and Variac for AC power adjustment. These methods are relatively efficient but have high cost. There was a need for a scheme that efficiently delivers partial power to devices [1-15, 31,40].

Pulse Width Modulation (PWM) is a scheme that provides an intermediate amount of electric power between fully on and fully off. PWM circuits output a square waveform with a varying on to off ratio. The average ratio can vary from 0 to 100 percent. This on time (T_{ON}) to off time period (T) ratio is called as duty cycle, which is expressed in percentage. Therefore, by this scheme, a variable amount of power is transferred to the load. The main advantage of PWM over the linear regulator is its efficiency. For example, at 50% level PWM will use 50% of power, that is almost transferred to load but on the other hand in linear regulator control scheme 50% of load power consumes 71% of full power where 50% of power goes to the load and the remaining 21% is dissipated as heat[1-15, 31,40].

The main applications of PWM are in power converters, audio amplifiers, and controlling the speed of motors. The output of the PWM is generally a fixed pulse frequency that is on and off for fixed period of time. PWM works well with digital control because of the on and off nature.

Digital controls are increasingly used in power converters because of their advantage when compared to analog controls. The main advantages of using digital controls over analog are the ability to perform more advanced and sophisticated functions that potentially result in improving power conversion efficiency and/or dynamic performance of the power converter, the ease of digital control function and loop upgradeability, and reduced sensitivity to component variations compared to analog controllers [1-12, 23-26, 30, 31, 33].

Digital controllers are discussed more in a later section. The next section discusses the operation of DC-DC buck converters and the associated control techniques.

1.2 Buck Converters

The DC-DC buck converter, or step down DC-DC converter, is used to step down the DC input voltage. They are used in applications such as powering small devices like cell phones to bigger and more power consuming servers.

The DC-DC buck converter circuit basically consists of two switches, an inductor, and capacitors. The operation of DC-DC buck converter is simple. The two switches control the inductor. When the switch is on, it connects the inductor to the source voltage, to store energy. When the switch is off it discharges energy to the load. The timing of the switch operations are determined by the PWM control signal. The controller can be either an analog controller or digital controller. The analog controllers are simple, low cost, and well established designs, but digital controllers are widely used.

The advantages of digital controllers are mentioned in section 1.1[1-12, 23-26, 30, 31, 33]. A simple schematic circuit of a buck converter controlled by an analog PWM is shown in Figure 1.1.

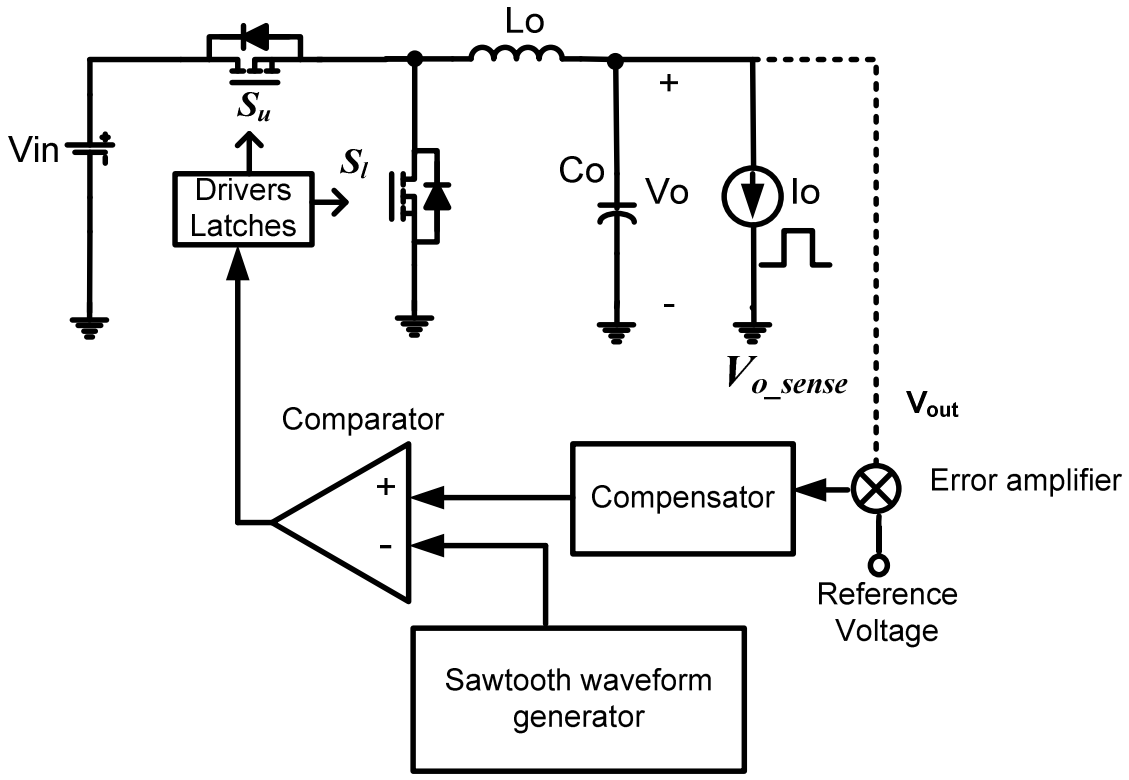


Figure 1.1: Schematic of a DC-DC Buck converter controlled by Analog PWM

Buck converters controlled by analog pulse width modulation (APWM) operate as follows. The compensator outputs an analog signal called the error signal. The carrier signal is a ramp (saw-tooth) that has a linear relationship between input signal and output pulse width signal. The error signal is compared with the carrier signal to provide amplitude to time domain conversion [1,2]. A block diagram of analog PWM is shown in Figure 1.2. The PWM is set high at the starting of switching frequency (F_{sw}) and resets when there is any difference between carrier waveform generator and control voltage [2].

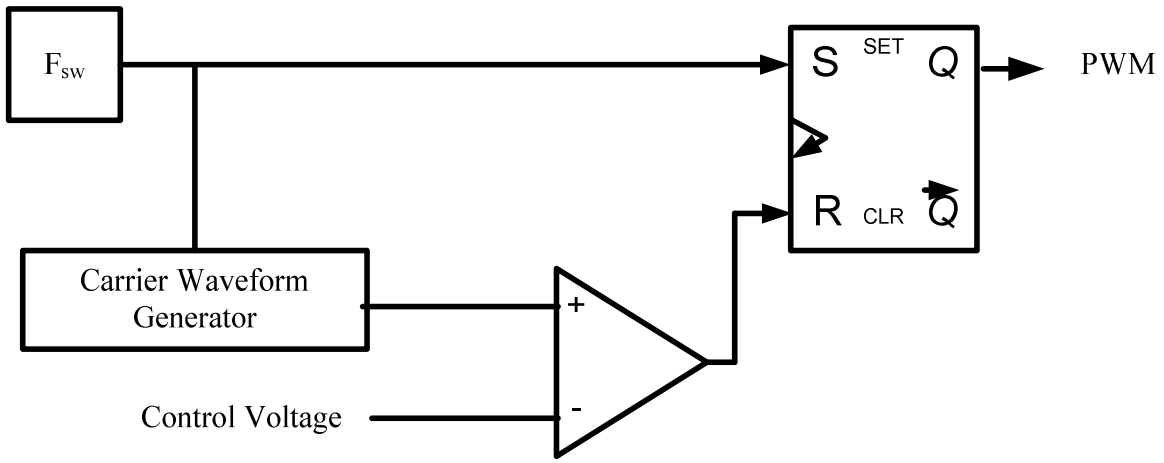


Figure 1.2: Block diagram of Analog PWM

A simple schematic circuit of the DC-DC Buck converter controlled by DPWM is shown in Figure 1.3. The analog to digital converter (ADC) is used to convert the analog voltage value to a digital value. The resolution of the DPWM depends on the number of ADC bits. The digital value is compensated and compared with the reference value which gives the duty cycle.

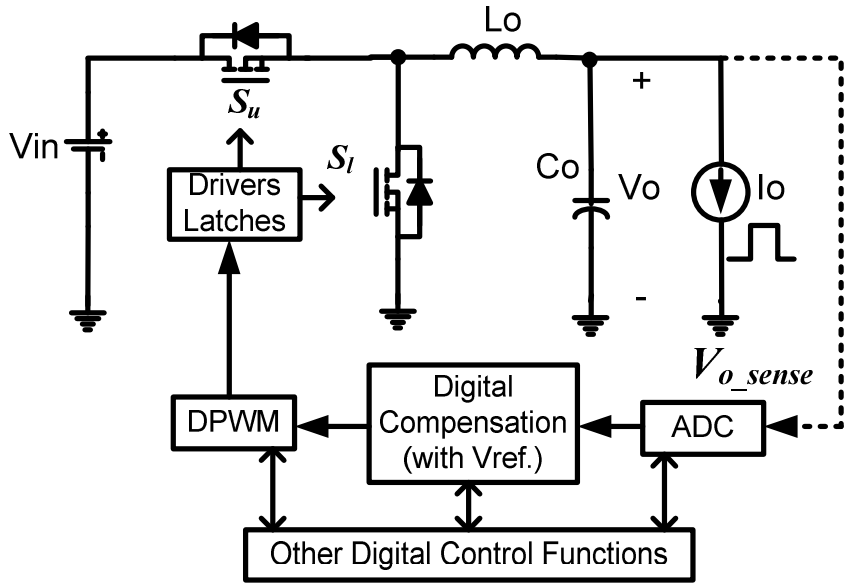


Figure 1.3: Schematic of a DC-DC Buck converter controlled by DPWM

Digital pulse width modulation (DPWM) provides a digital to time domain conversion. The time is quantized into number of discrete slots and is selected by a digital input d[n] instead of a carrier ramp signal. The duty cycle is compared with the time slots in order to generate the DPWM signal [2]. According to [2], the block diagram of digital PWM is shown in Figure 1.4.

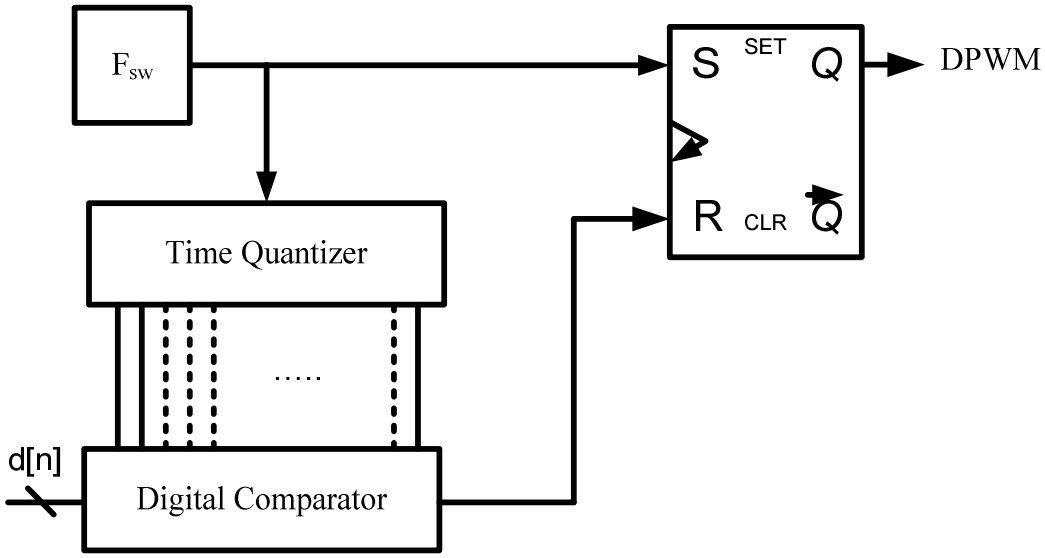


Figure 1.4: Block diagram of DPWM

1.3 Digital Controllers

A digital controller for switching mode power supplies (SMPS) is one of the fields that have attracted great research attention [1-14, 18, 30, 32, 33, 34]. According to [30], the reason for digital control becoming more popular in power electronics is its advantages over analog control, such as immunity to component variations and the ability to implement functions that improve the whole system performance. The digital controller consists mainly of three components. They are the analog to digital converter (ADC), digital compensation unit, and digital pulse width modulation (DPWM) unit. In Figure 1.5 the outline of a digital controller with switching converter is shown.

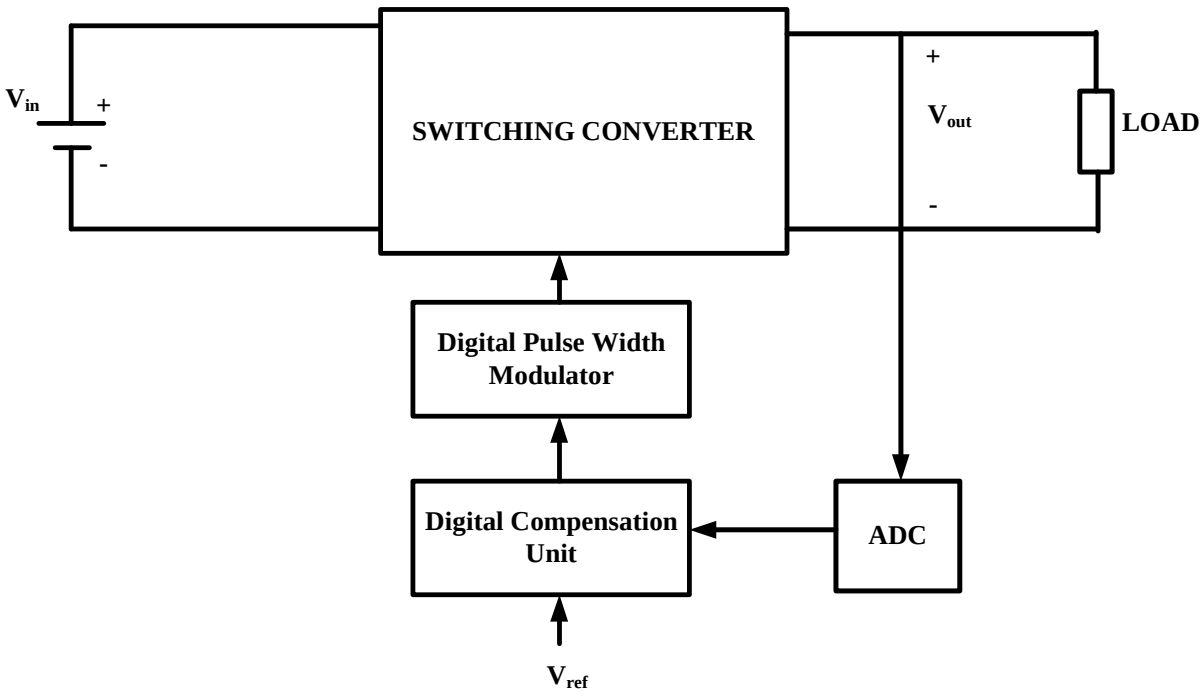


Figure 1.5: Outline of Digital Controller with switching converter.

According to [30] the digital controllers developed till now are the conventional architecture. In the conventional architecture, ADCs are used to digitize the converter state variables. The digital compensator unit determines the duty cycle, but this approach does not match the dynamic performance of the analog counterparts. The drawbacks of this architecture are delay in sampling or processing and limited resolution [18].

According to [30] development of alternative digital control architecture is needed that potentially enables a simple control architecture and faster dynamic performance. Analysis of [30, 32, 33, 34] suggests that the switching instants are determined by the combinations of system clock and intersection of controlled state variable and digitally controlled voltage and current ramps. In [32], two digital to analog converters (DAC) are used to control the analog peak mode modulator and the voltage mode modulator. In [30, 33], a similar principle is used, but it is applied to voltage-mode control of the synchronous buck converter. According to [30],

the main drawback in [33] is limit cycle oscillation when the equivalent series resistance (ESR) of the output capacitor is small. Analysis of [30] proposes a mixed signal, fixed frequency voltage mode controller for dc-dc converters where the derivative part of PID regulator is maintained in the analog domain. In this proposed controller the switch on is determined by the system clock and switch off is determined by comparing converter output voltage and instantaneous output voltage [30].

1.4 Principle of modulation

The pulse width modulation technique uses a rectangular wave whose pulse width can be modulated resulting in an average value waveform. This modulation can be done in different ways such as delta, delta-sigma, and digital, which are discussed below.

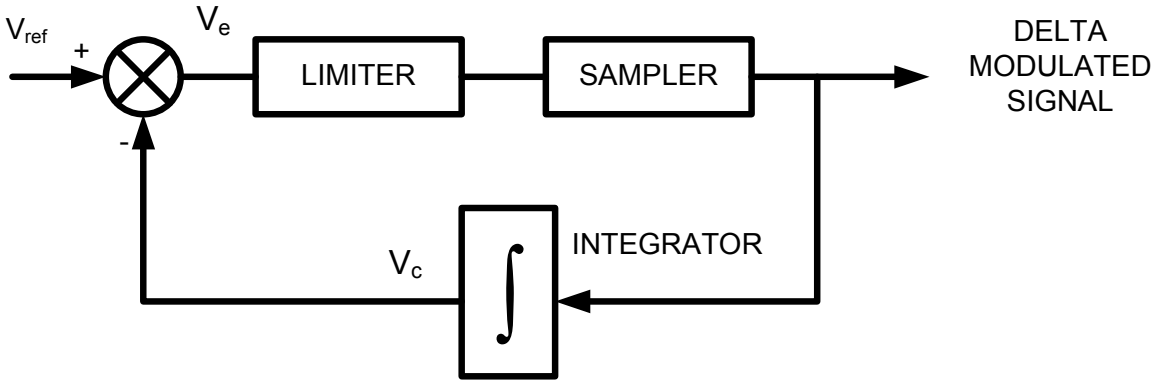


Figure 1.6: Block diagram of delta modulation.

The block diagram of delta modulation is shown in Figure 1.6. Delta modulation technique is known for its high stability and rapid response [35]. The delta modulation controller is relatively easy to implement when compared with other modulation controller techniques. The operation of delta modulation technique as follows. The carrier signals are obtained by integrating the output modulated signal. The control signal (V_{ref}) is compared with the carrier signal (V_c) and outputs the error signal (V_e). The error signal is quantized to produce the delta

modulated signal [35].The analysis of [35] suggests that this controller cannot be applied to the DC-DC converter because of equal rising and falling edge of the carrier signal. In order to overcome this drawback, delta-sigma modulation was proposed.

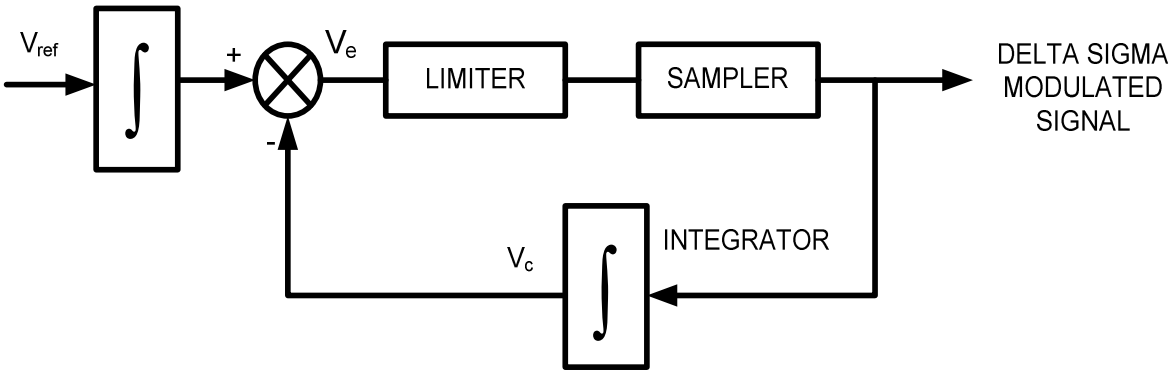


Figure 1.7: Block diagram of delta-sigma modulation.

The block diagram of delta-sigma modulation is shown in Figure 1.7. In delta-sigma modulation the control signal (V_{ref}) is fed forward to an integrator. In this way the slope of the integrator can be adjusted. Because of this feed forward signal, the positive and negative slope of the carrier signal is obtained. The rest of the operation is similar to the delta modulation. The delta-sigma modulation technique is widely used in data conversions and to achieve high resolution [36].

Digital modulation can be implemented in various ways such as counter based, delay line based and hybrid DPWM. Section 1.6 discusses in detail the various implementation of DPWM. This work mainly focuses on the digital pulse width modulation technique [1, 2, 14, 16, 20, 22].

1.5 Implementation of DPWM

This section discusses the various methods of implementing digital pulse width modulation, such as counter based, delay line based, and hybrid. This section also discusses some common modulator techniques. The three common modulators are leading edge, trailing edge, and double edge modulation. The next section discusses the operation and delay caused by digital pulse width modulators [1, 2, 14, 16].

1.5.1 Counter- based Digital Pulse Width Modulation

This section describes the basic operation of PWM when implemented in the digital domain using a counter. In analog PWM, the error signal is compared with ramp, and PWM pulses are generated. In digital PWM the duty cycle is compared with the counter value, and the DPWM signal is generated. A 10 bit duty cycle will be in the range of 0 to 1023. The transformation of analog to digital is performed by converting the error signal to duty cycle using an ADC. The ramp signal is generated using a counter. The resolutions of DPWM are finite when compared to the APWM. In other words, DPWM has better output regulation and less or no limit cycle oscillations. Counter based DPWM has modulation delays. These delays occur when there is a change in duty cycle [1, 2, 8, 12, 14, 16-18, 20, 22]. Counter based DPWM is implemented using counters as shown in Figure 1.8.

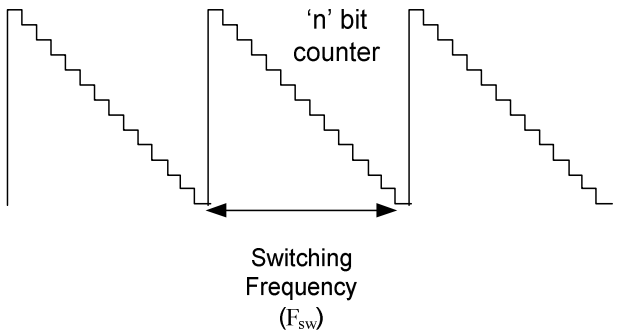


Figure 1.8: Implementation of counter based DPWM

The counter can be either up counter, down counter, or an up-down counter, depending on the modulation scheme. When the counter counts down, then it depicts the leading edge modulator. When the counter counts up, then it depicts the trailing edge modulator. When the counter counts up and down, then it depicts the dual edge modulator. The input clock frequency (F_{clk}) of the counter is directly proportional to switching frequency (F_{sw}) and number of bits (n). According to [1, 2, 12, 16] the relationship can be expressed as follows.

$$F_{clk} = F_{sw} * 2^n \quad (1.1)$$

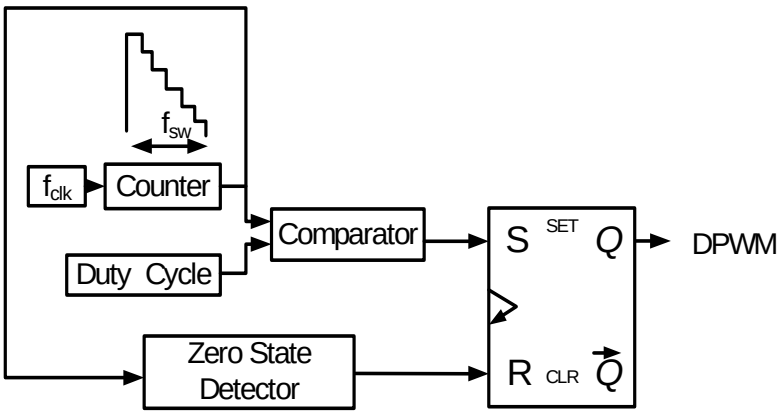
If the counter is 10 bit counter with the clock frequency of 350 MHz then the switching frequency would be 342 KHz. The main advantages of the counter based DPWM are its simplicity and linearity. In order to achieve high resolution the number of bits in the counter should be high.

The main disadvantage of counter based is need for high clock frequency and high power consumptions [1, 2, 12, 29]. For example a 10 bit DPWM with switching frequency 1 MHz, the required clock frequency will be approximately 1 GHz, and also power consumption will be high. Therefore implementation of high frequency, high resolution counter based DPWM would be a difficult [2, 12, 14, 16, 20]. The three common modulators implemented using counter based technique is discussed below.

a. Leading-edge Digital Pulse Width Modulation

The leading-edge DPWM block diagram and its operational waveform are shown in Figure 1.9. The duty cycle and counter are inputs to a comparator. The counter is a down counter. The output of the comparator turns the DPWM pulse on whenever the duty cycle is higher than the counter value. DPWM will be turned off only at the end of switching cycle. The S-R flip flop sets the DPWM high when the duty cycle is greater than counter value and it resets when the main counter finishes counting to zero.

Under the transient load condition at point t_3 as shown in Figure 1.9(b) the duty cycle drops below the counter but the modulator cannot respond to the change, it waits until the end of the switching cycle, to turn off the DPWM. This turn off delay results in overcharging the inductor. Therefore inductor delivers more power to output and cause extra overshoot or ring back in output voltage. Therefore, this conventional leading-edge modulation has delay in turning off the DPWM [2, 14, 16, 20].



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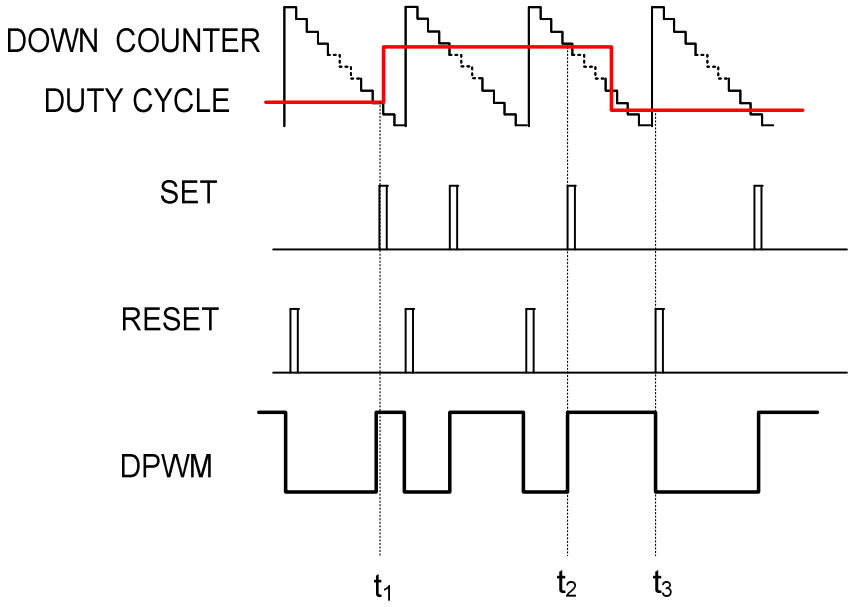
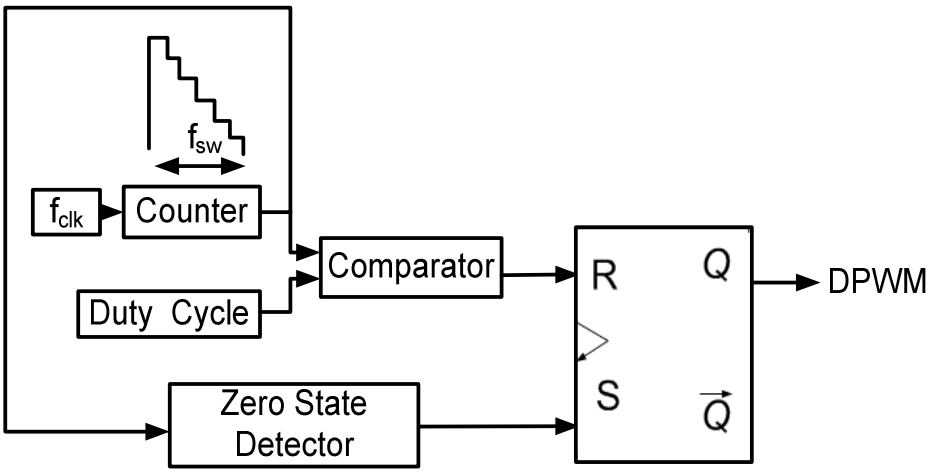


(b)

Figure 1.9: Leading-edge Digital Pulse Width Modulation (a) Block diagram and (b) Operational waveform

b. Trailing-edge Digital Pulse Width Modulation



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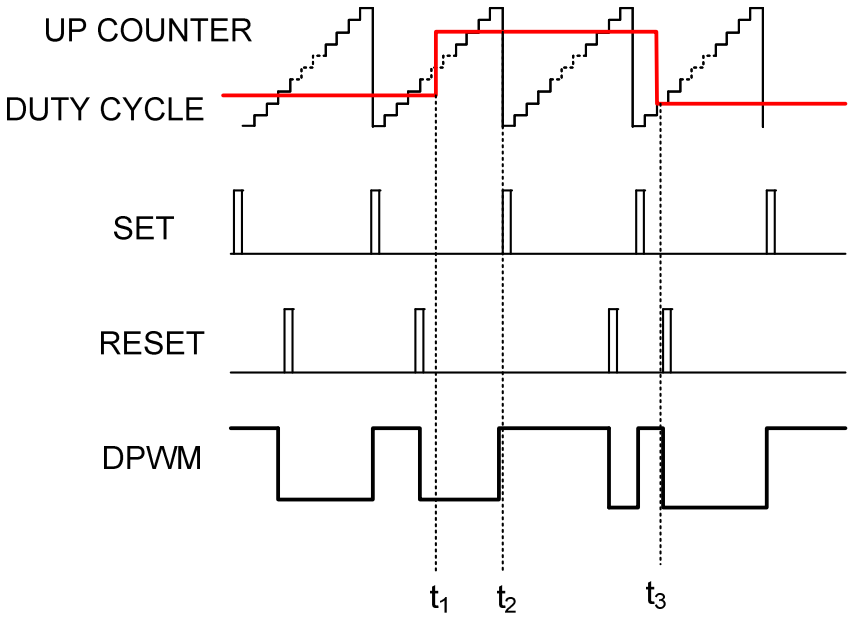


(b)

Figure 1.10: Trailing-edge Digital Pulse Width Modulation (a) Block diagram and (b) Operational waveform

Trailing-edge DPWM block diagram and its operational waveforms are shown in Figure 1.10. In trailing-edge modulation, the DPWM is turned on by the clock signal and is turned off by output of the comparator. The inputs to the comparator are similar to leading edge modulation. But here, the counter is an up counter. In this scheme, turning on the DPWM pulse is fixed, and turning off the pulse is done by output of the comparator. Therefore, initially at the starting of switching cycle, the DPWM is turned on, and if the duty cycle value goes below the counter, the comparator the DPWM is turned off. In this case after the DPWM is switched off by comparator and if the duty cycle goes high in the same switching cycle, then modulator will not respond to the change it waits until the next switching cycle. At point t_1 as shown in Figure 1.10 (b) the duty cycle goes above the counter but the modulator cannot respond to the change, it waits until the end of the switching cycle, to turn on the DPWM. Therefore this causes a turn on delay [2, 14, 16, 20].

c. Dual-edge Digital Pulse Width Modulation Scheme

The block diagram of dual-edge DPWM and its operational waveform are shown in Figure1.11. The counter in this conventional scheme is an up\down counter. In the first half of the switching cycle the counter acts as either up or down and in the second half of the cycle it acts either down or up, or vice versa. When the counter value is greater than duty cycle, then the DPWM pulse is set to high. Half of the switching cycle act as leading edge and other half of the switching cycle act as trailing edge.

Therefore, in this case turn on and turn off delay times exist and are shorter when compared to the leading edge and trailing edge modulator [2, 14, 16, 20].

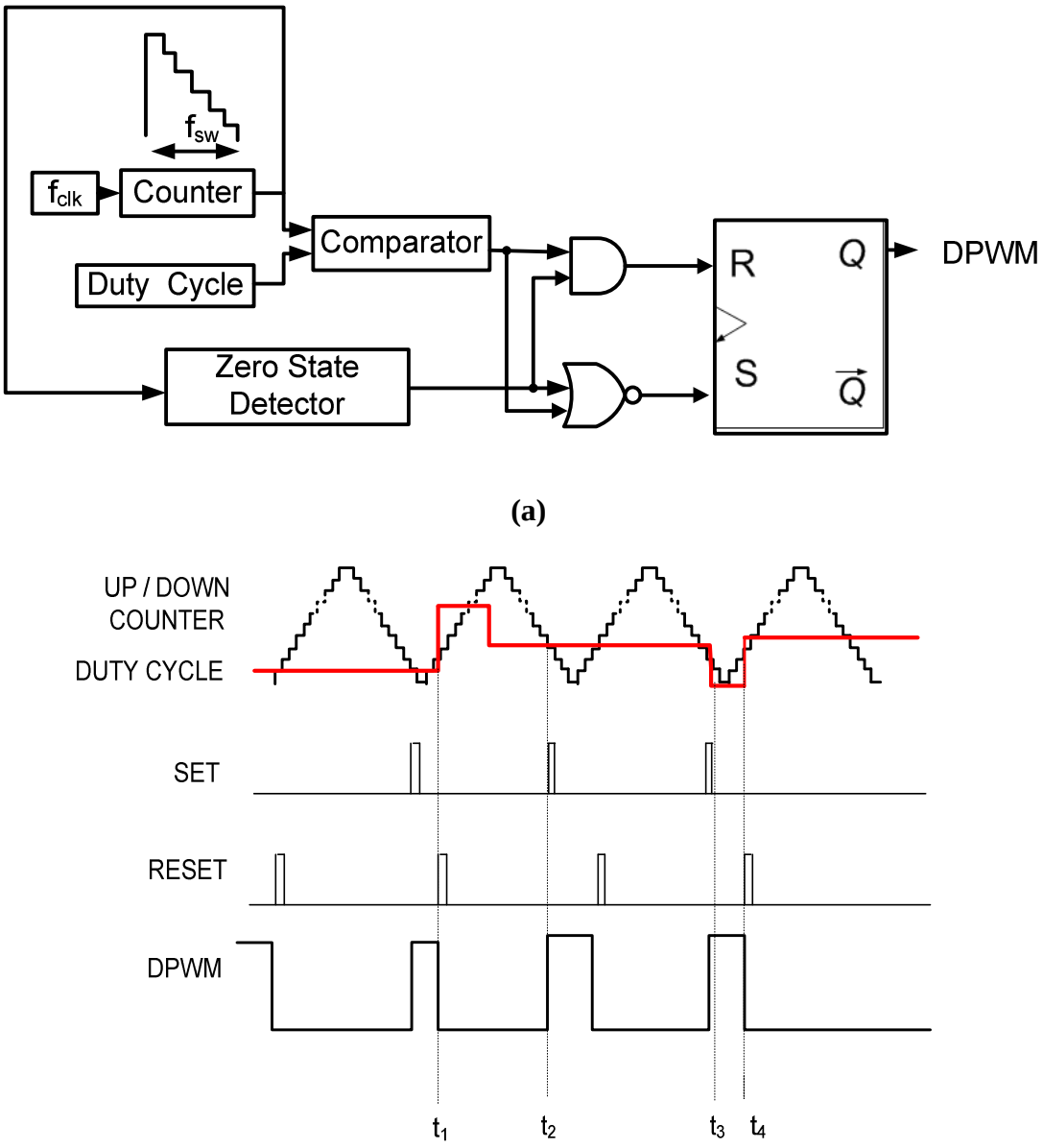
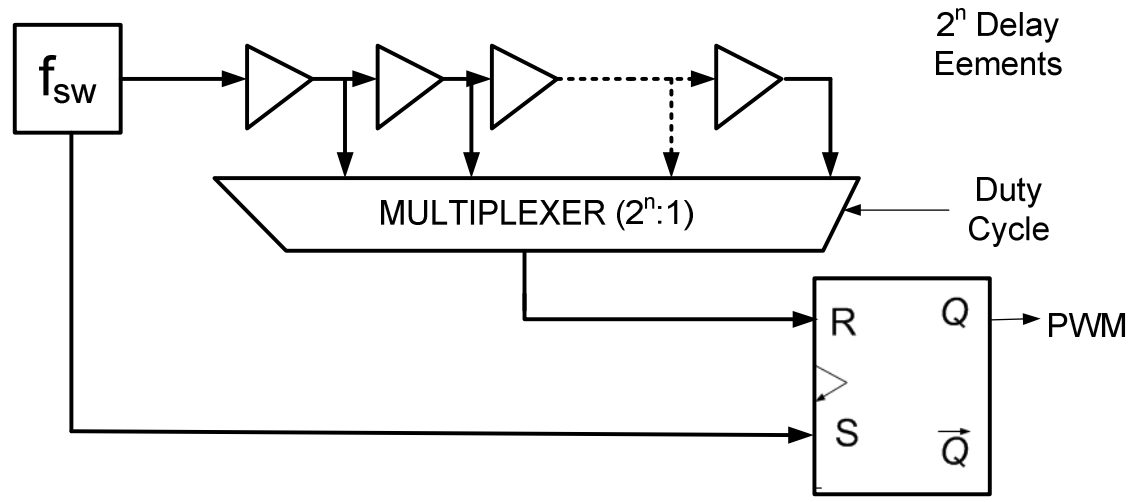


Figure 1.11: Dual-edge Digital Pulse Width Modulation Scheme
(a) Block diagram and (b) Operational waveform

1.5.2 Delay line based Digital Pulse Width Modulation

The block diagram of delay line based DPWM is shown in Figure1.12. . This type of modulation employs delay cells connected in cascade.



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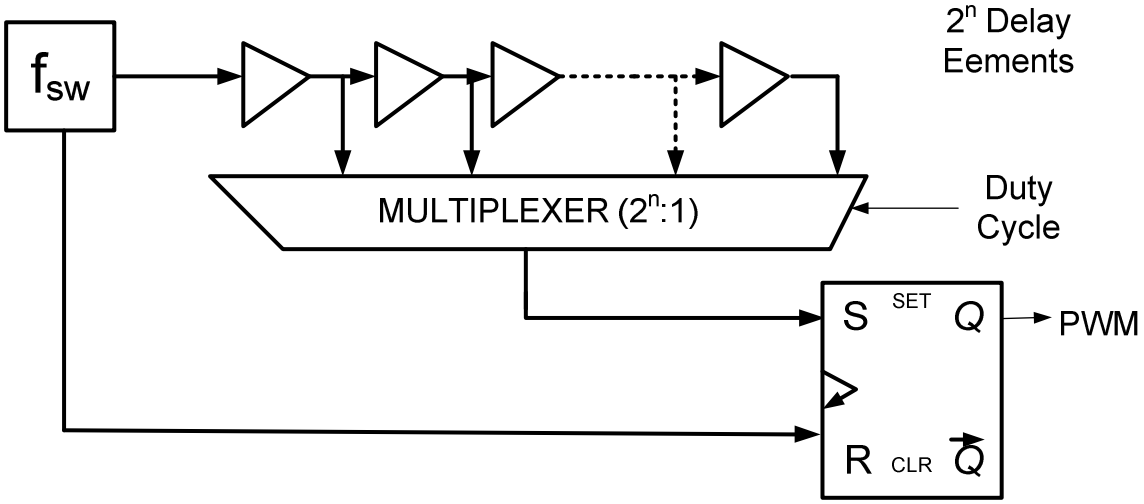


(b)

Figure 1.12: Delay line based Digital Pulse Width Modulation Scheme

(a) Trailing-edge delay line DPWM (b) Leading-edge delay line DPWM

The pulse width is quantized as a function of delay cells. For an 'n' bit duty cycle, 2^n delay elements are used. The selection of the delay cells is made by the multiplexer. The multiplexer is selected in such a way that for 'n' bit duty cycle, 2^n :1 multiplexer is used. Therefore, the control signal for the multiplexer is also 'n' bit. The value of these 'n' bits control signal is the duty cycle value. Selection of the delay cells are performed by the multiplexer's

control signal. Part (a) of Figure 1.12 shows the trailing edge delay line based DPWM. The DPWM is set by clock and the reset action is done by the delay elements. In this case turning off the DPWM is fixed. When there is more than one change in the duty cycle value the DPWM cannot respond to the change and it waits until the next switching cycle to turn on the DPWM. Therefore there exists the turn on delay.

Part (b) of Figure 1.12 shows the leading edge delay line based DPWM. The DPWM is set by the delay elements, and the reset action is performed by the clock. In this case, turning on the DPWM is fixed. When there is more than one change in the duty cycle value, the DPWM cannot respond to the change, and it waits until the next switching cycle to turn off the DPWM. Therefore there exists the turn off delay. When the DPWM The disadvantage of this modulation is due to semiconductor material properties there will be variation in process and temperature that causes the variation in cell delay. The other disadvantage of delay line based DPWM is, it occupies large area [2, 12].

1.5.3 Hybrid Digital Pulse Width Modulation

Hybrid digital pulse width modulation is the combination of counter based and delay line based modulation. The hybrid digital pulse width modulation scheme provides high resolution, high frequency DPWM when compared to counter based and occupies less area when compared to delay line modulation. For example, a 5 bit hybrid DPWM can be broken down as a three bit counter DPWM and two bit delay line based DPWM. Therefore by this combination the need for high clock frequency, variation due to process, temperature and large area will be eliminated. Counter based DPWM controls the most significant bit (MSB) of the duty cycle while the delay line based controls the least significant bit (LSB) of the duty cycle or it can also be vice versa.

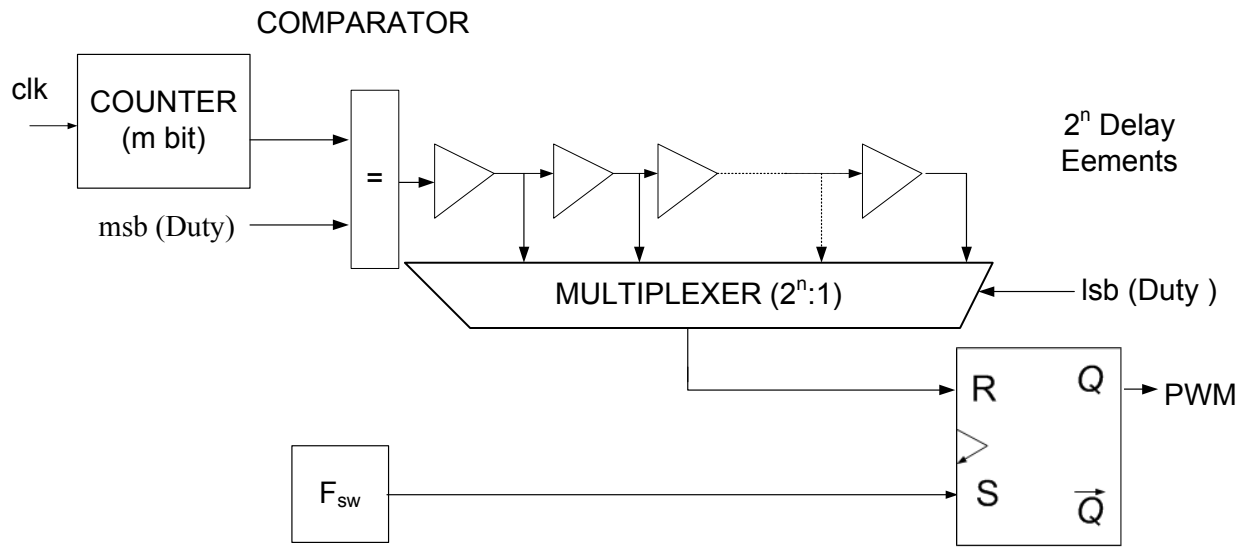


Figure 1.13: Block diagram of Hybrid Digital Pulse Width Modulation

For example in a 5 bit hybrid DPWM, 3 bit (m=3) counter counts from 000 to 111. And there are 4 delay elements with 4:1 multiplexer to select the delay cells. The 2 LSBs of the duty cycle are used as multiplexer control signal (n=2). The counter counts at each clock period. Initially the DPWM is set at the counter value of zero and the output of the counter is compared with MSBs of the duty cycle. When the counter reaches the duty cycle value it sends a signal for the delay line based DPWM. And the LSBs of the duty cycle will select the delay elements and sends a reset signal to the DPWM [12, 29]. The block diagram of hybrid DPWM is shown in Figure 1.13.

1.6 Thesis outline

As mentioned in earlier sections 1.6.1.a. and 1.6.1.b., during a transient event, there exists a modulation delay that can decrease performance of the buck converter. Therefore, a new modulation scheme is proposed to achieve fast response during transient event. The next chapter discusses in detail about proposed Modified Digital Pulse Width Modulation (MDPWM) and its implementation. Chapter 3 presents simulation results obtained using MATLAB\Simulink®.

The experimental set-up and the results are presented in Chapter 4 followed by the summary and future work in chapter 5.

CHAPTER 2

PROPOSED MODIFIED DIGITAL PULSE WIDTH MODUALATION

2.1 Introduction

Under a load step up current transient, there is an undershoot in the output voltage. Undershoot in the output voltage requires an increase in duty cycle to maintain a regulated output voltage, which increases the on time of the modulator. Under load step down current transient there is an overshoot in the output voltage. Overshoot in output voltage demands a decrease in duty cycle to maintain a regulated output voltage, which decreases the on time of the modulator [1, 2, 12, 14, 16].

In the conventional digital pulse width modulation schemes, the leading edge digital pulse width modulation exhibits turn off delay while the trailing edge digital pulse width modulation exhibits turn on delay. Therefore, a new modulation technique is proposed to reduce such delays. The main motivation behind reducing this delay is discussed in section 2.2, followed by discussion on the effect of these digital pulse modulation delays on the power converter in section 2.3, and in the later section the details and implementation of proposed MDPWM are presented.

2.2 Voltage deviation during load current transient events

Present integrated circuits (ICs) having high clock frequencies are accompanied by associated increases in the demand for power and fast transient response [16, 17, 19, 20].

Positive deviation from the nominal output voltage is called overshoot, and negative deviation from the nominal output voltage is called undershoot. The voltage deviation must be reduced in order to meet the load dynamic requirements. In order to maintain well regulated output voltage, the control signal must instruct the DPWM either to turn on or off early. If there is delay in the DPWM, then this may cause output voltage deviation.

Under load current transient events when the load increases or decreases, the control signal increases or decreases the on time of the DPWM signal to maintain a regulated output voltage. In most of the current applications, the transient response will be completed in one switching cycle. Conventional modulation may not respond to a change in the duty cycle in the same switching cycle [1-5, 14, 16, 19, 21]. The proposed modified digital pulse width modulation discussed in this chapter reduces the digital modulation delay of the conventional DPWM.

2.3 Effect of DPWM delay on converter's dynamic response

The purpose of the delay analysis is to improve the design of the converter and also to facilitate the design of the output capacitor. At load current transients, the delay caused by the DPWM, which is discussed in earlier sections, cannot be controlled by the capacitor design [14].

According to [25], the duty cycle resolution of counter based DPWM can be determined by (2.1):

$$\Delta D = f_{sw} / f_{clock} \tag{2.1}$$

Where ΔD is duty cycle resolution, f_{sw} is switching frequency and f_{clock} is clock frequency. According to [25], the relationship between the duty cycle resolution and output voltage resolution for a DC-DC buck converter is determined by (2.2):

$$\Delta V_o = V_{in} * \Delta D \quad (2.2)$$

ΔV_o is the output voltage resolution, and V_{in} is the input voltage. In the leading edge modulation scheme, under load current transient events, there exists a turn on delay. The worst case of this time delay occurs when there is a change in duty cycle value, at the starting of the switching cycle. According to [14] this maximum delay (t_d) can be expressed in terms of duty cycle (2.3):

$$t_d = T_{sw} * (1 - D + D/2) \quad (2.3)$$

Where the switching time is $T_{sw} = 1\backslash f_{sw}$. According to [1] the digital control system of buck converter is shown in Figure 2.1.

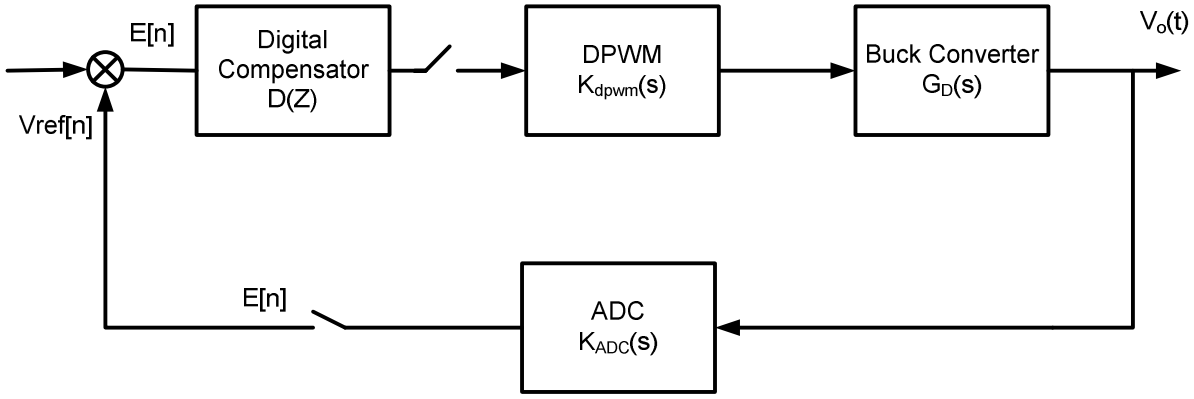


Figure 2.1: Digital control system of buck converter [1].

The open loop transfer function is

$$\frac{V_o}{V_{ref}} = D(Z) * Z\{K_{dpwm}(s) * G_D(s)\} \quad (2.4)$$

The closed-loop control to output transfer function is

$$C(Z) = \frac{D(Z) * Z\{K_{dpwm}(s) * G_D(s)\}}{1 + D(Z) * Z\{K_{dpwm}(s) * G_D(s) K_{a/d}(s)\}} \quad (2.5)$$

The transfer function of the DPWM is determined by (2.6)

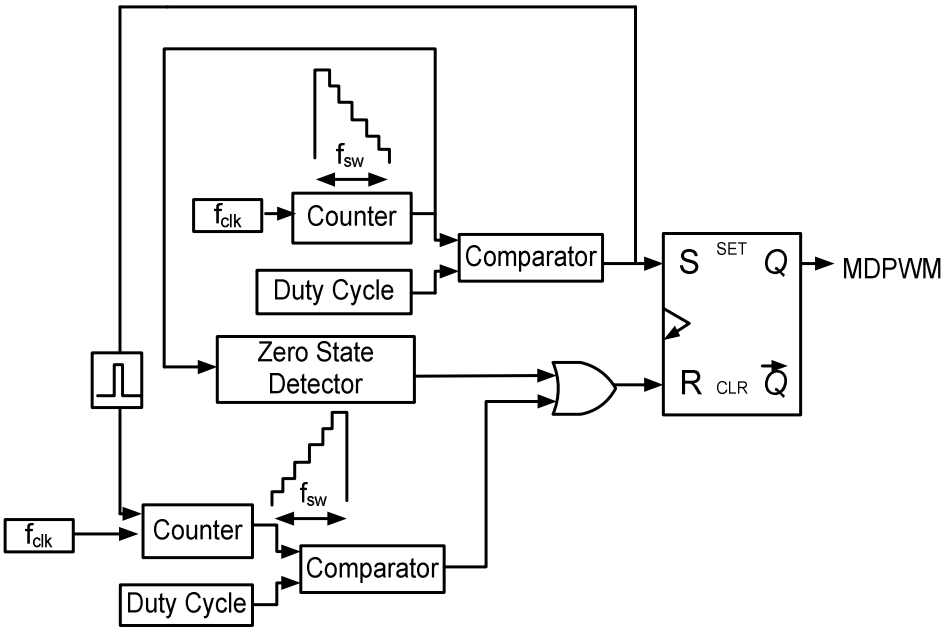
$$K_{dpwm}(s) = K_{dpwm} * e^{-(sT_{dpwm})} \quad (2.6)$$

$K_{dpwm} = 1 / \{(2^n{}_{dpwm}) - 1\}$ for 10 bit DPWM equal to $K_{dpwm} = 1 / 1023$, and T_{dpwm} is the delay between the time the DPWM input is updated and the time the switch duty ratio changes[1]. The transfer function of the converter depends on the transfer function of DPWM, controller and ADC. Therefore modulation delay affects the transfer function of the converter.

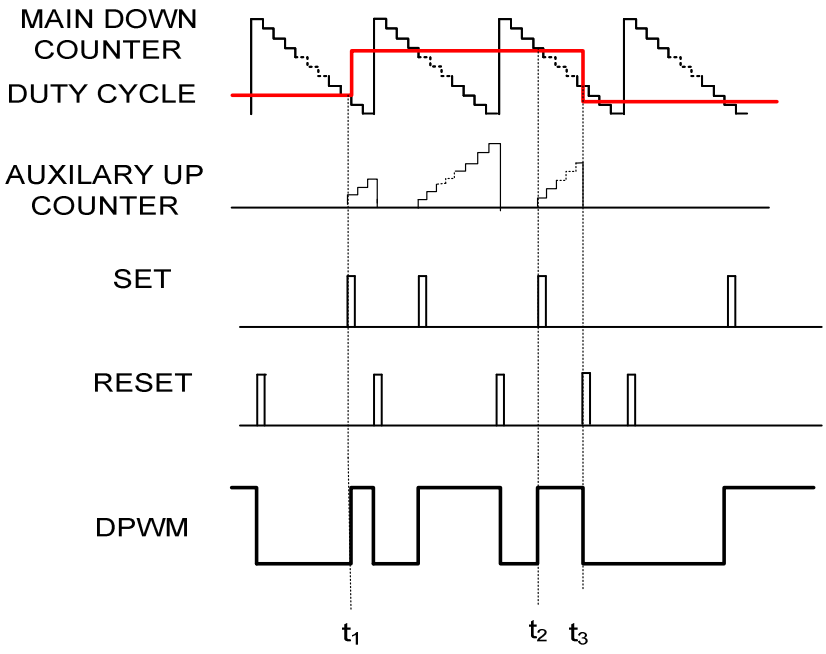
2.4 Counter based implementation of MDPWM

The basic concept of the proposed MDPWM scheme is the addition of the auxiliary counter in order to reduce the delay discussed in section 1.5. Figure 2.2 shows the reduction of turn off delay caused by the conventional leading-edge digital pulse width modulation.

The operation of MDPWM (to reduce the turn off delay) is as follows. The main counter is a down counter as it is the case in the leading-edge DPWM, and the auxiliary counter is an up counter. The auxiliary counter starts to count when the DPWM signal is set to high. At t_1, the DPWM signal is high and the auxiliary counter starts to count up until it reaches the duty cycle. In the conventional leading-edge modulation scheme the DPWM signal cannot be turned off any time after the DPWM signal is set to high. It can be turned off only when the main counter finishes counting. In contrary the proposed auxiliary counter can turn off any time with reduce turn off modulation delay.



(a)

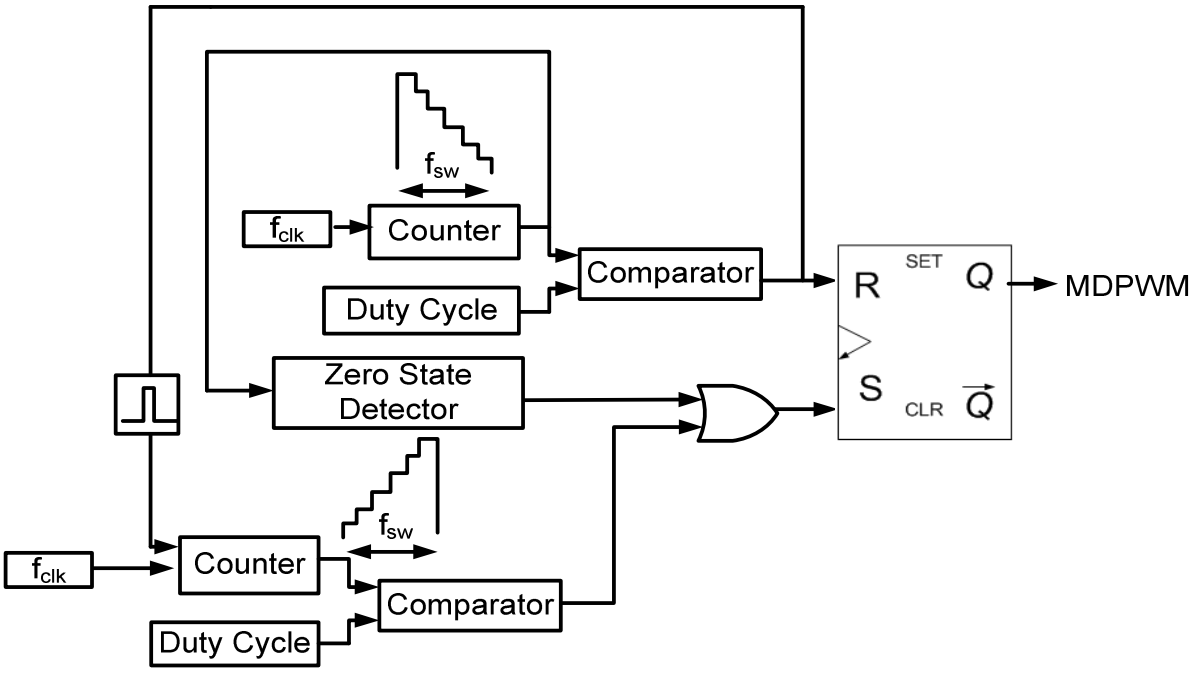


(b)

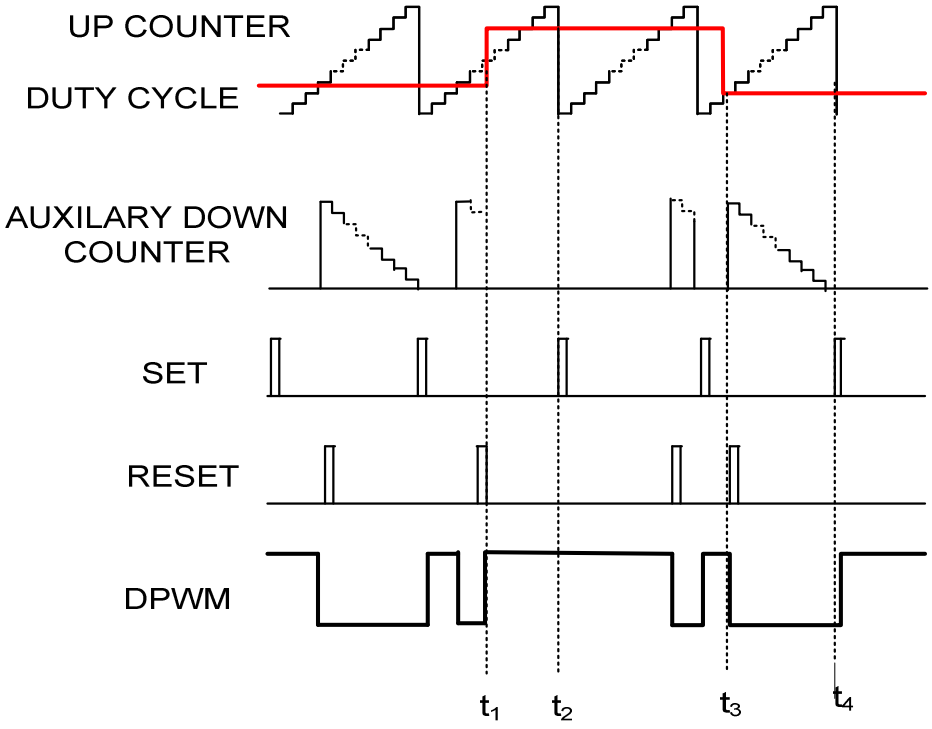
Figure 2.2: The Proposed MDPWM (Reduction of turn off delay) (a) Block diagram and (b) Operational waveform

At $t_{3,}$ the duty cycle drops from high to low, and the proposed modulator senses the change and resets the DPWM. It does not wait until the end of switching cycle to reset the DPWM. Therefore, in the proposed DPWM the turn off delay is reduced. This operation results in improvement in the output voltage overshoot. Figure 2.3 shows the reduction of turn on delay caused by the conventional trailing edge digital pulse width modulation.

The operation of MDPWM (to reduce the turn on delay) is as follows. The main counter is an up counter as it is the case in the trailing-edge DPWM and auxiliary counter is a down counter. The auxiliary counter starts to count when the DPWM signal is set to low. At t_3, the DPWM signal is low and the auxiliary counter starts to count up until it reaches the duty cycle. In the conventional modulation scheme the DPWM signal cannot be turned on any time after the DPWM signal is set to low. It can be turned on only when the main counter finishes counting. In contrast, the proposed auxiliary counter can turn on any time with reduce turn on modulation delay. At t_1 the duty cycle increases from low to high value and the proposed modulator senses the change and sets the DPWM. It does not wait until the end of switching cycle to set the DPWM. Therefore in the proposed DPWM the turn on delay is reduced. This operation results in improvement in the output voltage undershoot.



(a)



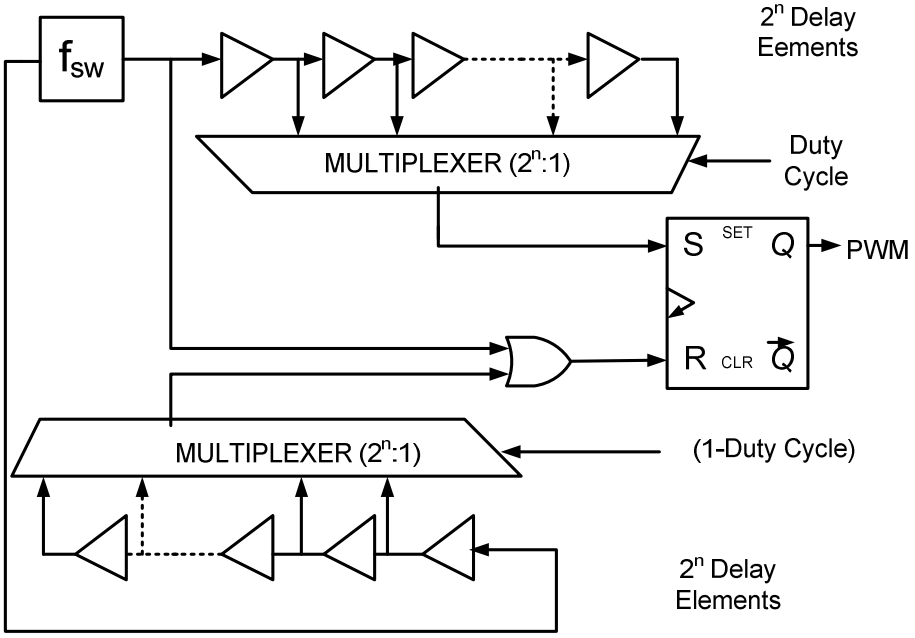
(b)

Figure 2.3: The Proposed MDPWM (Reduction of turn on delay) (a) Block diagram and (b) Operational waveform

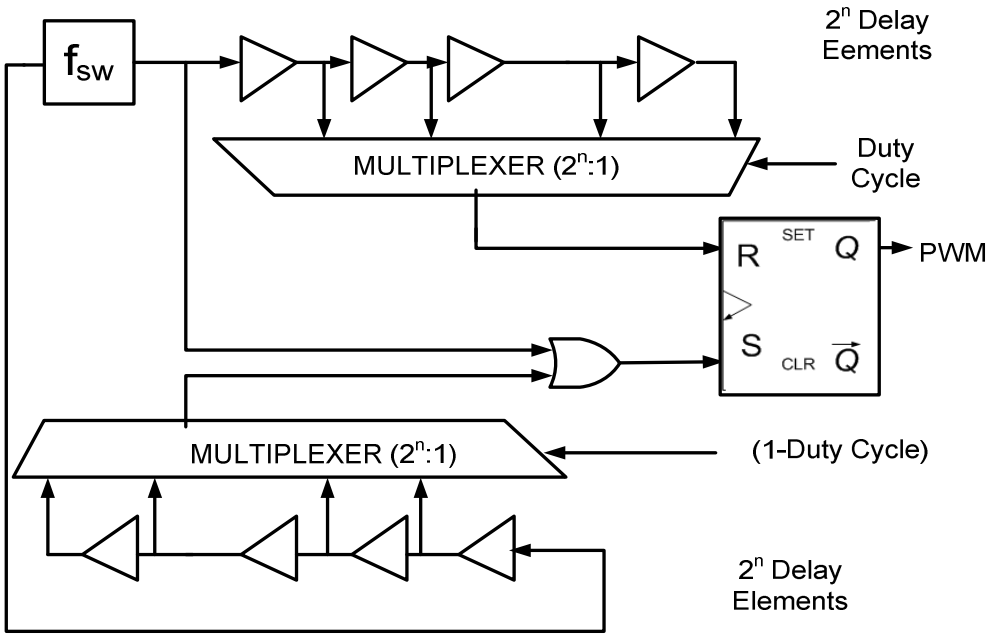
The proposed Modified Digital Pulse Width Modulation (MDPWM) scheme reduces the modulation delays that occur under load current transient conditions. Reduced modulation delay means reduced output voltage deviation from the reference voltage. The concept of the proposed MDPWM is to reduce the modulation delay by adding an auxiliary counter that helps either to turn on or turn off the control signal. In conventional DPWM techniques, there is either turn on or turn off delay, therefore, by adding an auxiliary counter to the modulation helps to reduce the delay.

2.5 Delay line based implementation of MDPWM

This section discusses the other possible implementation of proposed MDPWM. The proposed modulation scheme can also be implemented using delay line based DPWM. In the delay line based DPWM the number of delay cells depends on the number of bits of the DPWM. In conventional delay line based DPWM the pulse is set by the delay elements and the clock resets the DPWM. In the proposed MDPWM additional delay elements are added to reset the DPWM. Here the control signal for the multiplexer will be (1 - duty cycle). The implementation of MDPWM in using delay line to reduce turn off delay is shown in part (a) of Figure 2.4.



(a)



(b)

Figure 2.4: Delay line based implementation of MDPWM Scheme
(a) Reduction of turn off delay (b) Reduction of turn on delay

The DPWM pulse is set by the delay elements. The reset action is done by either a clock or the auxiliary delay elements. The auxiliary delay element resets the DPWM when ever there is more than one change in duty cycle, in one switching cycle. The implementation of MDPWM using delay line to reduce turn on delay is shown in part (b) of Figure 2.4. The DPWM pulse is reset by the delay elements. The set action is done by either a clock or the auxiliary delay elements. The auxiliary delay element sets the DPWM when ever there is more than one change in duty cycle, in one switching cycle.

The addition of auxiliary delay elements requires large area. The main disadvantages of the delay line based DPWM compared to the counter based implementation are possible non-linearity and large area. More investigation in this delay line based MDPWM is planned to be carried out in the future.

CHAPTER 3

COMPUTER SIMULATION RESULTS AND COMPARISION

3.1 Introduction

The computer software simulation results of the conventional DPWM and proposed MDPWM are presented in this chapter. The simulation results are obtained using Matlab®/Simulink® and PLECS® software. The open loop simulation were performed first, in order to verify the operation of the proposed MDPWM, and then followed by closed loop simulation results. The open loop simulation results are presented in Section 3.2, and the closed loop simulation results are presented in Section 3.3 and 3.4.

3.2 Open loop simulation results

In this section, the open loop simulation results of the conventional leading edge DPWM and proposed MDPWM are presented. In open loop simulations, the duty cycle is varied using a counter that switches between two constant values for a fixed time. This simulates the duty cycle that will be provided by the closed loop controller.

The open loop simulation is performed by a counter based 10 bit DPWM using 350 MHz clock. The switching frequency is calculated as 342 KHz using equation 1.1. The main counter is a down counter which resembles leading edge modulation. In this open loop simulation, the duty cycle is varied from 0.68 to 0.1.

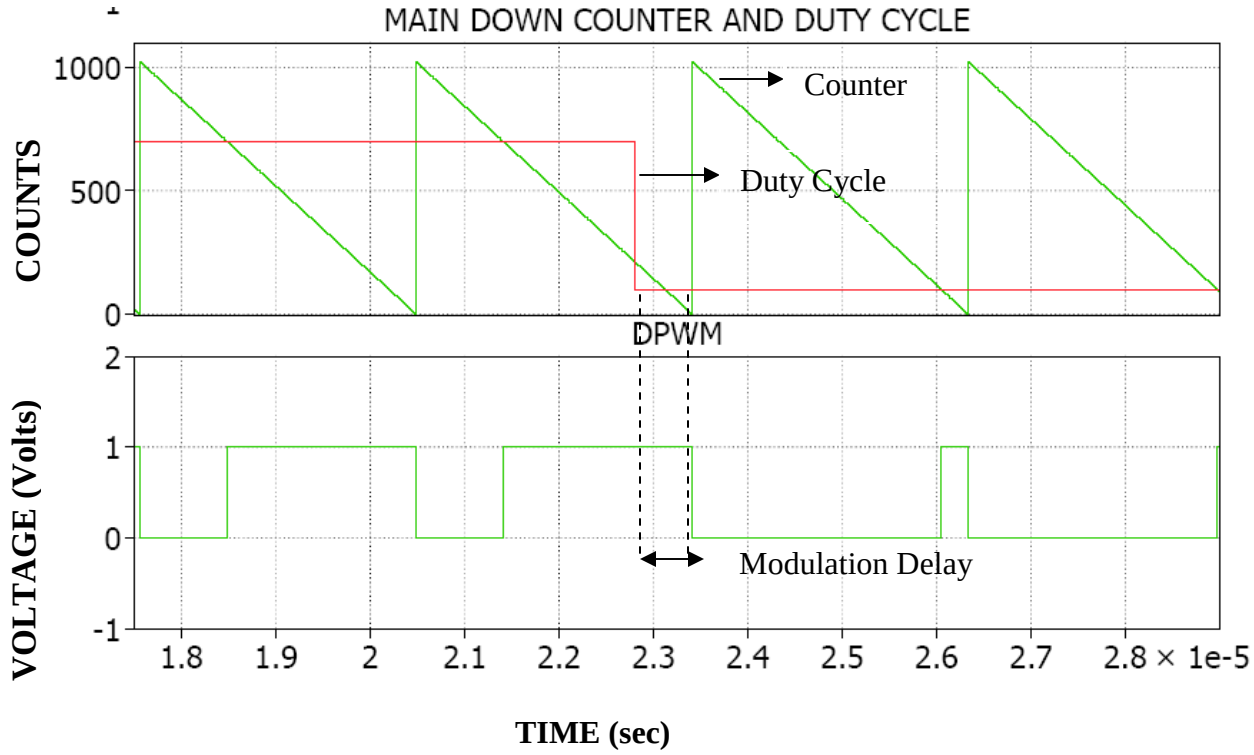


Figure 3.1: Open loop simulation results for conventional leading edge DPWM

Figure 3.1 presents the open loop results for the conventional leading edge DPWM. As shown in Figure1.9, when the duty cycle is higher than the counter value, the DPWM is set high by the comparator, and the DPWM signal resets when the counter value reach zero.

If there is any change in the duty cycle, it will not respond until next switching cycle. At 0.228 microseconds, there is a change in duty cycle, but the DPWM does not respond to the change and waits until the next switching cycle to turn off the DPWM. Therefore, turn off delay exists, which affects the dynamic performance of the closed loop system.

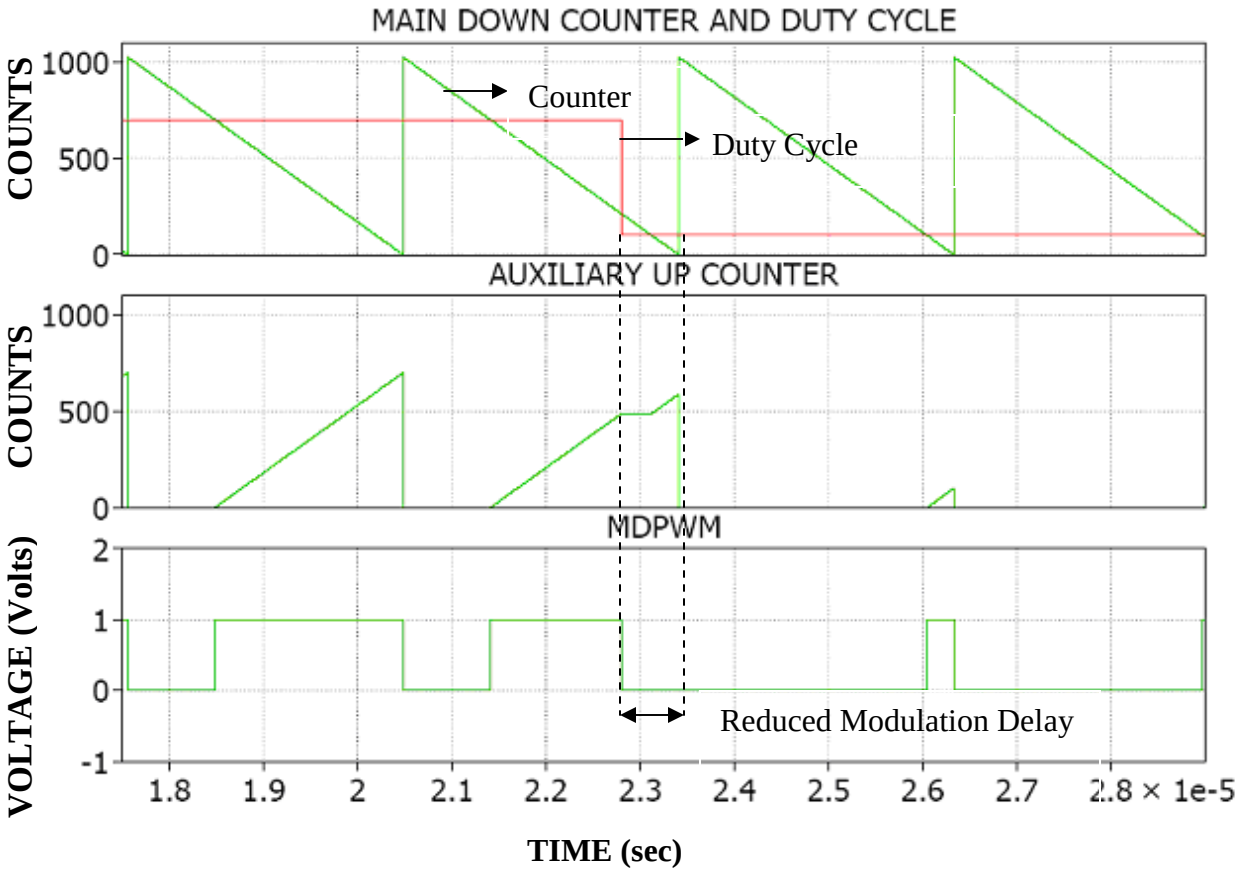


Figure 3.2: Open loop simulation results for MDPWM

Figure 3.2 presents the open loop results for the MDPWM. In the proposed modulation scheme, the auxiliary counter is added as shown in Figure 2.2 to reset the MDPWM when there is any change in the duty cycle value as discussed in chapter 2. The auxiliary counter starts to count when the MDPWM is set to high and it counts till the end of switching cycle as shown in Figure 3.2. When the duty cycle value goes below the counter in the middle of the cycle then the auxiliary counter resets the MDPWM. At 0.228 microseconds, the duty cycle is changed from 0.68 to 0.1 and the auxiliary counter resets the MDPWM. Therefore, the proposed modulation scheme responds to change in the duty cycle and reduces the turn off delay in this case.

3.3 Closed loop simulation model and its components

The specifications of the DC-DC buck power converter used for the closed-loop simulation of conventional and proposed MDPWM are the same. The specification of the DC-DC buck converter is as follows: V_{in} = 8V, V_o= 1.5V/ 3.3V, L= 440nH, C= 350µF, F_{sw} ~ 342 KHz, F_{clock} = 350 MHz, n $_{ADC}$ = 10 bits to sample output voltage.

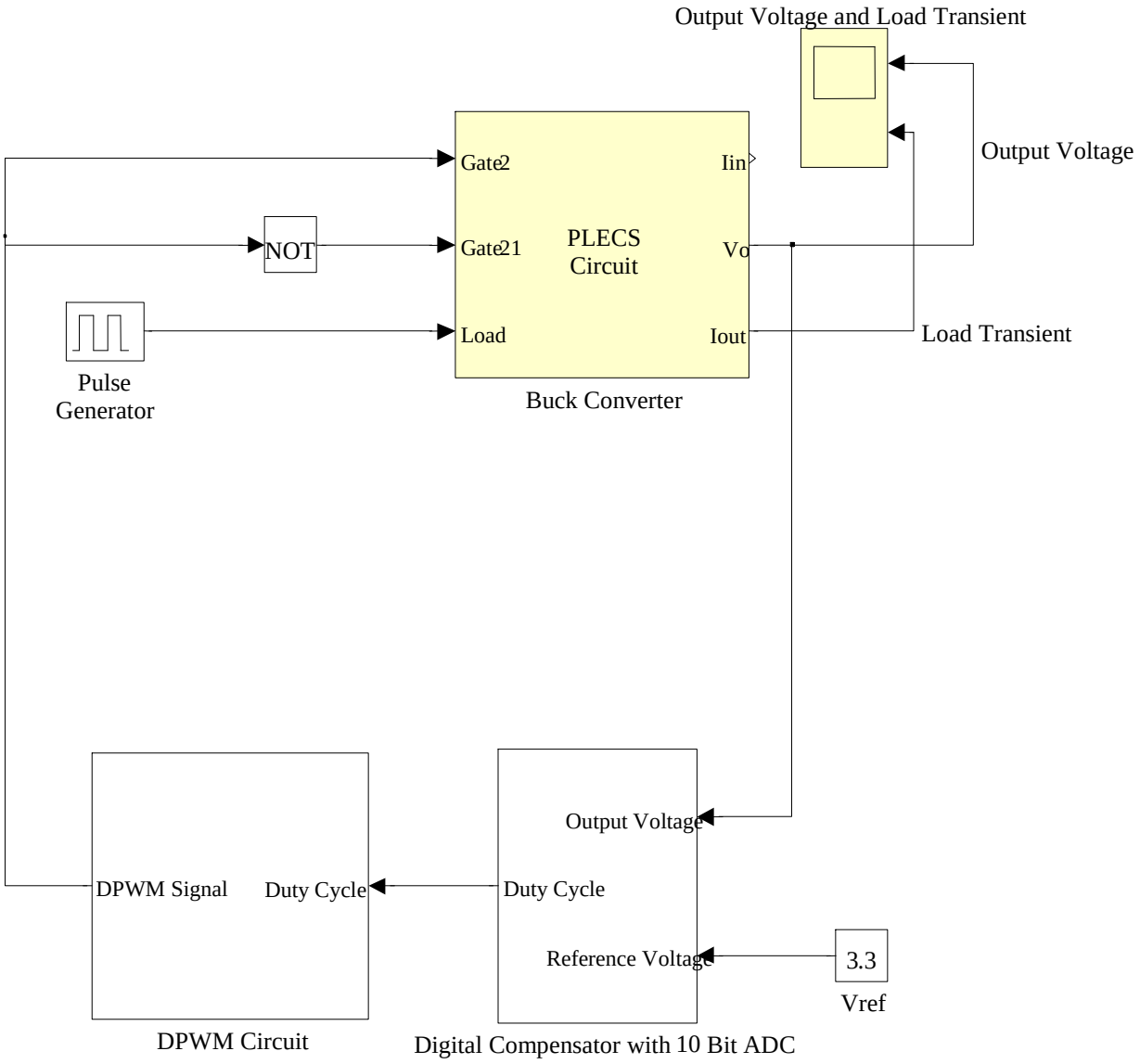
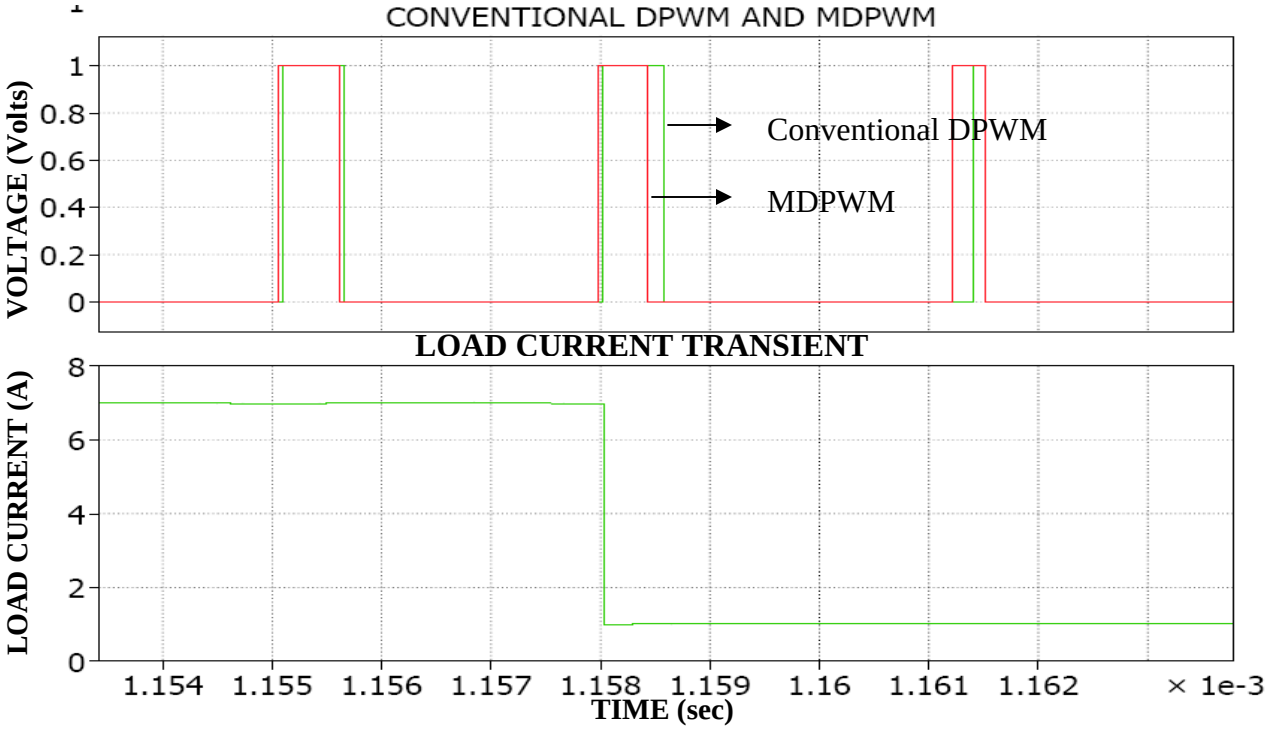


Figure 3.3: Closed-loop simulation model

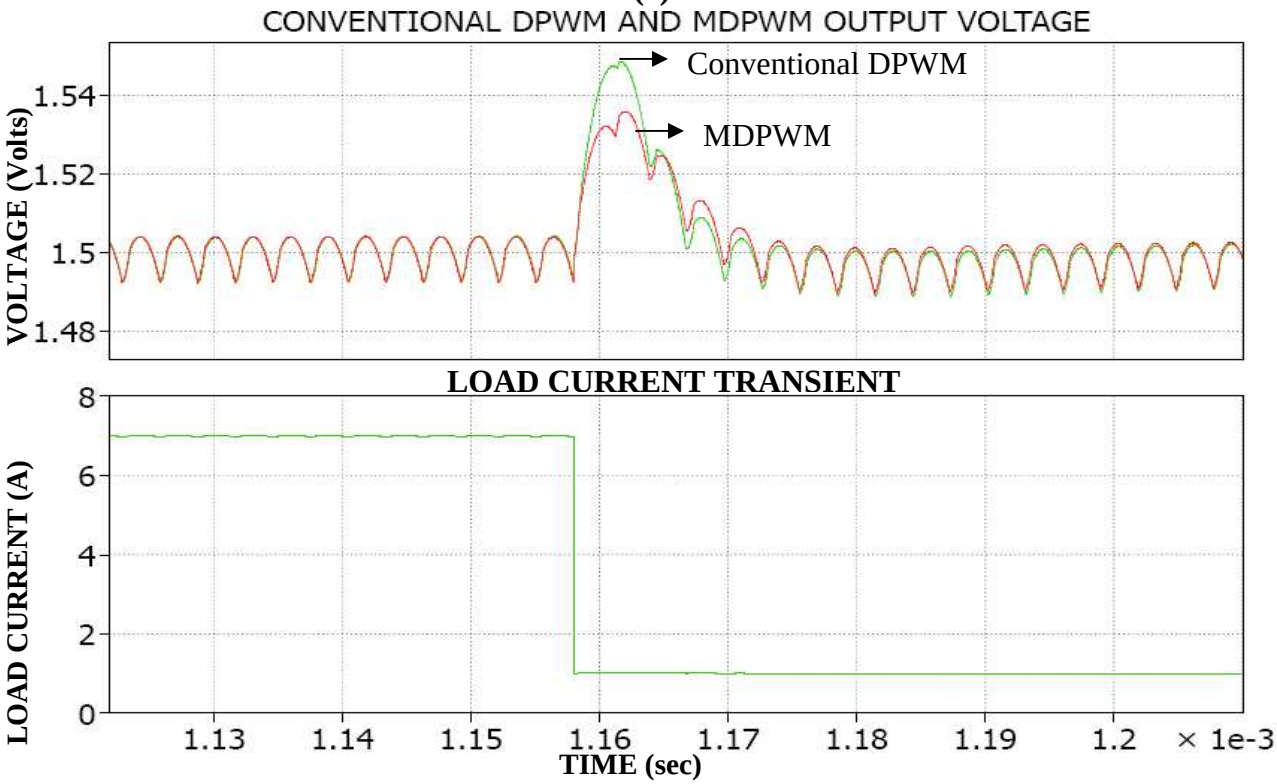
The simulation model has three main components: the DC-DC buck converter circuit, a digital compensator with 10 bit ADC, and a digital modulation unit. The PLECS® toolbox is used to build the buck converter. The input of the buck converter is 8 Volts. The simulation model of the closed- loop buck converter is shown in Figure 3.3. The simulation results are obtained for two reference voltages of 1.5 Volts and 3.3 Volts.

3.4 Closed- loop simulation results

The closed- loop simulation results of conventional and proposed MDPWM are presented in this section. The buck converter, with 8V input and 1.5 V output, are used in the simulation. The load step current transients are made when the DPWM is on to check whether the turn off delay is reduced. Load step current transient (Δi) of 6A, 15A, and 30A are applied as shown in figures 3.4, 3.5, 3.6. Part (a) of these figures shows the comparison between the conventional and the proposed DPWM signal during load current transient event. And part (b) of these figures shows the comparison between the conventional and the proposed DPWM output voltage signal. From part (a) figures, it is observed that at current transient events the proposed MDPWM signal has been turned off early when compared to the conventional DPWM. The turn off delay is reduced in proposed MDPWM. From part (b) figures it is observed that because of reducing the turn off delay using the proposed MDPWM there is an improvement (reduction) in output voltage overshoot. Therefore it is observed from the figures 3.4, 3.5, 3.6 that during the load step down current transients the conventional leading-edge modulator has a significant turn off delay while the proposed modulator has reduced turn off delay. Therefore, the proposed MDPWM has reduced turn off delays, unlike conventional DPWM modulators, leading to dynamic response improvement.

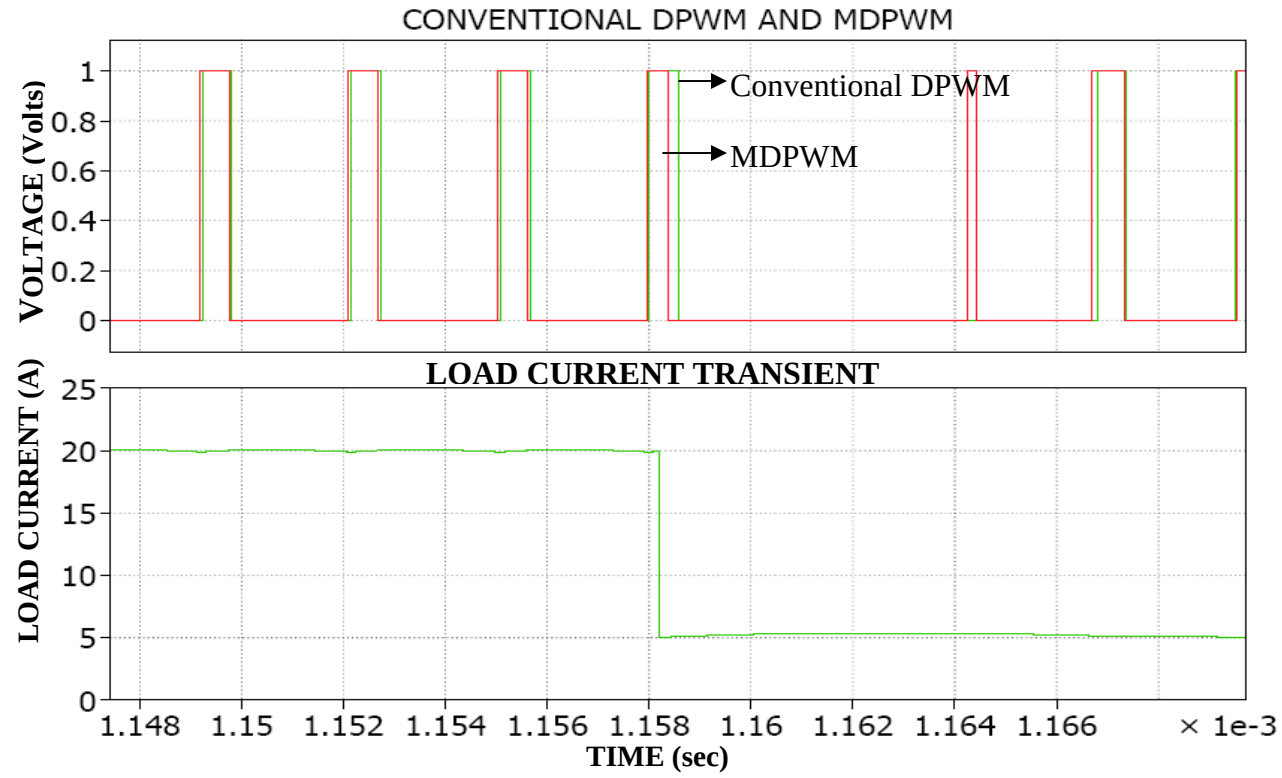


(a)

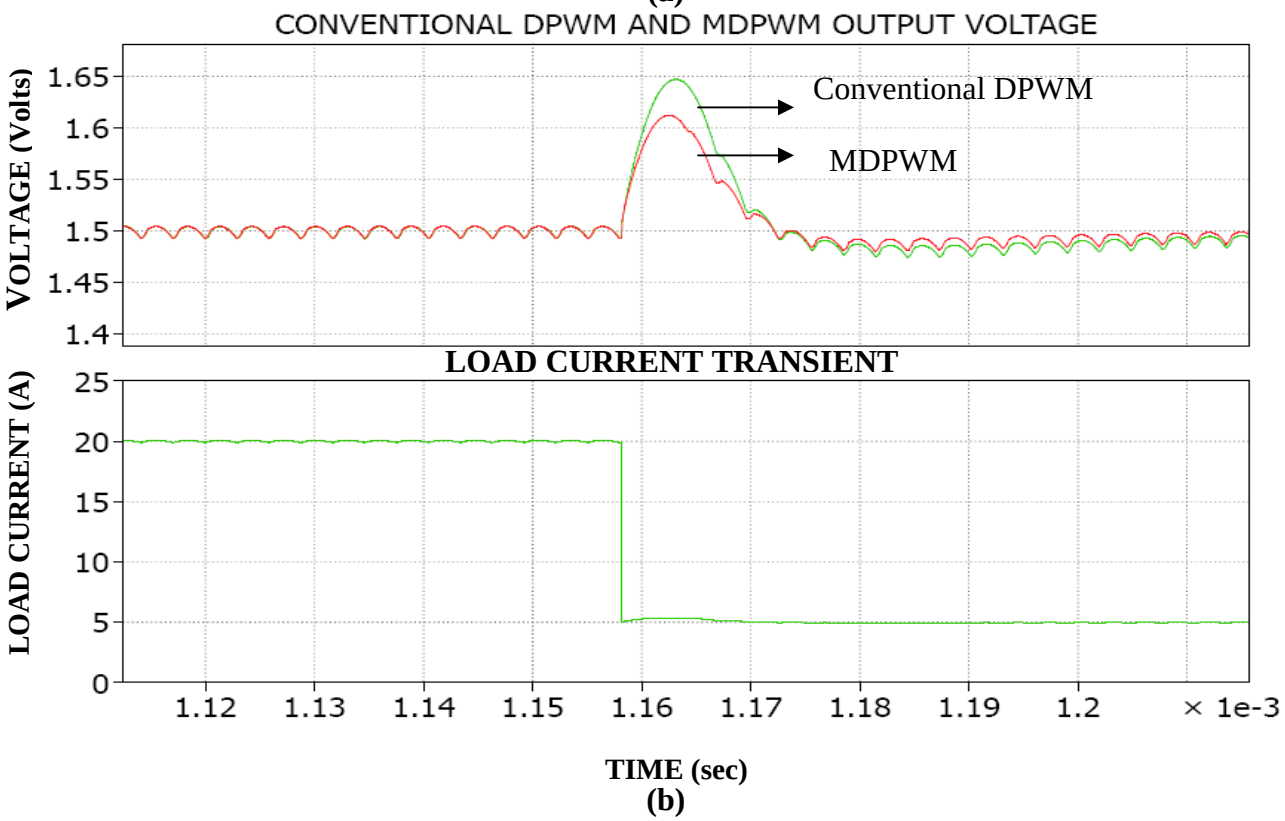


(b)

Figure 3.4: Closed loop simulation results for Vo=1.5V, Δi=6A (a) Load current transient during on time (b) Output voltage during load current transient

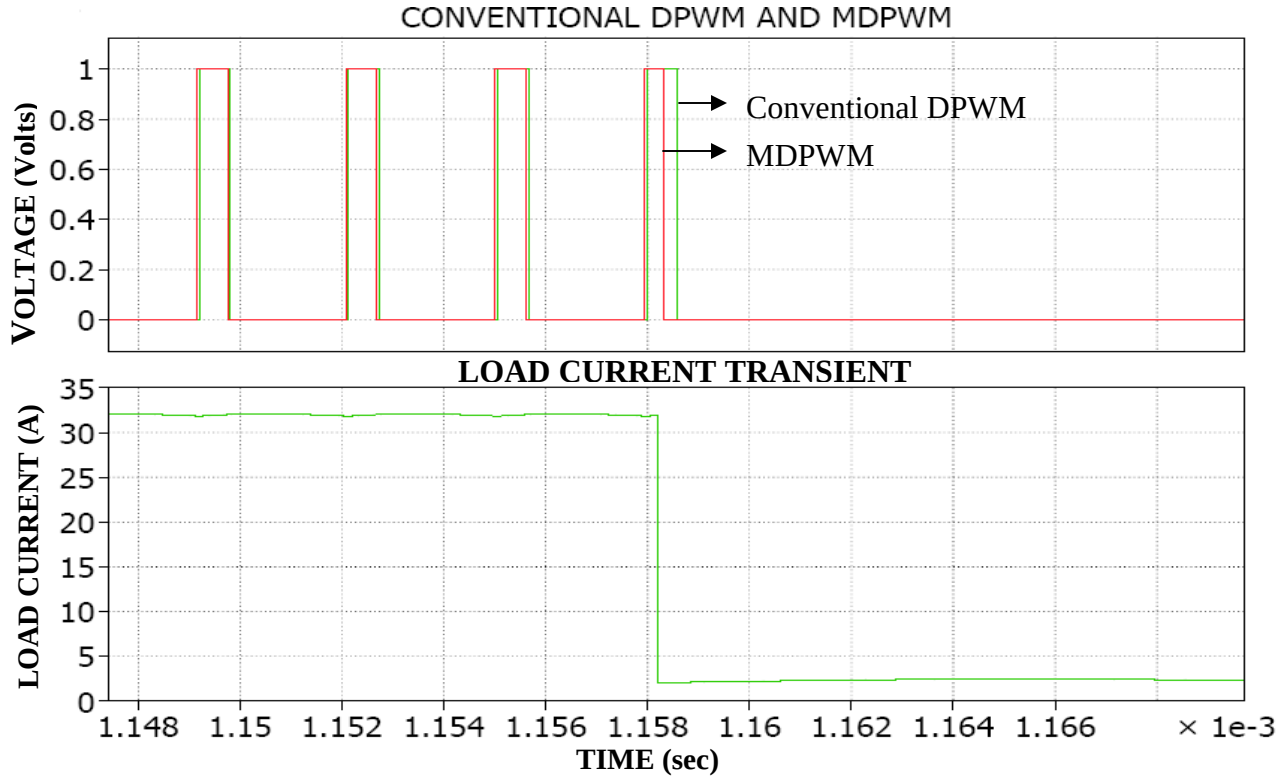


(a)

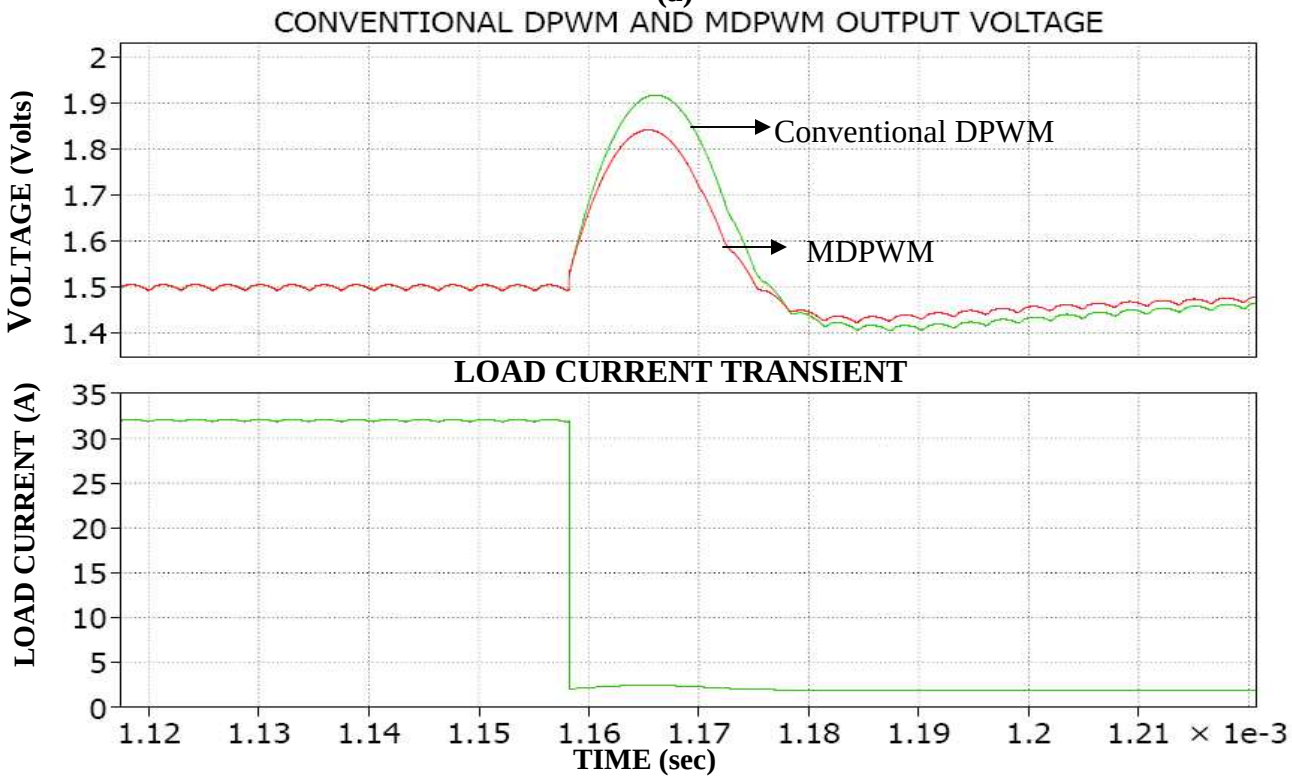


(b)

Figure 3.5: Closed loop simulation results for Vo=1.5V, Δi=10A (a)Load current transient during on time (b) Output voltage during load current transient

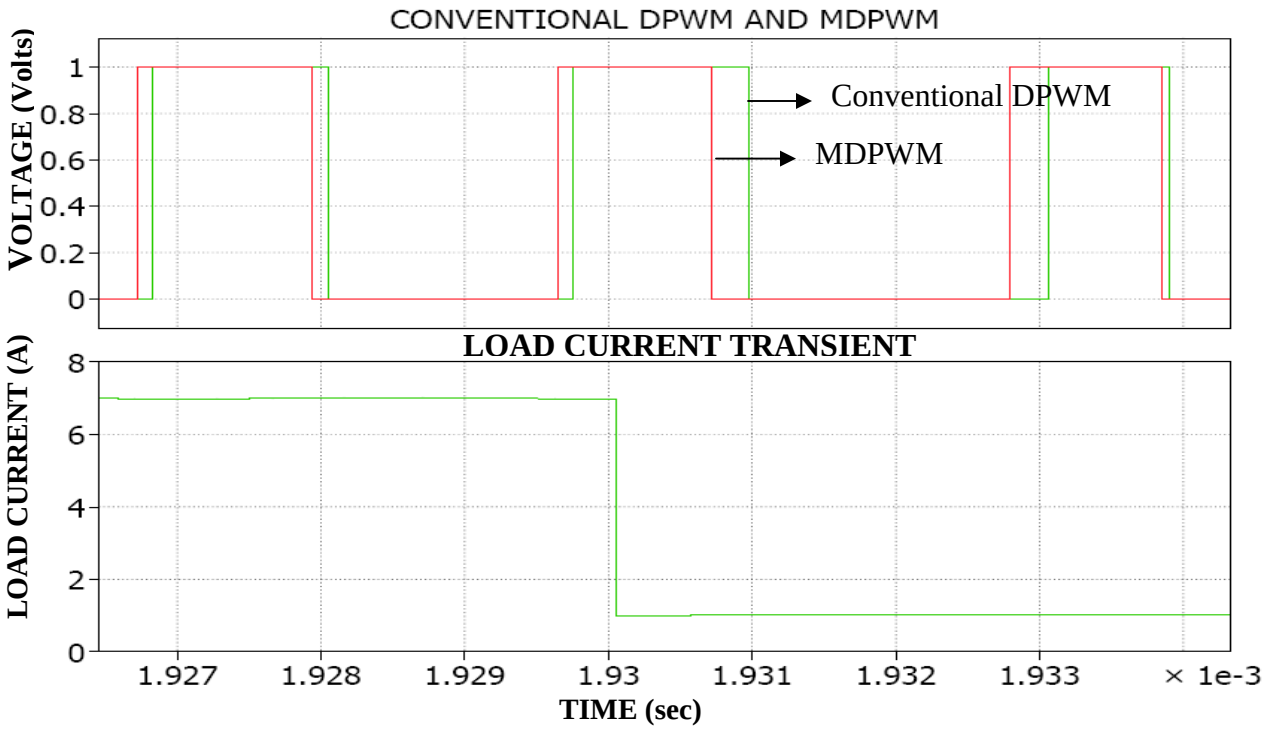


(a)

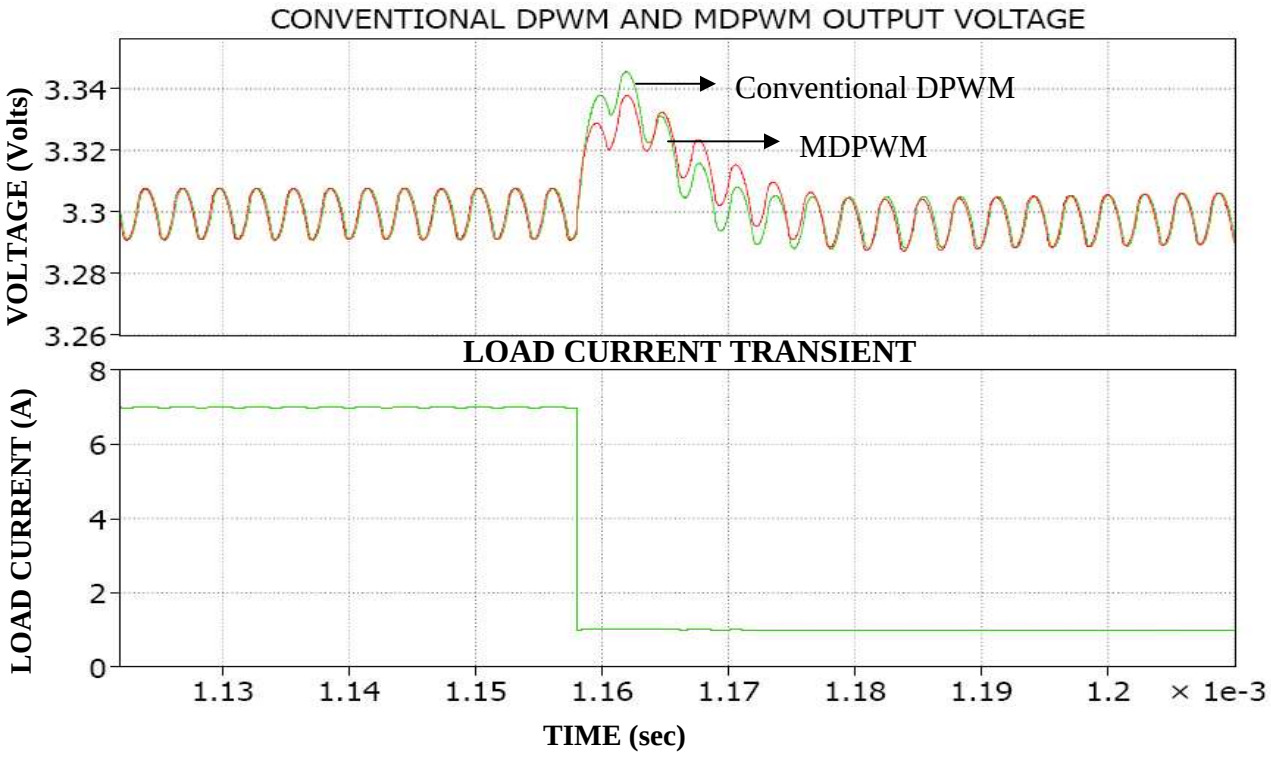


(b)

Figure 3.6: Closed loop simulation results for Vo=1.5V, Δi=30A (a) Load current transient during on time (b) Output voltage during load current transient



(a)



(b)

Figure 3.7: Closed loop simulation results for Vo=3.3V, Δi=6A (a) Load current transient during on time (b) Output voltage during load current transient

From the simulation results presented in this chapter, the turn off delay is reduced by the proposed MDPWM, and improvement in overshoot voltage is achieved. In the next chapter the experimental results are presented and discussed.

Chapter 4

EXPERIMENTAL WORK AND RESULTS

4.1 Introduction

This chapter presents the experimental set up and the results obtained for the conventional DPWM and the proposed MDPWM. The open loop results are obtained as discussed in the Chapter 3. In closed loop control of the power converter, the compensator calculates the value of duty cycle and provided to the modulator. The experimental set up is discussed in Section 4.2, followed by overview of Altera FPGA board used in the experiment, and then the open loop and closed- loop experimental results are presented

4.2 Experimental set-up

The experimental set up is illustrated in Figure 4.1. The following components are used for the experiment:

- Digitally controlled Single phase DC-DC Buck power converter.
- Altera DE 2 board.
- USB cable for FPGA programming and control.
- 9V DC wall mount power supply.
- DC Load: Chroma 6312.
- Chroma Programmable DC power Supply: 6201P-80-60.
- Tenma Laboratory DC power Supply 72-6615.

- Oscilloscope: Tektronix DPO7104.
- Connectors.

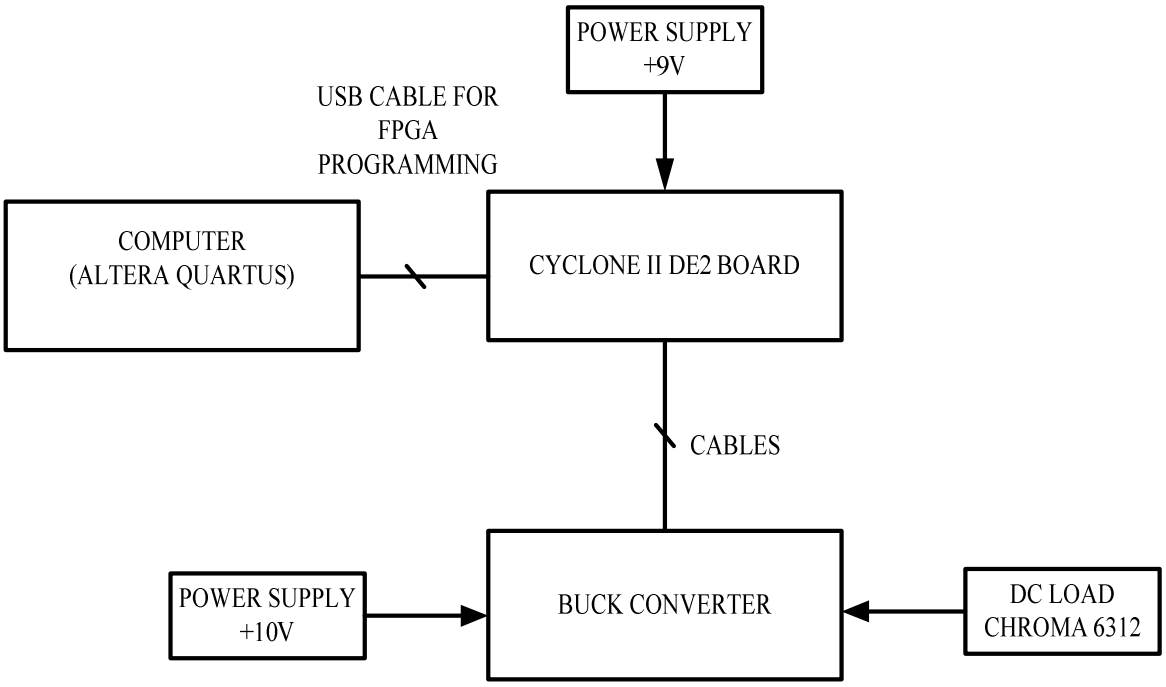


Figure 4.1: Schematic Experimental setup

An Altera Cyclone II EP2C35F672C6 chip is used to provide the closed loop control for the power converter. On the DE2 board, there is a built in 50 MHz clock. The main clock of 350 MHz is needed for the counter, and it is generated using a phase lock loop (PLL). The Quartus mega wizard built in PLL function is used to generate a 350 MHz clock. The program is written in verilog and downloaded to the DE2 board via USB programming cable. The buck converter is connected to the DE2 board via connectors. The input voltage is provided to the buck converter using Chroma Programmable DC power Supply. Chroma 6312 DC load is used as the output current load to the power converter.

4.3 An overview of Altera FPGA board

The Altera DE2 board has cyclone II 2C35 FPGA chip with 3500 logic elements, 475 user IOs, 35 embedded multipliers and 4 PLLs. It also includes a 50MHz clock, 27 MHz clock, and Sub-Multi Assembly (SMA) and external clock input [41]. An example picture of Altera DE2 board is shown in Figure 4.2 [39].

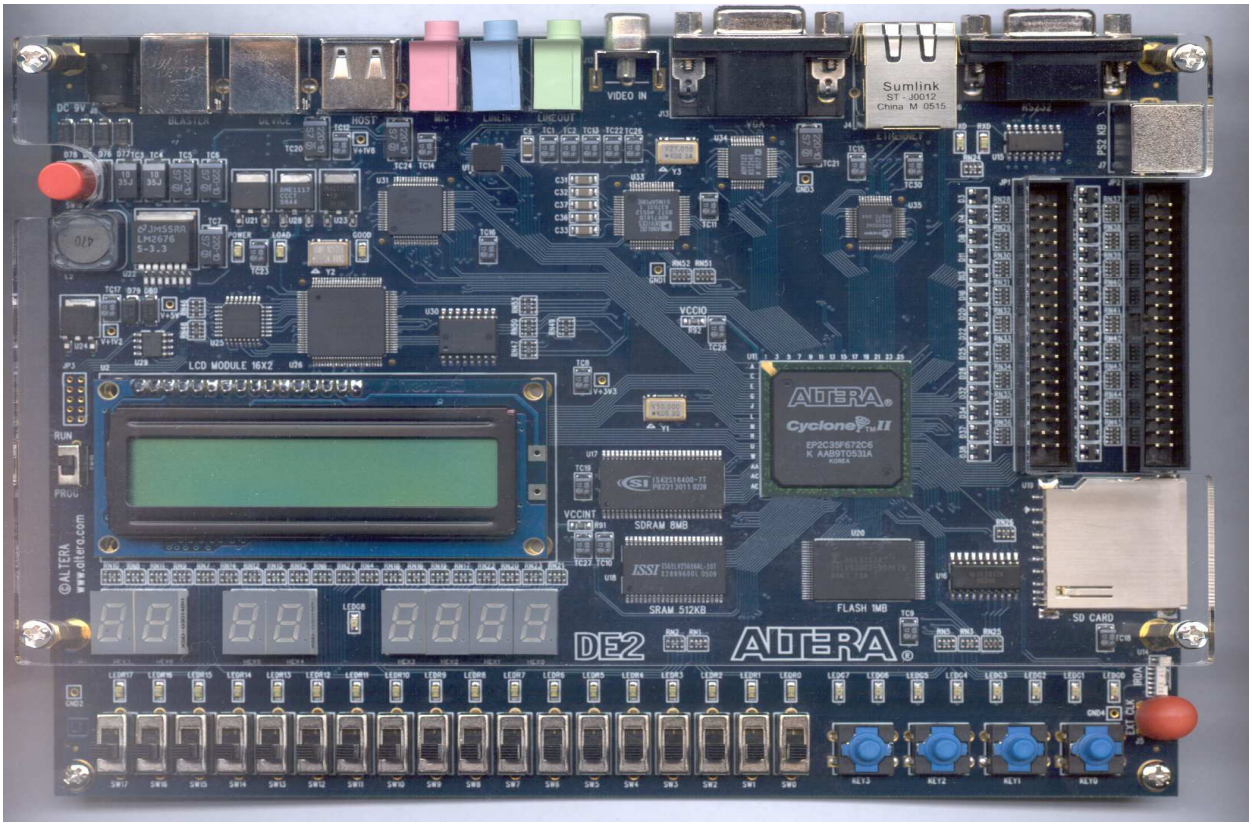


Figure 4.2: Picture of Altera DE2 board

The resources used from the FPGA board include:

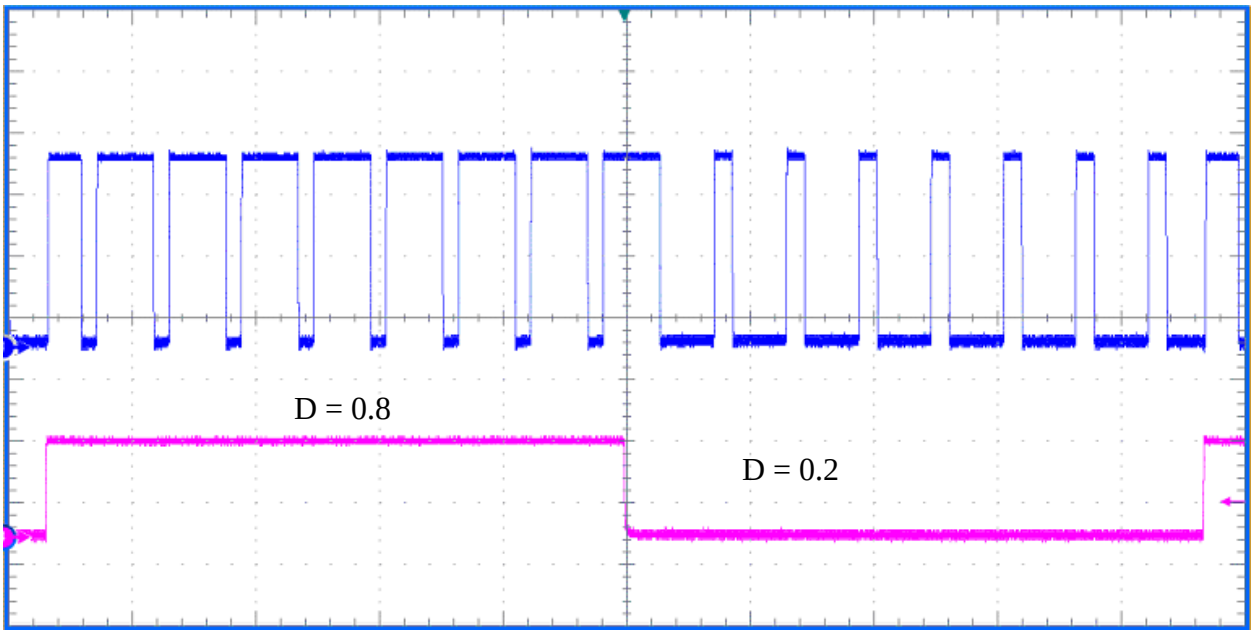
- 50 MHZ clock source
- Expansion header
- Phase lock loop (PLLs)
- Switches
- Other circuitry

Quartus is the software that supports the Altera DE2 board. The program is written in hardware descriptive language (HDL) and is compiled. At the end of compilation process, the quartus creates a SRAM (Static Random Access Memory) object file (SOF). This SOF file is downloaded to the DE2 board via joint test action group (JTAG) programming mode [39].

4.4 Open loop results

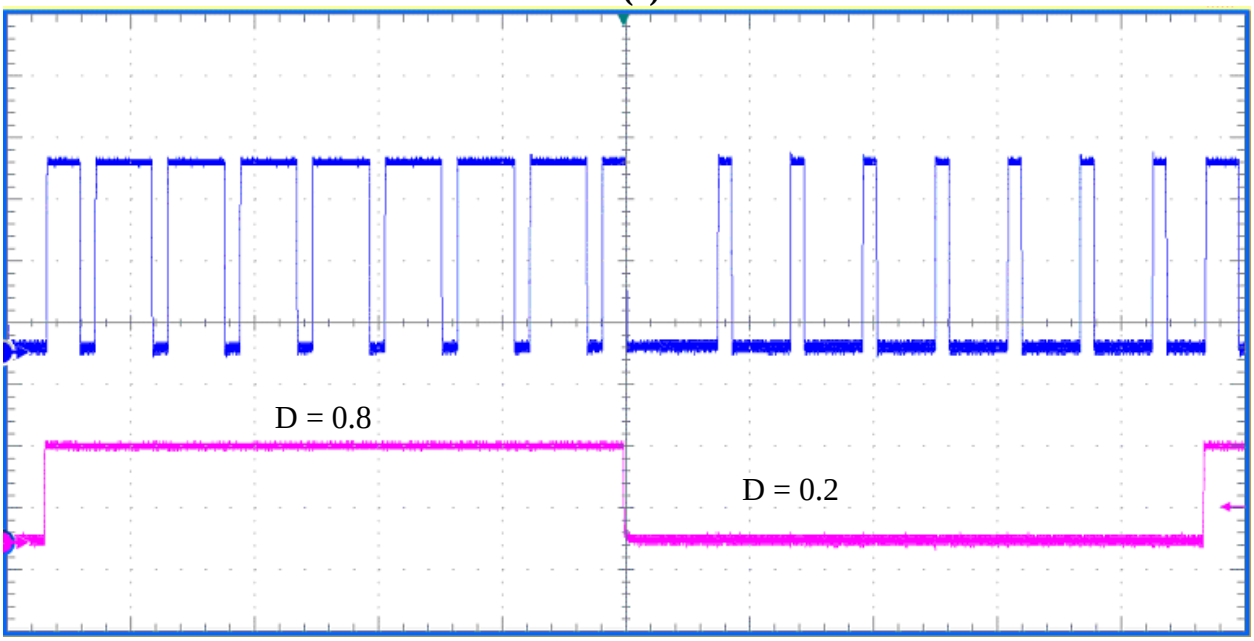
The open loop experiments are conducted by providing a duty cycle that switches between two constant values. The duty cycle transients occur in the FPGA, using a counter that switches between two constant values periodically. The open loop experiment does not have a compensator. The main reason for performing the open loop experiments is to verify the operation of the proposed modified digital pulse width modulation. The program is written in verilog and downloaded to the Altera FPGA board. The waveforms are recorded using Tektronix DPO7104 oscilloscope. Figure 4.3 and 4.4 shows the reduction of turn off delay while Figure 4.5 and 4.6 shows the reduction of turn on delay. In Figure 4.3 and 4.4, part (a) is the conventional leading-edge DPWM and part (b) is the proposed MDPWM. In each figure, the top trace is the DPWM or MDPWM output of the modulator and the bottom trace represents an indication of the duty cycle change/transient from 0.8 to 0.2 and vice versa (logic high for 0.8 and logic low for 0.2).

Figure 4.3 shows a zoom out view of several switching cycle during duty cycle step down of 0.8 to 0.2 for both conventional leading edge and MDPWM. It can be observed that the conventional leading edge and proposed digital pulse modulator have no turn on delay.



Horizontal axis: time, scale: 5µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

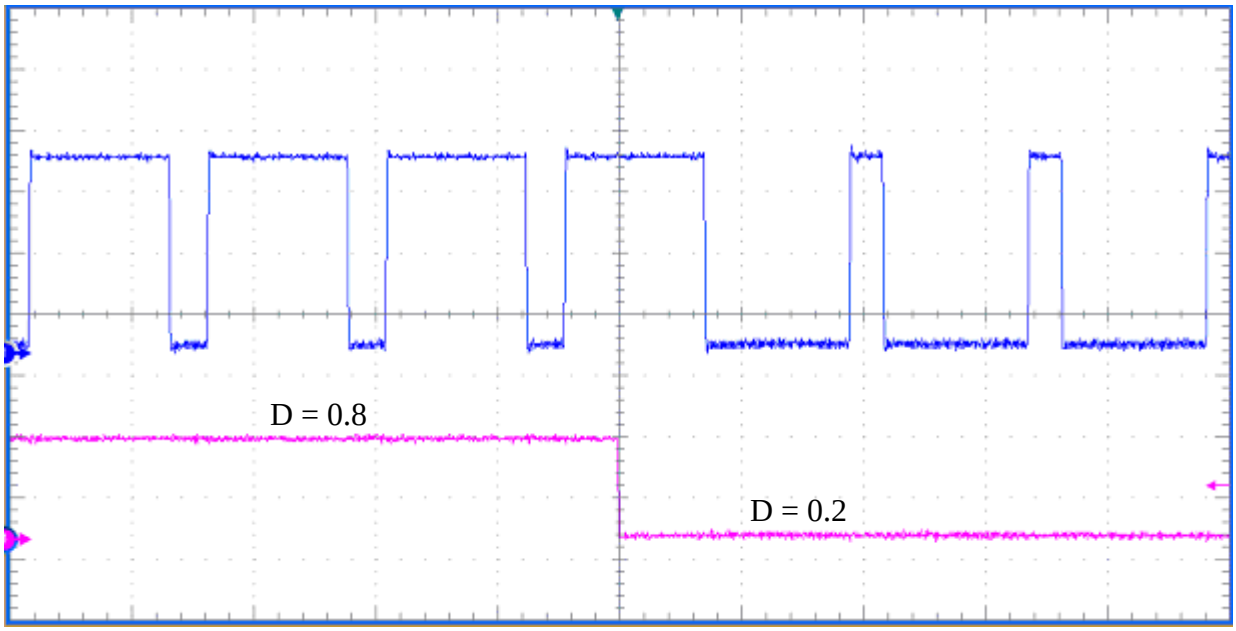
(a)



Horizontal axis: time, scale: 5µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

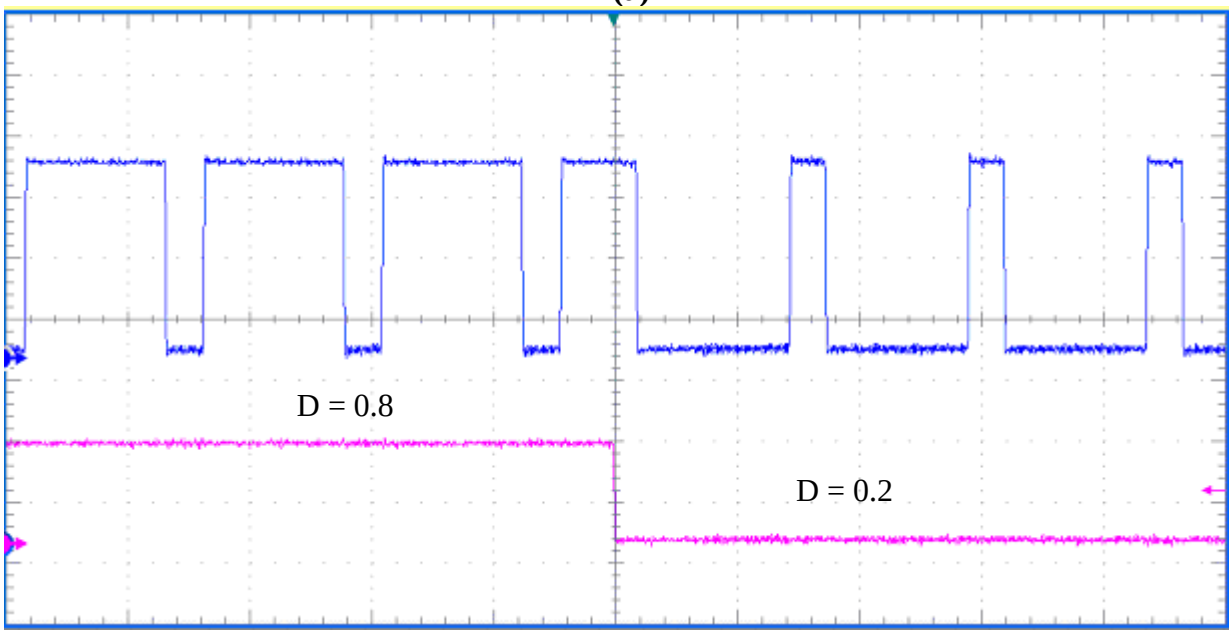
(b)

Figure 4.3: Several switching cycles view during duty cycle step-down from 0.8 to 0.2: (a)Conventional leading-edge DPWM (b) Proposed MDPWM.



Horizontal axis: time, scale: 2µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

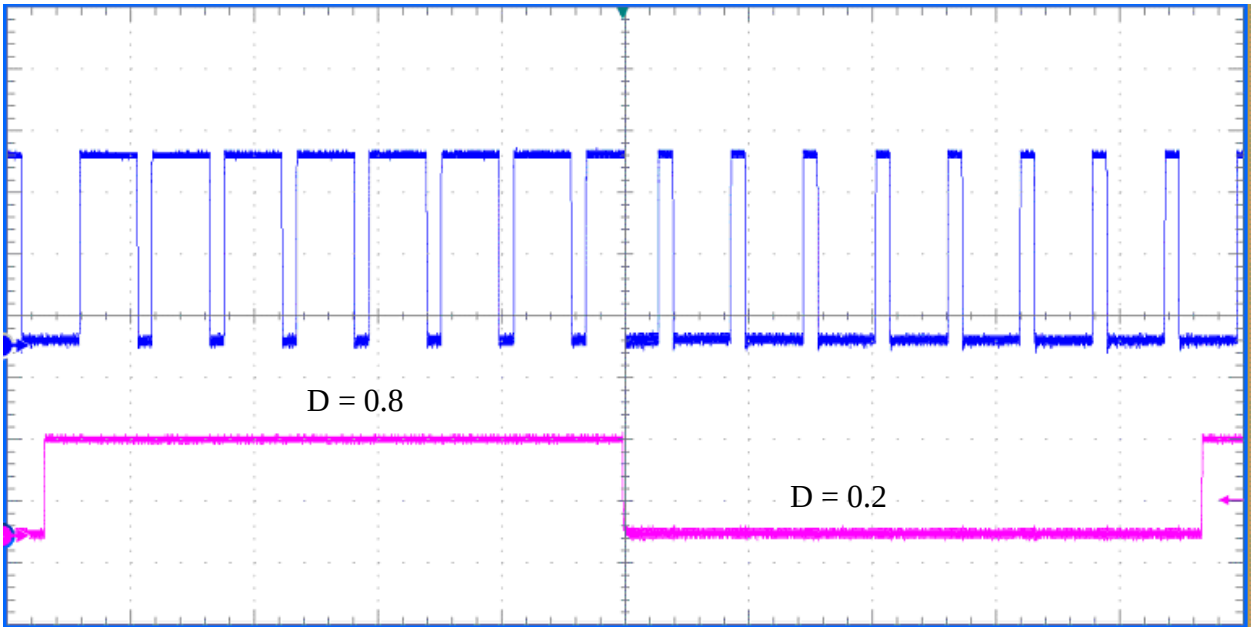
(a)



Horizontal axis: time, scale: 2µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

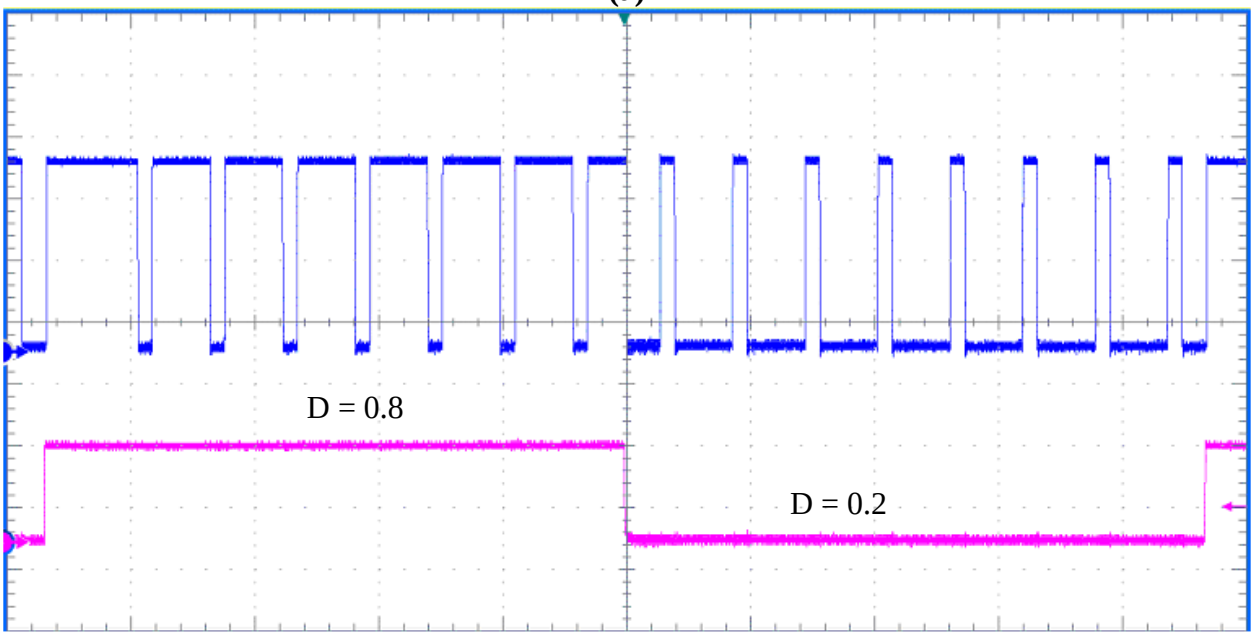
(b)

Figure 4.4: Zoomed view during step-down of duty cycle from 0.8 to 0.2. (a) Conventional leading-edge DPWM (b) Proposed MDPWM.



Horizontal axis: time, scale: 5µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

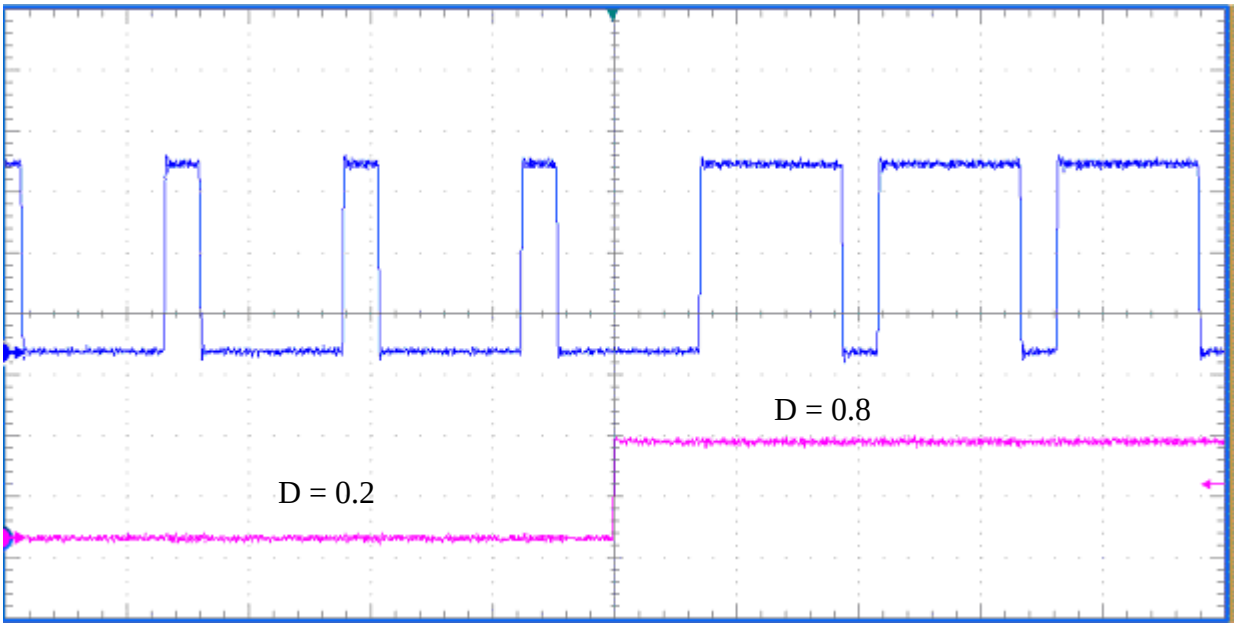
(a)



Horizontal axis: time, scale: 5µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

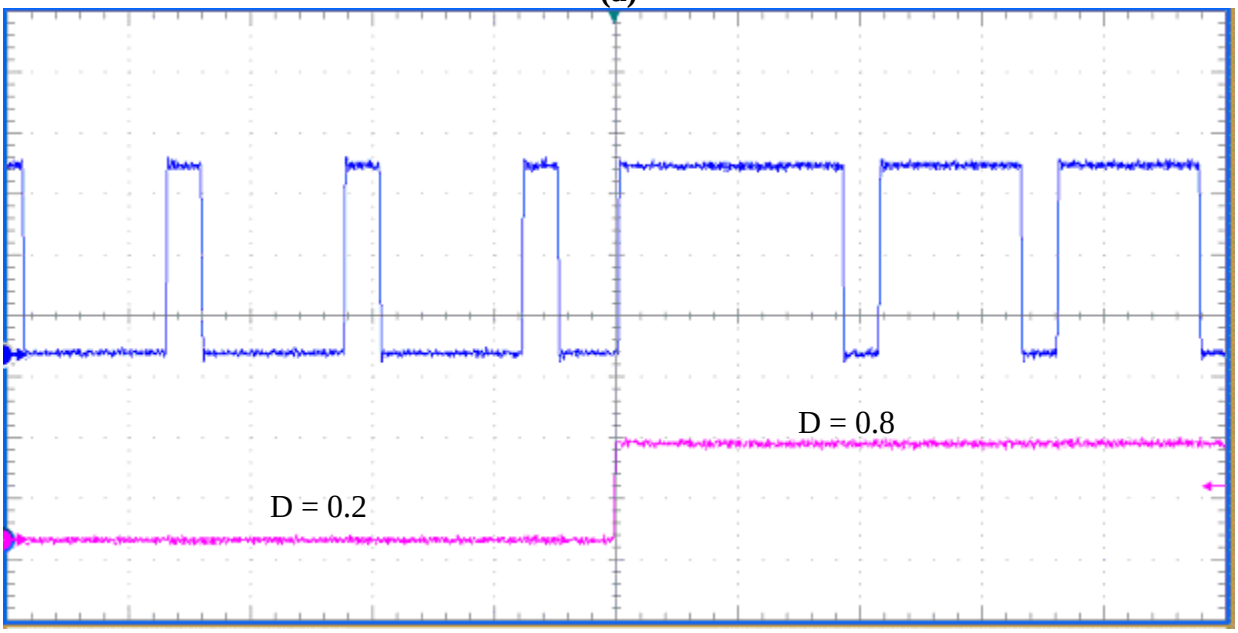
(b)

Figure 4.5: Several switching cycles view during duty cycle step-up from 0.2 to 0.8. (a) Conventional trailing-edge DPWM (b) Proposed MDPWM.



Horizontal axis: time, scale: 2µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

(a)



Horizontal axis: time, scale: 2µs/div.
Vertical axis: voltage, top trace: DPWM, scale: 1V/div.,
bottom trace: Duty Cycle Change Indication Signal, scale: 2V/div.

(b)

Figure 4.6: Zoomed view during step-up of duty cycle from 0.2 to 0.8.
(a) Conventional trailing-edge DPWM (b) Proposed MDPWM.

In Figure 4.4, the zoomed in view of the transient event from 0.8 to 0.2 duty cycle is shown. In the zoomed in view the duty cycle value is changed from 0.8 to 0.2 in the middle of the switching cycle when the DPWM is on, the auxiliary counter responds to the change and resets the DPWM. Therefore the turn off delay is reduced. In Figure 4.5 and 4.6, part (a) is the conventional trailing-edge DPWM and part (b) is the proposed MDPWM. In each Figure, the top trace is the DPWM or MDPWM output of the modulator and the bottom trace represents an indication of the duty cycle change/transient from 0.2 to 0.8 and vice versa (logic high for 0.8 and logic low for 0.2). Figure 4.5 and 4.6 verifies the reduction of turn on delay. Figure 4.5 shows the zoom out view of several switching cycles during duty cycle step up of 0.2 to 0.8 for both conventional trailing-edge and MDPWM. To reduce the turn on delay, the transient is made to occur when the DPWM is off so that early turn on action is verified. It can be observed that conventional trailing edge and proposed modulation have no turn off delay.

In Figure 4.6 the zoomed view of the transient event from 0.2 to 0.8 duty cycle are shown. In the zoomed view the duty cycle value is changed from 0.2 to 0.8 in the middle of the switching cycle, the auxiliary counter responds to the change by setting the DPWM to logic high. Therefore the turn on delay is reduced.

4.5 Closed- loop results

The closed- loop results of the conventional DPWM and proposed MDPWM are presented in this section. The output of the ADC serves as input to the program (quartus software). The supply range of the ADC is 3.3V and the conversion ranges, from 1V to 3V. The program is coded in verilog and downloaded to the Altera DE2 board. The connectors are used to connect the FPGA board and power converter board. The connector signals are

- Driver signals for power switches

- Clock signals
- Load control signal
- Signals from ADC
- Signals to DAC
- Power supply
- Ground connections

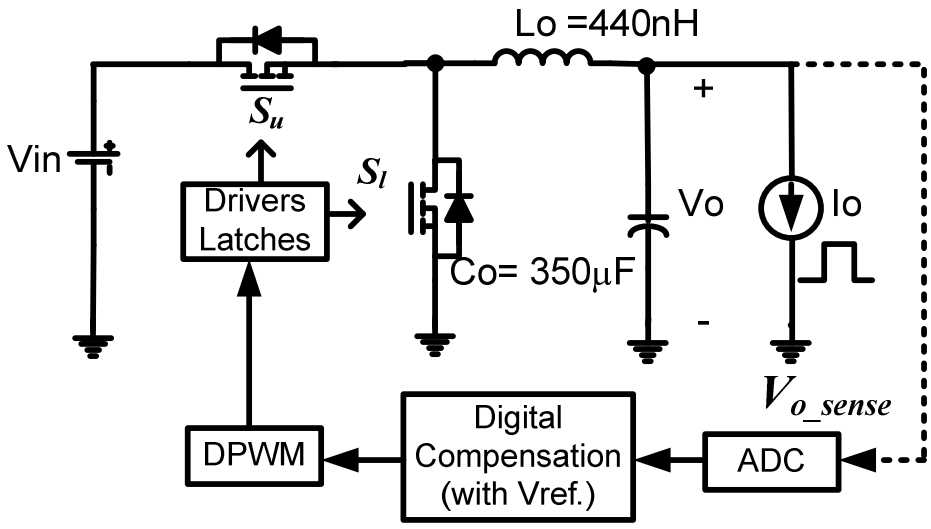
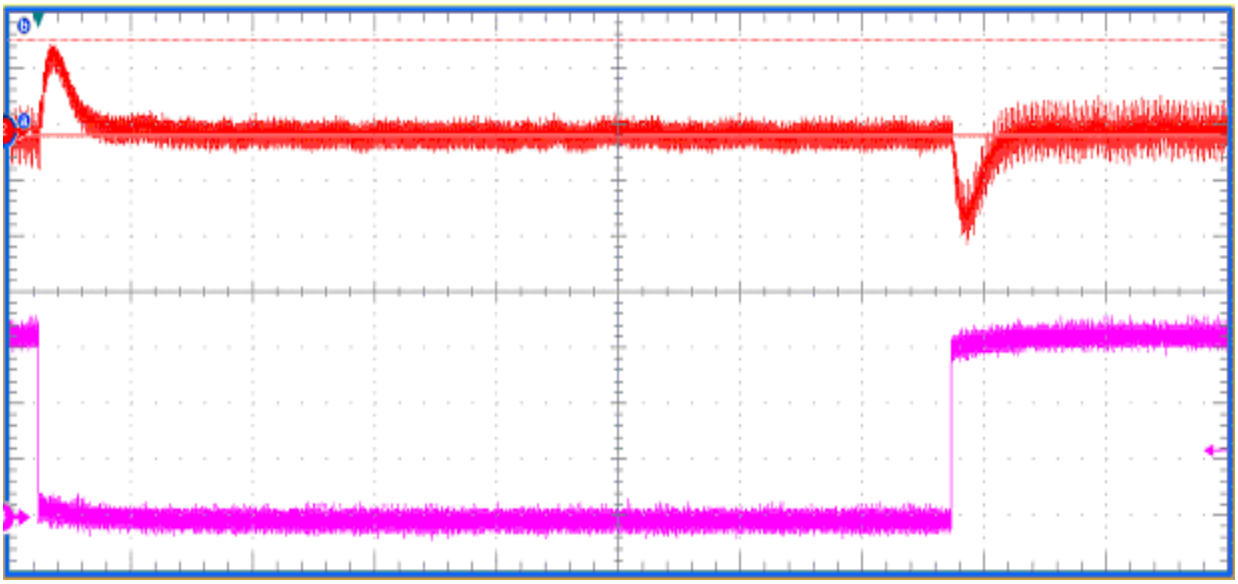


Figure 4.7: Schematic circuit diagram of buck converter

The experimental prototype has been realized with the following parameters: V_{in} = 9-12V, V_o=1.5V, L= 440nH, C= 350μF, F_{sw} ~ 342 KHz, F_{clock} = 350 MHz n $_{ADC}$ = 7 bits to sample output voltage.

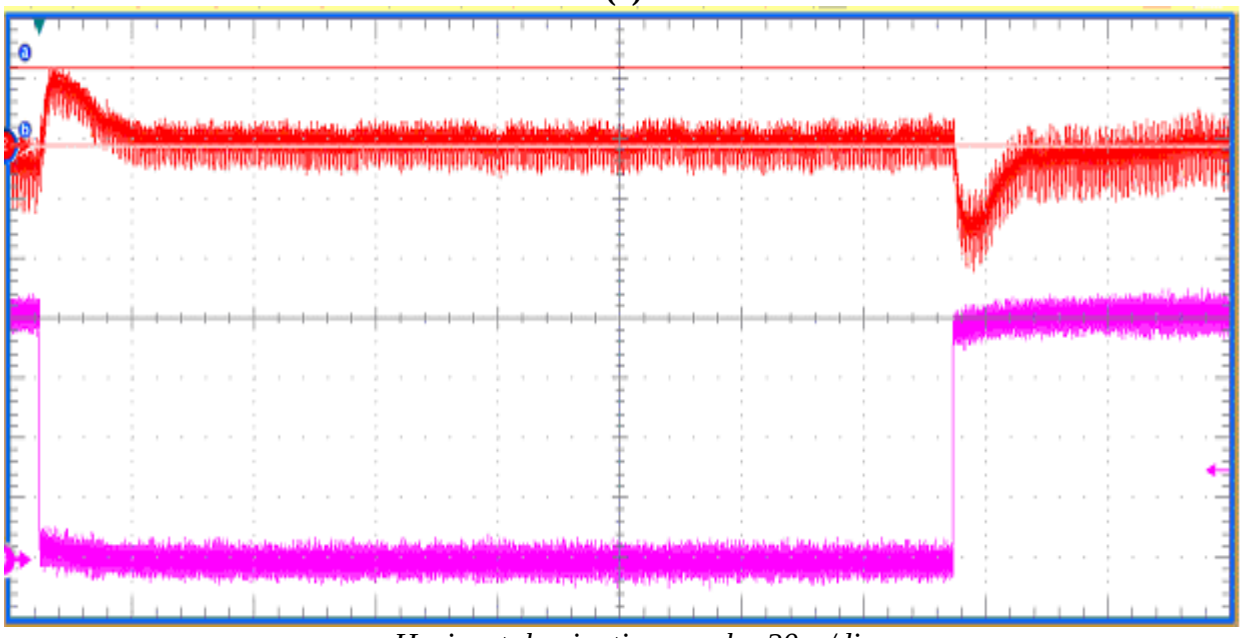
The compensator calculates the duty cycle value. The input to the compensator is the output of the Analog to Digital Converter (ADC). 7 bits of the ADC are used for calculating duty cycle. The schematic circuit diagram of the buck converter with its specification is shown in Figure 4.7. The load is applied externally using the DC load Chroma 6312.

The program is coded in verilog and downloaded to the Altera DE2 board using the programming cable. The duty cycle is limited in the code for safety purpose of the power stage.



Horizontal axis: time, scale: 20ns/div.
Vertical axis: voltage, Top trace: Output voltage, scale: 90mV/div.,
Bottom trace: Load current transient Indication Signal, scale: 1V/div.

(a)



Horizontal axis: time, scale: 20ns/div.
Vertical axis: voltage, Top trace: Output voltage, scale: 90mV/div.,
Bottom trace: Load current transient Indication Signal, scale: 1V/div.

(b)

Figure 4.8: Closed-loop experimental results (a) Conventional DPWM (b) Proposed MDPWM.

The signals to be noticed in oscilloscope are output voltage and the load current transient indication signal. The preliminary closed-loop experimental results of both the conventional and the proposed MDPWM are presented in Figure 4.8. The peak to peak voltage of the conventional leading edge DPWM is 153mV and proposed DPWM is 116mV. Therefore, for this design example the dynamic output voltage deviation is reduced by about 24%. Different design cases may lead to different levels of improvement.

It should be mentioned here that the improvement achieved by using the MDPWM comes at the expense of added control logic circuitry. The size of the added circuitry may be negligible compared to the otherwise needed additional output capacitance, it is very small compared to the power stage size, and it becomes even more negligible in higher power applications. Moreover, the additional power loss of this added circuitry becomes a smaller percentage of the total power loss as the power level of the converter increases and when newer digital logic technologies are used.

CHAPTER 5

SUMMARY AND FUTURE SCOPE

In recent years, digital control has obtained more attention in power electronic applications because of its advantages when compared to analog control, which include the ability of digital controllers to perform more advanced and sophisticated functions that potentially result in improving power conversion efficiency and/or dynamic performance of the power converter, ease of digital control function and loop upgradeability (or revision), and reduced sensitivity to components variations. However, there are also some challenges in digital control such as control loop delays that impact the dynamic performance of the power converters and the additional controller power consumption in some digital control implementations.

When the demand for power increases, the cost for maintaining voltage also increases. When the load withdraws high dynamic current with high slew rate, the voltage regulator cannot respond to the fast transient event. Therefore, the voltage regulator must be designed in order to meet all these demands. The output voltage needs to be settled fast under each transient response within the acceptable overshoot/undershoot. Delay in settling the output voltage may be compensated by adding capacitors. But adding the capacitor will increase the cost and size. Therefore, the voltage regulator should be designed to minimize the delay.

Chapter 1 presents a brief introduction about the pulse width modulation technique and various implementations. The reviews of analog and digital control were also presented. Figures 1.9, 1.10, 1.11, 1.12 explain the operation of various conventional modulation techniques and discuss the delay caused by it. Chapter 1 also gives a brief outline of this thesis work.

Chapter 2 discusses the need for new digital pulse width modulation technique for digital power converters. Under transient current events, when the load increases or decreases, the control signal increases or decreases the on time of the DPWM signal in order to maintain the output voltage. It discusses the relation between the control signal and its effect on the output voltage. The proposed digital pulse modulation scheme and its operational waveform are explained in Chapter 2.

The proposed modulation techniques reduce both the turn on and turn off delays. Figure 2.1 and 2.2 shows the block diagram and the operational waveforms of the proposed digital pulse width modulation technique. This proposed technique implementation is not constrained to counter based DPWM, it can also be implemented using delay line based DPWM. In this work the block diagram of proposed modulation using delay line is shown in Figure 2.3. Future work includes implementation and evaluation of delay line based proposed digital pulse width modulation technique.

The open loop and closed-loop simulation results are presented in Chapter 3. The closed-loop simulation model of the buck converter is shown in Figure 3.3. The simulation results shows reduction in dynamic deviation of the output voltage. Experimental results are presented in Chapter 4.

The experimental set up consists mainly of Altera DE 2 board, DC-DC buck power converter, power source, DC load and computer. Figure 4.1 shows the experimental set up block diagram. The FPGA program is written in verilog and is downloaded to the buck converter. For the open loop experiments a counter is used to obtain the load current transient action as discussed in Chapter 4. The close loop results are presented in Figure 4.7. A 24% reduction in the output voltage dynamic deviation is observed. These improvements are calculated using ac values.

The scope of future work will also include the implementation and evaluation of the proposed digital pulse width modulation technique in reducing the turn on delay caused by the conventional trailing edge modulation.

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