USER'S MANUAL

ELPIDA

New Features of DDR3 SDRAM

Document No. E1503E10 (Ver.1.0)
Date Published March 2009 (K) Japan
URL: http://www.elpida.com

INTRODUCTION

Readers

This manual is intended for users who design application systems using double data rate 3 synchronous DRAM (DDR3 SDRAM). Readers of this manual are required to have general knowledge in the fields of electrical engineering, logic circuits, as well as detailed knowledge of the functions and usage of conventional synchronous DRAM (SDRAM), double data rate synchronous DRAM (DDR SDRAM), and double data rate 2 synchronous DRAM (DDR2 SDRAM).

Explanatory Notes

Caution: Information requiring particular attention

Note: Footnote for items marked with Note in the text

Remarks: Supplementary information

Related Documents

Related documents indicated in this manual may include preliminary versions, but they may not be explicitly marked as preliminary.

Document Name	Document No.
HOW TO USE SDRAM USER'S MANUAL	E0123N
HOW TO USE DDR SDRAM USER'S MANUAL	E0234E
HOW TO USE DDR2 SDRAM USER'S MANUAL	E0437E

Notice

This document is intended to give users understanding of basic functions and usage of DDR3 SDRAM. Descriptions in this document are provided only for illustrative purpose in semiconductor product operation and application examples. And numerical values are not guaranteed values. For details about the functions of individual products, refer to the corresponding data sheet. The incorporation of these information in the design of the customer's equipment shall be done under the full responsibility of the customer. Elpida Memory, Inc. assumes no responsibility for any losses incurred by customers or third parties arising from the use of these information.

CONTENTS

CHAPTER 1 FEATURES OF DDR3 SDRAM (COMPARISON OF MAIN SPECIFICATIONS OF DDR, DDR2 AND DDR3)

DDR3 SDRAM has employed several new technologies for high-speed operation while inheriting the DDR2 SDRAM architecture.

Table 1-1 Comparison of Main Specifications of DDR, DDR2 and DDR3

Item	DDR	DDR2	DDR3
Data rate/pin CLK frequency	200/266/333/400 Mbps (100/133/166/200 MHz)	400/533/667/800 Mbps (200/266/333/400 MHz)	800/1066/1333/1600 Mbps (400/533/667/800 MHz)
Power supply (VDD/VDDQ)	2.5 ± 0.2 V	1.8 ± 0.1 V	1.5 ± 0.075 V
Interface	SSTL_2	SSTL_18	SSTL_15
Number of banks	4	4 or 8	8
Prefetch	2 bits	4 bits	8 bits
Burst length	2/4/8	4/8	4 (burst chop)/8
Posted CAS, Additive latency	No	Yes (AL = 0/1/2/3/4/5)	Yes (AL = 0/CL - 1/CL - 2)
RL, WL	RL = CL (no AL)	RL = AL + CL	RL = AL + CL
	WL = 1	WL = RL - 1 = AL + CL - 1	WL = AL + CWL
ZQ pin	N/A	N/A	Available. For ZQ calib.*[1]
/Reset pin	N/A	N/A	Available*[3]
DQ driver impedance (Ron)	Programmable	Programmable	Programmable
DQ driver calibration	N/A	For OCD calib.*[2]	For ZQ calib.*[1]
ODT function	N/A	Available	Available
ODT calibration	N/A	N/A	For ZQ calib.*[1]
Dynamic ODT	N/A	N/A	Available*[4]
CLK-DQS de-skew mechanism	N/A	N/A	Available (Write leveling, Read leveling)*[5]
Package	TSOP II	FBGA	FBGA

Notes: 1. ZQ Calibration: Calibrates DRAM ODT and Ron fluctuations with PVT (process, voltage, and temperature). External resistor (240Ω±1%) is inserted between DRAM ZQ pin and GND for reference. To perform ZQ calibration, ZQCL or ZQCS command is used. (This is a self-calibration in which DDR3 performs all the measurement and adjustment automatically.)

2. OCD (Off Chip Driver Calibration): Calibrates DRAM Ron fluctuation with PVT. The external device connected to DRAM performs impedance measurement and adjustment (not self-calibration). OCD is an optional feature in DDR2.
3. /RESET pin is introduced in DDR3 for system stability. /RESET is an active-low signal.
4. Dynamic ODT: ODT value during WRITE can be changed dynamically by enabling the dynamic ODT mode in advance by MRS command. As a result, signal quality is improved.
5. DDR3 DIMM uses fly-by topology for CMD/ADD/CLK signals to improve signal quality. This causes flight time difference between DQ/DM/DQS and CMD/ADD/CLK. DDR3 has de-skew mechanism to compensate flight time difference.

1.1 Main Features

1.1.1 Clock Frequency, Data Rate, Power Voltage and Interface

DDR3 SDRAM achieves high-speed operation about twice of that of DDR2 SDRAM, but suppresses the increase in power consumption by using a voltage of 1.5 V for the power supply and interface.

1.1.2 Number of Banks

DDR3 SDRAM has eight banks, which allows more efficient bank interleave access than that in the case of four banks.

1.1.3 Prefetch, Burst Length and tCCD

DDR3 SDRAM employs the 8-bit prefetch architecture for high-speed operation though DDR2 SDRAM employs 4-bit prefetch architecture. The bus width of the DRAM core has been made eight times wider than the I/O bus width, which enables the operating frequency of the DRAM core to be 1/8 of the data rate of the I/O interface section.

READ operation: Converts 8-bit data read in parallel from the DRAM core to serial data, and outputs it from the I/O pin in synchronization with the clock (at double data rate).

WRITE operation: Converts serial data that is input from the I/O pin in synchronization with the clock (at double data rate) to parallel data, and writes it to the DRAM core as 8-bit data.

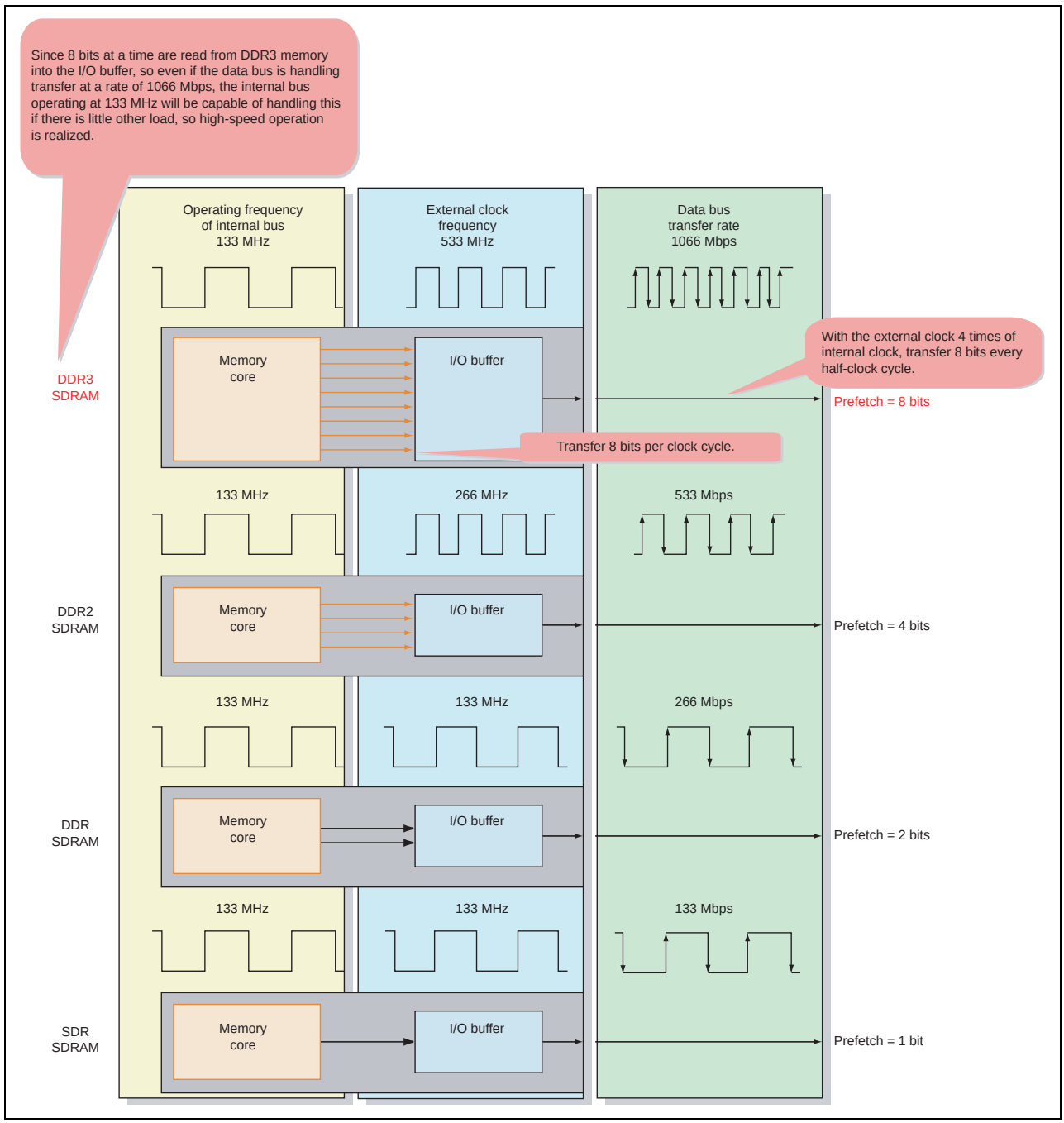

Figure 1-1 Comparison of DDR3 SDRAM, DDR2 SDRAM, DDR SDRAM, and SDR SDRAM Operations

Because of these features, the burst length is basically eight bits, but 4-bit burst length is also supported considering the inheritance from DDR2 SDRAM. In that case, however, data is treated as if the second-half four bits are masked in an 8-bit burst length access. (This is called the burst chop 4 mode (BC4).)

The column command interval (tCCD) also becomes 4tCK in connection with the 8-bit prefetch.

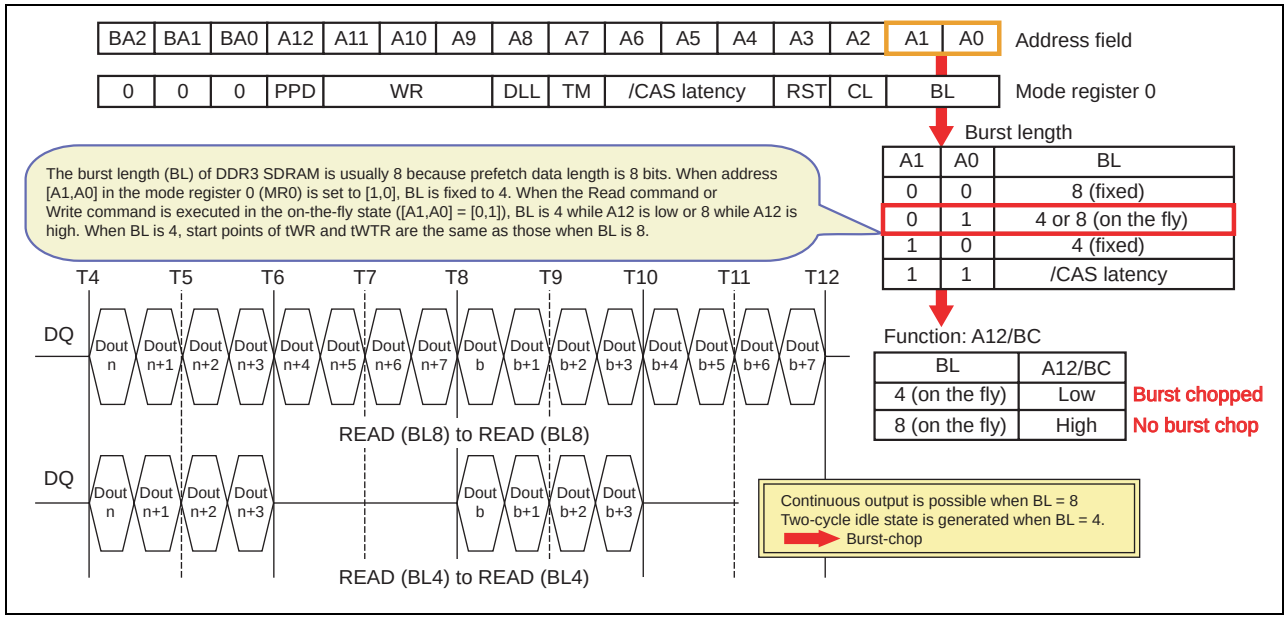

Figure 1-2 Illustration of Burst-Chop

1.1.4 Posted CAS and Additive Latency (AL)

DDR3 SDRAM also supports the posted CAS function and additive latency function.

For details of these functions, see our User's Manual HOW TO USE DDR2 SDRAM.

1.1.5 Read Latency (RL) and Write Latency (WL)

The time period from the issue of READ command to the output of the first data is called read latency (RL), and the time period from the issue of WRITE command to the input of the first data is called write latency (WL), which are shown by clock count. Definition of RL and WL is partly different between DDR2 SDRAM and DDR3 SDRAM.

Table 1-2 Differences in RL and WL between DDR2 SDRAM and DDR3 SDRAM

	DDR2 SDRAM	DDR3 SDRAM
RL (Read latency)	RL = AL + CL	RL = AL + CL
WL (Write latency)	WL = RL - 1 = AL + CL - 1	WL = AL + CWL
CL	(2), 3, 4, 5, 6	5, 6, 7, 8, 9, 10, (11)
AL	0, 1, 2, 3, 4, (5)	0, CL - 1, CL - 2
CWL	N/A	5, 6, 7, 8

[Legend]
AL: Additive latency
CL: CAS latency
CWL: CAS write latency

1.1.6 DQS (Data Strobe)

Only differential DQS is available in DDR3 SDRAM because finer timing control is required due to high data rate.

1.1.7 VREF Pin

DDR3 SDRAM separates the VREF signals for data and for command/address.

1.1.8 /RESET Pin

DDR3 SDRAM has employed the /RESET pin newly. The /RESET pin is driven low during power-on or initialization process or when a reset is required.

1.1.9 Output Driver Impedance (Ron), ODT and Calibrations

Output Driver Impedance (Ron):

– The output driver impedance (Ron) of DQ, DQS, /DQS, and DM is selectable in the same way as DDR2 SDRAM ([A5,A1] in MR1).

– Ron may fluctuate with the process, voltage, and temperature (PVT).

DDR2 SDRAM can calibrate Ron fluctuation due to PVT using the optional OCD (off-chip driver calibration) function, but DDR3 SDRAM uses the ZQ calibration function instead of the OCD function.

ODT (On Die Termination):

A termination resistor is provided in the chip to suppress signal reflection. This allows reduction in the number of external resistors and impovement in signal quality.

– ODT resistance Rtt is selectable in the same way as DDR2 SDRAM ([A9,A6,A2] in MR1, [A10,A9] in MR2)

– DDR3 SDRAM inherits the ODT function provided for DDR2 SDRAM, and provides extended ODT mode.

Synchronous ODT: ODT timing same as that of DDR2 SDRAM

Asynchoronous ODT: ODT timing in the slow exit power-down mode

Dynamic ODT: Function that can dynamically switch the ODT resistance during WRITE operation without MRS command, which impoves signal quality during WRITE operation.

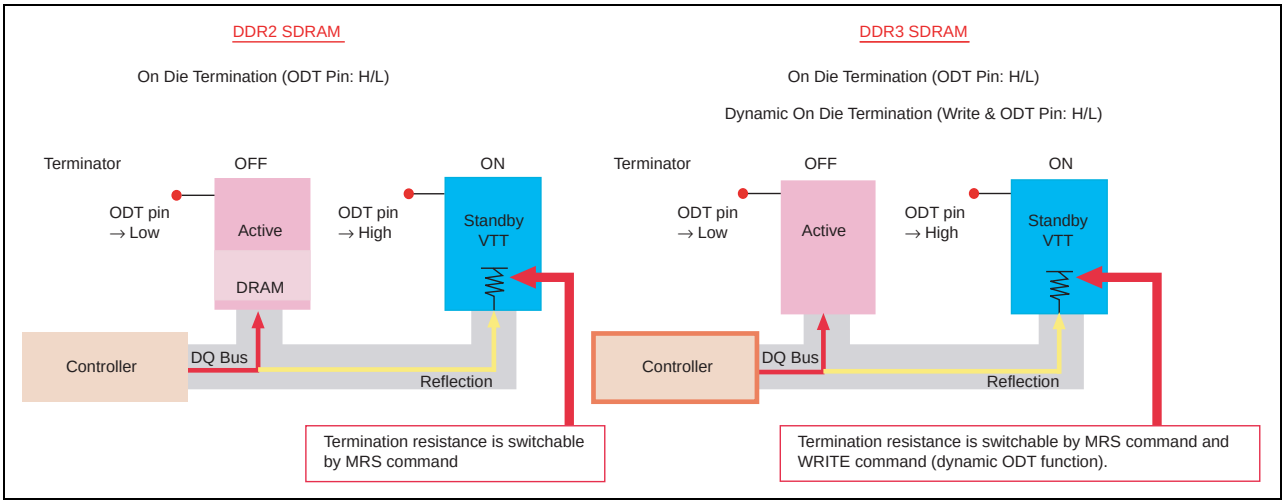

Figure 1-3 Comparison between ODT of DDR2 SDRAM and Dynamic ODT of DDR3 SDRAM

To achieve high-speed data transfer, a termination resistor is provided in DDR2 SDRAM and DDR3 SDRAM to suppress signal reflection on the bus.

Reflection of signals from each DRAM can be suppressed by controlling ON/OFF of the ODT pin (input: high/low).

DDR3 SDRAM can dynamically switch the termination resistance to improve signal quality during WRITE operation, enabling stable operation at a transfer rate of gigahertz level.

(The ODT termination resistance (RTT_Nom) and the termination resistance (RTT_WR) used for the dynamic ODT function can be set by the MRS. If the ODT pin is held high during WRITE operation with the dynamic ODT set to OFF, the value set by RTT_Nom is used for the termination resistance.)

1.1.10 ZQ Calibration

Although ODT resistance Rtt fluctuates with PVT in some cases, DDR3 SDRAM can calibrate the Rtt fluctuation due to PVT, which was not possible in DDR2 SDRAM. The ZQ calibration function is also used for Rtt calibration, as well as for Ron calibration.

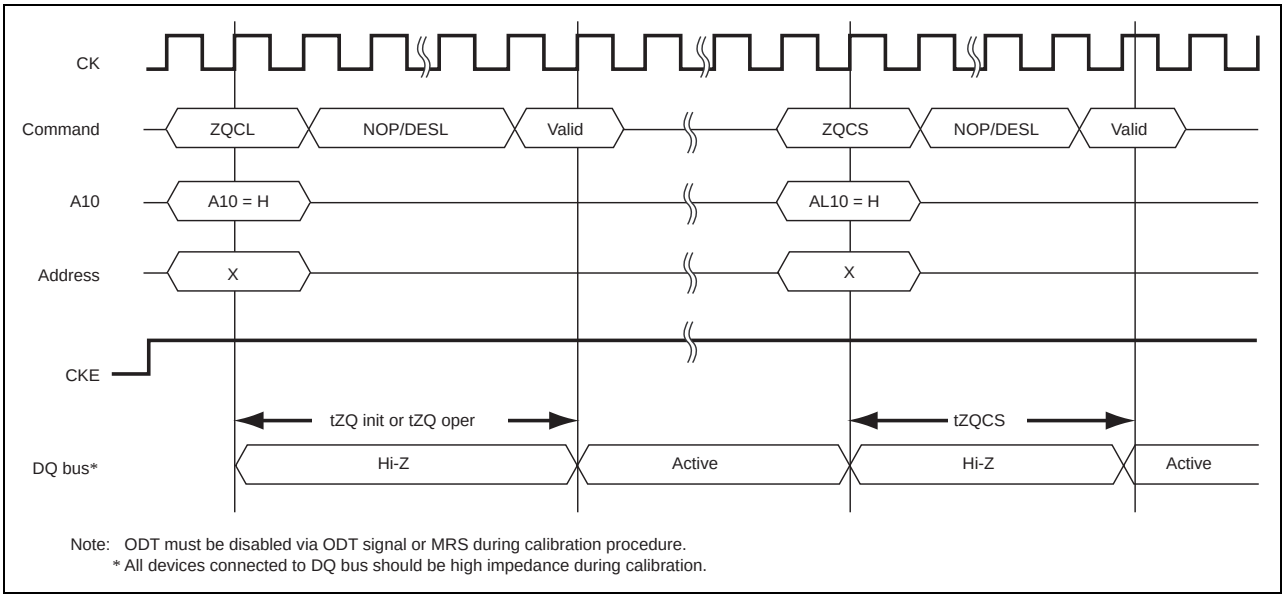

Figure 1-4 ZQ Calibration

The ZQ calibration function is essential for normal operation of DDR3. With the reference of the external resistance (240Ω ±1%) connected to the ZQ pin, DDR3 calibrates the Ron and Rtt values of the ZQ pin agaist temperature and voltage fluctuations (see figure 1-5).

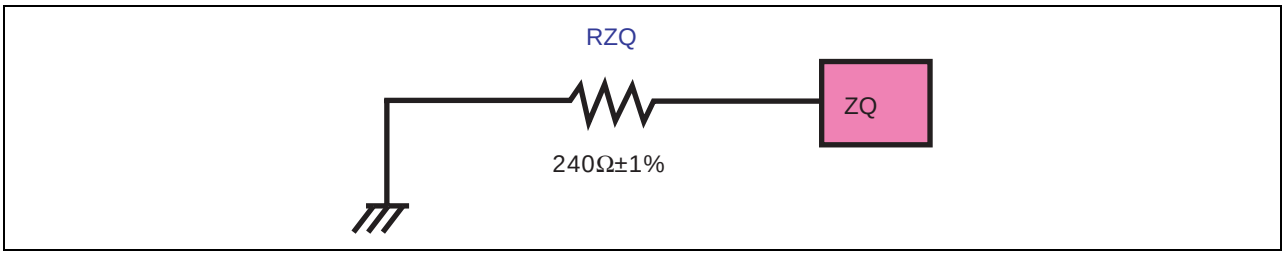

Figure 1-5 External Resistance (RZQ)

ZQ calibration commands include ZQ Calibration Long command executed during power-on and initialization processes, and ZQ Calibration Short command executed regularly during operation.

Table 1-3 ZQ Calibration Commands and their Execution Timings

Command	When to Issue
ZQCL (ZQ Calibration Long)	Power on/initialization
ZQCS (ZQ Calibration Short)	During operation

1.1.11 CLK-DQS Timing De-skew Mechanism

The DDR3 SDRAM memory module has introduced the fly-by topology (shown in figure 1-6) for the CMD, ADD and CLK signals to improve signal quality.

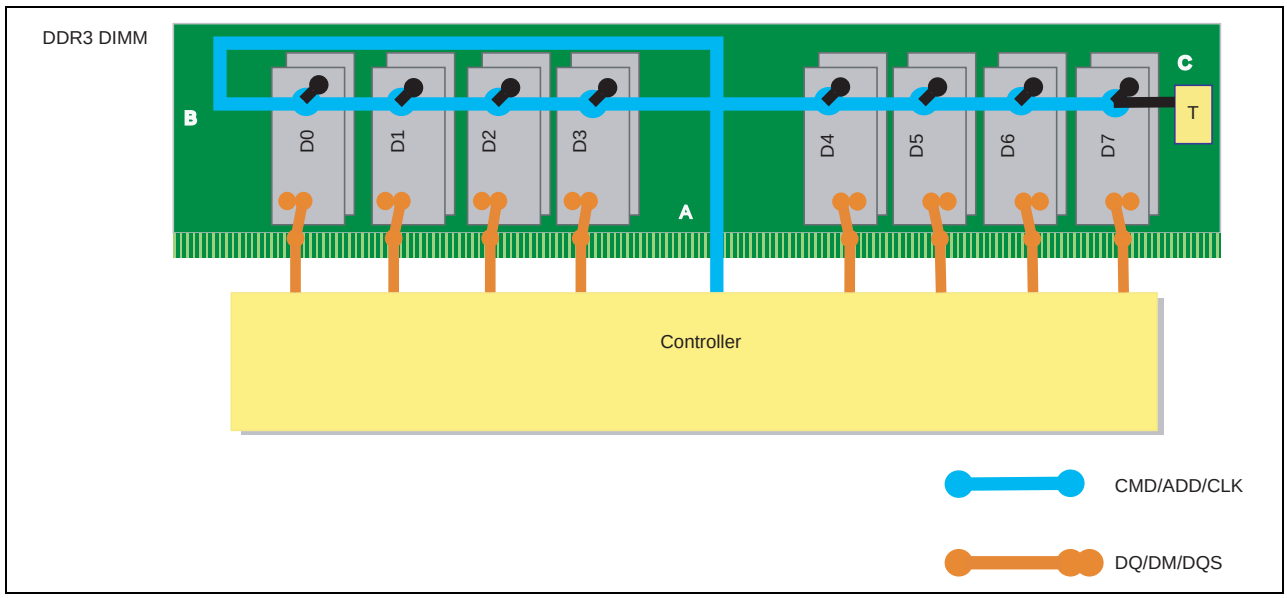

Figure 1-6 Fly-by Topology and Timing De-skew

This topology improves signal quality, but generates a difference in flight time between DQ signal and CMD/ADD/CLK signals (maximal at C in figure 1-6). Therefore, the controller must adjust the output timing of each signal. To this end, DDR3 is provided with the timing de-skew mechanism.

– Read leveling

DDR3 SDRAM outputs the predetermined data pattern. The controller adjusts the DQ/DQS capture timing using the multi purpose register (MPR).

– Write leveling

DDR3 SDRAM outputs the CLK-DQS skew information. The controller adjusts signal timings using the skew information so that the CMD, ADD, and CLK signals arrive at DDR3 at the same time as the DQ, DM, and DQS signals.

1.1.12 Write Leveling

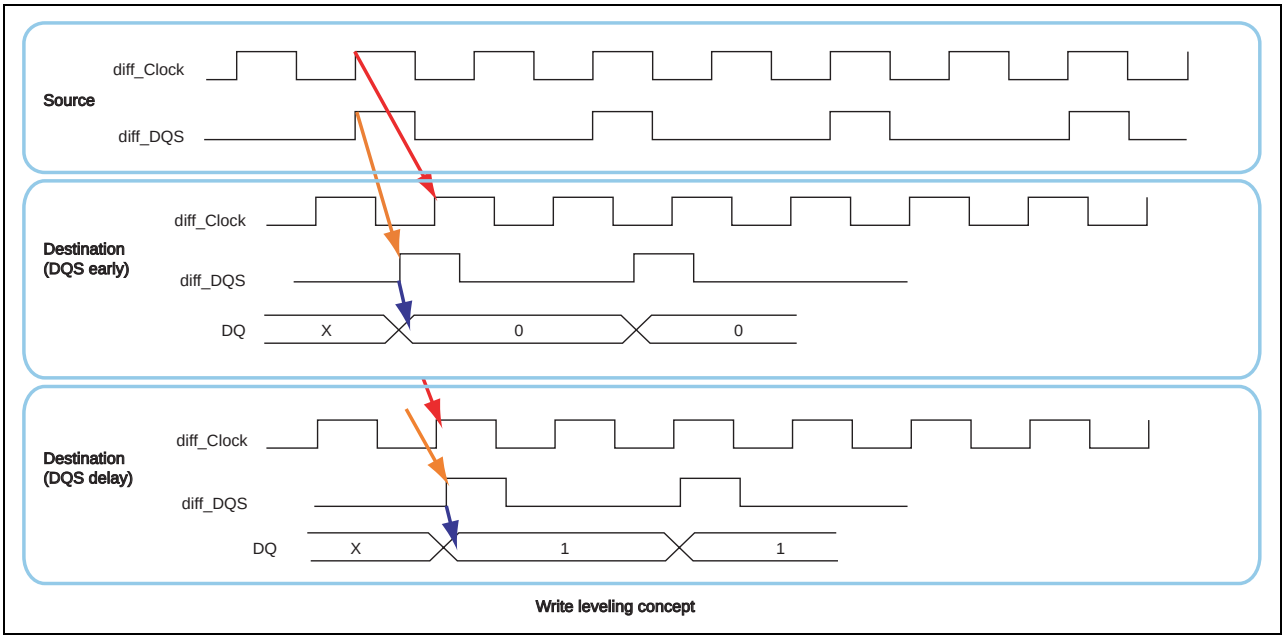

Figure 1-7 Conceptual Diagram of Write Leveling

エラー!

– Adjustment sequence

(1) Set write leveling to "enabled" in MR1 with the mode register set command.

(2) In write leveling mode, DDR3 samples the CLK signal at the rising edge of DQS and outputs the information from the DQ pin.

(3) Shift the DQS timing outputted from the controller. When CLK and DQS arrive at the destination at the same time, the DQ output changes.

[Description]

The DRAM feeds back the current status on the DQ pin (0: early, 1: late).

Based on this result, make a judgment and adjust the timing on the system side.

This function is always active while it is enabled by the setting. Therefore, disable this function after the adjustment.

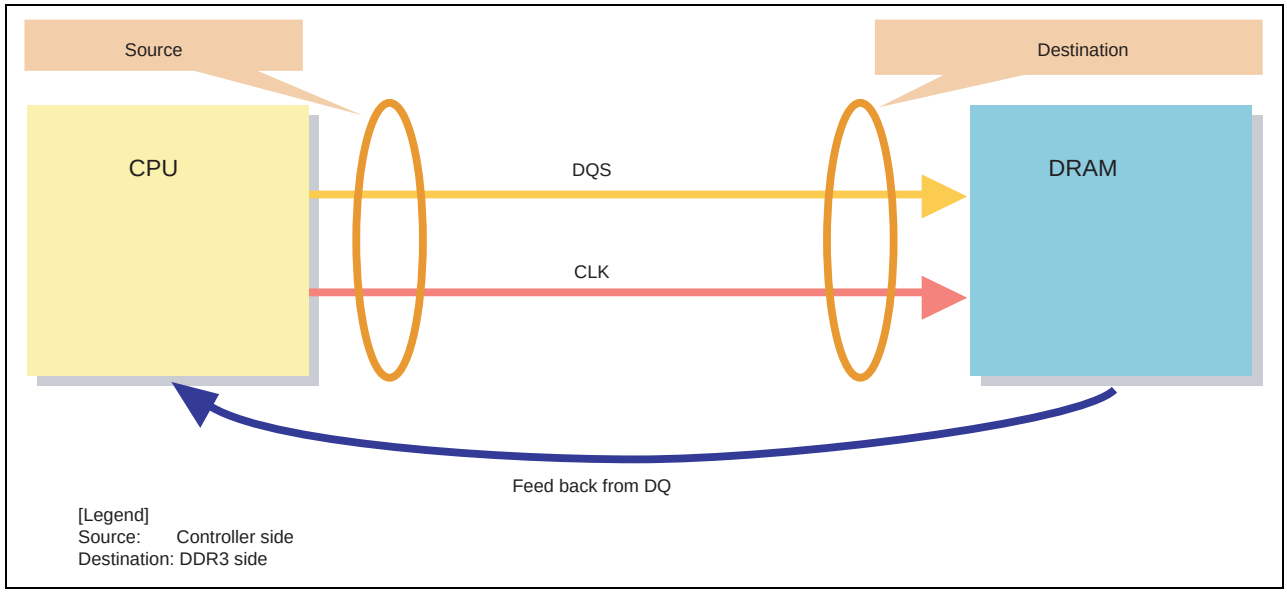

Figure 1-8 Conceptual Diagram

1.1.13 Multi Purpose Register (MPR)

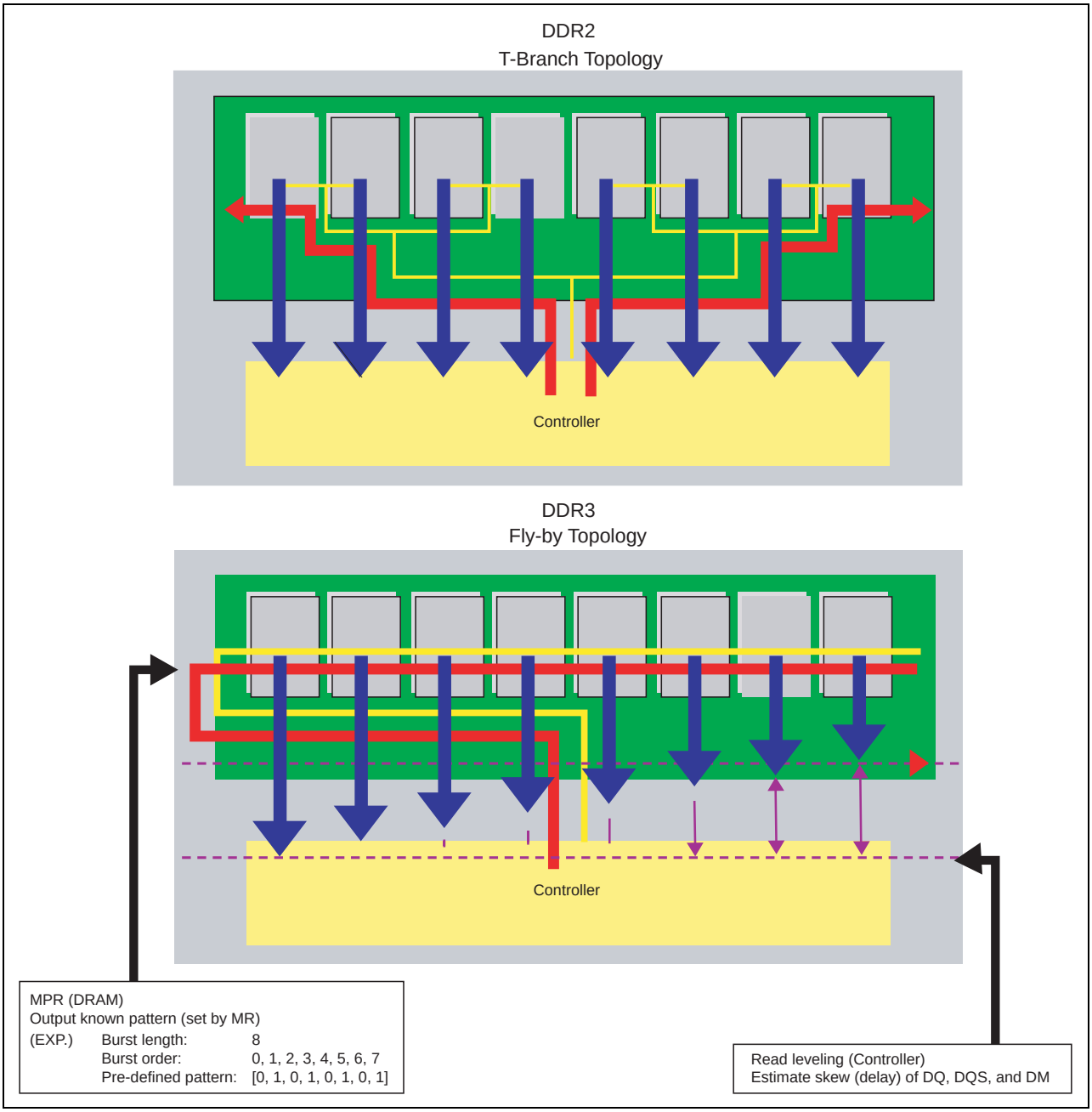

Figure 1-9 Conceptual Diagram of Multi Purpose Register (MPR)

Read leveling is a specification that adjusts the output skew from each DRAM on the controller side. Since DDR3 operates at high speed, correct data input may not be possible without timing adjustment.

In addition to the memory array, a ROM that retains specific data patterns is provided. The MPR function intended to assist the read leveling outputs data from the ROM.

The specific data patterns enable timing adjustment during READ operation.

Note: To use MPR, the controller side must be compatible with MPR.

The information in this document is current as March 2009. The information is subject to change without notice.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107