Yellowknife
Reference Platform Hardware Design Manual

Board Revision Level	**X4**
Document Revision Level	**1.0**

Registration Number:

Registration Name

1.0 Introduction

The Yellowknife (“YK”) X4 platform is a fourth-generation PowerPC/CHRP reference design. The design goals are to create a high-speed platform for use in embedded markets as well as evaluation of a MacOS licensable platform.

This document decsribes the basic architecture of the X4 version, as well as changes between the X2 and X4 platforms (which are otherwise very similar).

1.1 Features

Several features of the Yellowknife X4 platform are:

- PGA Socket allows easy installation of multiple types of PowerPC processors.
- Processor module automatically selects appropriate processor voltage selection.
- Supports two SDRAM DIMM modules up to 100 MHz.
- Supports on-board L2 (or L3) cache.
- Supports MacOS (for testing purposes only).

2.0 Functional Description

The following block diagram shows the architecture of the Yellowknife in detail.

2.1 Processor

The Power PC processor is provided on Yellowknife through a 17-by-17 PGA ZIF socket. This allows the easy installation of PowerPC 603, 604 and 750-class processor modules (the latter including the back-side L2 cache). This adapter, referred to as an “interposer”, identifies the level of voltage needed for the core of the processor (between 1.2V to 3.6V).

The socket also contains extra pins that allow it to support multiprocessing, and query an I2C ROM or encoded pattern on the interposer to access interposer configuration information.

The core frequency is set using 4 jumpers to select the proper PLL setting for a given clock frequency.

CHANGES: X4 adds compliance with the 5-bit voltage encoding standard of the second-generation interposers (X2 supported only the first generation, which had only 1 bit). Also added are access to the I2C/parallel interposer ID, and elimination of Doubletake support.

2.2 PCI Bridge/Memory Controller

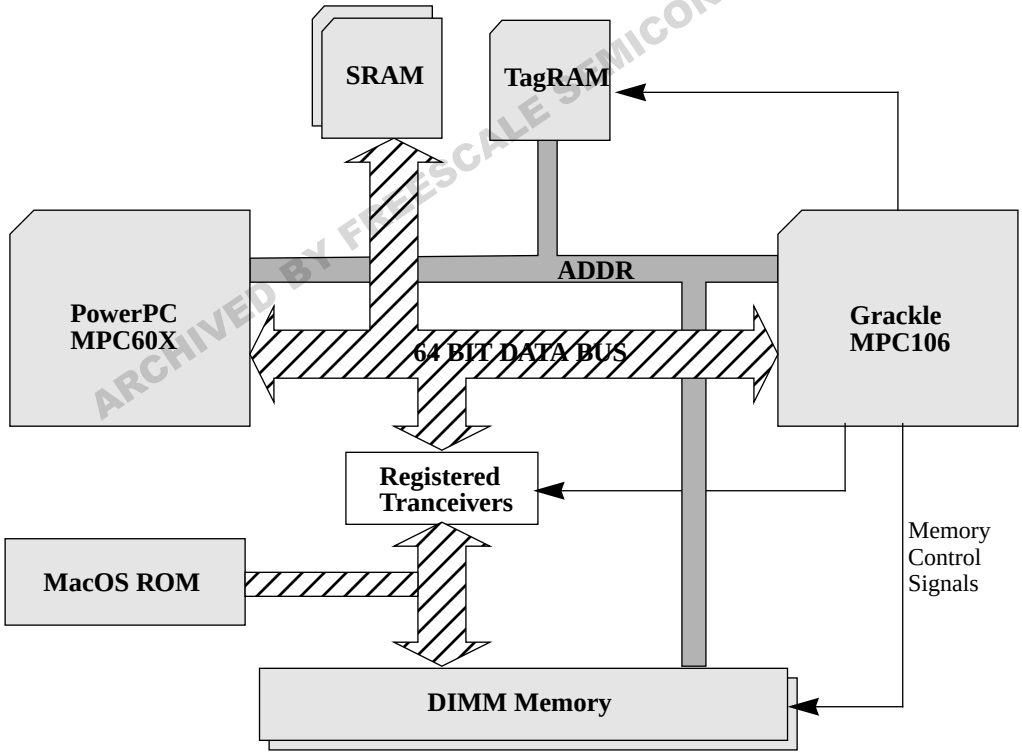
The PCI Bridge/Memory controller is the MPC106 V4, which now supports SDRAM and higher processor bus speeds. The MPC106 connects directly to the CPU bus with no additional logic required. The MPC106 responds to all CPU transactions, forwarding them to the memory controller or the PCI bus.

CHANGES: X4 replaces the automatic PLL settings with manual jumpers. This accomodates the new PCI/bus speed ratios supported by the MPC106 version 4.0. Processor bus speeds up to 100 MHz are supported.

2.3 Memory Architecture

The local bus (i.e. processor bus) is the primary interface to all of the system memory. The MPC106 serves as a memory controller for an array of SDRAM, as also as a ROM controller. The memory data bus is 64-bits wide, with additional bits optional to serve as parity checks (the MPC106 does not support ECC when using SDRAM).

FIGURE 1. Memory Architecture



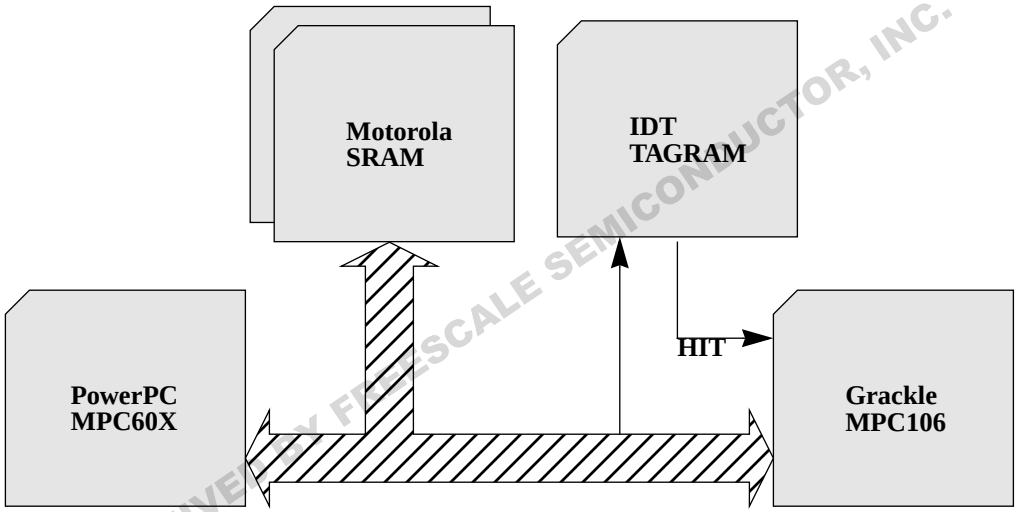
The MPC106 requires that the processor/cache data bus be separated from the DRAM array, so a 64-bit memory buffer is required. Because the memory bus may operate at very high speeds, with potentially high loading (~100 pF), registered transceivers are used. The design of the Yellowknife X4 memory system is described in great detail in application note AN17xx, “SDRAM System Design using the MPC106”.

CHANGES: X4 replaces 4 SIMM sockets (which were paired) with 2 DIMM sockets. The X4 only supports SDRAM, while X2 supported only EDO. X4 is tuned to operate at 83 MHz or above, and uses registered transceivers to accomplish this. To minimize loading at high speeds, the boot ROM has been moved to the ISA bus.

2.4 L2 Cache Memory

Cache for the YK system is provided through an on-board “TAGRAM” memory and a pair of high-speed SRAM memories. The IDT71216 provides the cache tag RAM and address comparator for the cache module. The SRAM parts are selected for the maximum speed available; if cache is desired, the SRAM parts must match the speed of the processor and SDRAM data bus.

FIGURE 2. Cache Architecture



CHANGES: X4 replaces the L2 COAST socket with on-board 100-pin TQFP SRAM. This is both cheaper and faster, allowing faster operation (83 MHz or greater). Since the cache is fixed at 512K, jumpers are no-longer needed.

2.5 Power Supply

Up to 7A of power is supplied to the processor’s core logic, using a 5-bit DAC-trimmed switching regulator. The regulator is contained on a daughter-card called the Voltage Regulator Module (VRM). Using the VID(4:0) control signals present on all second-generation modules, the appropriate voltage level for the processor is automatically selected. This voltage may range anywhere from 1.3V to 3.6V.

Uninstalled jumpers on the PCB may be installed to allow trimming the voltage for test purposes. To trim the voltage, cut the top-level trace between pins 1 and 2 and install three-position “Berg” headers at locations J45, J46, J47, J55, and J56. Once done, the following controls are possible:

Table 1: Optional VID Control

J45 VID4	J46 VID3	J47 VID2	J48 VID1	J49 VID0	Result
1-2	1-2	1-2	1-2	1-2	Interposer controls voltage settings.
out	out	out	out	out	No Interposer Installed
out	out	out	out	2-3	2.10V Core

Table 1: Optional VID Control

J45 VID4	J46 VID3	J47 VID2	J48 VID1	J49 VID0	Result
out	out	out	2-3	out	2.20V Core
out	out	out	2-3	2-3	2.30V Core
out	out	2-3	out	out	2.40V Core
out	out	2-3	out	2-3	2.50V Core
out	out	2-3	2-3	out	2.60V Core
out	out	2-3	2-3	2-3	2.70V Core
out	2-3	out	out	out	2.80V Core
out	2-3	out	out	2-3	2.90V Core
out	2-3	out	2-3	out	3.00V Core
out	2-3	out	2-3	2-3	3.10V Core
out	2-3	2-3	out	out	3.20V Core
out	2-3	2-3	out	2-3	3.30V Core
out	2-3	2-3	2-3	out	3.40V Core
out	2-3	2-3	2-3	2-3	3.50V Core
2-3	out	out	out	out	1.30V Core
2-3	out	out	out	2-3	1.35V Core
2-3	out	out	2-3	out	1.40V Core
2-3	out	out	2-3	2-3	1.45V Core
2-3	out	2-3	out	out	1.50V Core
2-3	out	2-3	out	2-3	1.55V Core
2-3	out	2-3	2-3	out	1.60V Core
2-3	out	2-3	2-3	2-3	1.65V Core
2-3	2-3	out	out	out	1.70V Core
2-3	2-3	out	out	2-3	1.75V Core
2-3	2-3	out	2-3	out	1.80V Core
2-3	2-3	out	2-3	2-3	1.85V Core
2-3	2-3	2-3	out	out	1.90V Core
2-3	2-3	2-3	out	2-3	1.95V Core
2-3	2-3	2-3	2-3	out	2.00V Core
2-3	2-3	2-3	2-3	2-3	2.05V Core

CHANGES: X4 replaces the on-board regulator with a VRM.

2.5.1 Power Key Control

Yellowknife X4 implements the MacOS compatible power control for ADB keyboards. When the power is off, a transition on the ADB_POWER* signal (to ground) controls the APC of the Super I/O, turning the system on. Once power is on, a MOSFET clamps the control signals using system power, preventing other transitions on the ADB_POWER* signal from affecting the APC. This prevents the ADB keyboard power button from turing off power before software has an opportunity to intervene.

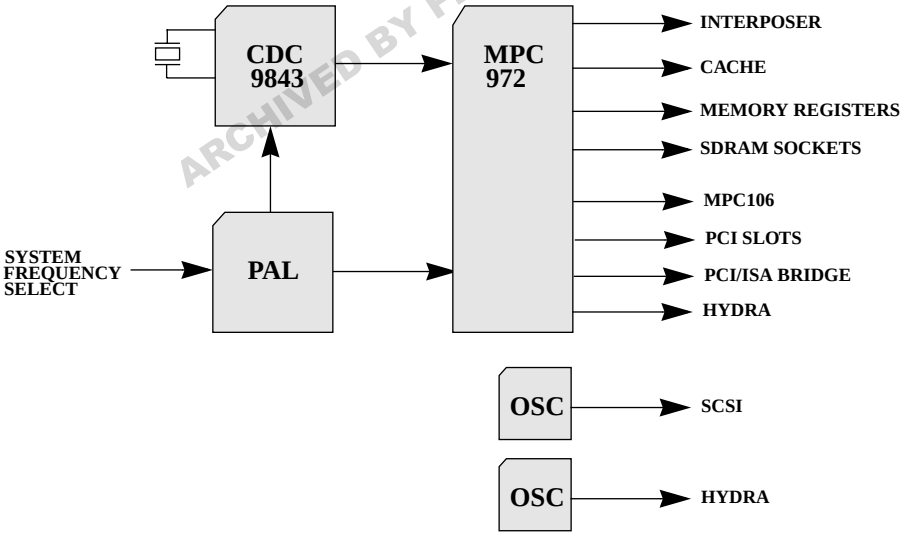
CHANGES: X4 implements the correct MacOS behavior for the ADB power key.

2.6 Clock System

Yellowknife uses two clock synthesizer IC's to create all of the clock frequencies needed. The first part is a CDC9843, an inexpensive device which uses a single 14.31818MHz crystal to synthesize a selectable system "base" clock of 50, 60, or 66 MHz. This device also generates 14.31818 MHz for ISA bus use, 24 MHz for the keyboard/mouse controller (within the Super I/O), and 48 MHz which is used to operate the MESH SCSI within the Hydra device. Although this devices also generates many 1X/2X clocks which might at first glance appear useful for generating the CPU, SDRAM and PCI clocks, this is not the case. The CDC9843 is unsuitable for such a purpose as it cannot not meet the tight restrictions on allowable skew between the 1X and 2X clocks which the MPC106 PCI/Memory controller demands.

To generate the tightly-controlled clocks for the CPU, SDRAM and PCI subsystems, the base clock generated by the CDC9843 is connected to a Motorola MPC972, which contains numerous dividers attached to an internal PLL-based clock synthesizer. Using this part, the skew-controlled clocks may be generated at virtually any speed combination desired.

FIGURE 3. Clock Architecture



Controlling the MPC972 is performed by selecting numerous feedback divider ratios. There are too many combinations to control them with jumpers (or even to list them all here); instead, the Yellowknife X4 uses a PAL to set the dividers based upon a simple three-position jumper header.

Table 2: Clock Options

J61 FS0	J34 FS1	J32 FS2	CDC9843	MPC972		
			Base Clock	Bus Clock	SDRAM Clock	PCI Clock
IN	IN	IN	25 MHz	50 MHz	50 MHz	25 MHz

Table 2: Clock Options

J61 FS0	J34 FS1	J32 FS2	CDC9843	MPC972		
			Base Clock	Bus Clock	SDRAM Clock	PCI Clock
IN	IN	out	30 MHz	60 MHz	60 MHz	30 MHz
IN	out	IN	33 MHz	66 MHz	66 MHz	33 MHz
IN	out	out	25 MHz	75 MHz	75 MHz	37 MHz
out	IN	IN	33 MHz	83 MHz	83 MHz	33 MHz
out	IN	out	30 MHz	90 MHz	90 MHz	30 MHz
out	out	IN	33 MHz	100 MHz	100 MHz	39 MHz
out	out	out	25 MHz	100 MHz	100 MHz	50 MHz

Separate 31.3344 MHz and 50 MHz oscillators are provided for the Hydra device, which is used exclusively MacOS related functions (Apple I/O, MESH SCSI controller, timers, etc.).

All clocks have unoccupied pads for 0805-type devices which can be used to attenuate clocks or adjust skew. These parts are not installed unless needed to meet radiated emissions standards.

CHANGES: X4 extensively changes the clocking system to accomodate the faster bus speeds, different PLL multipliers of the MPC106 (3:2 and 5:2 modes are added), and the need for many more clock signals for SDRAM support. Additionally, to support board testing below 50 MHz bus speeds, an external clock can be supplied to the MPC972, which can generate the proper bus, SDRAM and PCI clocks. Note that the PAL controlling the MPC972 dividers may need to be re-programmed to maintain the proper relationships between bus and PCI clocks that the MPC106 requires.

2.7 PCI-to-ISA Bridge

The PCI-to-ISA bridge provides a means of accessing ISA devices as well as integrating several system using the W83C553 component from Winbond. Pullup resistors configure this part to operate in “PowerPC Mode”, which configures the part to generate HRESET and adds the additional REQ4#/GNT4# arbiter controls.

An external 74F138 is used to convert the encoded DMA acknowledge signals to individual strobes (this saves a few pins on the bridge devices). A Fast part was specified solely due to its availability. Due to the relatively slow speed of the ISA bus, an LS138 or other equivalent-speed technology would be acceptable.

A small transistor drives a connector that would be attached to an 8-ohm speaker, to create the power-up “beep” or other low-quality sounds.

CHANGES: X4 removes the separate reset controller and uses the reset circuitry in the Winbond part. The Winbond also controls the access to the boot EPROM, which is now located on the ISA bus. The bridge chip responds to memory accesses immediately after reset.

2.8 Hydra

The Hydra ASIC from Apple implements several systems needed for MacOS compliance: MPIC interrupt controller, MESC SCSI controller, ADB controller, SCC GeoPort controller, and timers. This device requires three special clocks: a standard PCI clock, a 40-50MHz clock for the SCSI controller, and a 31.3344 MHz clock for the timers, etc.

Since there is no agreed-upon standard for Mac-style connectors on a PC chassis, and since these devices are not strictly necessary to support Windows-NT nor MacOS, Yellowknife places the ADB and SCC/GeoPort connectors on a dedicated connector card. This connector physically replaces one of the ISA slots on board. This allows a small plug-in board to contain the GeoPort drivers for the serial ports, and drivers for the Apple Desktop Bus (ADB).

The MCCS142236 provides the chassis-internal termination of the SCSI bus. The termination shares power via the connector for remotely powering termination. This power is limited to 1A, and is controlled via a self-resetting polyswitch fuse (in compliance with PC'97 guidelines, no destructive fuses are used).

CHANGES: X4 allows the interrupt signals to bypass the Hydra and connect directly from the Winbond into the processor. This allows configuring the board for embedded modes, where the Hydra is not needed.

2.9 Super I/O

The SuperI/O controller is based upon the National PC87308VUL/IBN device, which contains the serial, parallel, and floppy I/O controllers. The suffix "IBN" indicates that it contains the "Phoenix BIOS" implementation of the keyboard/mouse controller. Other parts are available but "IBN" is the current preferred BIOS for MacOS purposes.

The controller is a Plug-and-Play (PnP) device, which allows the internal controllers to be logically connected to any desired interrupt line. Additionally, this device contains the advanced power controller (APC), real-time clock (RTC) and a small array of RAM. All of these latter devices require battery voltage to maintain state while the power is switched off. This power is taken from the NVRAM battery (see Section 2.12 on page 13). The NVRAM in the Super I/O is too small for CHRP purposes and must be disabled by the firmware so as to eliminate interference with the external NVRAM.

The GPIO ports are used to implement miscellaneous status/control information such as:

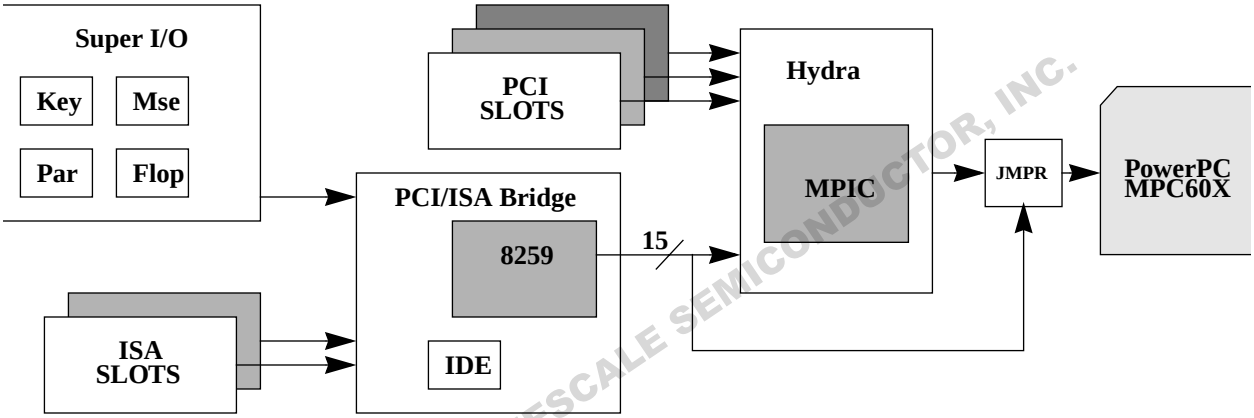
- F_EJECT* floppy eject control.
- SDA/SCK allows access to DIMM presence detect I2C EEPROMs.
- PID(0:2) allows access to parallel/serial interposer presence detect information.
- C512K* code can detect size of L2: 256K or 512K.

CHANGES: X4 allows installation of the compatible PC87307 Additionally, unused GPIO pins now allow access to the PID signals from the processor and to the I2C ports of the DIMM modules (through programmed I/O).

2.10 Interrupt Architecture

The following diagram shows the interrupt architecture for the Yellowknife. The use of the MPIC allows the possibility of multi-processor interposers, though at this time none are anticipated.

FIGURE 4. Interrupt Architecture



CHANGES: X4 adds a jumper to allow interrupts to from through the MPIC in Hydra (for MacOS) or to bypass Hydra and connect the 8259 core in the Winbond bridge directly to the processor. The latter is needed for embedded customers which will not need Hydra and so do not wish to program for it.

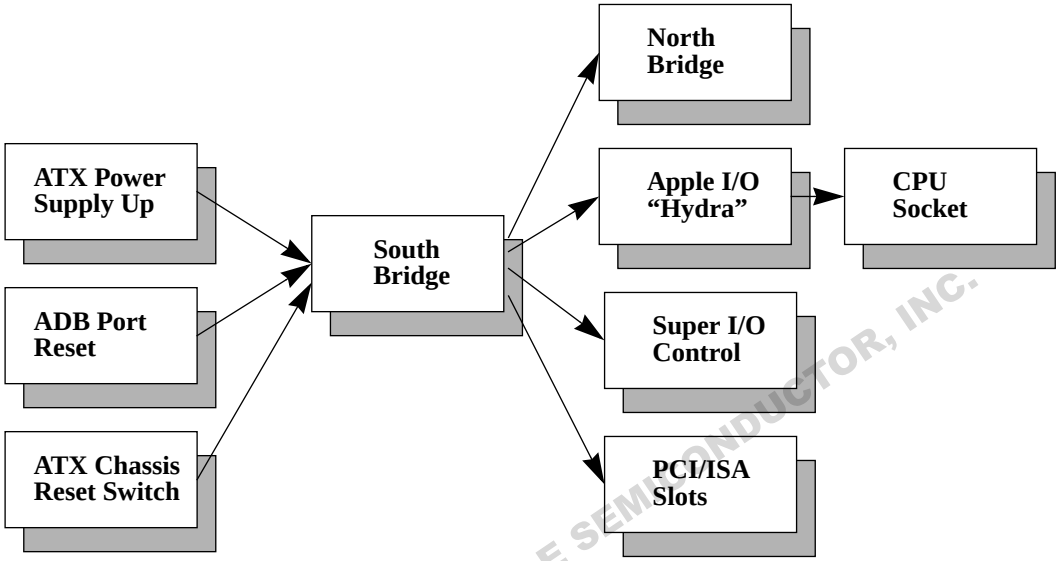
2.11 Reset Architecture

The reset circuitry controls the global reset signals based upon the following sources:

- ◆ PWRGOOD — Low until the power supply has been stabilized; high thereafter.
- ◆ ADB_RESET# — Pulsed low by the ADB controller (due to a keyboard sequence).
- ◆ RSTHDR# — Connected to ground by an external pushbutton switch (on the chassis).

These reset sources are merged and connected to the South Bridge, which in turn resets the rest of the system peripherals.

FIGURE 5. Reset Architecture

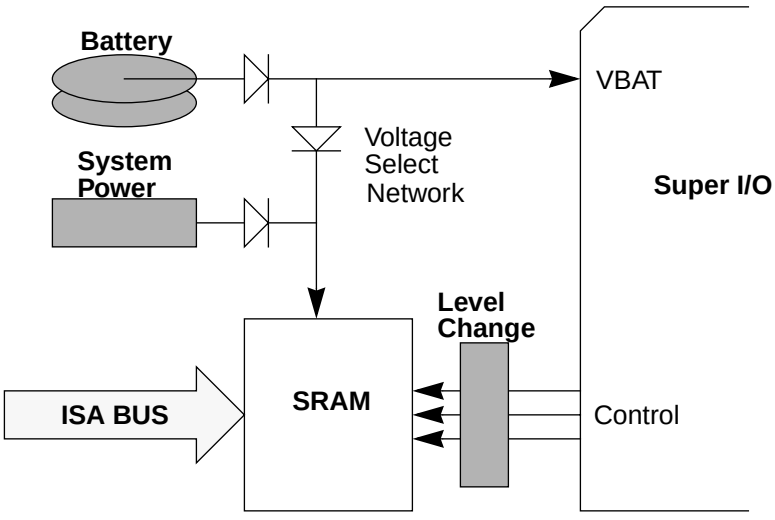


CHANGES: X4 deletes the external reset controller in favor of the Winbond's internal reset controller.

2.12 Battery-Backed Memory

Yellowknife does not use an integrated battery/SRAM product for non-volatile storage as some reference platforms do, nor does it use the internal SRAM provided on the Super I/O. The latter SRAM is too small for CHRP platforms; a minimum of 8K SRAM is necessary. Additionally, a battery is needed for the APC in the Super I/O , so to minimize cost an external battery is used and shared with the NVRAM, which is implemented with a low-voltage SRAM. Note that due to the voltage selection circuitry, the part operates on less than 5V and so must be protected from overvoltage on I/O signals.

FIGURE 6. Battery /NVRAM Architecture



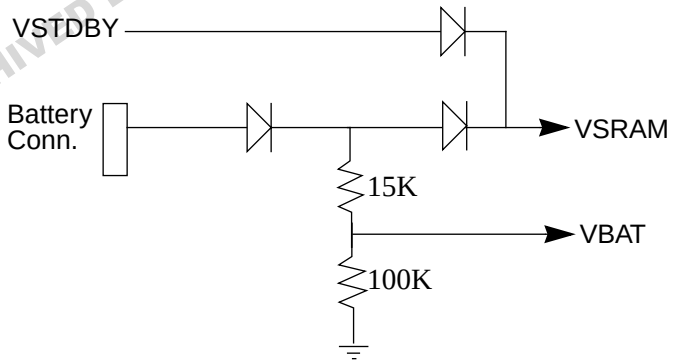
The NVRAM is provided by an external battery and an on-board static RAM. This is different from the previous generation of Motorola platforms which used integrated battery/ crystal/NVRAM/RTC modules from various vendors. A four-pin “Berg” header provides a connection to an external (usually lithium) 4.5V battery pack. The header is designed so that orientation is unimportant; however it is also diode-protected against reverse connections in the event the connector is installed offset by one, or if a two-pin header is used on the battery.

The Super I/O has rather stringent requirements on the relationship of VBAT and VSTDBY, as follows:

- VBAT < VSTDBY - 0.5V
- VBAT < VSTDBY * 1.2

Unless all of these requirements are met, the APC will not work. In order to meet these requirements, Yellowknife uses a voltage divider network to trim the VBAT to an acceptable level needed by the Super I/O. Since the current requirements are very small (less than 20 uA), high-valued resistors can be used to minimize wasted power.

FIGURE 7. VBAT Trim



The protected, trimmed battery voltage is connected to the APC of the Super I/O controller, which maintains the real-time clock and the power supply controller management. That subsystem handles the switching between battery and main power, but similar circuitry is needed for the external RAM. To maintain storage at lower power, a low-voltage SRAM is used (made by several vendors in a JEDEC standard package).

The above networks shows that the SRAM is typically powered by the standby voltage of the ATX power supply, so VBAT drain is minimized as long as the power supply is plugged in and AC mains are operating. Only when the system is unplugged does VSTDBY = 0V, and the supply current for the SRAM+RTC+APC drops to less than 5uA. This low current results in a V_F of the Schottky diodes (1N5817) of approximately 0.25V, so the battery can maintain the system over its expected lifetime as long as the battery voltage is above 3.0V.

In full operating mode, VCC = 5V, and the supply current is exclusively due to the SRAM (the APC does not draw power from the battery in this state) so the current demand is less than 20mA. VBAT will be supplied through the VCC-to-VBAT diode. The battery protection diode will be reverse biased so no current drain will occur until VCC drops below 4.15V.

Note also that since the SRAM is not operated at VCC, but at VCC-V_F, it is necessary to insure that inputs do not exceed the SRAM's maximum ratings of VCC-0.3V by using low-voltage TTL components to isolate the SRAM from the rest of the system. When the system is battery powered, the inputs are not driven so limits are cannot be exceeded. Under system power, the voltage to the SRAM is within this range even at high currents and low temperatures due to the 3.3V TTL drivers. Variations in the system VCC supply will match variations in the V_{SRAM} so the SRAM is safe from overvoltages.

2.13 I/O Ports

There are numerous I/O ports on the Yellowknife platform. Some are connectors located on the back panel in accordance with ATX chassis guidelines, others are attached via cables. The parallel, keyboard , mouse, and two serial connectors are on the back panel of the ATX chassis, eliminating cabling. These connectors are equivalent with standard PC-type connectors. Inside the chassis, the motherboard containsconnectors for cables to IDE and SCSI disk drives, a floppy disk, and an IrDA transciever.

The floppy connector is a standard CHRP connector, which is *not* the same as that used on a PC, though it is very similar. In particular, several pins have been redefined:

Table 3: Floppy Connector Changes

Pin	Old Function	New Function	Description
1	GND	F_EJECT#	Low strobe ejects the floppy.
3	GND	NC	Key
4	NC	MSEN0	Media sense 0.

The keyboard and mouse connections are 6-pin mini-DIN connectors for PS/2-type devices, similar to most modern PCs. The voltage supply for the keyboard and mouse is protected by a self-resetting fuse instead of the typical self-destructive fuse, as specified by the PC'97 guidelines.

The two serial ports are driven with the 75LP185. The 'LP185 is preferred because it has the ability to withstand 15kV ESD discharges without external circuitry. Equivalent parts such as the 75C185 are also available, but without the ESD protection. Many other manufacturers make suitable parts that may be used, such as the Maxim MAX211. If non-ESD protected parts are chosen, additional protection will be needed on the serial port signals.

The IrDA connector allows cabling to a standard IrDA modules available from a wide variety of sources, such as Hewlett-Packard, Novalog, etc.

2.14 Slots

YK contains three PCI slots, two ISA slots and one dedicated Apple I/O slot.

The three PCI slots are standard 32-bit, 33 MHz, 3.3V/5V types. The number cannot be expanded without the use of a bridge device due to the limitations on PCI bus loading and because of the limited number of PCI arbiter channels currently within the PCI-ISA bridge device.

Table 4: PCI Slot IDs

IDSEL	Config Address	South Bridge REQ/ GNT	Hydra Interrupt			
			INTA #	INTB #	INTC #	INTD #
AD14	0x8080_4000	0	XINT1	XINT2	XINT3	XINT4
AD15	0x8080_8000	2	XINT2	XINT3	XINT4	XINT1
AD16	0x8081_0000	3	XINT3	XINT4	XINT1	XINT2

Note that the PCI slots use the “rotating” interrupt assignment method. PCI cards typically implement only one function, and use only INTA#. For such cards, the slots can be treated as having completely independant interrupts. When multifunction cards are used, each slot may use multiple interrupt lines, possibly sharing them with an adjacent slot.

The two ISA slots are standard 16-bit ISA slots. The number can be easily expanded to the industry standard of three or four. Only two are present on Yellowknife due to the ATX chassis limitations, four-layer routing restrictions, and to the fact that the special Apple I/O card replaces one of the ISA slots.

The Apple I/O slot is used to allow place connectors for the ADB and GeoPort connectors. This connector is not standardized but was defined by Motorola and is used on other platforms as well.

3.0 Software

3.1 Memory Map

The default memory map for the Yellowknife X4 is “CHRP”, Map “B”, though the board can be configured to either mode. Refer to the MPC106 User’s Manual for details on the maps as viewed from the processor or from PCI.

CHANGES: X4 defaults to CHRP mode, while X2 defaulted to PREP mode.

4.0 Board Configuration

One design goal of the reference platform was the minimization of configuration jumpers. Some are regrettably necessary due to the need to support a wide variety of processors. The following sections describe all the jumpers in detail.

4.1 User-Settable Jumpers

Two or three pin “Berg” jumpers are used when user-changable options must be set.

4.1.1 System Frequency Selection

Jumpers J61, J34, and J32 ar e used to set the operating frequencies of the processor bus and the PCI bus.

Table 5: Clock Settings

J61 FS0	J34 FS1	J32 FS2	Bus Clock	PCI Clock
IN	IN	IN	50 MHz	25 MHz
IN	IN	out	60 MHz	30 MHz
IN	out	IN	66 MHz	33 MHz
IN	out	out	75 MHz	37 MHz
out	IN	IN	83 MHz	33 MHz
out	IN	out	90 MHz	30 MHz
out	out	IN	100 MHz	39 MHz
out	out	out	100 MHz	50 MHz

4.1.2 Processor Frequency Selection

Jumpers J35, J36, J38 and J40 are used to set the core, or internal, operating speed of the processor. This is the speed at which the processor performs instructions, as opposed to the speed at which it performs memory accesses. The core speed is always an integer or half-integer multiple of the “Bus Clock” speed selected with the System Frequency jumpers.

Table 6: Processor Clock Settings

J35 CP0	J36 CP1	J38 CP2	J40 CP3	PLL	Bus Clock	Core Clock
IN	IN	IN	IN	7X		
IN	IN	IN	out			
IN	IN	out	IN			
IN	IN	out	out	BYPASS		
IN	out	IN	IN	2X	60 ... 100	120 ... 200
IN	out	IN	out	6.5X		
IN	out	out	IN	2.5X	50 ... 100	125 ... 250
IN	out	out	out	4.5X	50 ... 60	225 ... 300

Table 6: Processor Clock Settings

J35 CP0	J36 CP1	J38 CP2	J40 CP3	PLL	Bus Clock	Core Clock
out	IN	IN	IN	3X	50 ... 83	150 ... 250
out	IN	IN	out	5.5X		
out	IN	out	IN	4X	50 ... 66	200 ... 266
out	IN	out	out	5X	50	250
out	out	IN	IN			
out	out	IN	out	6X		
out	out	out	IN	3.5X	50 ... 75	175 ... 262
out	out	out	out	OFF		

NOTE: Not all processors support all options. Additionally, since the Yellowknife does not directly support clock speeds below 50 MHz, many of the PLL settings are not directly usable.

4.1.3 MPC106 Frequency Selection

Jumpers J57, J59, J58 and J60 are used to set the ratio of the PCI bus clock to the processor bus clock, so the MPC106 can communicate in sync. with both. The core speed is always an integer or half-integer multiple of the “Bus Clock” speed selected with the System Frequency jumpers.

Table 7: Processor Clock Settings

J35 CP0	J36 CP1	J38 CP2	J40 CP3	PLL	PCI Clock	Bus Clock
IN	IN	IN	IN			
IN	IN	IN	out	1X	33	33
IN	IN	out	IN	1X	16 ... 25	16 ... 25
IN	IN	out	out	BYPASS		
IN	out	IN	IN	2X	33	66
IN	out	IN	out	2X	16 ... 25	33 ... 50
IN	out	out	IN	2.5X	33	83
IN	out	out	out	2.5X	16 ... 20	40 ... 50
out	IN	IN	IN	3X	25 ... 33	75 ... 100
out	IN	IN	out	3X	16	50
out	IN	out	IN			
out	IN	out	out			
out	out	IN	IN			
out	out	IN	out			
out	out	out	IN			
out	out	out	out	OFF		

4.1.4 COP Function Jumper

Jumper J39 must be installed to allow full operation of the COP processor debugging fea-

ture; in particular, the soft-start/soft-stop functions of COP will not work unless the jumper is installed properly.

Table 8: COP Jumper Settings

J39			Function
1	2	3	
■	■		Normal operation; power management uses QREQ*/QACK*
	■	■	COP operation; QACK* forced low.

4.1.5 Interrupt Flow Jumper

Jumper Jx is used to control the routing of interrupt signals to the processor. In positions 1-2, interrupts flow from the Winbond and Super I/O ISA and PCI interrupt into the Hydra MPIC core, merging with internal Hydra interrupt, and then on to the processor. In positions 2-3, interrupts bypass the Hydra MPIC and go directly to the processor.

Table 9: Interrupt Jumper Settings

J39			Function
1	2	3	
■	■		MacOS mode: Interrupts flow through Hydra MPIC.
	■	■	Embedded mode: Interrupts bypass Hydra MPIC

Note that to allow the embedde mode, PCI interrupts are connected to *both* the Hydra and the Winbond. Generally, only one or the other of these devices should be programmed to sense the PCI interrupt lines.

4.1.6 Processor Voltage Selection

Jumpers J45, J46, J47, J55, and J56 are used to optionally override the interposer voltage setting and impose a user-selected setting. To accomodate this, the top-level trace between pins 1 and 2 of all of these jumpers must be cut (use an X-acto knife); then, the jumpers (which are usually not installed) must be soldered in (use 3-position Berg headers). Once done, the jumpers allow forcing a VID(0:4) signal high, forcing low, or allowing the interposer to control. For more details, refer to Figure 1, “Optional VID Control,” on page 7.

4.1.7 Soft-start Override

By installing a shorting-plug on Header J44, pins 20 to pins 22 (i.e. on the side), the ATX power supply is forced on. This allows embedded customer s to ignore APC power control issues, and the MacOS related power signals.

4.2 Permanent Jumpers

Permanent jumpers are implemented with zero-ohm resistors permanently soldered to the motherboard to select certain configurations. To change these settings, these resistors must be added, changed or removed. This is no normally done by the end-user.

4.2.1 Processor Drive Strength

These resistors are used to modify the drive strength of the processor. The standard setting is “Normal” mode. Higher drive strengths can clear some problems but could cause others.

Table 10: CPU Drive Strength

R14 DS0	R38 DS1	Meaning
IN	IN	CPU is tri-stated
IN	out	1X : Normal drive strength
out	IN	1.5X : Strong drive strength
out	out	2X : Herculean drive strength

4.2.2 Map Selection

This resistor is used to select the memory map used by the MPC106. The default is “Map B” for CHRP compatibility.

Table 11: Map Selection

R10	Meaning
IN	Map “B”: CHRP
out	Map “A”: PREP

4.2.3 Cache Size Selection

These jumpers are used to set the size of the cache installed. Because the cache SRAM is soldered directly to the motherboard, changing the cache size is an involved operation. Still, for completeness, here are the settings.

Table 12: Cache Size Configuration

R350 CRB	R351 CRA	R352 CRB	Cache Size
out	IN	out	256K
IN	out	IN	512K

5.0 Layout Issues

The guidelines detailed in the Yellowknife X2 hardware reference manual may be of help, but the majority of the Yellowknife X4 layout is covered in great detail in the application note AN17xx, “SDRAM System Design using the MPC106”. Here are some general guidelines:

- The VRM power supply module should be positioned close to the PGA socket, such that the current flows through a heavy plane from the ATX power supply. Insure placement of the VRM does not interfere with the HP analyzer header if debugging is desired.
- The VRM power supply capacitors should be positioned very near the CPU socket.

The following traces should be routed to carry additional current capacity:

Table 13: Routing Power

Signal	Power
CORE_VDD	Sufficient for 7A.
TERMPWR	Sufficient for 1.5A.
J4	1A of +12V power (for fan).
J42-24	300mA
U11-28	100mA
VBAT	100mA

5.1 Swappable Pins

The following groups may be pin-swapped (excluding the obvious swappable discrete gates). Each line is considered a separate group.

MPC972	QA(0:3), QC(0:3)	QA/QC clock groups are swappable, as are split-terminated outputs.
MPC972	QB(0:3)	QB clock groups are swappable, as are split-terminated outputs.
IDT71216		A(12:0), TAG(11:1) All except A13/TA13/TD13
MCM69P737	A(0:16)	Cache addresses swappable.
MCM69P737	DQ(0:63)	Cache data swappable (byte mode not used).
74ALVCH16601	A(1:18) :: B(1:18)	Input and output pairs swappable.
DIMM	D(0:7) :: DQMB0	Byte lanes and associated controls.

	D(8:15) :: DQMB1 ... D(56:63) :: DQMB7	
SRAM	A(12:0)	All swappable.
SRAM	D(7:0)	All swappable.
RPAK		All swappable.

5.2 Documentation

The following manuals may be of use for understanding some of the components used on Yellowknife:

Table 14: Reference Documentation

Manual	Source	Document
SDRAM System Design using the MPC106	Motorola	AN17xx
Motorola MPC603 User's Manual	Motorola	MPC603UM/AD
Motorola MPC604 User's Manual	Motorola	MPC604UM/AD
Motorola MPC750 User's Manual	Motorola	MPC750UM/AD
Yellowknife X2 User's Manual	Motorola	YKX2UM/AD
Yellowknife Home Page	Motorola	www.mot.com/SPS/PowerPC/teksupport/refde-signs/yk.html
Motorola Processor/Cache Module Hardware Reference Manual	Motorola	MPCMAE/AD
PC87308VUL	National Semiconductor	N/A
WB83C553	Winbond	2565
Hydra ERS	Apple Computer	P/N 343S0181