EE 7.9.2 Release Notes

June 2011

© 2011 Mentor Graphics Corporation
All rights reserved.

This document contains information that is proprietary to Mentor Graphics Corporation. The original recipient of this document may duplicate this document in whole or in part for internal business purposes only, provided that this entire notice appears in all copies. In duplicating any part of this document, the recipient agrees to make every reasonable effort to prevent the unauthorized use and distribution of the proprietary information.

This document is for information and instruction purposes. Mentor Graphics reserves the right to make changes in specifications and other information contained in this publication without prior notice, and the reader should, in all cases, consult Mentor Graphics to determine whether any changes have been made.

The terms and conditions governing the sale and licensing of Mentor Graphics products are set forth in written agreements between Mentor Graphics and its customers. No representation or other affirmation of fact contained in this publication shall be deemed to be a warranty or give rise to any liability of Mentor Graphics whatsoever.

MENTOR GRAPHICS MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

MENTOR GRAPHICS SHALL NOT BE LIABLE FOR ANY INCIDENTAL, INDIRECT, SPECIAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER (INCLUDING BUT NOT LIMITED TO LOST PROFITS) ARISING OUT OF OR RELATED TO THIS PUBLICATION OR THE INFORMATION CONTAINED IN IT, EVEN IF MENTOR GRAPHICS CORPORATION HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

RESTRICTED RIGHTS LEGEND 03/97

U.S. Government Restricted Rights. The SOFTWARE and documentation have been developed entirely at private expense and are commercial computer software provided with restricted rights. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement provided with the software pursuant to DFARS 227.7202-3(a) or as set forth in subparagraph (c)(1) and (2) of the Commercial Computer Software - Restricted Rights clause at FAR 52.227-19, as applicable.

Contractor/manufacturer is:
Mentor Graphics Corporation
8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.
Telephone: 503.685.7000
Toll-Free Telephone: 800.592.2210
Website: www.mentor.com
SupportNet: supportnet.mentor.com/
Send Feedback on Documentation: supportnet.mentor.com/user/feedback_form.cfm

TRADEMARKS: The trademarks, logos and service marks ("Marks") used herein are the property of Mentor Graphics Corporation or other third parties. No one is permitted to use these Marks without the prior written consent of Mentor Graphics or the respective third-party owner. The use herein of a third-party Mark is not an attempt to indicate Mentor Graphics as a source of a product, but is intended to indicate a product from, or associated with, a particular third party. A current list of Mentor Graphics' trademarks may be viewed at: www.mentor.com/terms_conditions/trademarks.cfm.

Table of Contents

Chapter 1
Constraint Editor System (CES)

Problems Fixed

- **dts0100271764** — wants CES-DxDesigner GUI to control of diff pair impedance
- **dts0100274545** — width and clearance entries in CES hierarchical linked to the master scheme
- **dts0100323184** — In CES, It should improve so that '0' cannot be entered to Trace width.
- **dts0100328878** — Can not see netclasses applied to clearance rule when CES is opened readonly
- **dts0100334127** — ER: Assign Nets to New Bus Constraint Class dialog need the existing and New class panes reversed
- **dts0100338011** — renaming netclass in CES duplicates the netclass to the new name
- **dts0100477551** — CES should write a log file when PinPairs and FromTos disappear
- **dts0100534502** — user defined constraints should be usable for other projects and users
- **dts0100584418** — Would like to use regular expression in Auto Assign Differential Pairs
- **dts0100605158** — CES diff pair information is not seen on forward annotation.
- **dts0100629506** — Import / Export Net Class to Net Class clearance rules from one design to another does not work and no messages.
- **dts0100635276** — CES Documentation: Provide information on how package direction is determined for package clearance rules
- **dts0100637040** — Cannot open CES in stand-alone mode from Dashboard using the rght-click pop-up from a project, Open With -> CES, (Linux)
- **dts0100686407** — CES EP Mask to objects images are wrong and must be changed.
- **dts0100697275** — CES Nets > Dynamic and Static Overshoot Properties Descriptions fields are confusing and incorrect
- **dts0100701485** — CES users in concurrent mode have different default values in CES when use different WDIRs localizations
- **dts0100702484** — When remote accessing to a Dual Monitor system where CES dialog "Assign nets to Nets to Classes" window does not appear if docked on the 2nd monitor
- **dts0100702838** — Please encrypt ce_ee.cns file.

- **dts0100710991** — Reapply constraint template is grayed out when Template Status is Changed, why?
- **dts0100713187** — Documentation for CES parallelism rules prevents parallelism violations from being reported correctly.
- **dts0100717637** — The \7.9EE\docs\htmldocs\stackupeditor_hl_user folder and contents are removed after loading WG7.9 Update1
- **dts0100719698** — ces.ini in project directory is ignored
- **dts0100720229** — Stackup cannot be saved because of critical errors. Unlocked Object Is Invalid. Stackup is messed up and cannot be modified.
- **dts0100725158** — CES adds exlamation mark to Constraint class for Formal Reuse Block
- **dts0100729250** — CES crashes if more than 2 objects are deleted in Navigator
- **dts0100734271** — DxDesigner Backup routine hangs at 70% and does not complete.
- **dts0100735180** — Please remove warning about different WDIR directories
- **dts0100738794** — Assign Nets to Netclass by right mouse button in the Nets-spreadsheet does not work
- **dts0100739128** — In the case of Diff Pair Electrical nets, if you enter a min/max value at the level of Physical net, the same value will be propagated to other Physical nets.
- **dts0100752226** — Conversion failed. Error (-1146): Error converting CES Parts and Components. Error (-1145) in EE2007.3
- **dts0100757994** — class to class clearances cannot be changed in some schemes in CES
- **dts0100760825** — When a type is declared to a variable in VBA, the Name property of Constraint is returned by Boolean in VBA.
- **dts0100762011** — CES Diagnostics crashes on this design with "The fromto is duplicated in database" errors
- **dts0100768096** — Error: Formula parser error: V3-122: duplicate pin in record

Known Problems and Workarounds

- **dts0100437810** — Reuse: After placing a Reuse block and packaging, reference designators in formulas were not updated accordingly.

  Workaround: Please manually change the formula.

- **dts0100635944** — I couldn't work on DxD when CES Diagnostic is running

  Workaround: Please wait untill Diagnostic finishes.

- **dts0100708806** — Net Class is not propagated from template to the nets in this scenario

  Workaround: reassign constraint template on these nets to see newly created net class.

- **dts0100769449** — Disconnect on global symbol caused errors in CES Output dialog

  Workaround: run CES Diagnostics in case of these error message to check database integrity

- **dts0100770582** — Deltas are not solved for DiffPairs when match group is defined on CC level

  Workaround: After defining match group on constraint class level, user has to import once again actuals to see deltas

Additional Information

There is an issue currently with the plane-to-plane clearance values in CES not properly reflecting the correct values. Expedition PCB does not support different plane-to-plane clearance values for use with different Schemes (rule areas). Therefore in CES, this value can only be defined for the rules in the (Master) scheme and the plane-to-plane clearance constraint cell in all of the other schemes is not editable. CES should update this cell in all of the other schemes when the value is updated in the (Master) scheme is updated, however there is currently an issue with this, and the values aren't updated. However it should be noted that the incorrect value is not actually used by Expedition PCB. The values in the (Master) scheme are the only values used in the layout.

Chapter 2
Design Capture

Problems Fixed

- **dts0100575137** — After placing a new device with assigned Cell Name, the Part Number value becomes a Cell Name value on the DC schematic and this will cause the packager error
- **dts0100575158** — New placed parts: The Part Name or Reference Designator value becomes a Cell Name value on DC schematic after Back Annotation
- **dts0100618560** — Many Parts are missing from BOM
- **dts0100696745** — All fields except "Ready" are missing from the Status Bar in Design Capture EE7.9
- **dts0100699573** — Place Device filter fields are only half height when installed on Vista.
- **dts0100734577** — DC/DV fails on packaging. ERROR: Duplicate physical nets. More than one physical net has the same Common DataBase assigned net name.
- **dts0100742178** — Compile & Package results in PCB flat netname that shorts two different nets together.
- **dts0100747799** — Duplicate flatnames causing short in PCB
- **dts0100755061** — DC crashes when placing ReUse Block
- **dts0100759733** — Placing RB in existing design causes DC to crash

Chapter 3
DMS Librarian

Problems Fixed

- **dts0100559548** — update_cache_wg.sh -update A,D : update fails if part already exists in LMC
- **dts0100571526** — Bulk checking in / out
- **dts0100596260** — DMSL dialog has incorrect message
- **dts0100608176** — IPC Error:10061 during update cache.
- **dts0100616152** — Altering the pinout of a symbol or cell will cause update_cache to fail
- **dts0100616760** — Bulk check out in DMS Librarian
- **dts0100616925** — DX symbol which using a multiple parts and one part/symbol is updated then other parts cannot be imported in.
- **dts0100642428** — Loosing Network connection from DMSL to DMS causes all items in the sandbox to have the wrong status
- **dts0100667608** — User would like the ability to select multiple items in the library upon which an action can then be taken.
- **dts0100739020** — "Associate part/mapping to a component" fields limited to 30 character display - cannot scroll right or use other methods to select long pdb names.
- **dts0100762057** — The change in update cache causes problems in customer's datamodels.

Known Problems and Workarounds

- **dts0100605659** — Reuse Block may be verified in sandbox with different version of CAD element than available in cache

  Workaround: Verified Reuse Block can be downloaded to a Central Library and reference symbols, cells or padstacks that are different from the ones used to verify the Reuse Block. When a Reuse Block is verified in DMS Librarian or LFM they are verified against the CAD objects in a librarian sandbox. Those objects in the librarian sandbox could have, in DMS, a life cycle state that is ignored by update_cache. In this situation, the CAD objects in the production cache could be older/different than the CAD objects the Reuse Block was verified against. There are several workarounds to this situation, first use a 'Reuse Block Only' type sandbox for all Reuse Block verification. This ensures that all CAD objects used to verify a Reuse Block are the same objects that are present in the production cache, granted that the same options for update_cache are used when creating both caches. Next, make sure all CAD objects associated with a Reuse Block are checked into DMS and the life cycle status for those objects has to be set to a status that update_cache would push those objects to the production library.

- **dts0100726447** — Update Cache Wizard fails (issues error) when the browsed for .ior path contains a space; the path needs to be in quotes.

  Workaround: Copy the ior file to a location without spaces.

- **dts0100764895** — [KTWZDS] Update Cache fails to add Logical-Physical re-use block

  Workaround: Reuse Blocks that are created with components that reference generic mappings will fail to be downloaded unless the generic mappings are also in the production library. The Reuse Block checker is comparing the wrong data and will return and error when trying to download a Reuse Block that contains components with generic mappings. The workaround is to run update_cache with the -pdb switch to download the generic mappings and then run update_cache to download the Reuse Blocks.

Chapter 4
DxDesigner

Problems Fixed

- **dts0100138600** — Still no way to enable 2.0 output format in partslister
- **dts0100141113** — EE - Add the ability to assign sequential reference designators (refdes) to components in a design using various strategies
- **dts0100199611** — variable field length in partlister
- **dts0100220918** — Change component does not maintain refdes
- **dts0100244246** — Tab delimited Partslist
- **dts0100273141** — Partlister should read partliter.ini from active project or from <mentor_inst>\2005EXP\standard directory .
- **dts0100287738** — Infohub is not coming on Linux
- **dts0100323900** — Open DxDesigner project is very slow if 20 libraries are placed in the remote drive (~15 minutes)
- **dts0100331689** — Want Changes made through the DxDataBook Properties dialog box saved in a file instead of registryre
- **dts0100374537** — Partlister should be implemented as tool to make bill of materials instead of icdb2bom
- **dts0100433428** — Symbol Window needs to dynamically update after Cent Lib changes are made
- **dts0100459144** — Flat netnames in DC needs to be assignrd in DxDesigner based on the existing CDB in DC.
- **dts0100461610** — There is no possibility to change the order of field "ITEM", "QTY", and "REFERENCE"
- **dts0100461965** — Archive leaves temporary files after running
- **dts0100464416** — [SilkTest] Font and color settings are ignored - defined in prp file
- **dts0100487122** — Edif schematic: Schematic is not exported when sheets have different name than 1,2,3...
- **dts0100501743** — Ref Designator Instance Value does not show up in EDIF netlist

- **dts0100505705** — The new part lister does not allow some outputs which were possible with the previous version (EE2005.x)
- **dts0100510917** — In DxDesigner offer a way to keep or not refdes during a copy between pages or between projects
- **dts0100521706** — iCDBPartlister is missing the REFDES Sort feature that was available in 2005 Architecture
- **dts0100564372** — In the iCDB architecture, Block::AddLine Method uses extremely small units that make the AddLine function unusable
- **dts0100572481** — Migration of hierarchical designs from PADS2007.4 to PADS 9.0 changes hierarchical net names.
- **dts0100579515** — File->Print-> Range in DxDesigner only prints the first and last page
- **dts0100585107** — Request ability to scale symbol in the symbol editor
- **dts0100596613** — databook icon missing when smart utilities are installed
- **dts0100597100** — Using Undo after moving bus elements, leaves the ripper bit number in the wrong position.
- **dts0100598235** — Line Thickness option is missing from Print dialog in EE2007.1
- **dts0100599256** — Symbol Update fails - 'Can't load symbol file block. Symbol block is not read from iCDB.'
- **dts0100599506** — Line Thickness option is missing from DxPDF dialog in EE2007.3
- **dts0100621834** — Is there any possibility to map the fonts used inside DC?
- **dts0100623982** — Tie Dots aren't written to CCZ output from DxDesigner
- **dts0100627380** — Partlister argumenst are order specific
- **dts0100627765** — Documentation is needed for the commands and options that appear in the Dx Output window.
- **dts0100628522** — LineSimLink Does not recognize POWER (Global) Nets
- **dts0100632422** — The icdbPartsLister in the command line does not work in the Linux Red Hat 4 and Red Hat 5 environments.
- **dts0100634775** — Add new option to decide if OUT-ANALOG connections should be ignored.
- **dts0100636564** — Parts Lister - need to be able to define one Ref Desg per line using standard Ref Designator in GUI
- **dts0100642380** — Add Exclude Sheet command on RMB
- **dts0100643328** — Standard Definition columns remain checked when a custom ipl file is opened with the columns unselected.

- **dts0100643348** — Documentation: Dxdb.ini is still referenced in documentation eventough it has been removed from the tool support
- **dts0100654828** — Application.ActiveView.ActiveBlock.SheetSize=VDSHEET_A3_SIZE does not update the "Drawing Size" value in the GUI
- **dts0100655575** — On a project converted from DC to DxD the Expedition forward annotation commands unplace two components.
- **dts0100655599** — On a project converted from DC to DxD the Expedition forward annotation commands unplace a bounch of components
- **dts0100671398** — Type-o in DxDesigner User's manual page 138
- **dts0100671763** — Connectivity lost on rippers when Undo is used
- **dts0100677153** — Part Lister - support for variants
- **dts0100677549** — Ability to setup both the RefDes start and the RefDes Suffix on a block symbol or RefDesStart and RefDes Prefix
- **dts0100680615** — The variant title block info does not allow instance values for certain specified properties
- **dts0100688197** — DxD crashes with instant exit when creating variant schematic (DMS Library)
- **dts0100692022** — White objects should export as black when colors on white option used for Export PDF
- **dts0100692562** — Need to document the behavior when renaming nets on the Navigator Tree as opposed to renaming nets on a sheet.
- **dts0100695568** — System Scalable Font mapping option causes the misalignment of texts (properties & labels) in the pdf output than in DxD.
- **dts0100699135** — System Scalable Font mapping option causes symbol level property strings to appear 20-25% wider in the pdf output than in DxDesigner. DR 00634067 fixed font mapping only for schematic level text.
- **dts0100708365** — DxPDF ignores Scale Factor in Setup>Settings>Font Mappings, .pdf Text not scaled, does not match schematic
- **dts0100710950** — The PCB Interface does not use the config file setting from the project file
- **dts0100713031** — CL View dynamic filtering far too slow with non-local distributed libraries
- **dts0100715862** — Grid On/Off button and setting is not controlled by DxDesigner.xml setting
- **dts0100716163** — The wrong slot symbol is created on a new sheet in PCB Interface
- **dts0100717761** — RB cannot be dissolved
- **dts0100718458** — Improvement for description of Connections method (Net object)

- **dts0100719142** — Hierarchical Port deleted when "/" is used in netname
- **dts0100721568** — @DATETIME property remains on the design in DxD2007.
- **dts0100721942** — Texts change colour on white background
- **dts0100722453** — PCB Interface: Wrong state of checkbox Use Custom Configuration after browsing to configuration file.
- **dts0100722711** — DRC-109 issues bogus errors in 7.9.1 regarding nets not being ripped from bus. Regression from 7.9
- **dts0100723475** — Using Automatically Propagate adds block name / label to underlying net when adding annotate symbol to that net
- **dts0100724188** — "generic" as a selection of layout tools
- **dts0100724587** — Port symbol deleting after pop / push
- **dts0100725156** — Please rename option "Report extra internal or flat connection on ripped nets" for drc-121 check.
- **dts0100725398** — Multi pass search seems to corrupt the database
- **dts0100725904** — Running "PCLS_OK" from Dashboard toolbox fails.
- **dts0100727283** — Templates require case sensitivity in the wdir path.
- **dts0100727648** — "CLibPDF: Too many images: 32. Increase limits by cpdf_setDocumentLimits()." on exporting project with >31 embedded objects (OLEs) to PDF .
- **dts0100728483** — packager locks up. Gets to "clustering is complete" and stops.
- **dts0100728676** — EDIF Schematic Export fails with any design with named sheets
- **dts0100728852** — Deleting a Block via the the Navigator window removes random Variant Unplace/Replace Modification data
- **dts0100729249** — Unable to package design with re-use blocks
- **dts0100729914** — vnsd.exe remains in process list
- **dts0100731022** — ODBC error - Invalid character value for cast specification on column number 1
- **dts0100731203** — The "vp520.err" file is created on desktop in the machine.
- **dts0100732759** — DxDesigner hangs at "Place from Schematic"
- **dts0100732768** — DC2DX translates DC Font .12 inch to smaller value in DxD which impact text ledgibility in translated library
- **dts0100732891** — EEFLOW: Addin ee_utils is not installed when only DxDesigner is selected

- **dts0100733056** — DxD PDF does not recognize scaled Font
- **dts0100733308** — Rotation of Properties is not kept after Replacing rotated part
- **dts0100733489** — Running attached script crashes DxDesigner in Linux, on windows get "Object doesn't support" error message
- **dts0100733556** — If the "Check for missing value" suboption of drc-401 is used, vdrc.exe will crash.
- **dts0100734984** — drc-504: check that net connected to a tap has the expected Global Signal Name value
- **dts0100736287** — Page will not translate in EE2007.8 or translates in EE7.9.1 but pin / net disconnect
- **dts0100736302** — DxDesigner should try to repair text binding to net segment on schematic open (Error 12001)
- **dts0100737782** — DxDesigner hangs when a bus containing diff pairs is selected
- **dts0100738282** — Severe performance regression when cross probing between Expedition and DxDesigner in EE7.9.1 versus EE2007.8
- **dts0100738427** — European Notation only correct for resistor Values
- **dts0100739770** — DxD - Updating a single Reuse Block takes 4 1/2 hours.
- **dts0100741247** — Delete Local Symbol does not always work
- **dts0100741391** — DxDesigner crashes if client A is removing port from block while client B is connecting net to the port.
- **dts0100741398** — Centlib.prp file for the EE7.9.1 tutorial has incorrect entry for Value.
- **dts0100741831** — DC2DX - Does not translate Pin Type.
- **dts0100742123** — DxD going offline when updating block symbol in concurrent mode
- **dts0100742205** — Case sensitivity issue in the VHDL configuration file
- **dts0100742211** — Wrong bus mapping in VHDL configuration
- **dts0100742520** — DxDesigner hangs for about 6 minutes while crossprobing with Expedition (Elbit design).
- **dts0100745928** — CES_Load.txt file ERRORS opening a translated Hierarchical DC/Exp to DxD/Exp
- **dts0100746307** — DxDesigner crash when using File Open Block Browse and then push on composite block within that design
- **dts0100749260** — scaling translations using orcad.cnv increases the pin length
- **dts0100749708** — DxDesigner behavior in graphical "line" object selection and moves

- **dts0100750030** — DA2DX translator crash
- **dts0100750930** — DXD - Reuse Block Symbol update removes RB Layer mapping property
- **dts0100751477** — When connecting two buses with the same name, DxDesigner crashes.
- **dts0100751533** — Cross Reference if "Format Prefix" is empty and you click on "More Format Options" DxDesigner crashes
- **dts0100752938** — Running DRC-121 crashes Verify
- **dts0100753176** — DC2DX translator fails with 'Unable to obtain data for design block' and othere errors.
- **dts0100753866** — DxDesigner Diagnostics prompt reuse block symbol update for design migrated from 2007.8 to 7.9.1
- **dts0100754246** — Japanese menu problem in "Find and Replace Text" dialog.
- **dts0100755372** — DxDataBook needs to support Oracle version 11
- **dts0100756002** — Non understandable message in DxArchiver
- **dts0100757291** — Running Packager with 'Verify' does not flag Pin Number errors but 'Package Symbols' does.
- **dts0100759172** — CADStar translation shorts nets
- **dts0100759542** — Bit numbers are moved so far away when increasing the space of each bus nets by using "Shift+Ctrl+Mouse Wheel".
- **dts0100760262** — Unexpected connection occurs and DxDesigner crashes.
- **dts0100764950** — DxDesigner crash on DxDiagnostics, runtime error , memory up to 2GB
- **dts0100769769** — The PDF output, from an ICT project, fails with the message "PDF document cannot exceed 1024 pages"

Known Problems and Workarounds

- **dts0100504235** — Preview window in Symbols addin does not display bitmaps in symbols.

  Workaround: Place the symbol in the schematic to see the bitmap.

- **dts0100505027** — Extract schematic - haven't got information when ports are not defind.

  Workaround: Define hierarchical ports using Setup->Settings->Special Components tab before creating blocks.

- **dts0100505660** — Design is translated to block while migration.

  Workaround: Sometimes when a project contains multiple top-level designs after migration not all designs are created automatically. You can still do that manually in the Navigator by selecting a block (which in fact should be a design) and from the right mouse button menu select 'Create Design' option.

- **dts0100508265** — vlib: Error: Unable to parse the integer token 'ffff00' from the "string. when exporting HPGL file from DxDesigner

  Workaround: HPGL file can be generated on Windows platform.

- **dts0100509882** — DxWebPack does not work in Windows Vista as a server.

  Workaround: The path to dxdbweb.dll must be set in "ISAPI and CGI Restrictions" option on server level in IIS.

  Next, DxDataBook server must be configured in DxDBConfig tool. There are two tabs: "DxDB Client Access" and "Browser Access".

  "DxDB Client Access" - use this tab to choose ODBC Data Source Name and to add database aliases to chosen data source. Database aliases allow to define the set of data source names visible to DxDataBook client. After configuring this tab, it is possible to connect to DxDB Server and specified database from DxDataBook.

  "Browser Access" - use this tab of DxDBConfig to specify the database configuration file that you want to use in the web extension to DxDataBook. After selecting DBC file, all tables configured in this file will be visible in explorer. It is needed to restart the web server in IIS after configuring the DxDBConfig. After restarting, It is possible to connect to DxDB web server from DxDataBook and from explorer.

- **dts0100608634** — Allegro, RINF and keyin netlisters do not work if there is a space in the sheet name.

  Workaround: Do not use spaces in schematic name.

- **dts0100637797** — (Solaris) Environment variable (%var_name%) in .prj file not supported.

  Workaround: use one of the following syntax:

  ```
  $var_name
  ${var_name}
  ```

- **dts0100673417** — The "Substitute symbol(s)" option may not work properly if there is a "sym" folder in project folder.

  Workaround: Delete or rename the sym folder if it is possible.

- **dts0100685731** — DxD crashes on exit

  Workaround: working script should be terminated prior to closing DxDesigner to avoid crash.

- **dts0100718201** — Bom Report changes in VM should enable a VM save

  Workaround: Change some Bom report settings and then change some other VM settings to trigger the enable of save.

- **dts0100758212** — iCES lost selection after net was conected to component

  Workaround: Please select object in host application again.

- **dts0100287738** — Infohub is not coming on Linux

  Workaround: In window Preferensces (Edit> Preferences) please uncheck "Use the internal Dashboard Web Browser" and in combo box provides patch to alternative browser. Now InfoHub opens in alternative browser and works fine.

Chapter 5
Expedition PCB

Problems Fixed

- **dts0100001067** — Support Scaling for Drawing Cells
- **dts0100018026** — Forward Annotation: Fixed Nested cells issue where they are not removed from PCB after deleting part in Schematic
- **dts0100306836** — Support for comparison report between instance layout cells and library cells
- **dts0100351014** — PDF: SLOT width size is larger in the PDF than in design
- **dts0100411916** — ODB++: BoardThickness not present in ODB++ and output.
- **dts0100414701** — ODB++ : Some, but not all unused component pads not being included in the ODB++ output
- **dts0100441736** — Push Drawing cell: Fixed Text rotation/mirroring issue when drawing cell is pushed
- **dts0100460402** — Translation: Fixed crashes during SKILL extraction for Allegro to ExpPCB translation
- **dts0100546511** — Translations: LMS2EXP and BS2EXP do not convert Fablink and LMS Drawing and Generic Geometry Type geometries
- **dts0100582670** — Review Hazards: All to All for Estimated Crosstalk definitions within CES does not get reported correctly in Review Hazards
- **dts0100587429** — RF: Support for parametric meanders
- **dts0100599826** — ODB++: Support teardrop attribute on teardrops wrote out in ODB++
- **dts0100600978** — MVO: Support for traingle pattern MVO
- **dts0100604331** — Mouse stokes: "Displays help on strokes" shows the main "ExpeditionPCB user guide" screen instead of "Mouse strokes" help page.
- **dts0100606070** — Review Hazards: All to All for Estimated Crosstalk definitions within CES does not get reported correctly in Review Hazards
- **dts0100615628** — DXF: Mounting Hole Plane Clearance incorrectly generated by DXF Export as 1/2 the Clearamce in PCB, when the Clearance is a complete Circle.
- **dts0100616066** — Translation: Library translator must automatically handle geometry technologies

- **dts0100617638** — Dynamic Planes: A modified Thermal tie width can get reset when a part is within a rule area on closing and opening the design
- **dts0100619854** — OpenGL: Outline data disappears if you turn on the check box of mirror view on display control.
- **dts0100627530** — OpenGL: Locked Traces at 45˚ disappear in mirror View when zooming in
- **dts0100634697** — PDF: Engine can't generate the same PDF output file as Extended Print.
- **dts0100637367** — PDF: Find within PDF output for RefDes does not zoom in enough to the part
- **dts0100643663** — Editor Control: Cannot set .025mm (Route) grid with .125mm (via) grid which should be supported
- **dts0100645803** — Export CCZ: Fixed performance degradation on export of CCZ
- **dts0100652559** — ODB++: Exported ODB++ file can create an error in Valor Universal Viewer
- **dts0100652703** — ODB++: Add Drill Tolerances to ODB++ Output
- **dts0100653017** — ODB++: Some properties appear in ODB++ file with spaces instead of underscore
- **dts0100673009** — Dynamic Planes: Switching to Variant design view changes display of plane metal
- **dts0100681869** — Plane Obstruct: Dipslayed incorrectly when on all layers, stays vissible when in display control "Planes shapes and obstructs" is turned off
- **dts0100682765** — Documentation: Expedition PCB User's Guide, Interactive Routing, Test Points Documentation has some errors
- **dts0100689247** — PDF: Old Export PDF options to add Header or Trailer text that were available in Expedition are missing from Extended Print PDF export
- **dts0100690256** — PDF: Find location is incorrect in generated output
- **dts0100694484** — Testpoints: Locking testpoint causes open netline to appear
- **dts0100695981** — Dyanmic Planes: Short between tie-legs and plane in graphics and gerber files
- **dts0100702196** — Reuse Blocks: Net(0) is not taken over netname / netclass when passing through net contains more than ONE via.
- **dts0100703690** — Cell Editor: Window cannot be restored from the taskbar in Windows 7 64-bit
- **dts0100704366** — ODB++: Mechanical cells have same reference in ODB++ file and should be unique

- **dts0100706839** — Automation: Pro Batch Engine objects "PDFOutput" and "PDFOutputSheet" ignore several property values
- **dts0100707014** — ODB++: Multiline properties on parts included in ODB++ data break downstream tools
- **dts0100709606** — Editor Control: Net filter and grid settings doesn't get applied if a design is on a remote server and using RSCM
- **dts0100710109** — Automation: PadstackEditor - Need ability to control units for individual objects via automation
- **dts0100711804** — Dynamic Planes: Unable to assign any net to a Plane Layer 13 in Plane Assignment dialog
- **dts0100713753** — Translators: Error during techfile translation for Allegro too ExpPCB - Unexpected token '<layerSet>'
- **dts0100714993** — Automation: AssemblyRefDes has to be called twice for AssemblyOutlines to be made visible
- **dts0100715769** — ODB++: Information on User layers missing in ODB++ output
- **dts0100717219** — Gerber: ARCs with dashed line style are exported as circles incorrectly
- **dts0100717389** — Documentation: The tolerance of "T" Topology is taken from the default entry and NOT from CES.
- **dts0100718513** — Cell Update: Cell modification cause loss of Thermal Overrides after FWDAnno or Replace Cell
- **dts0100719624** — Dynamic Planes: A thermal tie does not keep the Rotation rule in defined in Plane Classes
- **dts0100720308** — Automation: NC Drill generated by automation changes the drill prefs file Quantity to HoleName and deletes Title lines
- **dts0100720576** — Extended Print: Output PDF causes arcs in a polygon shape to be output as circles.
- **dts0100722578** — Dynamic Planes: Metal Shorting to pads for a specific use case.
- **dts0100723915** — Export CCZ: CCZ output with Cell option has performance issues
- **dts0100724880** — Automation: Cannot set EPcbPlaneDataState with automation because its ReadOnly
- **dts0100725225** — Automation: Component.Place does not use the bottom cell from the PDB
- **dts0100725411** — Automation: The DRC engine in Automation Pro can't read the drc file of EE7.9.
- **dts0100726304** — Copy Trace: Crashes Expedition PCB for this use case.

- **dts0100726449** — Export HyperLynx: Does not include Part Numbers for RLC if VALUE property is specified in PCB
- **dts0100726529** — Review Hazards: Crash after Update Hazard Count selected Review Hazards
- **dts0100727543** — Move Part: Crashes when the designer moves a specific part in this use case.
- **dts0100728224** — Plow: Crashes on attempting to route Diff Pair breakouts which were created by Copy Trace
- **dts0100730651** — Dynamove: Doesn't shove the selected segments like previous releases.
- **dts0100731959** — ODB++: Donut pad is not filled in ODB++ output
- **dts0100734078** — PDB Editor: Does not delete Symbol Reference if part is deleted.
- **dts0100734334** — Extended Print: assembly bottom text appears on assembly top
- **dts0100734768** — DRC: Expedition uses Octagonal clearances around round Via and SMD pads instead of a truly round clearance for DRC
- **dts0100734980** — ODB++: Output using metric option cannot create IPC netlist in vSure
- **dts0100736423** — Plow: Cannot route a group of vias and smt pins of the same net because of loop prevention.
- **dts0100736815** — Forward Annotation: Improved loading performance of a keyin netlist with cell containing very high pin count
- **dts0100737021** — Forward Annotation: Fixed crash when local cell database does not match design.
- **dts0100738414** — ODB++: Missing Smd pads in parts using the pkg group 'Bare die' in output
- **dts0100738812** — EVM: Fixed performance decrease in Expedition if working with EVM with hazard graphics enabled.
- **dts0100738825** — Automation: Expedition will crash if a reference designator of a component is part of a group will be changed using Automation
- **dts0100739828** — Dynamic Planes: Modification of cell cause loss of tie-leg edits after FWDAnno in design
- **dts0100741401** — Review Hazards: When reviewing Differential Pairs --> Convergence hazards software can crash.
- **dts0100742628** — Dynamic Planes: Fixed Thermal tie shorting to different pad with different net names within design
- **dts0100743244** — Extended Print: PDF output shows reference designators for Test Points - TP's.
- **dts0100743438** — Dynamic Planes: Thermal Overrides can cause shorts in some designs

- **dts0100743808** — Review Hazards: Selection of Online->Match Lenth hazard crashes in this design when VP's are not placed
- **dts0100744621** — Translations: Fixed Allegro to Expedition skill script error
- **dts0100745673** — Dynamic Planes: Fixed Short between Plane and traces within design
- **dts0100745843** — Translators: Centlib.prp file within seed library is corrupted when property is added by translator.
- **dts0100746197** — DRC Visualization: Expedition can crash when fixing errors after DRC Visualization is run.
- **dts0100747100** — Translators: Allegro to Expedition translation issue - padstack could not be found
- **dts0100747451** — Translators: Missing pad error translating from Allegro to Expedition
- **dts0100749488** — MVO: Expedition can crash if we place multiple via's into a custom pad
- **dts0100750131** — Variant Manager: Manage Fablink XE variant data when design data changes make it out of date.
- **dts0100750552** — Export ICX: Duplicate Plane shapes with same coordinates with obstructs causes crash
- **dts0100753163** — Forward Annotation: Uses large amount of memory with DC/DV Net Properties design
- **dts0100754176** — Translators: Generating Padstack HKP FIle fails in Allego to Expedition translation for buried/blind vias
- **dts0100754424** — Draw: Excessive memory usage when dragging and panning in Draw mode
- **dts0100755439** — BGA Escapes: Expedition can crash when routing to escape border
- **dts0100755834** — Dynamove: Memory Leak when stretching serpentine trombones with arcs manually rotated at 45 degrees
- **dts0100756859** — Forward Annotation: A crash can happen if test point RefDes changes in the schematic conflict with layout test points.
- **dts0100756913** — Copy Trace: Expedition can sometimes crash when coping vias
- **dts0100757720** — Variant Manager: Takes a long time to show the Variant view and selecting the parts.
- **dts0100757764** — Dynamic Planes: Creates short when moving a traces within plane for this testcase.
- **dts0100758280** — Translations: Skill scripts for Allegro to Expedition translation not handling layers correctly for Allegro V16.3. All features are on Layer 0.
- **dts0100758922** — Export Gencad: GenCad placing bottom component pads and testpoints on TOP in GenCad

- **dts0100759521** — Teardrops: Crash when attempting to open design for edited teardrops on T-Junctions
- **dts0100759599** — Copy Trace: DRC off to add multiple vias to SMD pad snaps to pad orgin
- **dts0100759653** — Variant Manager: Crash when creating FLXE variant data specific to padstacks with very long names
- **dts0100759852** — Dynamic Planes: Expedition can crash when creating the Tear drops with Dynamic Planes enabled.
- **dts0100759994** — ODB++: Generated using automation engine is missing tie legs to some parts.
- **dts0100760228** — Review Hazards: Expedition crashed when CES constraint class name has "-" and is a matched group.
- **dts0100760715** — Translators: Error when migrating with LMS to Central Library
- **dts0100761579** — Export CCZ: Crash when exporting CCZ and padstacks are missing from design
- **dts0100761861** — Review Hazards: Place and move of 7 specific parts makes the design crash when hazard graphics enabled
- **dts0100762251** — ODB++: Dropping SMD Pads on many parts when part of Bare Die cell type
- **dts0100763876** — Plow: Crash during plow when pad growing is enabled.
- **dts0100764104** — Dynamove Trace: Crash can occur when moving trace in specific design situation.
- **dts0100765152** — RF: Expedition PCB crash when change the RF group clearance rule
- **dts0100765179** — RF: Expedition crash when import RF part -filter from ADS
- **dts0100766437** — Plow: Improved plow when using Any Angle Push/Shove when vias are under pads.
- **dts0100769632** — Library Services: Drawing cell user layer text gets moved to Assembly layers when having > 130 user layers
- **dts0100729143** — Xtreme PCB: Failed to open in Xtreme because of a layer stackup issue, PCB Diagnostics now fixes this issue.
- **dts0100739203** — Xtreme PCB: Session running out of sync after Batch DRC because of duplidate mechanical cells in same location
- **dts0100751760** — Xtreme PCB: session crash when placing a multivia object
- **dts0100734941** — Xtreme PCB: Client failed to load initial design copy of design for specific use case.

Known Problems and Workarounds

- dts0100003060 — Renumbering pins creates netlines between pins with different pin number

  Workaround: Temporarily add additional pins and rename the new pin to be one of the problem pins. Then the pin can be renumbered and the net name will change.

- **dts0100157420** — Reuse Blocks do not support instantiated padstack or cell changes being replicated once placed in design.

  Workaround: Instance changes made in the RB physical circuit in the library must be manually done after placed in a target design.

- **dts0100324957** — Detailed View and Display Control menu open can crash application when running Print preview.

  Workaround: Close Display Control before running print preview.

- **dts0100459782** — Expedition can crash when trying to subtract text from draw object.

  Workaround: Don't subtract text from draw object.

- **dts0100497372** — RF: When running OpenGL the field displaying 'dx/dy, Angle and Len' is not refreshed correctly.

  Workaround: Turn off OpenGL

- **dts0100569838** — Expedition can crash on exit due to testpoints with missing pins

  Workaround: Design can be fixed by resetting cells

- **dts0100654997** — Adv. Packaging: Virtual Pins that are auto balanced do not move correctly when Wire Bonds are used within the Topology.

  Workaround: Move the Virtual Pin to the user defined location manually.

- **dts0100655360** — Changing nets from Complex to Custom Topologies will not remove the existing Virtual Pins from the nets topology.

  Workaround: Change from Complex to MST, apply this topology within ExpPCB, then change to Custom.

- **dts0100674723** — Windows 7 - Copying Trace with a large copy set has a very difficult time refreshing after pan and zoom. Makes it impossible to place.

  Workaround: Turn on View-Enable OpenGL, and these problems will go away.

- **dts0100678308** — Sandboxes restricted to only allow parts on bottom will not allow parts to be moved.

  Workaround: Enable editing for both Top and Bottom.

- **dts0100711280** — Review Hazards not immediately updating on Update Hazard Count for hazards introduced by new constraints in CES

  Workaround: The Review Hazards Dialog may need to be closed and reopened to refresh the dialog when CES Constraint changes are made.

- **dts0100722441** — OpenGL mode does not work on Linux using latest driver for ATI Radeon

  Workaround: There are two possible workarounds:

  1.Use the older driver (ati-driver-installer-10-7-x86.x86_64).

  2.Delete the mgc_egs_prober executable from the install location.

- **dts0100751147** — Allow multiple undocks or change documentation to say only one undock is allowed

  Workaround: Once you have Undocked a design, use Job Wizard to make multiple copies of the Undocked design.

- **dts0100765638** — New value of thermal conductivity set in CES stackup does not show up in BoardSim when a board is extracted from ExpeditionPCB through PI interface

  Workaround: Manually enter the thermal-conductivity values directly in HyperLynx's Stackup Editor.

- **dts0100582670** — Do not support All to All for Estimated Crosstalk definitions within CES. Review Hazards will not report violations.

  Workaround: Define the rules by net or netclass.

- **dts0100687645** — Expedition crashes when closing form editor without stopping the forms execution

  Workaround: Select the "black square" icon in the Form Editor which causes the form to stop executing. Once you have done this, selecting the X on the form will no longer crash.

- **dts0100717455** — Project file was not updated with a new RootBlock name which caused Packager failure

  Workaround: If working concurrently on Linux with DxD and Expedition PCB, first exit Expedition PCB if you are going to rename the root schematic in DxD.

- **dts0100719583** — rule areas can not be assigned to schemes with names longer then 40 chers

  Workaround: If characters exceed 40 on Net Class scheme, rename it to something less than 40 if you are to assign this to a Rule Area in Expedition.

- **dts0100721130** — Update RB does not work if changes are made to Expedition variant grid within the CL

  Workaround: The changes must be made to the front-end then FA must be run in the RB editor. This will activate the Update RB process.

- **dts0100724089** — We are no longer flagging Pad Entry hazards if you turn on and then off Extended PE/Allow Odd Angle

  Workaround: Pad Entry Hazards can be put back by turning off Extended Pad Entry/Allow Odd Angle in two steps. Step 1: Uncheck Allow Odd Angle and Hit Apply. Step 2: Uncheck Extended Pad Entry and Hit Ok.

- **dts0100772121** — Graphics on user layers may not be visible if the design contains more than the supported 250 user layers

  Workaround: Do not exceed the supported number of user layers (250) in the design.

- **dts0100725213** — Xtreme/AdvTopo - Locking traces on net with balanced loads causes VPs to move

  Workaround: Semi-fix the VP, then lock the traces.

Chapter 6
Extended Print

Problems Fixed

- **dts0100646885** — Extended print of multiple pages results in filled areas that should not be filled
- **dts0100739777** — Some circles will be big size in the HPGL2.

Known Problems and Workarounds

- **dts0100469574** — Can not print layout design on LaserJet printer

  Workaround: Use 64 MB printer. It works fine. Problem is with using 32 MB printer.

- **dts0100469945** — Nothing prints when trying to use the spooling command

  Workaround: User needs to use valid switches.

- **dts0100480126** — Ezprint GUI sub window i.e load configuration is not active.

  Workaround: The user has to select the EzPrint window, drag it so that he can view the Configuration window and then select the Configuration window.

Chapter 7
FabLinkXE

Problems Fixed

- **dts0100541882** — Drawing Editor checks out xefablinkpro license if it exists
- **dts0100640867** — Missing Layer order control (i.e. which layer is plotted on top of which layer).
- **dts0100670252** — Rule Area's are visible in PDF Outputs of Drawing Editor
- **dts0100674996** — Can not fill page when using the Assign Current View option in Expedtion PCB
- **dts0100679347** — Contour pattern is always shown as filled in PDF when it is set to different fill pattern in Display Control dialog
- **dts0100680566** — Drawing Editor Crashes while re-refferencing the design.
- **dts0100680770** — PDF from Drawing Editor is not WYSIWYG
- **dts0100702949** — ODB++ omitting custom layer
- **dts0100716549** — For Panel design, PDF output does not show proper Hash pattern
- **dts0100717855** — crash when importing PCB
- **dts0100740612** — Fablink XE crashes after File> Export> CCZ if any design is not placed on a panel
- **dts0100741275** — For a PCB instance, Data on User draft Layers as DXF -Assy Part Number Top/Bottom is missing in pdf - WYSWYG
- **dts0100747945** — Manufacturing Output Validation shows lots of unknown errors and stops due to maximum hazards(10,000)
- **dts0100762039** — FablinkXE freezes by Extend in Draw mode toolbar

Known Problems and Workarounds

- **dts0100496447** — DE :layerstackup representation is not correct in Drawing Editor

  Workaround: User can manually edit the text in layer stackup as required

- **dts0100676731** — When one of the Variant definition is deleted in ExpeditionPCB, Drawing Editor crashes during design update

  Workaround: If the variant has been deleted in the design and is used in the Drawing Editor, please update the variant assignment for the deleted variant instance to the one which exists before doing the design update or design reference. Or update design data.

- **dts0100680244** — FablinkXE crashes while generating NC drill data on Panel in which board placed with flip option.

  Workaroud: Do not add new "custom columns" or "FCF" on a panel till NC Drill is generated once for the placed design. Once it has been generated, then subsequently there is no issue in using this.

- **dts0100703708** — FablinkXE shows additional Board outline for a design with pending FA

  Workaround: After packaging the design, before opening Fablink XE, the user needs to invoke BSXE and perform Forward Annotation, then open the design in Fablink XE.

- **dts0100713332** — If negative plane data has not been generated, cannot cancel Gerber Output and save settings

  Workaround: There is a workaround for this issue (i.e. to generate the gerber after generating negative plane data

- **dts0100760031** — Drawing Editor crashes during paste detail view.

  Workaround: "Copy and Paste without doing Edit in Middle". If you do edit, then select again and do copy

- **dts0100775770** — If placed design size exceeds Drawing sheet Border, DE crashes while placing design using Drawing Setup dialog box

  Workaround: Parag: In Drawing Editor on Solaris platform, using Drawing Setup dialog box do not place designs that are larger than the sheet border.

Chapter 8
HyperLynx Analog

Problems Fixed

- **dts0100641822** — Spice primitive resistor should not have TC3 property when HLASE simulator is set
- **dts0100654604** — When I enter a PHASE value in the SpicePrimative:v_sin source, the resultant sine wave in the simulation does not shift over in the transient simulation
- **dts0100672762** — Document ADMS versions that are compatible with Hyperlynx Analog
- **dts0100686494** — HLA should include the subcircuit referenced by another subcircuit
- **dts0100692536** — HLA should accept variable parameter values
- **dts0100728716** — AMS2010.2 support
- **dts0100734231** — Linux - 'Client Application has not connected after 30 seconds' error and Ezwave does not start.

Known Problems and Workarounds

- **dts0100719006** — Generics not managed properly with block multi-instantiation

  Workaround: Change design methodology. To create a block with a different name if there is a need to use different generics in one of the blocks.

Chapter 9
iCDB

Problems Fixed

- **dts0100679016** — Case sensitivity and the PathsMap.cfg in a mixed platform environment
- **dts0100715274** — Auto backup of iCDB should be time based
- **dts0100715547** — RSCM Server cannot be installed stand alone
- **dts0100725722** — Documentation implies iCDBNetServer ports do not require opening if not using RSCM
- **dts0100726556** — icdb.dat in the library's Cert\database folder is updated simply by selecting the entry in DxDesigner
- **dts0100728293** — batchInstall.BAT fails with Update install when iCDB Server Monitor is not selected in Base install
- **dts0100747414** — CES shows net (connected to RWTERM symbol) which should be excluded from list of physical nets in the design.

  ```
  ERROR - Physical net '$1N6610' referenced in CES by electrical net '$1N6610' was not found in the layout design.
  ```

- **dts0100748431** — RSCM daemon going deadlocked
- **dts0100750987** — Archiver prompts Requesting emergency server stop and MiniDump and fails to create correct archive
- **dts0100757566** — icdb diagnostic warnings
- **dts0100758846** — When files exist in the cdbback folder, iCDBNetServer can grow to enormous sizes

Known Problems and Workarounds

- **dts0100637765** — After RSCM is down CES was unable to reconnect.

  Workaround: All users need need to open project in the same way (UNC or mapped drive)

Chapter 10
ICX Pro Explorer

Problems Fixed

- **dts0100694900** — ICX PRO crash on simulate net with EBD
- **dts0100717922** — ICXPro - Unable to write results spreadsheet data using the "Save Copy As..." function from the spreasheet itself
- **dts0100697429** — ICXPro Explorer: Cannot find 'Calculated Er for metal layers from surrounding dielectrics' in user guide

Known Problems and Workarounds

- **dts0100328520** — Sweeping stackup and tline in ICX Pro Explorer advance lab3 cause Waveform Analyzer out of memory

  Workaround: set environment variables ICX_WFM_ANALYZER_INITIAL_MEMSIZE and ICX_WFM_ANALYZER_MAX_MEMSIZE to higher values, like 512M and 1024M
- **dts0100405823** — when a SPICE model is edited, the change is ignored and the simulator continues to use a cached version of the model

  Workaround: Force to reload those kind of models manually in Model Manager to pick up the model changes and update the Model Builder cache
- **dts0100519995** — Local Cache incompatibility between unix and WinXP/WinVista platforms for vhdl models

  Workaround: remove Local Cache directory when running ADMS simulation between different platforms
- **dts0100703560** — ICXPro/ADMS - Need to document OS requirements for Linux support of the 2009.2b ADMS release

  Workaround: Run the software on Linux 5.3 (update 3) or greater

- **dts0100652099** — can't export a net to ICX Pro Explorer from CES (invoked from BA) when ICX Pro Explorer window is opened with diffrent net extracted

  Workaround: Turn off UAC (User Account Control) and restart the machine. If you want to have UAC enabled turn it on after restart. You will have to reboot the machine again but it solves the problem.

  To turn off UAC:

  a. Click Start, and then click Control Panel

  b. In Control Panel, click User Accounts.

  c. In the User Accounts window, click User Accounts.

  d. In the User Accounts tasks window, click Turn User Account Control off.

- **dts0100770964** — No information in ICX Pro Explorer documentation that Thermal Conductivity cannot be used in simulation

  Workaround: These values are not passed to HyperLynx Thermal via the interfaces, these need to be reset in HyperLynx thermal (from HL 8.2 release)

- **dts0100771799** — Can't export a net to ICX Pro Explorer from CES launched from BA or Layout tools in RE flow

  Workaround: Invoke Explorer from command line and open the .tms file generated from CES export.

- **dts0100775006** — Single-ended vias and differential via is mixed up for this test case

  Workaround: Generally differential pairs should be routed with differential vias, however in some cases we may use single-ended vias in a differential pair. Export of differential pair from ICX Pro Verify to HyperLynx LineSim has some limitations in this scenario. It is recommended to analyze the via structures in ExpeditionPCB and correct via models in LineSim if necessary. Editing of vias in HyperLynx can be done in padstack editor dialog. User can add via or differential via to the exported schematic to replace or correct the existing via models in HyperLynx using symbol palette.

Chapter 11
ICX Pro Verify

Known Problems and Workarounds

- **dts0100517882** — Design could not be loaded into ICX Pro Verify stand-alone while could be into Expedition PCB

  Workaround: Open the design in ExpeditionPCB first and than load the design in Verify

- **dts0100718866** — removed static overshoot high constraint should not have any impact on actual value for dynamic logic low state

  Workaround: To get the dynamic overshoots measured, _both_ static low and static high limits must be defined

Chapter 12
Installation

Problems Fixed

- **dts0100702154** — If the restart of the computer by the installer of GW2ODB (ODBGateway to ODB++Install) of EE7.9 is done, after a restart, a script error will occur and the installer of EE7.9 will be canceled.
- **dts0100731008** — ERROR: The system was unable to find the specified registry key or value.
- **dts0100743966** — Client - Server Expedition batch install needs manual intervention
- **dts0100756008** — EE7.9, EE7.9.0 and EE7.9.1 can't coexist on Linux without deleting the mainwin registry:

Chapter 13
I/O Designer

Problems Fixed

- **dts0100274676** — Error when the Xilinx pin file name is .PAD (instead of .pad)
- **dts0100605410** — IOD 7.4 not allowing assignments from Quartus II 9.0, QSF file, for differential pairs.
- **dts0100606974** — Related to dts0100345625. This is for IOD8.0. It needs to support ee2007 DxDesigner project settings for borders.
- **dts0100614855** — Net Name Delimiter setting is not used
- **dts0100614950** — IOD 8.0 Does not recognize the "use ieee.std_logic_misc.all;" line in VHDL files
- **dts0100692612** — Import/Export of Quartus 9.1 QFS constraints file into/out-of IOD is corrupting the constraints file
- **dts0100720178** — EE7.9.1: When local PDB option is chosen, exporting symbols to CL resulted in two errors/warnings.
- **dts0100721114** — Unable to generate schematic sheets with custom border.
- **dts0100730724** — IOD crashes (iod_dx.exe), when attempting to import symbols
- **dts0100731381** — Crash during updating .fpc using .pin file
- **dts0100741048** — IOD should rather use borders from CL than adding borders to local symbols
- **dts0100745410** — Customer needs to use devices not yet included into the tool library
- **dts0100750587** — Bad allocation error when attempting to open FPC database in IOD.
- **dts0100752733** — lpc is not supported in WG but message about license is displayed
- **dts0100765282** — DIFFCLOCK type unavailable for specific pin/pins
- **dts0100766126** — Customer requires FPGA device

Known Problems and Workarounds

- **dts0100472491** — Symbol pins are out of grid after schematic and symbols export to DxD in case of different grid settings.

  Workaround: Please ensure the same grid settings between DxDesigner and I/O Designer before symbol's creation in I/O designer.

- **dts0100511732** — IOD fails to read in Quartus generated xChange file

  Workaround: Change\use for all those IO standard names only upper case letters.

- **dts0100635126** — Import from DV schematic is required even after import

  Workaround: 1) Open schematic in Design View

  2) Import Schematic Design again

  Status of Schematic Design now match

- **dts0100635569** — Error messages when DV project without CES is used

  Workaround: Enable CES to read net ordering data properly and to avoid error messages

- **dts0100637000** — IOD no responding for 12 min after select all pins (cross probing on)

  Workaround: Don't select large number of pins if cross probing is turned on.

- **dts0100639987** — Exporting Part Data works improperly in case Expedition is running.

  Workaround: Close Expedition PCB while export PDB is performed

- **dts0100644719** — Not valid error message is displayed and layout is not shown after saving scheme

  Workaround: Reload database

- **dts0100670942** — [Symbols Generator] If symbols are created with Flat design type then there should be no warning about signals not placed on functional symbol.

  Workaround: Please ignore the warnings

- **dts0100679922** — [Symbols Generator] Hierarchical connection broken after create/update symbols.

  Workaround: It is highly recommended to re-create symbols with new Symbols Generator instead of using symbols created in older IOD versions in order to avoid such problems.

- **dts0100681038** — IOD does not use HDL signal name during resizing bus

  Workaround: After resize do following steps:

  1) Start Signal "Rename" and change existing "HDL name" to any other name. Accept change

  2) Start Signal "Rename" again and change to required value. Accept change

- **dts0100682528** — Wrong color settings for ports are used during export to DV

  Workaround: Use "Graphic line" preference to set port color

- **dts0100683321** — [Symbols Generator] For databases with old symbols, duplicated pins can occur on symbols after SG is run to create symbols

  Workaround: Recreation of all symbols with new SG does not give the effect and no duplicated pins are created.

- **dts0100684754** — Assignment is not restored after extending bus and undo

  Workaround: Restore assignment manually

- **dts0100685174** — Importing swap from DV project does not work when "Pin number" is used as port label

  Workaround: Use "Pin name" as port label. Do not use "Pin number" as pcb port label

- **dts0100716173** — IOD doesn't check if user can edit symbol in case of library from DMS

  Workaround: Checkout symbols and part before exporting from IOD to CL

- **dts0100752023** — Default IO standard is not exported to CES

  Workaround: If you want all I/O Standards to be set in CES, please change all I/O Standards in IOD to non-default values and export them to CES

- **dts0100766090** — Provide to backward compatibility in constrain which set current strength (MAX_MA, MIN_MA)

  Workaround: Open constrains file in text editor and replace:

  CURRENT_STRENGTH_NEW "MAX_MA" to CURRENT_STRENGTH_NEW "MAXIMUM CURRENT and

  CURRENT_STRENGTH_NEW "MIN_MA" to CURRENT_STRENGTH_NEW "MINIMUM CURRENT"

- **dts0100767099** — Borders are not placed when was not already used in DxD schematic

  Workaround: Open DxD, insert border you want to be generated by IODesigner on any schematic and then remove placed border. Export schematic from IOD to DxD again. Now border is properly placed

- **dts0100769440** — Diff buses on functional symbol are wrongly updated after rerange

  Workaround: Delete symbols and generate new set of symbols

- **dts0100598642** — [WG2007.6]IOD asks for path to project file during exporting schematic from synchronization wizard

  Workaround: Use Export/Schematic and Symbols from main menu instead of exporting from Synchronization Wizard

- **dts0100634294** — IOD exports broken schematic. Functional block is empty.

  Workaround: Functional symbols' names should be different than design name as it causes problems in IOD-DxD integration.

- **dts0100636152** — IOD can create netlist project only for PADS.

  Workaround: Create netlist project in DxDesigner, select layout tool: Allegro

- **dts0100637257** — Schematic update tool fails if DxDesigner was not started before (not registered) on linux.

  Workaround: Please start/register DxDesigner before schematic update tool is used.

- **dts0100716494** — Update Power Signal doesn't delete power signal which are not needed

  Workaround: Delete all power signals and run Update Power Signals again.

- **dts0100716742** — I cannot recreate symbols with the same settings until I remove all of my symbols before.

  Workaround: Please remove all symbols before you create them.

- **dts0100718856** — Builtins are placed improperly from time to time - no connection on IOD generated schematic. Package failed in DxD.

  Workaround: Export schematic once again from I/O Designer - after second and further exports builtins are connected properly.

- **dts0100720197** — EE7.9.1: Exported symbols in CL don't show their attached pictures.

  Workaround: Add requested graphics through Symbol Editor.

- **dts0100720675** — It's possible to lock only one element of diff signal.

  Workaround: To lock differential signal please select its parent.

- **dts0100720799** — Export symbols to central library overwrites symbols even if they are already locked.

  Workaround: Ensure the symbol in the central library symbol partition is not locked (open or being edited) before overwriting symbol with the same name (and version) from IOD

- **dts0100722155** — During apply scenario there are assignment errors and it is caused by unravel with 'Use unused pins'.

  Workaround: In FPGA database set swap group for all unassigned pins to empty

- **dts0100774839** — [WG] Different colors are used for iod generated symbols on Symbol View and on generated schematic

  Workaround: To change color of generated symbols, change setting for "Graphics Rectangle" to required color

Chapter 14
Librarian Flow Manager

Problems Fixed

- **dts0100596542** — DMSL/LFM: drop-down for selecting partitions is not in alphanumeric order.
- **dts0100758216** — To delete a cell in DMSL/LFM, the Package must first be deleted in DMS. This is a regression from DMS7.8!

Chapter 15
Library Manager

Problems Fixed

- **dts0100405857** — Part disappears out of library after Move if conflicting pin definition
- **dts0100591940** — Symbol Editor is very slow when working with lots of pins
- **dts0100703493** — Server/client install: Library Manager will not run
- **dts0100725044** — Pin name is changed unintentionally in some case
- **dts0100733646** — Add DXDB_LIBNAME to Property file (DxD flow only)
- **dts0100736089** — Symbol Editor Crashes When Trying to Edit Properties
- **dts0100736269** — Special properties for annotate symbols cannot be added
- **dts0100737790** — Cell Editor Automation of EE7.9.1 became very slow compared with EE2007.8.
- **dts0100743199** — Extraneous Placement Outline data crashes Cell Editor even in EE 7.9.1
- **dts0100745849** — Server/client install: Library Manager will not run without copying vec70.dll to system32 on client machine.
- **dts0100746940** — Symbol Editor crashes when dragging vector pin from Pins window onto symbol - crash
- **dts0100751982** — Symbol editor crashes when renaming set of pin names using Symbol > ADD Properties os Symbol Editor.
- **dts0100757452** — Padstack editor crashes if you use editor commands after using "delete" key on the keyboard.
- **dts0100769240** — Duplicated pins after Save As

Known Problems and Workarounds

- **dts0100002473** — Need to keep symbol being moved into a full Symbol Library.

  Workaround: Create and use multiple symbol partitions. Do not store all symbols in a single symbol partition
- **dts0100018307** — Option to overwrite existing data in library, regardless of TIMESTAMP

Workaround: Delete the time stamp information from the CELL_OPEN line. Example, every symbol opens with a *CELL_OPEN line that contains time stamp information (e.g.: *CELL_OPEN +2.5V 9 2005/01/28@15:03:19) . For each symbol that needs to be modified, the date@time portion should be removed so that it is regenerated upon running ASCII_In.

- **dts0100155914** — ASCII Import ignored data not flagged as warning

  Workaround: Ensure that all solderpaste objects in a cell are closed shapes (for example, rectangles, polygons, and so forth) to avoid this problem.

- **dts0100156288** — Open polyline SolderPaste objects

  Workaround: Solderpaste objects must be a closed polygon.

- **dts0100330431** — Signal Vision / Signal Analyser checkbox is grayed out but CHECKED in case of DxD library

  Workaround: Temporarily change the FlowType key in the CL's .cfg file from "DX" to "DC" ; Open LM and unCheck the box, Close LM, change the FlowType key back to "DX"

- **dts0100395519** — Vertical coordinates entered in tcl commands seem to be mirrored

  Workaround: Normally, Positive coordinates entered are to the right or above the origin, and negative coordinates are to the left or below the origin, depending upon X or Y axis.. When using the Dx Symbol Editor API, these coordinates are reversed.

- **dts0100415649** — Parts and Cells used in UnVerified ReUse blocks can be deleted from the CL. An error should be issued (as currently done with Verified RBs).

  Workaround: Ensure that all Reuse Blocks are Verified before deleting any parts and cells from the Central Library

- **dts0100453024** — Error changing DC flow LT to "CES Enabled": "Unable to access the LogicDB at Work\Layout_Temp\LogicDB.lgc"

  Workaround: Ignore the error message

- **dts0100459897** — DC Reuse: FA Error attempting to Migrate UnVerified (without RB cell) CES-enabled DC-flow RB

  Workaround: Manually enable CES for Reuse Designs after migration

- **dts0100460114** — Dx Reuse: Plane definition is lost after FA during Reuse Verification.

  Workaround: Re-define the Plane definition when Reuse Block is placed in the Host design.

- The only plane definitions that will be seen by the user are the ones based on a physical plane shapes placed within the RB Cell.

- **dts0100489429** — In the RB editor, Save RB function looks at the iCDB snapshot in the Back-end when checking to see if all instance data is absorbed

  Workaround: Run FA again after Absorbing the schematic data and then Save (Verify) will complete OK.

- **dts0100498141** — Help for DC flow Symbol Editor doesn't work on VISTA

  Workaround: Download the WinHlp32.exe from Microsoft website.

- **dts0100498548** — Error when opening a DC-flow CL when only DC-flow LM is installed: "WDIR EV doesn't contain %SDD_HOME%\standard path."

  Workaround: Add the following path to the WDIR variable:

  ```
  C:\Mentor_2007\2007EE\SDD_HOME\standard
  ```

  If DC is also installed, the path is added automatically.

- **dts0100561271** — "Global Signal Name" written back to ASCII symbol file not NETNAME

  Workaround: (if backward compatibility to 2005.x is required):

  - Modify the global symbols to use NETNAME instead of Global Signal Name.

  - Map NETNAME to "Global Signal Name" in the map.cfg file, on the 2007.5 workstation.

- **dts0100562047** — Incompatibility with 2007 libraries

  Workaround: After migrating the CL to 2007.5, edit the Centlib.prp file and change the Version from 16 to 15 (at the end of the Comments section).

- **dts0100589736** — Linux only - you will get crash of Library Services and Library Manager when you switch from "export to ascii" to "import from ascii" radio butons in Cell tab in Library Services dialog

  Workaround: If after entering an HKP filename, you want to import an HKP file (instead of export), then blank out the filename path prior to selecting the Import button.

- **dts0100621058** — Dual Release Support: If older release has Padstack Editor open, the "Reserved Partition" is lost when same CL is opened (and re-indexed) using 2007.7.

  Workaround: When using a single CL for both old and new version of EE flow software, use the older version of LM to edit the CL (best option), or at least do not edit the CL (padstack editor in this case) using both old and new versions at the same time.

- **dts0100673657** — [Library Manager]: can not invoke Simulation Model Properties Dialog from 2 instances of library manger invoked at the same time

  Workaround: When working with HLA models, use only a single instance of Library Manager. If you need to switch libraries, close LM and reopen a new instance of LM before opening the other Central Library.

- **dts0100676383** — Attempting to Copy a model fails with error "A model file with the same name exists in the destination directory".

  Workaround: When attempting to copy a single model that is located in a .lib fle, manually copy the model information into a new model file and import or copy it into LM

- **dts0100676387** — If a Part is deleted from the CL, its still listed in the "Associated Parts" in the Model Mapping section.

  Workaround: Manually modify xml file in appropriate section to remove the part reference in the Model Mapping.

- **dts0100679981** — RB fails to verify, gives "Error copying iCDB databas"

  Workaround: Turn off .zip files in the Options for Google Desktop

- **dts0100748936** — Cell.Verified() property use 0 to set the status to "verified" and use 1 to set the status to "unverified". It is different from what is defined in the reference manual.

  Workaround: For the Cell.Verified property, use 0 to set the status to "verified" and use 1 to set the status to "unverified". This is different from what is defined for the enumerators in the reference manual.

- **dts0100762946** — Opening a CL by other users from any workstation must be prevented when Library Integrity Checker is running.

  Workaround: Ensure that no other users have the library open in Library Manager or DMS Librarian when Integrity Checker is running.

- **dts0100442194** — Cannot define implicit and explicit power pins in PDB Editor and cannot package

  Workaround: Power pins for a given part must either be defined as implicit or explicit, but not both.

- **dts0100703493** — Server/client install: Library Manager will not run

  Workaround: The current workaround for switching releases is to delete the vec*.dll's from the system32 directory before changing configurations.

Chapter 16
Smart Utilities

Problems Fixed

- **dts0100734342** — Crash when reading a big differential View file
- **dts0100737902** — Generate Cover Layer does nothing
- **dts0100743189** — Smart Utilities: Generate Cover Layer command ignores orientation of padstacks
- **dts0100749045** — Differential View shows the incorrect result for custom pads placed on the bottom side
- **dts0100753994** — Smart Utilities - dynamic tune doesn't work

Chapter 17
Variant Manager

Problems Fixed

- **dts0100653279** — EE Variant Manager: Part Label, Part Name & Part Number all show the same value in schematic Variant View.
- **dts0100720739** — Failed to write Variants to iCDB Database, can't create variants anymore
- **dts0100738205** — cannot save new variants

Known Problems and Workarounds

- **dts0100595777** — RBB: Error issued when generating variant view in DxDesigner using dbc file pointing to remote DMS db.

  Workaround: The error can be ignored since the functionality still works even after the error

Chapter 18
Additional Release Information

- When switching between EE7.9.2 and EE7.9.x, you must run the “configurator clean” option. See technote mg549565 for further details.

End-User License Agreement

The latest version of the End-User License Agreement is available on-line at:
www.mentor.com/eula

IMPORTANT INFORMATION

USE OF ALL SOFTWARE IS SUBJECT TO LICENSE RESTRICTIONS. CAREFULLY READ THIS LICENSE AGREEMENT BEFORE USING THE PRODUCTS. USE OF SOFTWARE INDICATES CUSTOMER'S COMPLETE AND UNCONDITIONAL ACCEPTANCE OF THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT. ANY ADDITIONAL OR DIFFERENT PURCHASE ORDER TERMS AND CONDITIONS SHALL NOT APPLY.

END-USER LICENSE AGREEMENT ("Agreement")

This is a legal agreement concerning the use of Software (as defined in Section 2) and hardware (collectively "Products") between the company acquiring the Products ("Customer"), and the Mentor Graphics entity that issued the corresponding quotation or, if no quotation was issued, the applicable local Mentor Graphics entity ("Mentor Graphics"). Except for license agreements related to the subject matter of this license agreement which are physically signed by Customer and an authorized representative of Mentor Graphics, this Agreement and the applicable quotation contain the parties' entire understanding relating to the subject matter and supersede all prior or contemporaneous agreements. If Customer does not agree to these terms and conditions, promptly return or, in the case of Software received electronically, certify destruction of Software and all accompanying items within five days after receipt of Software and receive a full refund of any license fee paid.

1. **ORDERS, FEES AND PAYMENT.**

   1.1. To the extent Customer (or if agreed by Mentor Graphics, Customer's appointed third party buying agent) places and Mentor Graphics accepts purchase orders pursuant to this Agreement ("Order(s)"), each Order will constitute a contract between Customer and Mentor Graphics, which shall be governed solely and exclusively by the terms and conditions of this Agreement, any applicable addenda and the applicable quotation, whether or not these documents are referenced on the Order. Any additional or conflicting terms and conditions appearing on an Order will not be effective unless agreed in writing by an authorized representative of Customer and Mentor Graphics.

   1.2. Amounts invoiced will be paid, in the currency specified on the applicable invoice, within 30 days from the date of such invoice. Any past due invoices will be subject to the imposition of interest charges in the amount of one and one-half percent per month or the applicable legal rate currently in effect, whichever is lower. Prices do not include freight, insurance, customs duties, taxes or other similar charges, which Mentor Graphics will state separately in the applicable invoice(s). Unless timely provided with a valid certificate of exemption or other evidence that items are not taxable, Mentor Graphics will invoice Customer for all applicable taxes including, but not limited to, VAT, GST, sales tax and service tax. Customer will make all payments free and clear of, and without reduction for, any withholding or other taxes; any such taxes imposed on payments by Customer hereunder will be Customer's sole responsibility. If Customer appoints a third party to place purchase orders and/or make payments on Customer's behalf, Customer shall be liable for payment under Orders placed by such third party in the event of default.

   1.3. All Products are delivered FCA factory (Incoterms 2000), freight prepaid and invoiced to Customer, except Software delivered electronically, which shall be deemed delivered when made available to Customer for download. Mentor Graphics retains a security interest in all Products delivered under this Agreement, to secure payment of the purchase price of such Products, and Customer agrees to sign any documents that Mentor Graphics determines to be necessary or convenient for use in filing or perfecting such security interest. Mentor Graphics' delivery of Software by electronic means is subject to Customer's provision of both a primary and an alternate e-mail address.

2. **GRANT OF LICENSE.** The software installed, downloaded, or otherwise acquired by Customer under this Agreement, including any updates, modifications, revisions, copies, documentation and design data ("Software") are copyrighted, trade secret and confidential information of Mentor Graphics or its licensors, who maintain exclusive title to all Software and retain all rights not expressly granted by this Agreement. Mentor Graphics grants to Customer, subject to payment of applicable license fees, a nontransferable, nonexclusive license to use Software solely: (a) in machine-readable, object-code form (except as provided in Subsection 5.2); (b) for Customer's internal business purposes; (c) for the term of the license; and (d) on the computer hardware and at the site authorized by Mentor Graphics. A site is restricted to a one-half mile (800 meter) radius. Customer may have Software temporarily used by an employee for telecommuting purposes from locations other than a Customer office, such as the employee's residence, an airport or hotel, provided that such employee's primary place of employment is the site where the Software is authorized for use. Mentor Graphics' standard policies and programs, which vary depending on Software, license fees paid or services purchased, apply to the following: (a) relocation of Software; (b) use of Software, which may be limited, for example, to execution of a single session by a single user on the authorized hardware or for a restricted period of time (such limitations may be technically implemented through the use of authorization codes or similar devices); and (c) support services provided, including eligibility to receive telephone support, updates, modifications, and revisions. For the avoidance of doubt, if Customer requests any change or enhancement to Software, whether in the course of

receiving support or consulting services, evaluating Software, performing beta testing or otherwise, any inventions, product improvements, modifications or developments made by Mentor Graphics (at Mentor Graphics' sole discretion) will be the exclusive property of Mentor Graphics.

3. **ESC SOFTWARE.** If Customer purchases a license to use development or prototyping tools of Mentor Graphics' Embedded Software Channel ("ESC"), Mentor Graphics grants to Customer a nontransferable, nonexclusive license to reproduce and distribute executable files created using ESC compilers, including the ESC run-time libraries distributed with ESC C and C++ compiler Software that are linked into a composite program as an integral part of Customer's compiled computer program, provided that Customer distributes these files only in conjunction with Customer's compiled computer program. Mentor Graphics does NOT grant Customer any right to duplicate, incorporate or embed copies of Mentor Graphics' real-time operating systems or other embedded software products into Customer's products or applications without first signing or otherwise agreeing to a separate agreement with Mentor Graphics for such purpose.

4. **BETA CODE.**

4.1. Portions or all of certain Software may contain code for experimental testing and evaluation ("Beta Code"), which may not be used without Mentor Graphics' explicit authorization. Upon Mentor Graphics' authorization, Mentor Graphics grants to Customer a temporary, nontransferable, nonexclusive license for experimental use to test and evaluate the Beta Code without charge for a limited period of time specified by Mentor Graphics. This grant and Customer's use of the Beta Code shall not be construed as marketing or offering to sell a license to the Beta Code, which Mentor Graphics may choose not to release commercially in any form.

4.2. If Mentor Graphics authorizes Customer to use the Beta Code, Customer agrees to evaluate and test the Beta Code under normal conditions as directed by Mentor Graphics. Customer will contact Mentor Graphics periodically during Customer's use of the Beta Code to discuss any malfunctions or suggested improvements. Upon completion of Customer's evaluation and testing, Customer will send to Mentor Graphics a written evaluation of the Beta Code, including its strengths, weaknesses and recommended improvements.

4.3. Customer agrees to maintain Beta Code in confidence and shall restrict access to the Beta Code, including the methods and concepts utilized therein, solely to those employees and Customer location(s) authorized by Mentor Graphics to perform beta testing. Customer agrees that any written evaluations and all inventions, product improvements, modifications or developments that Mentor Graphics conceived or made during or subsequent to this Agreement, including those based partly or wholly on Customer's feedback, will be the exclusive property of Mentor Graphics. Mentor Graphics will have exclusive rights, title and interest in all such property. The provisions of this Subsection 4.3 shall survive termination of this Agreement.

5. **RESTRICTIONS ON USE.**

5.1. Customer may copy Software only as reasonably necessary to support the authorized use. Each copy must include all notices and legends embedded in Software and affixed to its medium and container as received from Mentor Graphics. All copies shall remain the property of Mentor Graphics or its licensors. Customer shall maintain a record of the number and primary location of all copies of Software, including copies merged with other software, and shall make those records available to Mentor Graphics upon request. Customer shall not make Products available in any form to any person other than Customer's employees and on-site contractors, excluding Mentor Graphics competitors, whose job performance requires access and who are under obligations of confidentiality. Customer shall take appropriate action to protect the confidentiality of Products and ensure that any person permitted access does not disclose or use it except as permitted by this Agreement. Customer shall give Mentor Graphics written notice of any unauthorized disclosure or use of the Products as soon as Customer learns or becomes aware of such unauthorized disclosure or use. Except as otherwise permitted for purposes of interoperability as specified by applicable and mandatory local law, Customer shall not reverse-assemble, reverse-compile, reverse-engineer or in any way derive any source code from Software. Log files, data files, rule files and script files generated by or for the Software (collectively "Files"), including without limitation files containing Standard Verification Rule Format ("SVRF") and Tcl Verification Format ("TVF") which are Mentor Graphics' proprietary syntaxes for expressing process rules, constitute or include confidential information of Mentor Graphics. Customer may share Files with third parties, excluding Mentor Graphics competitors, provided that the confidentiality of such Files is protected by written agreement at least as well as Customer protects other information of a similar nature or importance, but in any case with at least reasonable care. Customer may use Files containing SVRF or TVF only with Mentor Graphics products. Under no circumstances shall Customer use Software or Files or allow their use for the purpose of developing, enhancing or marketing any product that is in any way competitive with Software, or disclose to any third party the results of, or information pertaining to, any benchmark.

5.2. If any Software or portions thereof are provided in source code form, Customer will use the source code only to correct software errors and enhance or modify the Software for the authorized use. Customer shall not disclose or permit disclosure of source code, in whole or in part, including any of its methods or concepts, to anyone except Customer's employees or contractors, excluding Mentor Graphics competitors, with a need to know. Customer shall not copy or compile source code in any manner except to support this authorized use.

5.3. Customer may not assign this Agreement or the rights and duties under it, or relocate, sublicense or otherwise transfer the Products, whether by operation of law or otherwise ("Attempted Transfer"), without Mentor Graphics' prior written consent and payment of Mentor Graphics' then-current applicable relocation and/or transfer fees. Any Attempted Transfer without Mentor Graphics' prior written consent shall be a material breach of this Agreement and may, at Mentor Graphics' option, result in the immediate termination of the Agreement and/or the licenses granted under this Agreement. The terms

of this Agreement, including without limitation the licensing and assignment provisions, shall be binding upon Customer's permitted successors in interest and assigns.

5.4. The provisions of this Section 5 shall survive the termination of this Agreement.

6. **SUPPORT SERVICES.** To the extent Customer purchases support services, Mentor Graphics will provide Customer updates and technical support for the Products, at the Customer site(s) for which support is purchased, in accordance with Mentor Graphics' then current End-User Support Terms located at http://supportnet.mentor.com/about/legal/.

7. **AUTOMATIC CHECK FOR UPDATES; PRIVACY.** Technological measures in Software may communicate with servers of Mentor Graphics or its contractors for the purpose of checking for and notifying the user of updates and to ensure that the Software in use is licensed in compliance with this Agreement. Mentor Graphics will not collect any personally identifiable data in this process and will not disclose any data collected to any third party without the prior written consent of Customer, except to Mentor Graphics' outside attorneys or as may be required by a court of competent jurisdiction.

8. **LIMITED WARRANTY.**

8.1. Mentor Graphics warrants that during the warranty period its standard, generally supported Products, when properly installed, will substantially conform to the functional specifications set forth in the applicable user manual. Mentor Graphics does not warrant that Products will meet Customer's requirements or that operation of Products will be uninterrupted or error free. The warranty period is 90 days starting on the 15th day after delivery or upon installation, whichever first occurs. Customer must notify Mentor Graphics in writing of any nonconformity within the warranty period. For the avoidance of doubt, this warranty applies only to the initial shipment of Software under an Order and does not renew or reset, for example, with the delivery of (a) Software updates or (b) authorization codes or alternate Software under a transaction involving Software re-mix. This warranty shall not be valid if Products have been subject to misuse, unauthorized modification or improper installation. MENTOR GRAPHICS' ENTIRE LIABILITY AND CUSTOMER'S EXCLUSIVE REMEDY SHALL BE, AT MENTOR GRAPHICS' OPTION, EITHER (A) REFUND OF THE PRICE PAID UPON RETURN OF THE PRODUCTS TO MENTOR GRAPHICS OR (B) MODIFICATION OR REPLACEMENT OF THE PRODUCTS THAT DO NOT MEET THIS LIMITED WARRANTY, PROVIDED CUSTOMER HAS OTHERWISE COMPLIED WITH THIS AGREEMENT. MENTOR GRAPHICS MAKES NO WARRANTIES WITH RESPECT TO: (A) SERVICES; (B) PRODUCTS PROVIDED AT NO CHARGE; OR (C) BETA CODE; ALL OF WHICH ARE PROVIDED "AS IS."

8.2. THE WARRANTIES SET FORTH IN THIS SECTION 8 ARE EXCLUSIVE. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS MAKE ANY OTHER WARRANTIES EXPRESS, IMPLIED OR STATUTORY, WITH RESPECT TO PRODUCTS PROVIDED UNDER THIS AGREEMENT. MENTOR GRAPHICS AND ITS LICENSORS SPECIFICALLY DISCLAIM ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY.

9. **LIMITATION OF LIABILITY.** EXCEPT WHERE THIS EXCLUSION OR RESTRICTION OF LIABILITY WOULD BE VOID OR INEFFECTIVE UNDER APPLICABLE LAW, IN NO EVENT SHALL MENTOR GRAPHICS OR ITS LICENSORS BE LIABLE FOR INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOST PROFITS OR SAVINGS) WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY, EVEN IF MENTOR GRAPHICS OR ITS LICENSORS HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. IN NO EVENT SHALL MENTOR GRAPHICS' OR ITS LICENSORS' LIABILITY UNDER THIS AGREEMENT EXCEED THE AMOUNT RECEIVED FROM CUSTOMER FOR THE HARDWARE, SOFTWARE LICENSE OR SERVICE GIVING RISE TO THE CLAIM. IN THE CASE WHERE NO AMOUNT WAS PAID, MENTOR GRAPHICS AND ITS LICENSORS SHALL HAVE NO LIABILITY FOR ANY DAMAGES WHATSOEVER. THE PROVISIONS OF THIS SECTION 9 SHALL SURVIVE THE TERMINATION OF THIS AGREEMENT.

10. **HAZARDOUS APPLICATIONS.** CUSTOMER ACKNOWLEDGES IT IS SOLELY RESPONSIBLE FOR TESTING ITS PRODUCTS USED IN APPLICATIONS WHERE THE FAILURE OR INACCURACY OF ITS PRODUCTS MIGHT RESULT IN DEATH OR PERSONAL INJURY ("HAZARDOUS APPLICATIONS"). NEITHER MENTOR GRAPHICS NOR ITS LICENSORS SHALL BE LIABLE FOR ANY DAMAGES RESULTING FROM OR IN CONNECTION WITH THE USE OF MENTOR GRAPHICS PRODUCTS IN OR FOR HAZARDOUS APPLICATIONS. THE PROVISIONS OF THIS SECTION 10 SHALL SURVIVE THE TERMINATION OF THIS AGREEMENT.

11. **INDEMNIFICATION.** CUSTOMER AGREES TO INDEMNIFY AND HOLD HARMLESS MENTOR GRAPHICS AND ITS LICENSORS FROM ANY CLAIMS, LOSS, COST, DAMAGE, EXPENSE OR LIABILITY, INCLUDING ATTORNEYS' FEES, ARISING OUT OF OR IN CONNECTION WITH THE USE OF PRODUCTS AS DESCRIBED IN SECTION 10. THE PROVISIONS OF THIS SECTION 11 SHALL SURVIVE THE TERMINATION OF THIS AGREEMENT.

12. **INFRINGEMENT.**

12.1. Mentor Graphics will defend or settle, at its option and expense, any action brought against Customer in the United States, Canada, Japan, or member state of the European Union which alleges that any standard, generally supported Product acquired by Customer hereunder infringes a patent or copyright or misappropriates a trade secret in such jurisdiction. Mentor Graphics will pay costs and damages finally awarded against Customer that are attributable to the action. Customer understands and agrees that as conditions to Mentor Graphics' obligations under this section Customer must: (a) notify Mentor Graphics promptly in writing of the action; (b) provide Mentor Graphics all reasonable information and assistance

to settle or defend the action; and (c) grant Mentor Graphics sole authority and control of the defense or settlement of the action.

12.2. If a claim is made under Subsection 12.1 Mentor Graphics may, at its option and expense, (a) replace or modify the Product so that it becomes noninfringing; (b) procure for Customer the right to continue using the Product; or (c) require the return of the Product and refund to Customer any purchase price or license fee paid, less a reasonable allowance for use.

12.3. Mentor Graphics has no liability to Customer if the action is based upon: (a) the combination of Software or hardware with any product not furnished by Mentor Graphics; (b) the modification of the Product other than by Mentor Graphics; (c) the use of other than a current unaltered release of Software; (d) the use of the Product as part of an infringing process; (e) a product that Customer makes, uses, or sells; (f) any Beta Code or Product provided at no charge; (g) any software provided by Mentor Graphics' licensors who do not provide such indemnification to Mentor Graphics' customers; or (h) infringement by Customer that is deemed willful. In the case of (h), Customer shall reimburse Mentor Graphics for its reasonable attorney fees and other costs related to the action.

12.4. THIS SECTION 12 IS SUBJECT TO SECTION 9 ABOVE AND STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS FOR DEFENSE, SETTLEMENT AND DAMAGES, AND CUSTOMER'S SOLE AND EXCLUSIVE REMEDY, WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT OR TRADE SECRET MISAPPROPRIATION BY ANY PRODUCT PROVIDED UNDER THIS AGREEMENT.

13. **TERMINATION AND EFFECT OF TERMINATION.** If a Software license was provided for limited term use, such license will automatically terminate at the end of the authorized term.

13.1. Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement immediately upon written notice if Customer: (a) exceeds the scope of the license or otherwise fails to comply with the licensing or confidentiality provisions of this Agreement, or (b) becomes insolvent, files a bankruptcy petition, institutes proceedings for liquidation or winding up or enters into an agreement to assign its assets for the benefit of creditors. For any other material breach of any provision of this Agreement, Mentor Graphics may terminate this Agreement and/or any license granted under this Agreement upon 30 days written notice if Customer fails to cure the breach within the 30 day notice period. Termination of this Agreement or any license granted hereunder will not affect Customer's obligation to pay for Products shipped or licenses granted prior to the termination, which amounts shall be payable immediately upon the date of termination.

13.2. Upon termination of this Agreement, the rights and obligations of the parties shall cease except as expressly set forth in this Agreement. Upon termination, Customer shall ensure that all use of the affected Products ceases, and shall return hardware and either return to Mentor Graphics or destroy Software in Customer's possession, including all copies and documentation, and certify in writing to Mentor Graphics within ten business days of the termination date that Customer no longer possesses any of the affected Products or copies of Software in any form.

14. **EXPORT.** The Products provided hereunder are subject to regulation by local laws and United States government agencies, which prohibit export or diversion of certain products and information about the products to certain countries and certain persons. Customer agrees that it will not export Products in any manner without first obtaining all necessary approval from appropriate local and United States government agencies.

15. **U.S. GOVERNMENT LICENSE RIGHTS.** Software was developed entirely at private expense. All Software is commercial computer software within the meaning of the applicable acquisition regulations. Accordingly, pursuant to US FAR 48 CFR 12.212 and DFAR 48 CFR 227.7202, use, duplication and disclosure of the Software by or for the U.S. Government or a U.S. Government subcontractor is subject solely to the terms and conditions set forth in this Agreement, except for provisions which are contrary to applicable mandatory federal laws.

16. **THIRD PARTY BENEFICIARY.** Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Microsoft Corporation and other licensors may be third party beneficiaries of this Agreement with the right to enforce the obligations set forth herein.

17. **REVIEW OF LICENSE USAGE.** Customer will monitor the access to and use of Software. With prior written notice and during Customer's normal business hours, Mentor Graphics may engage an internationally recognized accounting firm to review Customer's software monitoring system and records deemed relevant by the internationally recognized accounting firm to confirm Customer's compliance with the terms of this Agreement or U.S. or other local export laws. Such review may include FLEXlm or FLEXnet (or successor product) report log files that Customer shall capture and provide at Mentor Graphics' request. Customer shall make records available in electronic format and shall fully cooperate with data gathering to support the license review. Mentor Graphics shall bear the expense of any such review unless a material non-compliance is revealed. Mentor Graphics shall treat as confidential information all information gained as a result of any request or review and shall only use or disclose such information as required by law or to enforce its rights under this Agreement. The provisions of this Section 17 shall survive the termination of this Agreement.

18. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** The owners of certain Mentor Graphics intellectual property licensed under this Agreement are located in Ireland and the United States. To promote consistency around the world, disputes shall be resolved as follows: excluding conflict of laws rules, this Agreement shall be governed by and construed under the laws of the State of Oregon, USA, if Customer is located in North or South America, and the laws of Ireland if Customer is located outside of North or South America. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of the courts of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the chairman of the Singapore International

Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section. This section shall not restrict Mentor Graphics' right to bring an action against Customer in the jurisdiction where Customer's place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.

19. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.

20. **MISCELLANEOUS.** This Agreement contains the parties' entire understanding relating to its subject matter and supersedes all prior or contemporaneous agreements, including but not limited to any purchase order terms and conditions. Some Software may contain code distributed under a third party license agreement that may provide additional rights to Customer. Please see the applicable Software documentation for details. This Agreement may only be modified in writing by authorized representatives of the parties. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.

Rev. 100615, Part No. 246066