RUBY-D711VG2AR
RUBY-D712VG2AR

Industrial Motherboard
ATX Board

User's Manual

Version 1.1c

Table of Contents

How to Use This Manual

The manual describes how to configure your RUBY-D711/D712VG2AR system board to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1: System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2: Hardware Configuration. Show the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3: System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4: BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5: Troubleshooting. Provide various of useful tips to quickly get RUBY-D711/D712VG2AR running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. The vendor may make supplement or change in the products described in this document at any time

Chapter 1
System Overview

1.1 Introduction

Powell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new RUBY-D711/D712VG2AR in response to market demand for a simplified embedded system board (ESB) that combines a smaller footprint, lower power consumption, robust computing power and with longevity support.

RUBY-D711/D712VG2AR is based on Intel® C206/Q67 Express Chipset supporting the latest processor for INTEL® QUAD CORE™ i5 / i7 CPU by LGA 1155 socket. Aimed squarely at customers who seek flexible expansions such as PCIe X16, PCIeX8(PCIeX4 signal), PCIeX4(PCIeX1 signal), four PCI slots and one Mini PCIe socket. It can run dual integrated display via VGA/DVI-D/HDMI. Also the RUBY-D711/D712VG2AR features high memory capacity, four 240-pin DIMM sockets that support DDR3 SDRAM up to 16 GB; dual Intel® GbE LANs (one of which can support iAMT 7.0); plus SATA (supporting RAID 0, 1, 5, 10), Audio and USB.
RUBY-D711/D712VG2AR Intel® Quad Core™ i5 / i7 processor-based industrial ATX motherboard, the applications in such areas as factory automation, gaming, medical, digital signage, surveillance security monitoring and kiosks

1.2 Check List

The RUBY-D711/D712VG2AR package should cover the following basic items

One RUBY-D711/D712VG2AR Industrial Mother board
✓
✓ One SATA Cable
✓ One I/O Shield bracket
✓ One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main Processor**
  Intel® Dual Core/Quad Core LGA1155 processor
  CPU clock bus: 1333/1066/800 MHz
- **Chipset**
  Intel® C206 Express chipset (RUBY-D711VG2AR)
  Intel® Q67 Express chipset (RUBY-D712VG2AR)
- **System BIOS**
  AMI BIOS
- **Main Memory**

  -Four 240-pin DDR3 DIMM socket support up to 16GB dual channel 1066/1033MHz memory

  -RUBY-D711VG2AR supports ECC and Non-ECC memory

  -RUBY-D712VG2AR supports Non-ECC memory

- **Expansion Interface**
  One PCI-E x16 slot
  One PCI-E x8 slot (PCIeX4 signal)
  One PCI-E x4 slot(PCIeX1 signal)
  Four PCI slots
- **SATA Interface**
  Six SATA ports(Two SATA 6Gb/s, Four SATA 3Gb/s)
- **Serial Port**
  Support three RS232 and one RS232/422/485
- **USB Interface**
  Support Eight USB ports, four on rear I/O and four on board header for internal devices
- **Audio Interface**
  Connector for Mic-In, Line-In and Line-Out
- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar
- **Watch Dog Timer**
  Support WDT function through software programming for enable/disable and interval setting
  General system reset
- **On-board Ethernet LAN**
  Two Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel 82579LM & 82574L GbE Ethernet Controller
- **High Drive GPIO**

One pin-header for 16 bit GPIO(8bit in & 8bit out)

- **System Monitoring Feature**
  Monitor system temperature and major power sources.

- **Outline Dimension (L x W)**
  312.8mm (12.3″) X 243.8mm (9.6″)
- **Power Requirements**

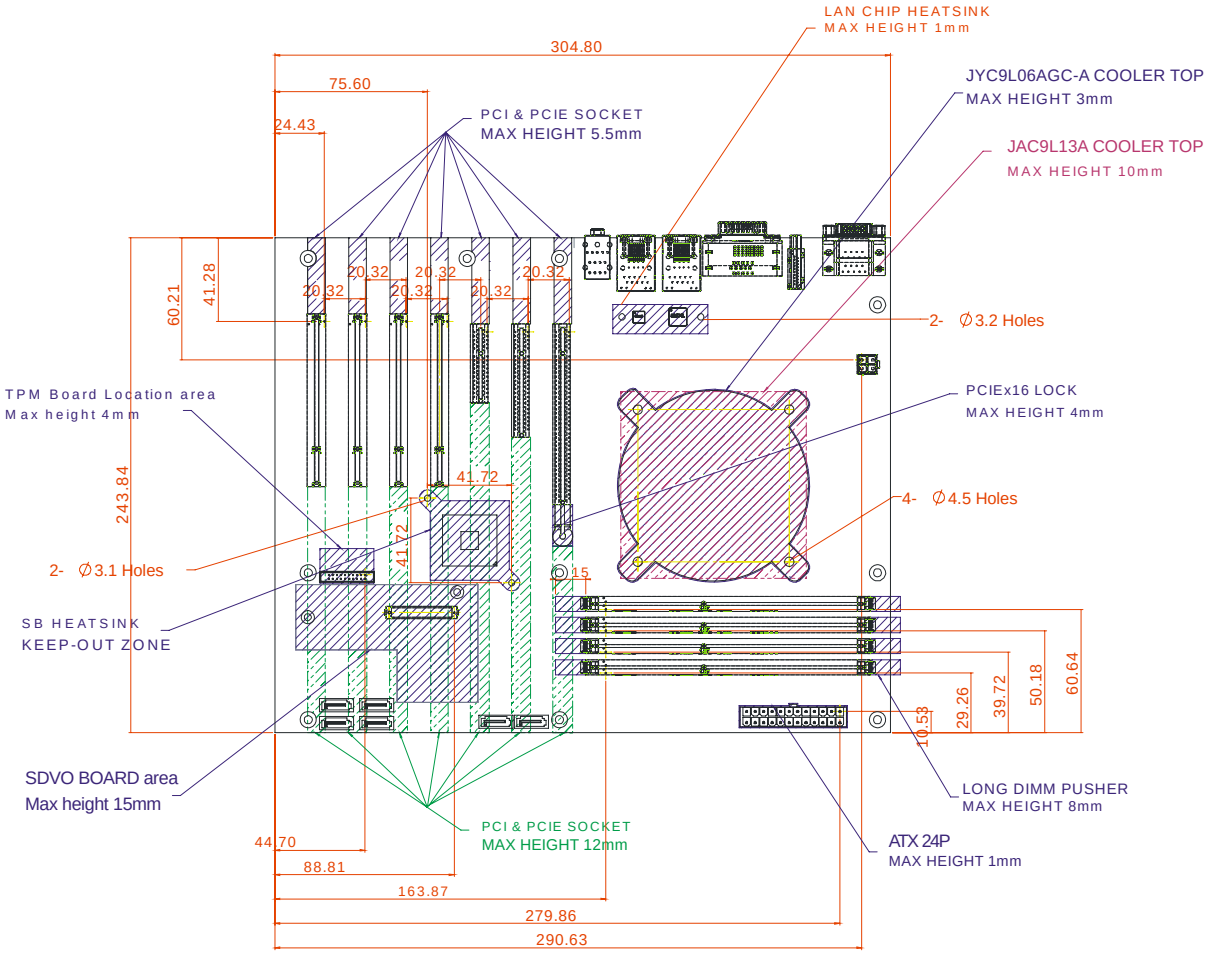
Item	Power ON	Full Loading 10Min	Full Loading 30Min
CPU +12V	2.54	3.54	3.27
System +12V	1.52	2.04	2.57
System +3.3V	0.93	1.24	1.24
System +5V	1.8	2.32	2.4
System+ Device +12V	4.43	5.74	5.71
System+ Device +5V	2.41	3.24	3.16
USB Loading Test	4.78V/ 450mA		

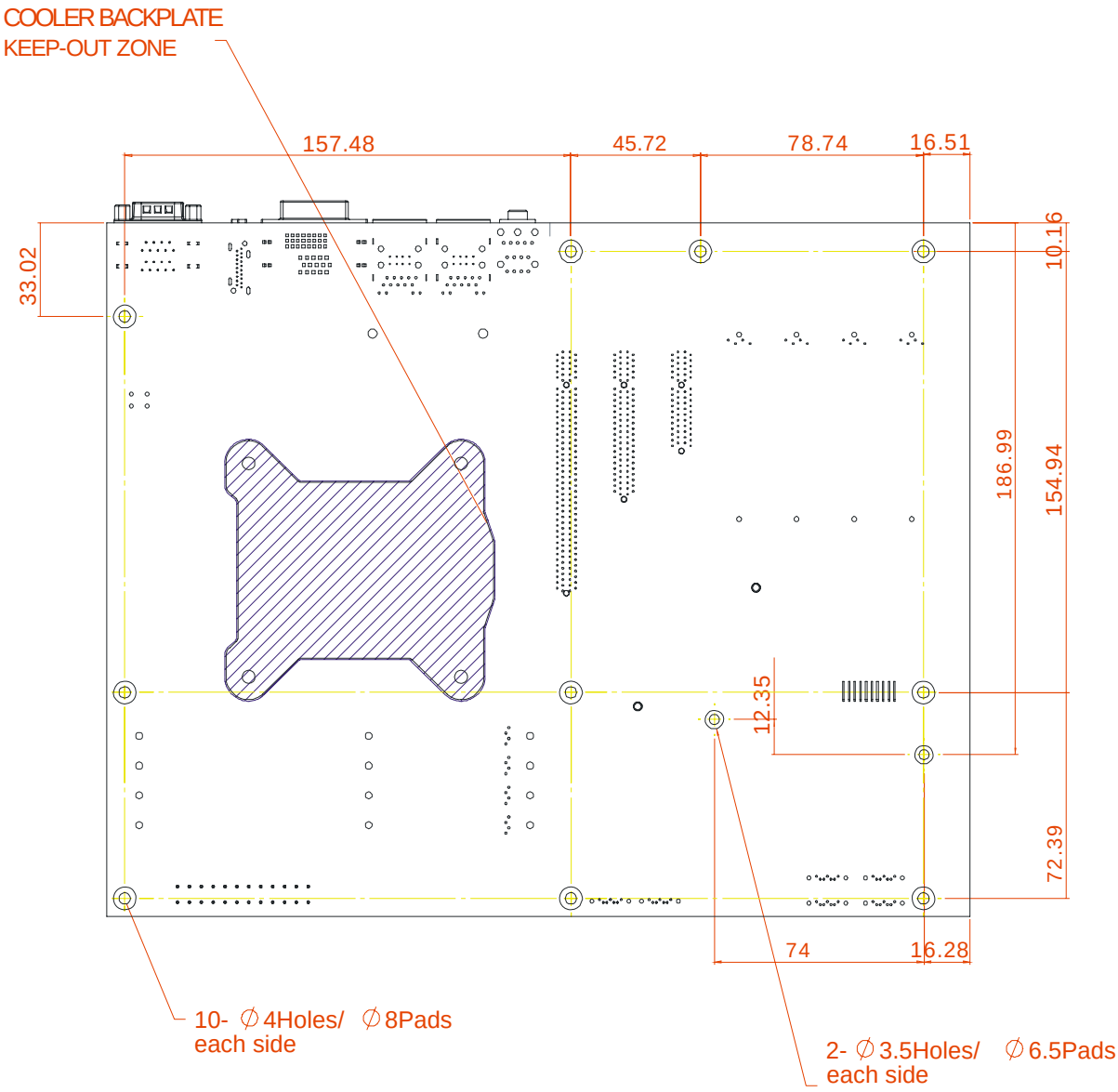
Configuration:

CPU Type	Intel® Core™ i5-2400 CPU 3.1GHz(ES) L3:6M
SBC BIOS	Portwell, Inc. RUBY-D711/D712 BIOS Rev.: R1.00.E1 (05092011)
Memory	Apacer PC3-8500 2GB*1 (ELPIDA J1108BFBG-DJ-E)
VGA Card	Onboard Intel® HD Graphics Family (Sandy Bridge)
VGA Driver	Onboard Intel® HD Graphics Family Version 14.46.5.5361
LAN Card	Onboard Intel® 82574L/82579LM Gigabit Network Connection
LAN Driver	Intel® 82574L/82579LM Gigabit Network Connection Version
Audio Card	Onboard Realtek ALC662 High Definition Audio Controller
Audio Driver	Realtek ALC662 High Definition Audio Version 5.10.0.6343
USB 2.0 Driver	Intel® 6 Series/C200 Series Chipset Family USB Enhanced Host Controller Version 9.2.0.1013
SATA HDD	WD WD1002FEX 1TB
CDROM	LITE-ON LH-20A1S
Power Supply	FSP400-60PFN

- **Operating Temperature**
  0 °C ~ 60 °C
- **Storage temperature**
  -20 ~ 80 °C
- **Relative Humidity**
  0% ~ 90%, non-condensing

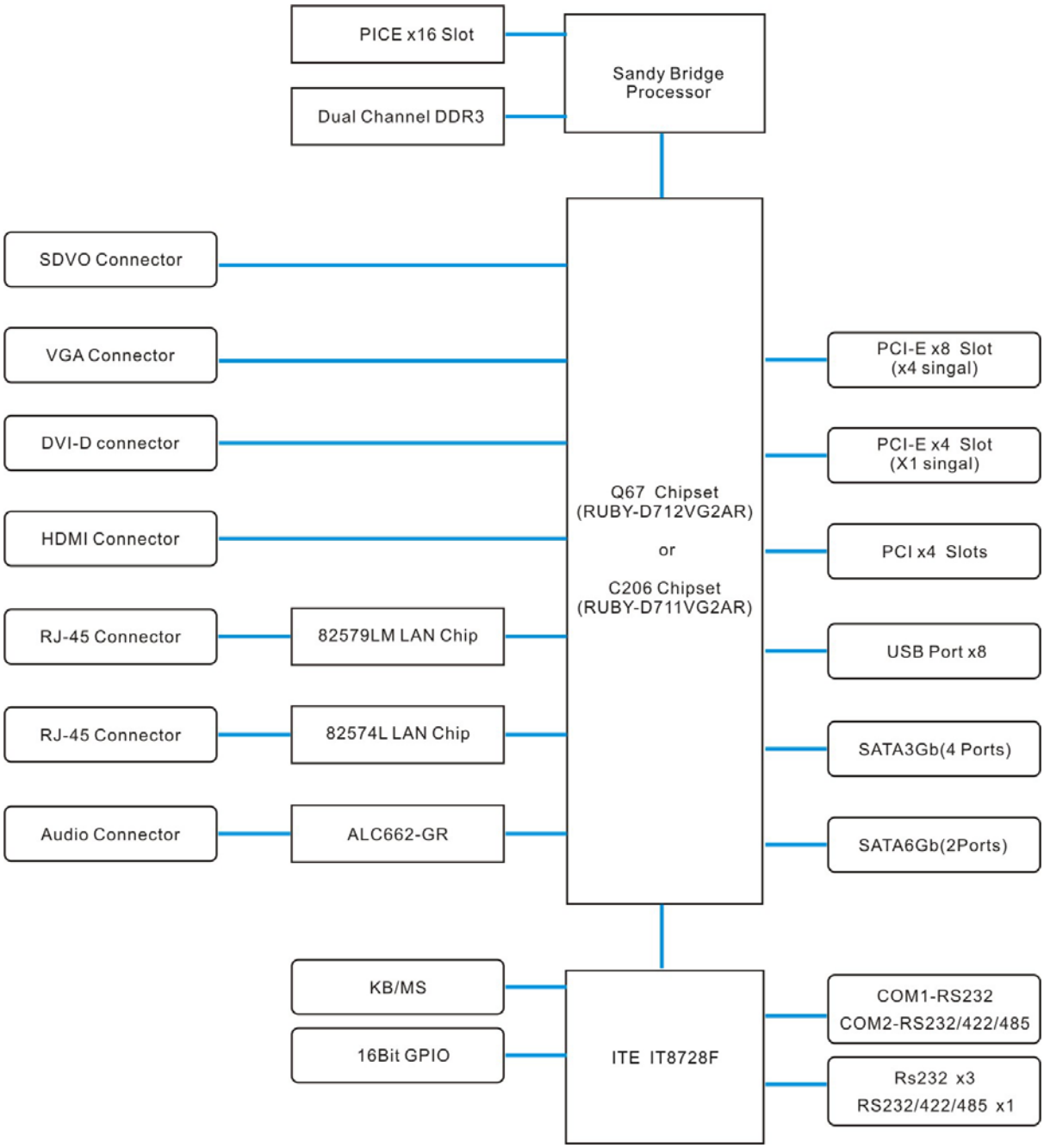
1.3.1 Mechanical Drawing




COOLER BACKPLATE
KEEP-OUT ZONE
157.48
45.72
78.74
16.51
33.02
10.16
186.99
154.94
12.35
72.39
74
16.28
10- ∅4Holes/ ∅8Pads
each side
2- ∅3.5Holes/ ∅6.5Pads
each side

1.4 System Architecture

All of details operating relations are shown in RUBY-D711/D712VG2AR System Block Diagram.



RUBY-D711/D712VG2AR System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on RUBY-D711/D712VG2AR are in the proper position. The default settings shipped from factory are marked with an asterisk (★).

2.1 Jumpers

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".

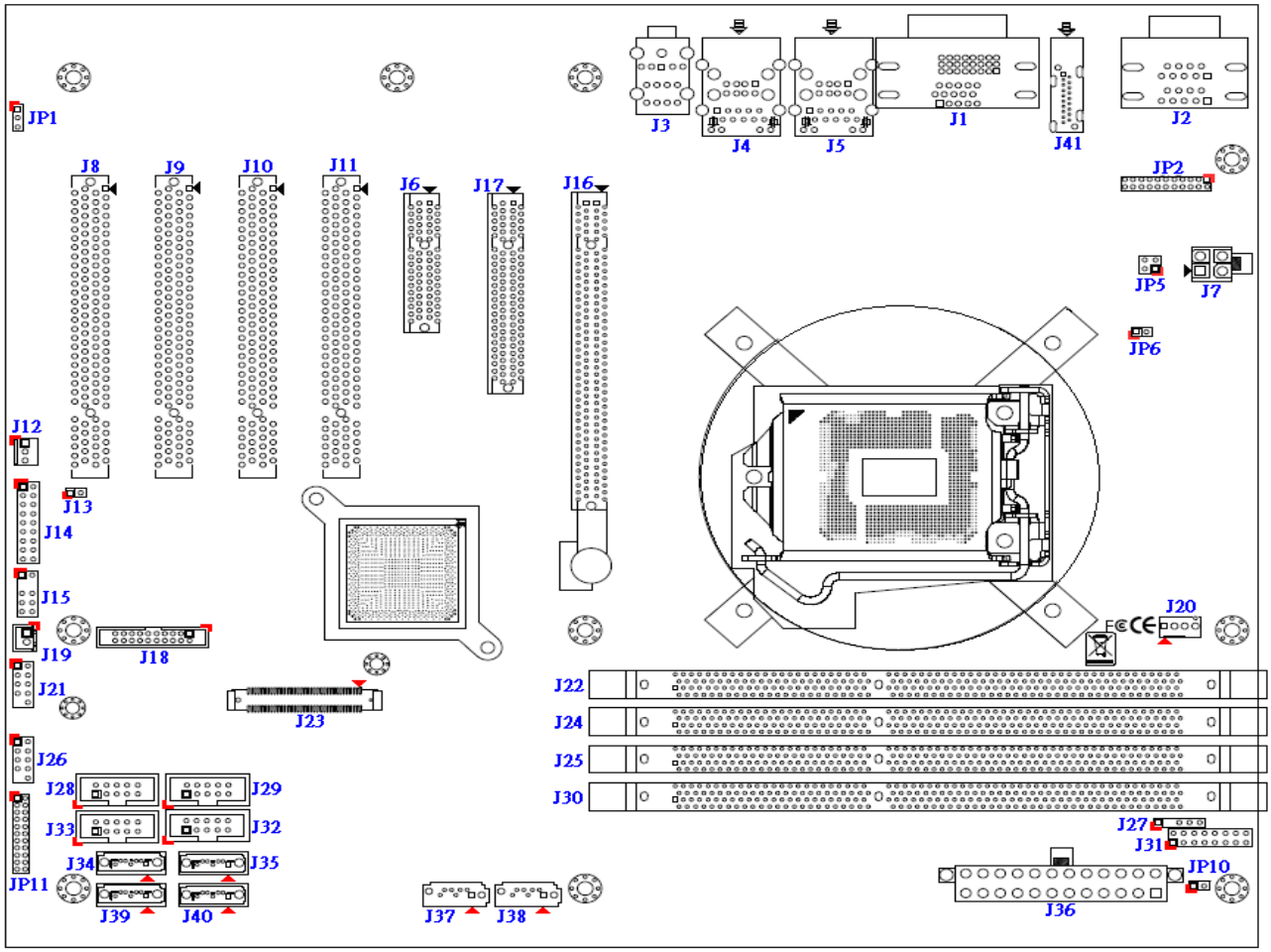
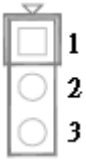


Figure 1-1 RUBY-D711/D712VG2AR Top-side Jumper and Connector Locations

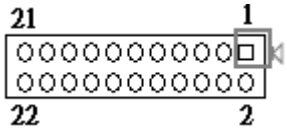
Pin Assignments of Connectors

JP1: CLEAR CMOS



JP1	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents

JP2: COM2 (J2) Interface Selection



JP2	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

JP5: PCI Express Bifurcation Selection

JP5	Function
Short (1-2 , 3-4)	1 x8, 2 x4 PCI Express (Support Three slot)
Short (1-2),Open(3-4)	2 x8 PCI Express (Support Two slot)
Open (1-2 , 3-4)	1 x16 PCI Express (Support One slot) ★
Open (1-2),Short (3-4)	reserved

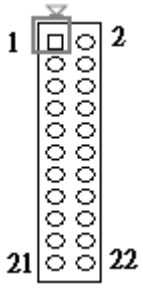
JP6: VCCSA Voltage Slection

JP6	Function
1-2 Short	0.85 V
1-2 Open	0.925 V ★

JP10: ATX / AT Mode Select

JP10	Function
1-2 short	ATX emulation AT mode
1-2 open	ATX mode ★

JP11: COM4 (J29) Interface Selection



JP11	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
J1	DVI-D Connector	
J2	COM1 & COM2 Serial Port Connector	COM2 Support 232/422/485
J3	Audio connector	
J4	USB 0&1/100+Giga Lan Connector (LAN1) 82579LM	
J5	USB 8&9/100+Giga Lan Connector (LAN2) 82574L	
J6	PCIE x4 Slot	Only Support x1 signal
J7	ATX 4Pin 12V Power Connector	
J8、J9、J10、J11	PCI Slot	
J12	SYSTEM FAN Power Connector	

J13	WDT LED Connector	
J14	16Bit GPIO Connector	
J15	External Keyboard/Mouse Connector	
J16	PCIE x16 Slot	
J17	PCIE x8 Slot	only Support x4 signal
J18	TPM(Trusted Platform Module) Connector	
J19	Case Open Connector	
J20	CPU FAN Power Connector	
J21、26	External USB Connector	
J22、J24、J25、J30	DDR3 Long DIMM	
J23	SDVO Connector	
J27	SMBus Connector	
J28、J29、J32、J33	COM3~COM6 Serial Port Connector	COM4 Support 232/422/485
J31	Front Panel System Connector	
J34、J35、J39、J40	SATA Connector	Support 1、2 Module
J36	ATX Connector	
J37、J38	SATA Connector	Support 1、2、3 Module
J41	HDMI Connector	

J1: DVI-D Connector

PIN No.	Signal Description	PIN No.	Signal Description	PIN No.	Signal Description
1	D2-	9	D1-	17	D0-
2	D2+	10	D1+	18	D0+
3	SHIELD1	11	SHIELD2	19	SHIELD3
4	D4-	12	D3-	20	D5-
5	D4+	13	D3+	21	D5+
6	DDCCLK	14	VCC	22	SHIELD4
7	DDCDATA	15	GND	23	CLK+
8	NC	16	HPDET	24	CLK-
C5	GND				

J2: COM1 & COM2 Serial Port Connector

PIN No	Signal Description		
	RS-232	RS-422 (COM2)	RS-485 (COM2)
1	DCD (Data Carrier Detect)	TX-	DATA-
2	DSR (Data Set Ready)	N/C	N/C
3	RXD (Receive Data)	TX+	DATA+
4	RTS (Request to Send)	N/C	N/C
5	TXD (Transmit Data)	RX+	N/C
6	CTS (Clear to Send)	N/C	N/C
7	DTR (Data Terminal Ready)	RX-	N/C
8	RI (Ring Indicator)	N/C	N/C
9	GND (Ground)	GND	GND
10	N/C	N/C	N/C

Note:
J2(COM2) could be configurable as RS-232/422/485 with jumper JP2.

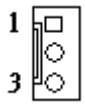
J3: Audio connector

PIN No.	Signal Description
1(Bule)	Line-In
2(Green)	Line-Out
3(Red)	MIC-In

J7: ATX 4Pin 12V Power Connector

PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

J12: SYSTEM FAN Power Connector

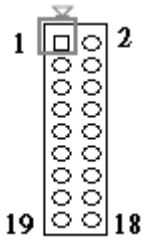


PIN No.	Signal Description
1	Ground
2	Fan speed control
3	Fan on/off output

J13: WDT LED Connector

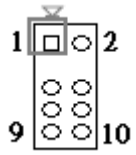
PIN No.	Signal Description
1	WDT (+)
2	WDT (-)

J14: 16Bit GPIO Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO8
3	GPIO1	4	GPIO9
5	GPIO2	6	GPIO10
7	GPIO3	8	GPIO11
9	GPIO4	10	GPIO12
11	GPIO5	12	GPIO13
13	GPIO6	14	GPIO14
15	GPIO7	16	GPIO15
17	Ground	18	+5V

J15: External Keyboard/Mouse Connector

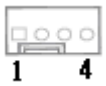


PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Keyboard Clock

J19: Case Open Connector

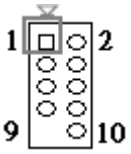
PIN No.	Signal Description
1	GND
2	Case open

J20: CPU FAN Power Connector



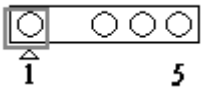
PIN No.	Signal Description
1	Ground
2	+12V
3	Fan on/off output
4	Fan Speed control

J21/26: External USB Connector



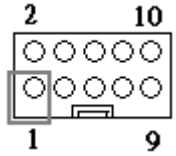
PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground
9	Key (No pin)	10	N/C

J27: SMBus Connector



PIN No.	Signal Description
1	SMBus_CLK
2	N/C
3	Ground
4	SMBus_DAT
5	+5V

J28/29/32/33: COM3~COM6 Serial Port Connector

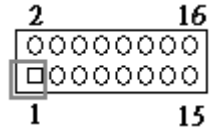


PIN No	Signal Description		
	RS-232	RS-422 (COM4)	RS-485 (COM4)
1	DCD (Data Carrier Detect)	TX-	DATA-
2	DSR (Data Set Ready)	N/C	N/C
3	RXD (Receive Data)	TX+	DATA+
4	RTS (Request to Send)	N/C	N/C
5	TXD (Transmit Data)	RX+	N/C
6	CTS (Clear to Send)	N/C	N/C
7	DTR (Data Terminal Ready)	RX-	N/C
8	RI (Ring Indicator)	N/C	N/C

9	GND (Ground)	GND	GND
10	N/C	N/C	N/C

Note:
J29(COM4) could be configurable as RS-232/422/485 with jumper JP11.

J31: Front Panel System Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	PWR_LED(+)	2	Speaker(+)
3	PWR_LED(-)	4	N/C
5	J4 LAN1_ACT(+)	6	N/C
7	J4 LAN1_LINK(-)	8	Speaker(-)
9	J5 LAN2_LINK(-)	10	GND
11	J5 LAN2_ACT(+)	12	Power Button
13	HDD_LED(+)	14	Rest
15	HDD_LED(-)	16	GND

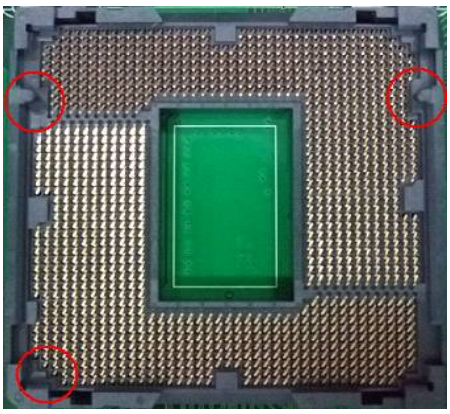
Chapter 3
System Installation

This chapter provides the instructions to set up the system. The additional information is enclosed to help you set up onboard devices

3.1 Intel® 2nd Generation of Core i7/i5/i3

LGA-1155 CPU Socket

Pin1 corner of the CPU Socket
Alignment key
Alignment key



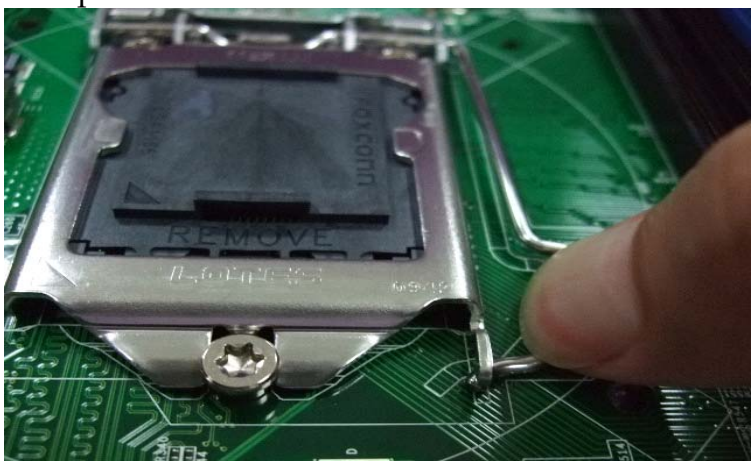
LGA-1155 CPU

Yellow Triangle Pin1 of the CPU
Notch
Notch

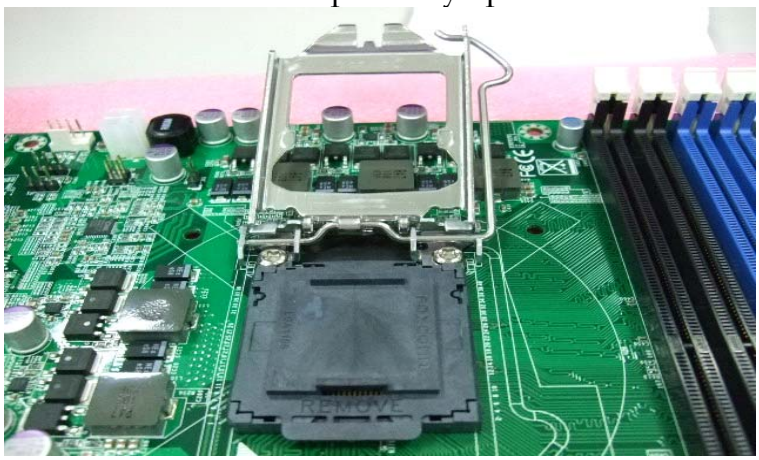
Please remember to locate the alignment keys on the CPU socket of the motherboard and the notches on the CPU.

LGA-1155 CPU Installation Steps
Before install the CPU, please make sure to turn off the power first!!

1. Open the load lever.



2. Lift the load lever up to fully open



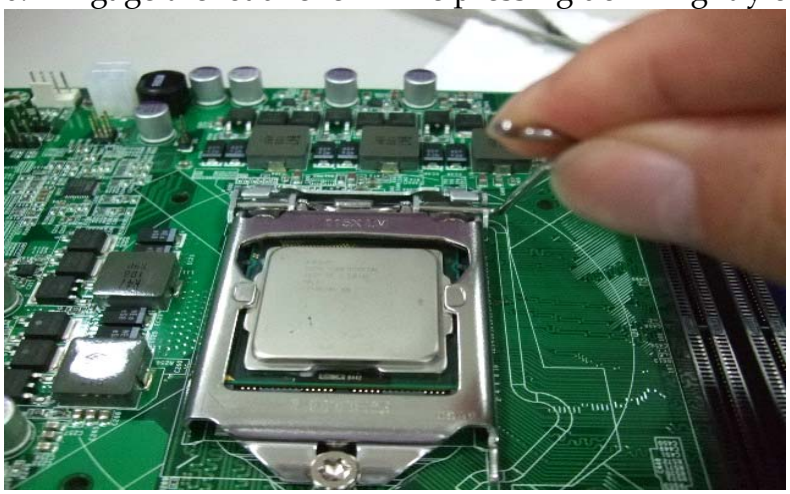
3. Remove the plastic cap on the CPU socket. Before you install the CPU, always cover it to protect the socket pin.

4. After confirming the CPU direction for correct mating, put down the CPU in the socket housing frame. Note that alignment keys are matched.

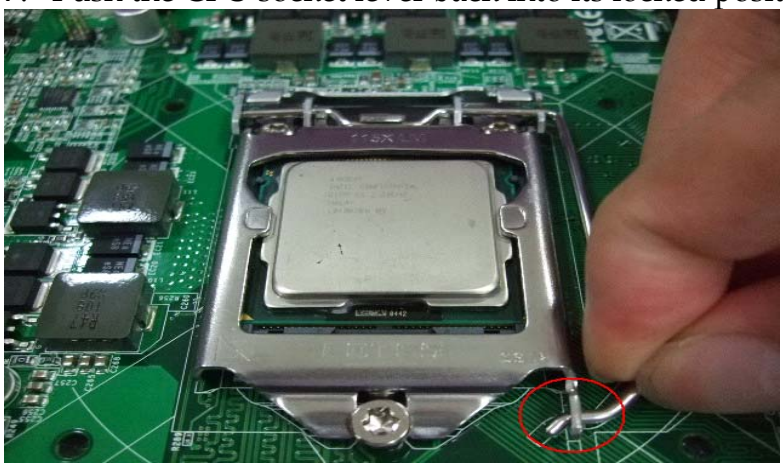
Alignment key

5. Make sure the CPU has been seated well into the socket. If not, take out the CPU and reinstall.

6. Engage the load lever while pressing down lightly onto the load plate.



7. Push the CPU socket lever back into its locked position.



8. Please make sure four hooks are in proper position before you install the coole.

3.2 Main Memory

RUBY-D711/D712 provide 4 x240 pin DIMM sockets (Dual Channel) which supports Dual channel 1066/1333 DDR3-SDRAM as main memory, non-register function. RUBY-D711VG2AR supports ECC and Non-ECC memory. RUBY-D712VG2AR supports Nn-ECC memory. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.

Before locking, make sure that all modules have been fully inserted into the card slots

Note:
To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your RUBY-D711/D712 into standard chassis or proprietary environment, please perform the following::

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module at right position
Step 3 : Place PCOM-B216VG-VI into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note
Please refer to section 3.3.1 to 3.3.7 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

RUBY-D711/D712 uses state-of-art Intel® Q67 PCH chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for previous Windows Operating Systems such as Windows XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in RUBY-D711/D712 CD-title.
Moreover, if using some old OS, the driver may not be supported anymore. We recommend to change the different OS to comply with this new chipset.

3.3.2 Intel® HD Graphics Family

With latest Intel® Core i Sandy Bridge series structure, RUBY-D711/D712 Intel® HD Graphic is built in with CPU. Therefore 2nd Generation Core i CPUs provide HD integrated Graphic support sharing on board physical memories. RUBY-D711/D712 has both internal VGA & DVI interface. This combination makes RUBY-D711/D712 an excellent piece of multimedia hardware
With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express Graphic card can take over the system display.

※To use Intel® Integrated HD Graphic, it's required to choose the CPU which has Integrated Graphic built-in. Otherwise there will be no display whatsoever.

3.3.3 Intel® PROSet Gigabit Ethernet Controlle

Drivers Support

Please find Intel® 82574L and 82579LM LAN driver in /Ethernet directory of RUBY-D711/D712 CD-title. The drivers support Windows XP/Vista/Win7.

3.3.4 Audio Controller

Please find Intel® High Definition Audio driver form PCOM-B216VG-VI CD-title. The drivers support Windows 2000 /XP/Vista/Win7.

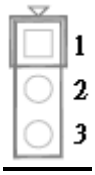
3.3.5 Intel® Active Management Technology (Intel® AMT)

Please find the latest Intel® 7.0 driver from RUBY-D711/D712 CD-title. The drivers support Windows XP/Vista/Win7

3.4 Clear CMOS Operation

Please find Realtek ALC662-GR (High Definition Audio driver) form RUBY-D711/D712 CD-title. The drivers support Windows XP/Win7.

JP1: CLEAR CMOS



JP1	Function
1-2 Short	Normal Operation
2-3 Short	Clear CMOS Contents

3.5 WDT Function

The Watchdog Timer of motherboard consists of 8-bit programmable time-out counter and a control and status register.

WDT Controller Register
There are two PNP I/O port addresses that can be used to configure WDT.

2Eh: EFIR (Extended Function Index Register, for identifying CR index number)
2Fh: EFDR (Extended Function Data Register, for accessing desired CR)

WDT Control Mode Register
The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

RUBY-D711/D712 allows users to control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to ITE IT8728F data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

WDT Control Command Example

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define SIO_Port      0x2E
#define    SIO_Port2 0x4E
#define GPIO_LDN  0x07

void Enter_IT872x_SIO() {
            outportb(SIO_Port, 0x87);
            outportb(SIO_Port, 0x01);
            outportb(SIO_Port, 0x55);
            outportb(SIO_Port, 0x55);

}

void Set_LDN(unsigned char LDN) {
            outportb(SIO_Port, 0x07);
```

```
        outportb(SIO_Port+1, LDN);
        printf("LDN=%x\n", LDN);
}

void Set_Register(unsigned char offset, unsigned char value) {
        outportb(SIO_Port, offset);
        outportb(SIO_Port+1, value);
        printf("Write offset:%x = %x\n", offset, value);
}

int main(void) {

        printf("test string\n");
        Enter_IT872x_SIO();

        Set_LDN(GPIO_LDN);

        Set_Register(0x72, 0xC0);
        Set_Register(0x73, 0x05);
        printf("System will reset in 5 seconds\n");

        return 0;
}
```

3.6 GPIO

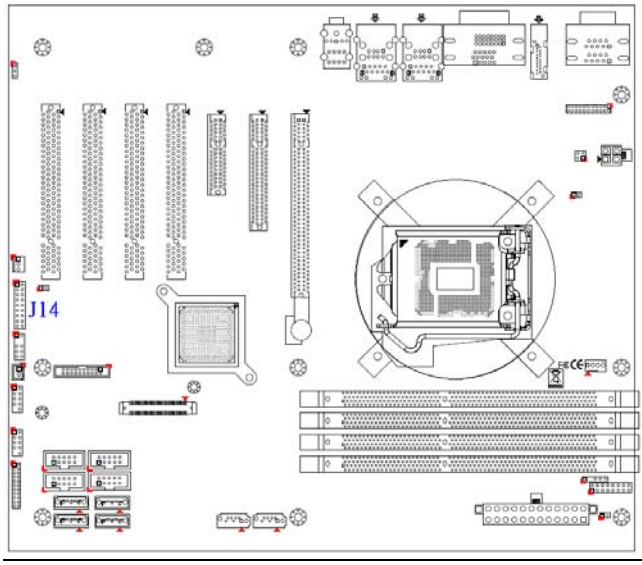
The motherboard provides 8 input / output ports that can be individually configured to perform a simple basic I/O function.

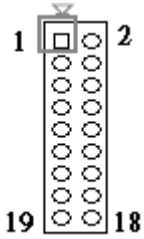
GPIO Pin Assignment
The RUBY-D711/D712 provides 8 input/output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.
The GPIO port is located on JP14 shown as follows. Please note: **Do not short the Pin 17 and Pin 18 of the J14!**

The control for the GPIO signals is handled through a separate 2-byte I/O space.
J14: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO8
3	GPIO1	4	GPIO9
5	GPIO2	6	GPIO10
7	GPIO3	8	GPIO11
9	GPIO4	10	GPIO12
11	GPIO5	12	GPIO13
13	GPIO6	14	GPIO14
15	GPIO7	16	GPIO15
17	Ground	18	+5V

Note:
All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each Fan.





GPIO Control Command Example (C Language)

```
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>

#define SIO_Port            0x2E
#define SIO_Port2           0x4E
#define GPIO_LDN              0x07
#define GPIO_Base           0x0A00

//Enter SIO
void Enter_IT872x_SIO() {
        outp(SIO_Port, 0x87);
        outp(SIO_Port, 0x01);
        outp(SIO_Port, 0x55);
        outp(SIO_Port, 0x55);

}

//Select LDN
void Set_LDN(unsigned char LDN) {
        outp(SIO_Port, 0x07);
        outp(SIO_Port+1, LDN);
        //printf("LDN=%x\n", LDN);
}

//Set register offset to Value
void Set_Register(unsigned char offset, unsigned char value) {
        outp(SIO_Port, offset);
        outp(SIO_Port+1, value);
        //printf("Write offset:%x = %x\n", offset, value);
}

//Or register
void Or_Register(unsigned char offset, unsigned char value) {
        outp(SIO_Port, offset);
        outp(SIO_Port+1, inp(SIO_Port+1) | value);
        //printf("Write offset:%x = %x\n", offset, value);
}

//And register
void And_Register(unsigned char offset, unsigned char value) {
        outp(SIO_Port, offset);
        outp(SIO_Port+1, inp(SIO_Port+1) & value);
        //printf("Write offset:%x = %x\n", offset, value);
}
```

```
int main(void) {

        int result;
        printf("RUBY-D711/D712 GPIO Test:\n");

        //pin1 =11
        //pin3 =12
        //pin5 =47
        //pin7 =50
        //pin9 =74
        //pin11=75
        //pin13=76
        //pin15=77

        //pin2 =14
        //pin4 =35
        //pin6 =36
        //pin8 =37
        //pin10=70
        //pin12=71
        //pin14=72
        //pin16=73

        Enter_IT872x_SIO();
        Set_LDN(GPIO_LDN);

        //Enable GPIO
        //Or_Register(0xC0,0x46)          //11,12,14
        //Or_Register(0xC2,0xE0)          //35,36,37
        //Or_Register(0xC3,0x80)          //47
        //Or_Register(0xC4,0x01)          //50

        //Set Output
        Or_Register(0xC8,0x06); //11,12
        Or_Register(0xCB,0x80); //47

        Or_Register(0xCC,0x01); //50
        Or_Register(0xCE,0xF0); //74,75,76,77

        //Set Input
        And_Register(0xC8,0xEF);        //14
        And_Register(0xCA,0x1F);        //35,36,37
        And_Register(0xCE,0xF0);        //70,71,72,73

        //output high
        outp(GPIO_Base+0,0x06); //11,12
```

```
outp(GPIO_Base+3,0x80); //47
outp(GPIO_Base+4,0x01); //50
outp(GPIO_Base+6,0xF0); //74,75,76,77

result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x10) result=0;
if ((inp(GPIO_Base+2)&0xE0)!=0xE0) result=0;
if ((inp(GPIO_Base+6)&0x0F)!=0x0F) result=0;

if (result==0){

        printf("Test fail!!\n");

        return 1;
}


//output low
outp(GPIO_Base+0,inp(GPIO_Base+0)&0xF9);        //11,12
outp(GPIO_Base+3,inp(GPIO_Base+3)&0x7F);        //47
outp(GPIO_Base+4,inp(GPIO_Base+4)&0xFE);        //50
outp(GPIO_Base+6,inp(GPIO_Base+6)&0x0F);        //74,75,76,77

result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x00) result=0;
if ((inp(GPIO_Base+2)&0xE0)!=0x00) result=0;
if ((inp(GPIO_Base+6)&0x0F)!=0x00) result=0;

if (result==0){

        printf("Test fail!!\n");
        return 1;

}

////////////////////////////////////////////////

//Set Input
And_Register(0xC8,0xF9);        //11,12
And_Register(0xCB,0x7F);        //47

And_Register(0xCC,0xFE);         //50
And_Register(0xCE,0x0F);        //74,75,76,77

//Set output
Or_Register(0xC8,0x10); //14
Or_Register(0xCA,0xE0); //35,36,37
```

```
        Or_Register(0xCE,0x0F); //70,71,72,73

        //output high
        outp(GPIO_Base+0,0x10); //14
        outp(GPIO_Base+2,0xE0); //35,36,37
        outp(GPIO_Base+6,0x0F); //70,71,72,73

        result=1;
        if ((inp(GPIO_Base+0)&0x06)!=0x06) result=0; //11,12
        if ((inp(GPIO_Base+3)&0x80)!=0x80) result=0; //47
        if ((inp(GPIO_Base+4)&0x01)!=0x01) result=0; //50
        if ((inp(GPIO_Base+6)&0xF0)!=0xF0) result=0; //74,75,76,77

        if (result==0){

                printf("Test fail!!\n");

                return 1;
        }

        //output low
        outp(GPIO_Base+0,inp(GPIO_Base+0)&0xEF);        //14
        outp(GPIO_Base+2,inp(GPIO_Base+2)&0x1F);        //35,36,37
        outp(GPIO_Base+6,inp(GPIO_Base+6)&0xF0);        //70,71,72,73

        result=1;
        if ((inp(GPIO_Base+0)&0x06)!=0x00) result=0; //11,12
        if ((inp(GPIO_Base+3)&0x80)!=0x00) result=0; //47
        if ((inp(GPIO_Base+4)&0x01)!=0x00) result=0; //50
        if ((inp(GPIO_Base+6)&0xF0)!=0x00) result=0; //74,75,76,77

        if (result==0){

                printf("Test fail!!\n");
                return 1;

        }

        //getchar ();

        printf("Test Pass!!\n");
        return 1;
}
```

Chapter 4
BIOS Setup Information

RUBY-D711/D712 is equipped with the UEFI AMI BIOS stored in SPI Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, RUBY-D711/D712 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

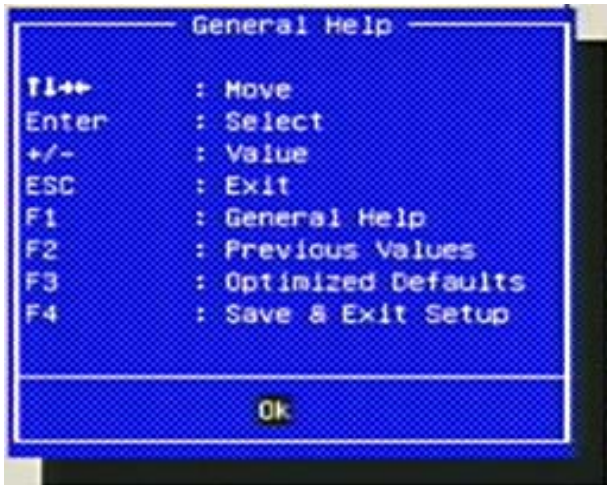
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also reset by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

Press <F1> to Run SETUP or Resume

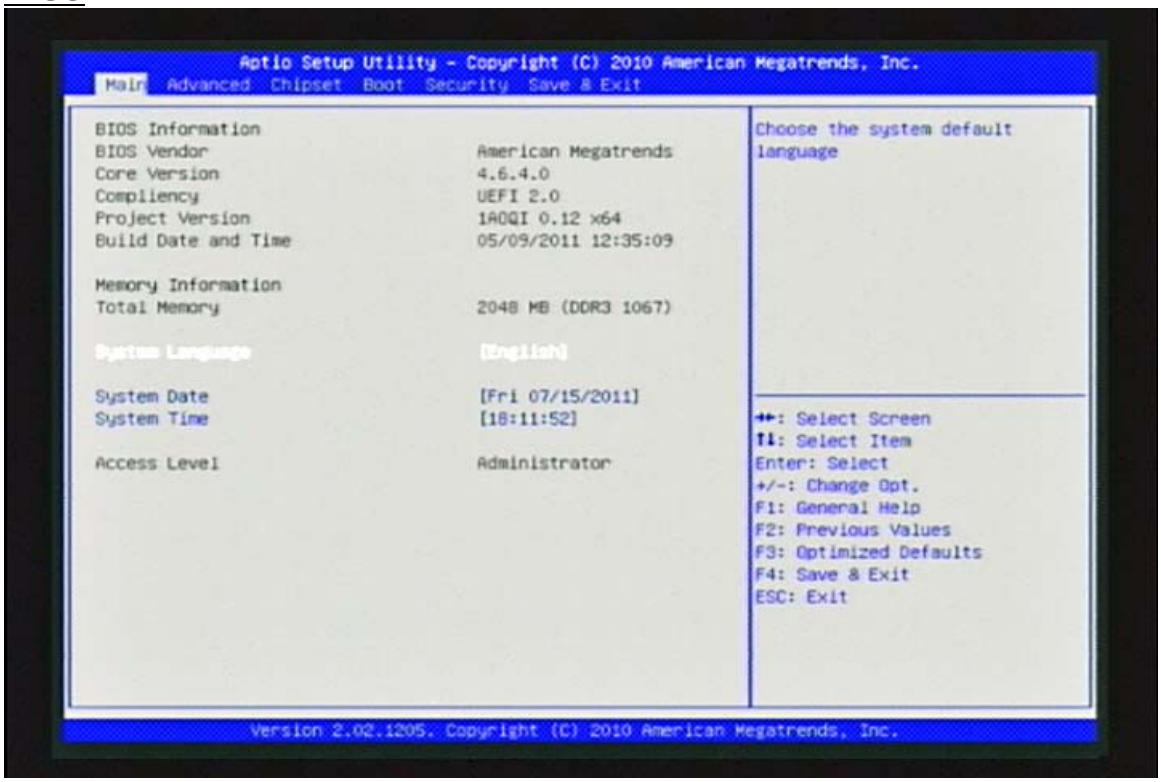
The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.

BIOS



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

System Time

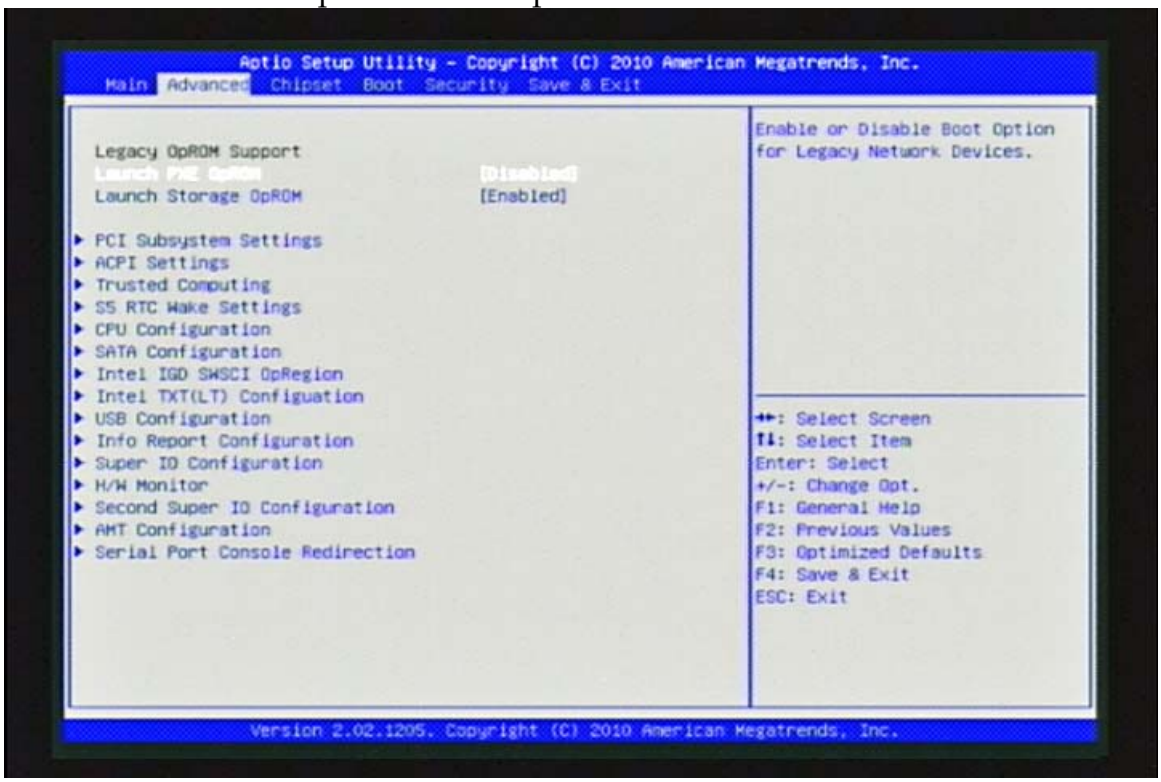
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

4.3 Advanced

Use this menu to set up the items of special enhanced features.



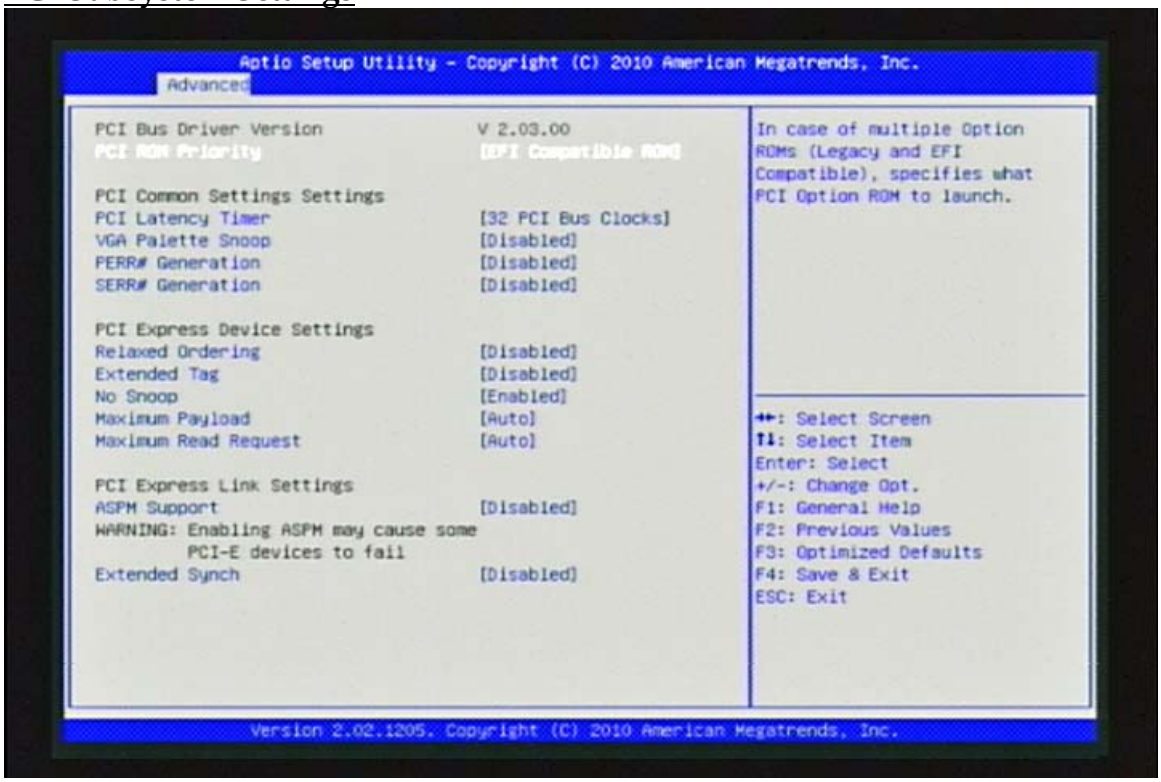
Launch PXE OpROM
Enable of Disable Boot Option for Legacy Network Devices.

Choices: Disabled, Enabled.

Launch Storage OpROM
Enable of Disable Boot Option for Legacy Mass Storage devices.

Choices: Disabled, Enabled.

PCI Subsystem Settings



PCI ROM Priority

In case of multiple Options (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.

Choices: EFI Compatible ROM, Legacy ROM

PCI Latency Timer

Choices: 32 PCI, 64 PCI, 96 PCI, 128 PCI, 160 PCI, 192 PCI, 224 PCI, 248 PCI Bus Clocks.

VGA Palette Snoop

Choices: Disabled, Enabled.

PERR# Generation

Choices: Disabled, Enabled.

SERR# Generation

Choices: Disabled, Enabled.

Relaxed Ordering

Choices: Disabled, Enabled.

Extended Tag

Choices: Disabled, Enabled.

No Snoop
Choices: Disabled, Enabled.

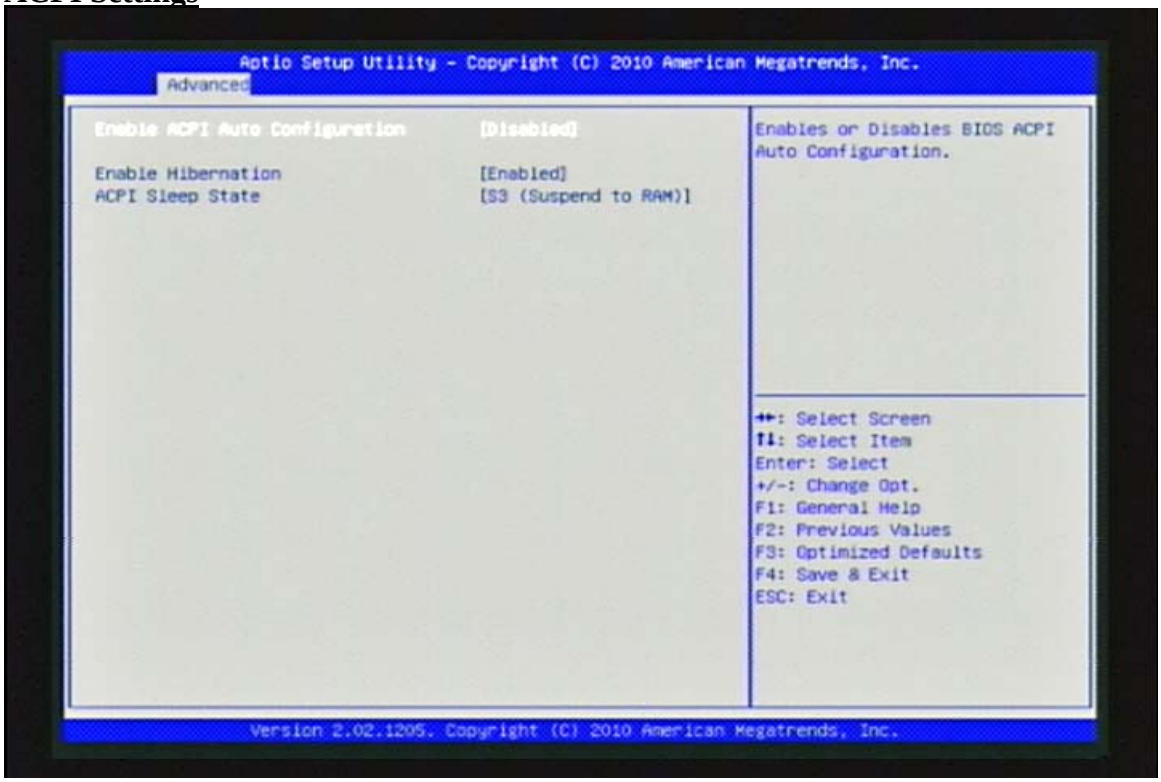
Maximum Payload
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

Maximum Read Request
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes.

ASPM Support
Choices: Disabled. Auto, Force L0.

Extended Synch
Choices: Disabled, Enabled.

ACPI Settings

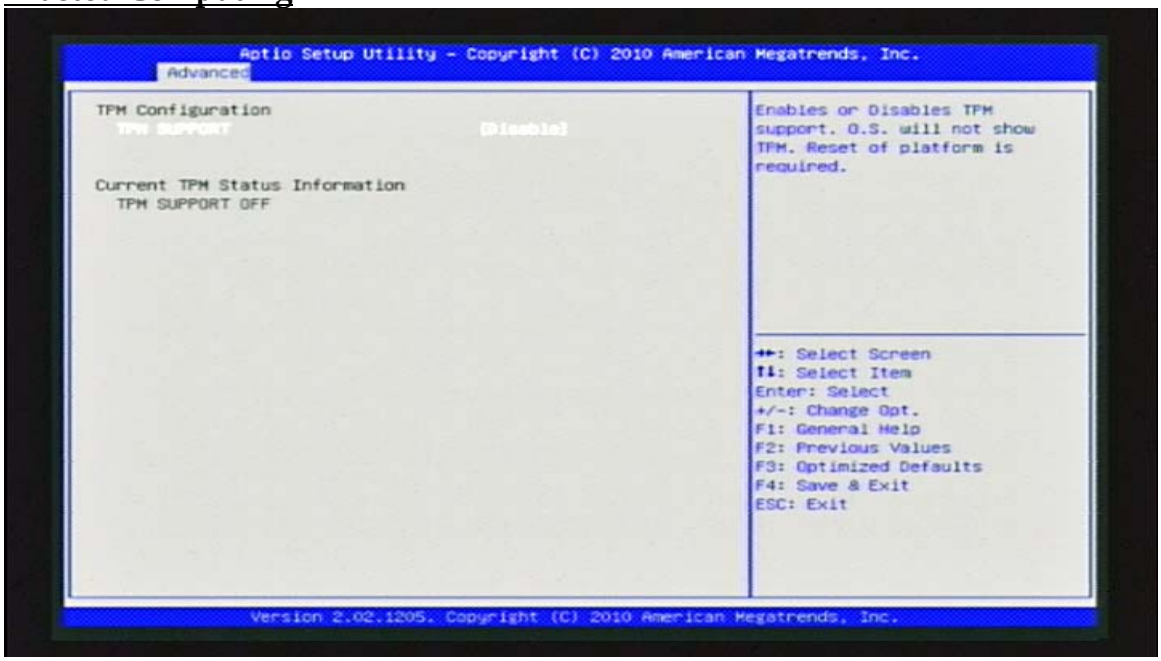


Enable ACPI Auto Configuration
Choices: Enabled, Disabled.

Enable Hibernation
Choices: Enabled, Disabled.

ACPI Sleep State
Choices: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM).

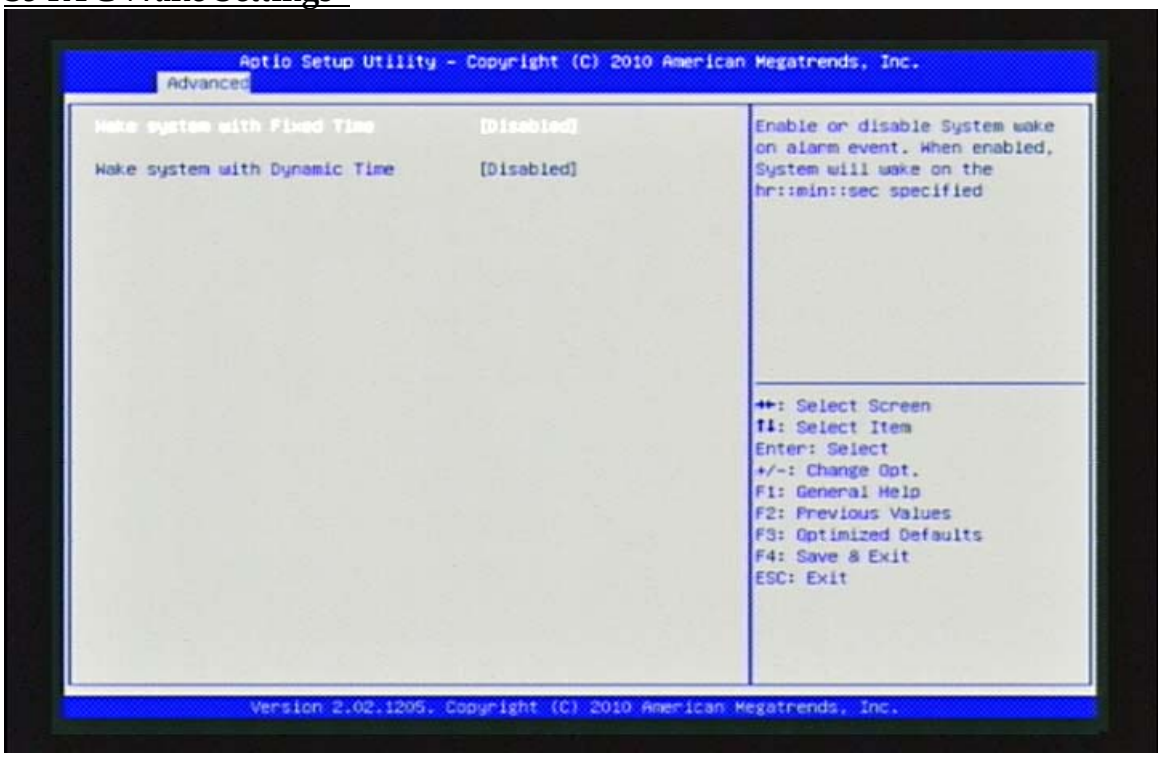
Trusted Computing



TPM SUPPORT
Enable or disable TPM Support

Choices: Enabled, Disabled.

S5 RTC Wake Settings



Wake system with Fixed Time
Enable or disable system wake on alarm event. When enabled, System will wake on the hr:min:sec specified

Choices: Enabled, Disabled.

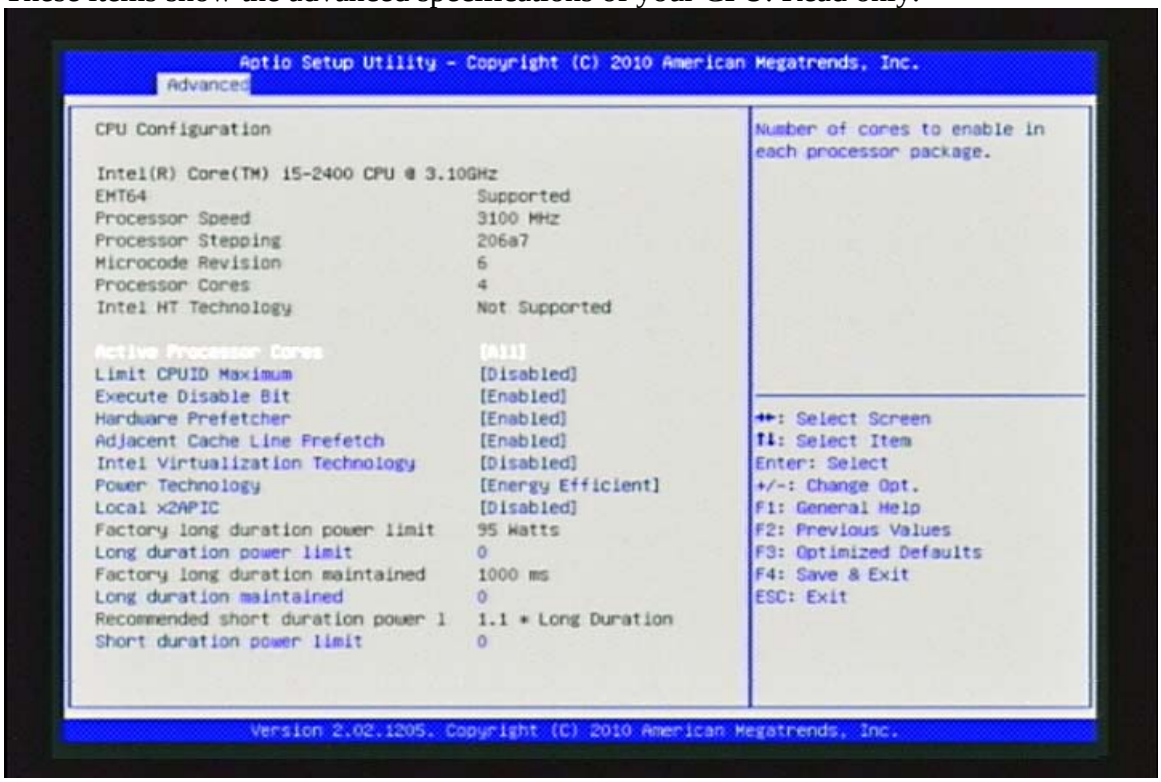
Wake up hour
Choices: 0-23

Wake up Minute
Choices:0-59

Wake up second
Choices:0-59

Wake system with Dynamic Time
Choices: Enable, Disable

CPU Configuration
These items show the advanced specifications of your CPU. Read only.



Active Processor Cores
Choices: All, 1,2,3,4 (Depending on CPU cores)

Limit CPUID Maximum
Choices: Disabled, Enabled

Execute Disable Bit
Choices: Disabled, Enabled

Hardware Prefetcher
Choices: Disabled, Enabled

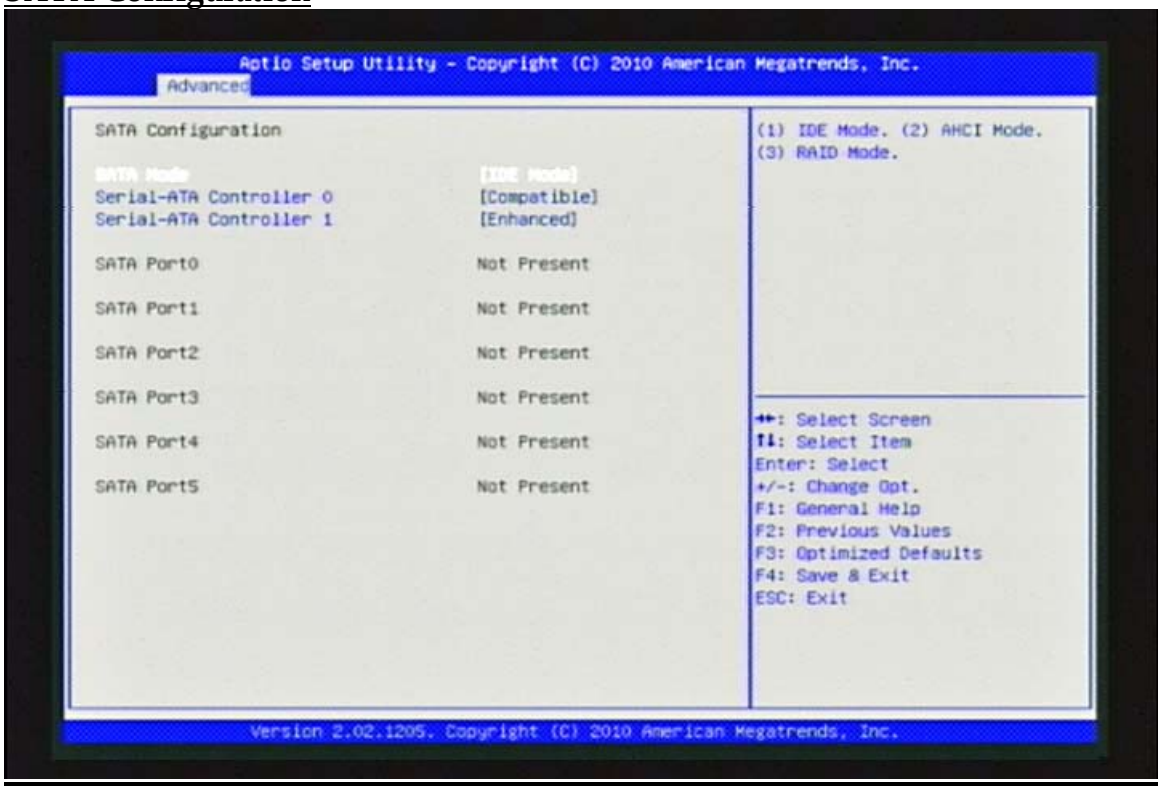
Adjacent Cache Line Prefetch
Choices: Disabled, Enabled

Intel Virtualization Technology
Choices: Disabled, Enabled

Power Technology
Choices: Disabled, Energy Efficient, Custom

Local x2APIC
Choices: Disabled, Enabled

SATA Configuration

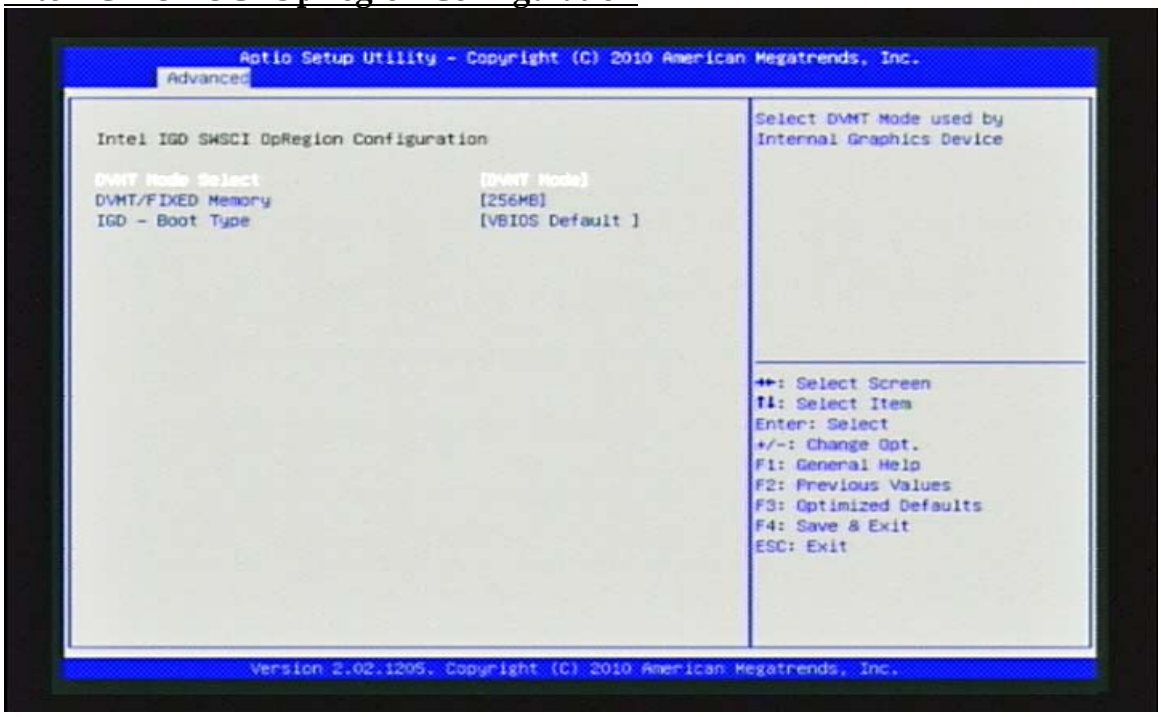


SATA Mode
Choices: Disabled, IDE Mode, AHCI Mode, RAID Mode

Serial-ATA Controller 0
Choices: Disabled, Enhanced, Compatible

Serial-ATA Controller 1
Choices: Disabled, Enhanced

Intel IGD SWSCI OpRegion Configuration

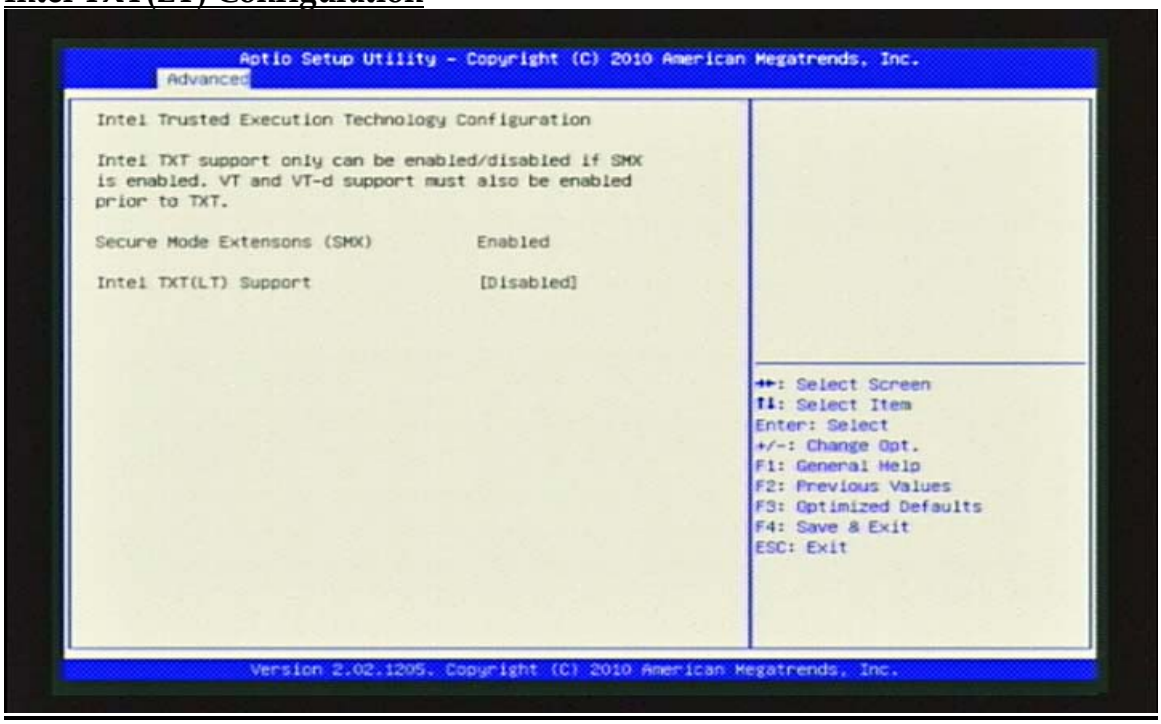


DVMT Mode Select
Choices: Fixed Mode, DVMT Mode

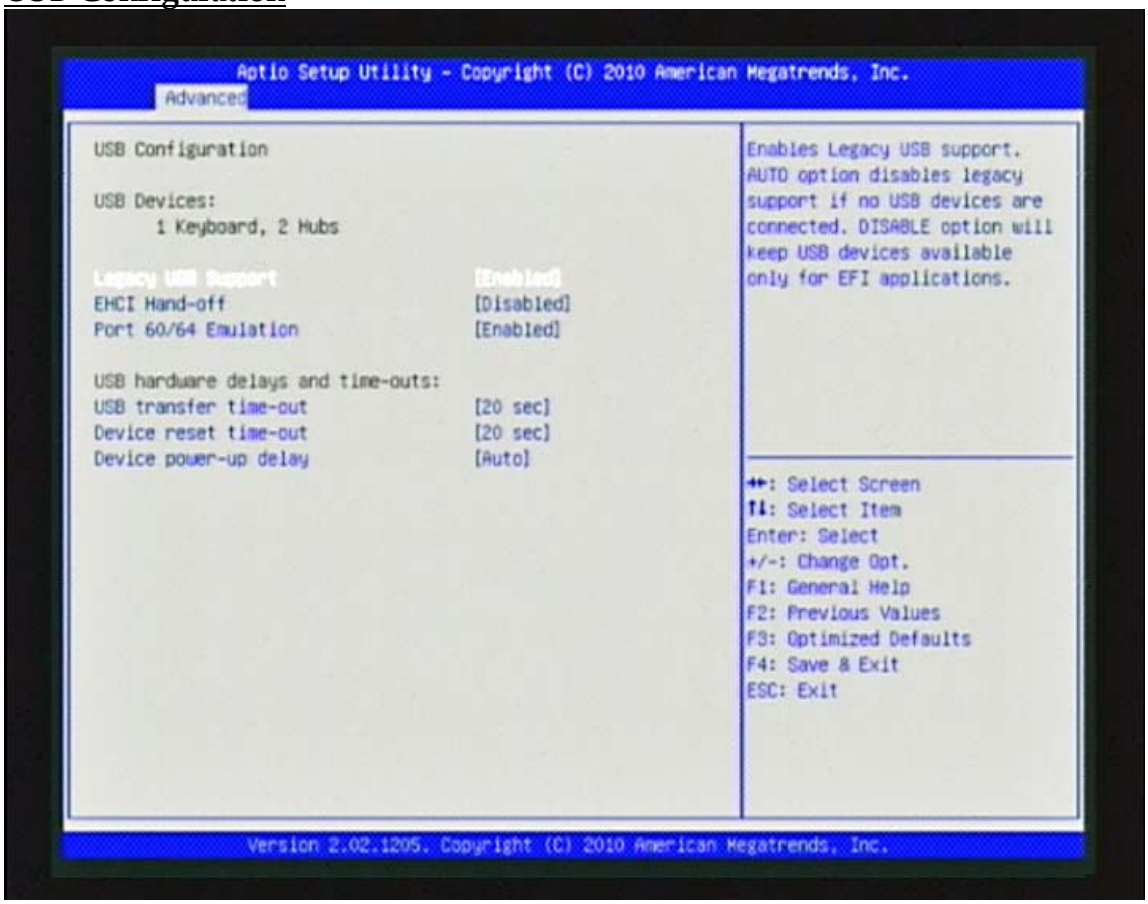
DVMT/FIXED Memory
Choices: 128MB, 256MB, Maximum

IGD – Boot Type
Choices: VBIOS Default, CRT, DVI, HDMI

Intel TXT(LT) Configuration



USB Configuration



Legacy USB Support
Choices: Disabled, Enabled

EHCI Hand-off
Choices: Disabled, Enabled

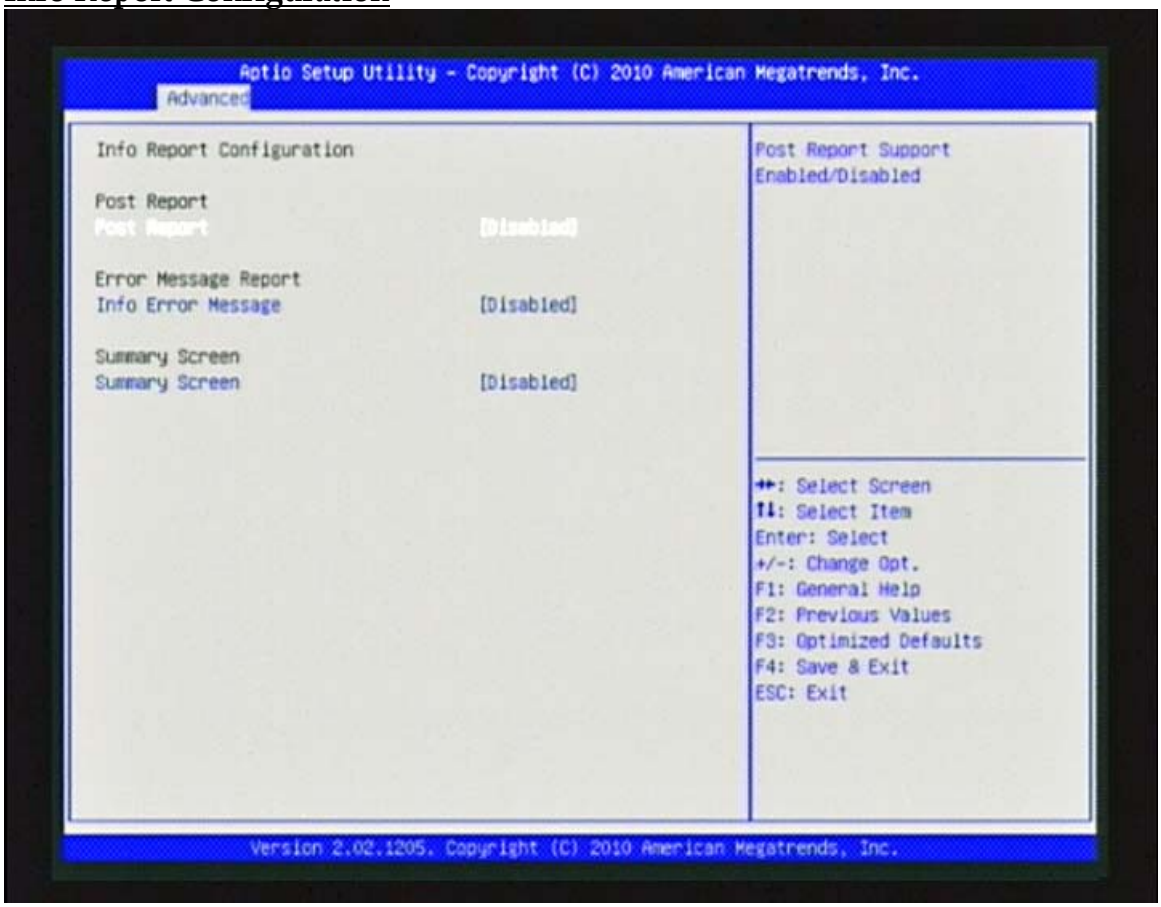
Port 60/64 Emulation
Choices: Disabled, Enabled

USB Transfer time-out
Choices: 1, 5, 10, 20 sec

Device reset time-out
Choices: 10, 20, 30, 40 sec

Device power-up delay
Choices: Auto, Manual

Info Report Configuration

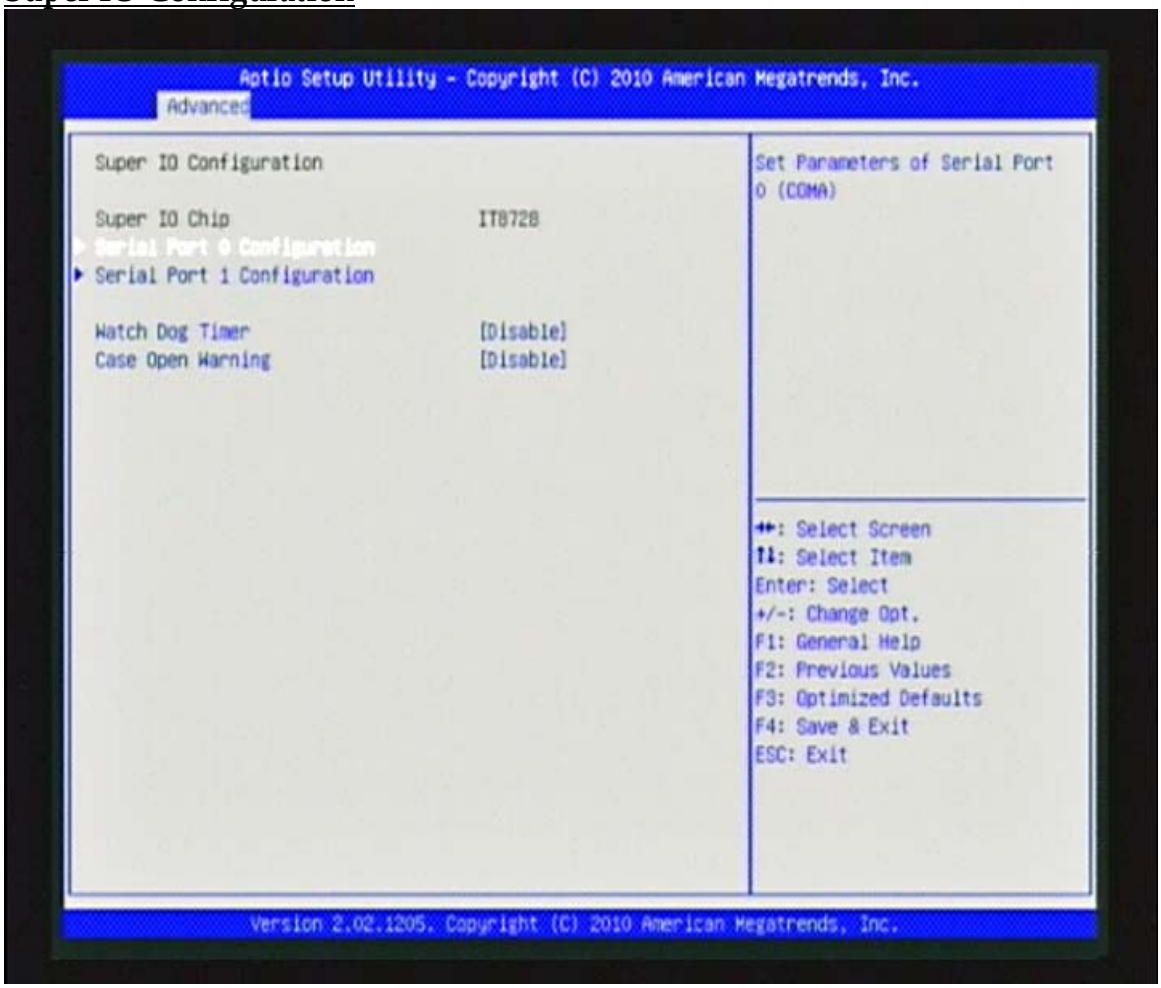


POST Report
Choices: Disabled, Enabled

Info Error Message
Choices: Disabled, Enabled

Summary Screen
Choices: Disabled, Enabled

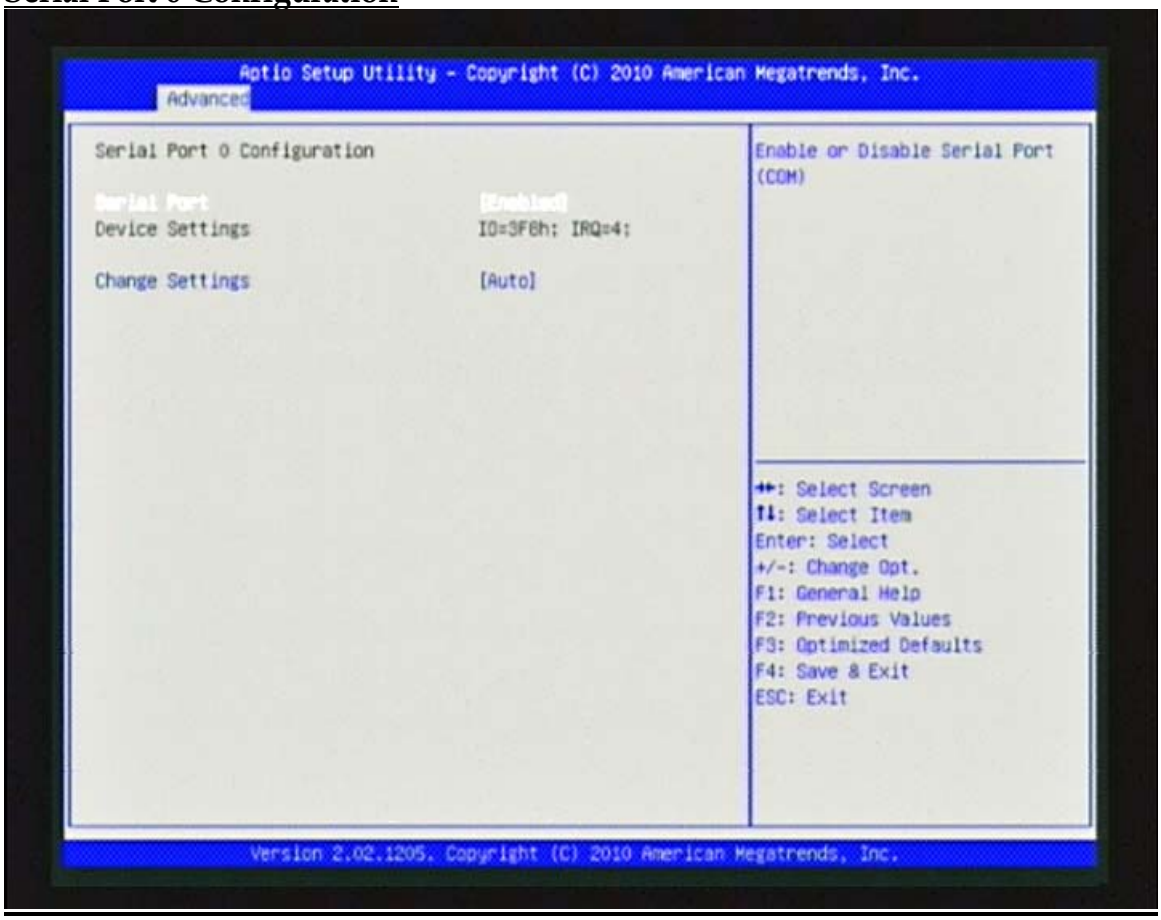
Super IO Configuration



Watch Dog Timer
Choices: Disabled, 10, 20, 30, 40, 50, 60 Seconds

Case Open Warning
Choices: Disabled, Enabled

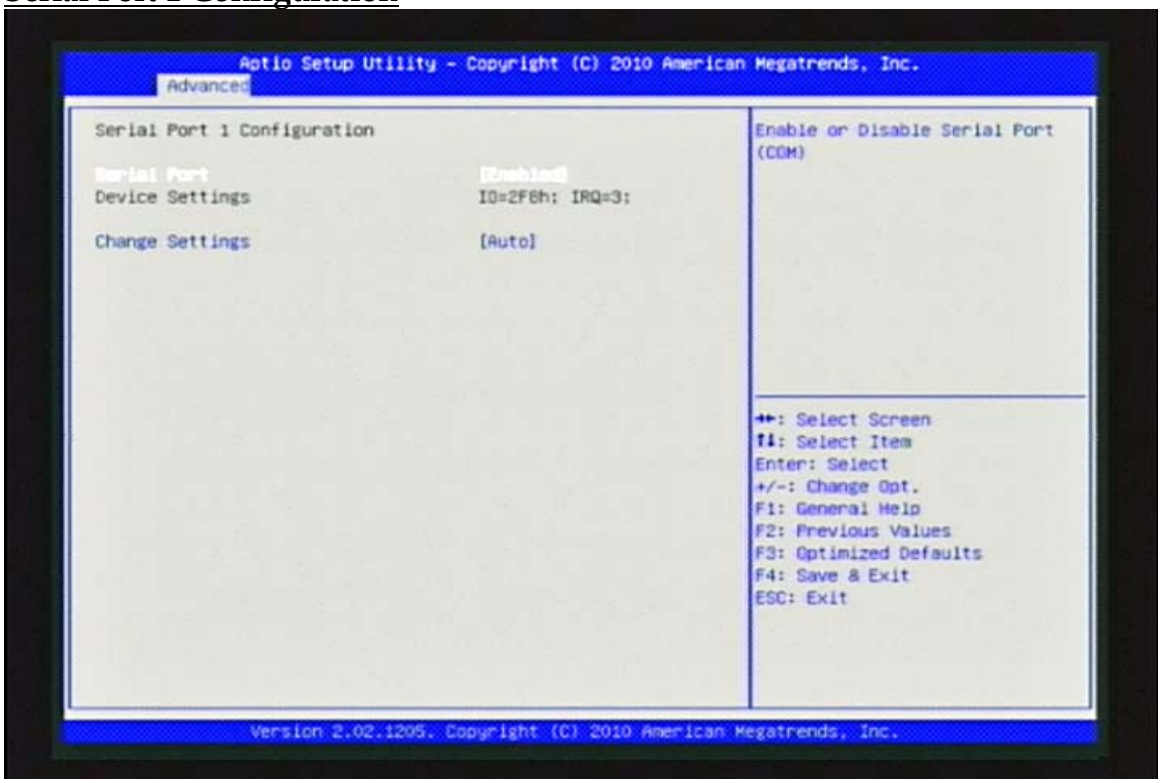
Serial Port 0 Configuration



Serial Port
Choices: Disabled, Enabled

Change Settings
Choices: Auto,
IO=3F8h; IRQ=4;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

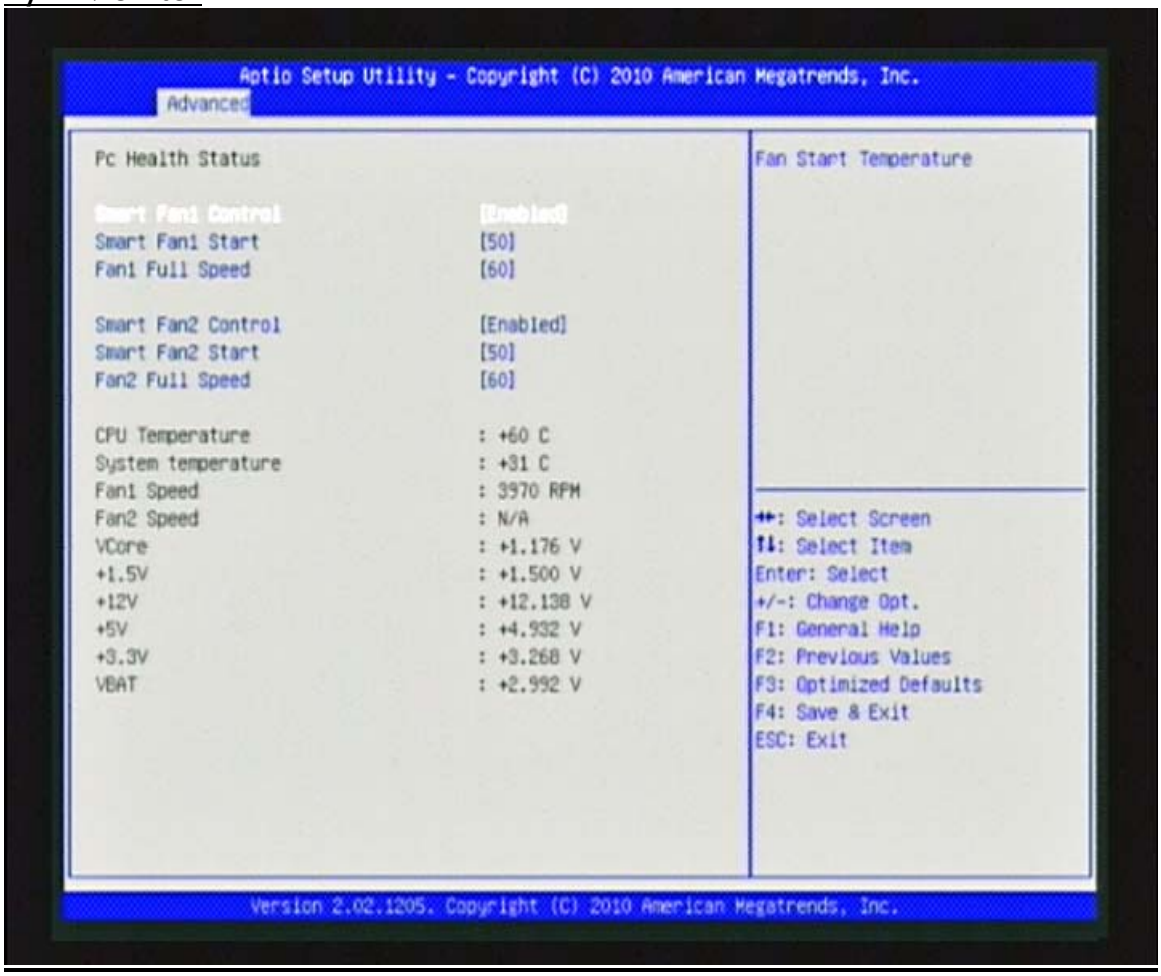
Serial Port 1 Configuration



Serial Port
Choices: Disabled, Enabled

Change Settings
Choices: Auto,
IO=2F8h; IRQ=4;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

H/W Monitor



Smart Fan1 Control
Choices: Disabled, Enabled

Smart Fan1 Start
Choices: 25, 30, 35, 40, 45, 50, 55, 60, 65, 70

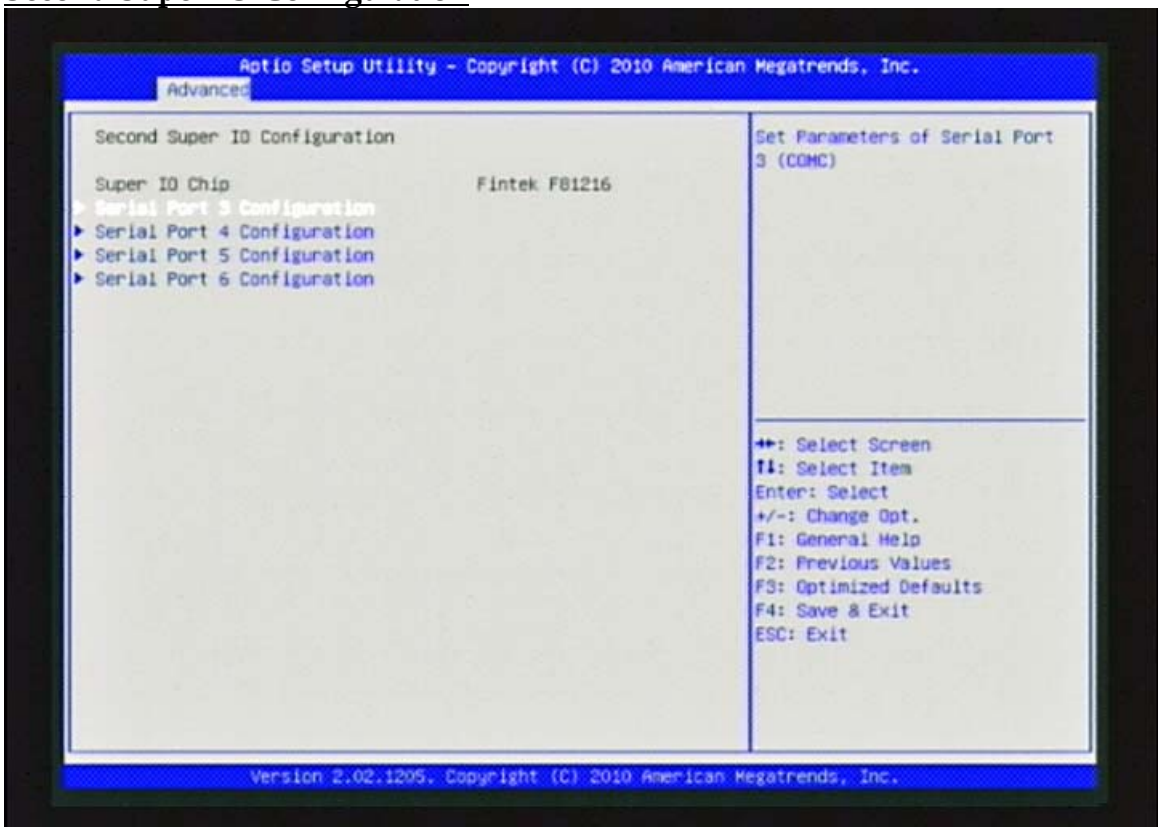
Fan1 Full Speed
Choices: 60, 65, 70, 75

Smart Fan2 Control
Choices: Disabled, Enabled

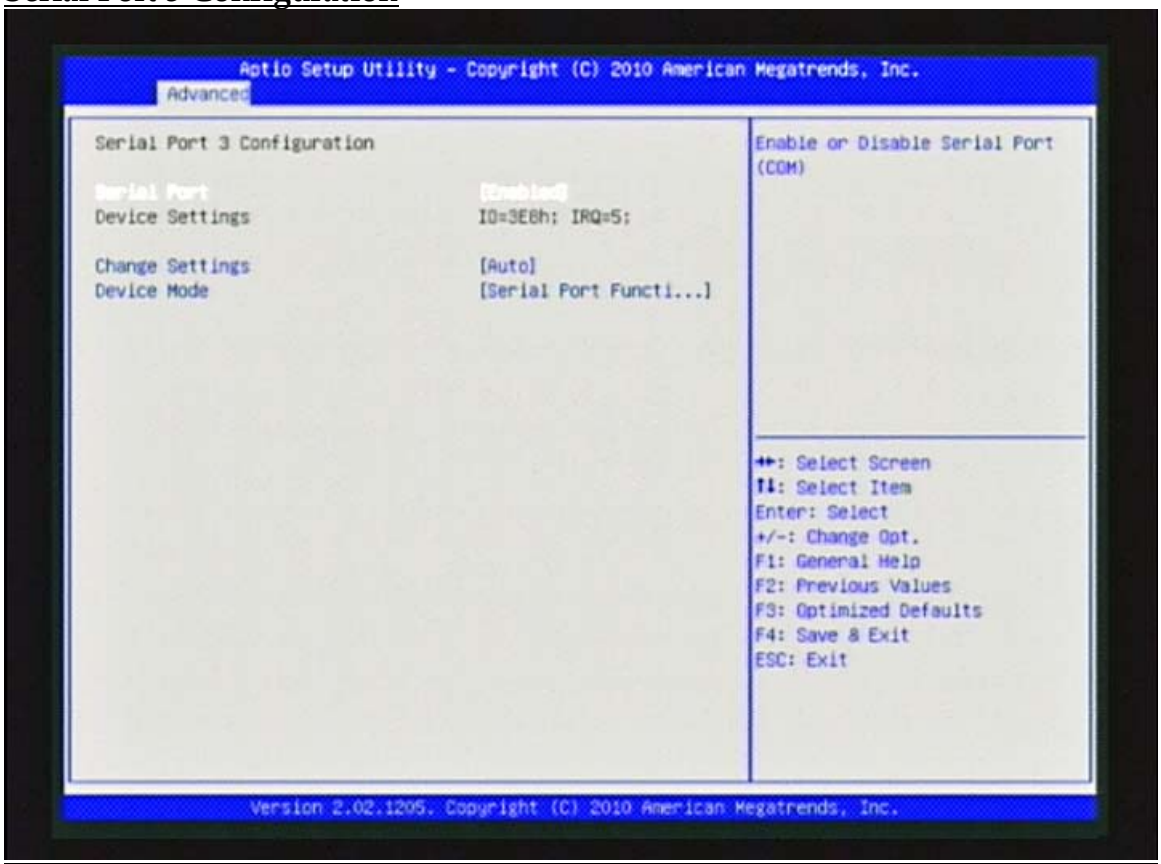
Smart Fan2 Start
Choices: 25, 30, 35, 40, 45, 50, 55, 60, 65, 70

Fan2 Full Speed
Choices: 60, 65, 70, 75

Second Super IO Configuration



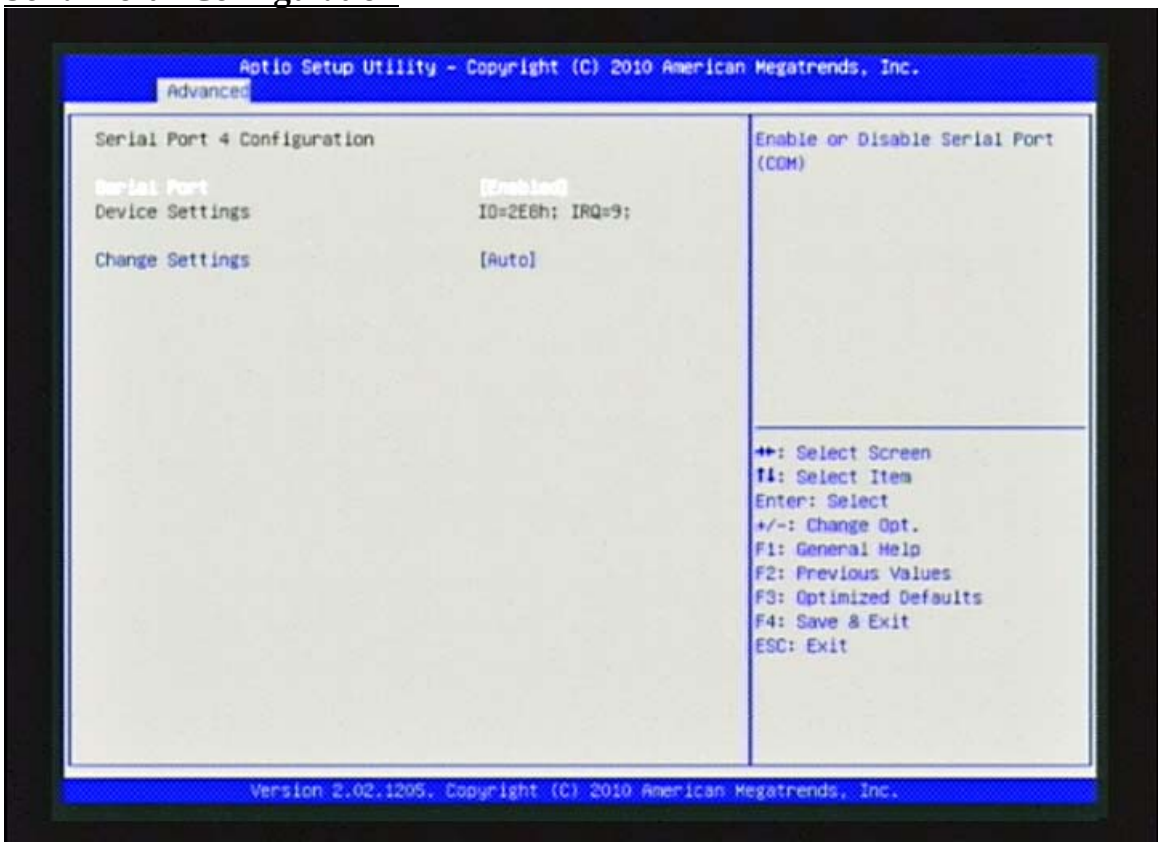
Serial Port 3 Configuration



Serial Port
Choices: Disabled, Enabled

Change Setting
Choices: Auto,
IO=3F8h; IRQ=3;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

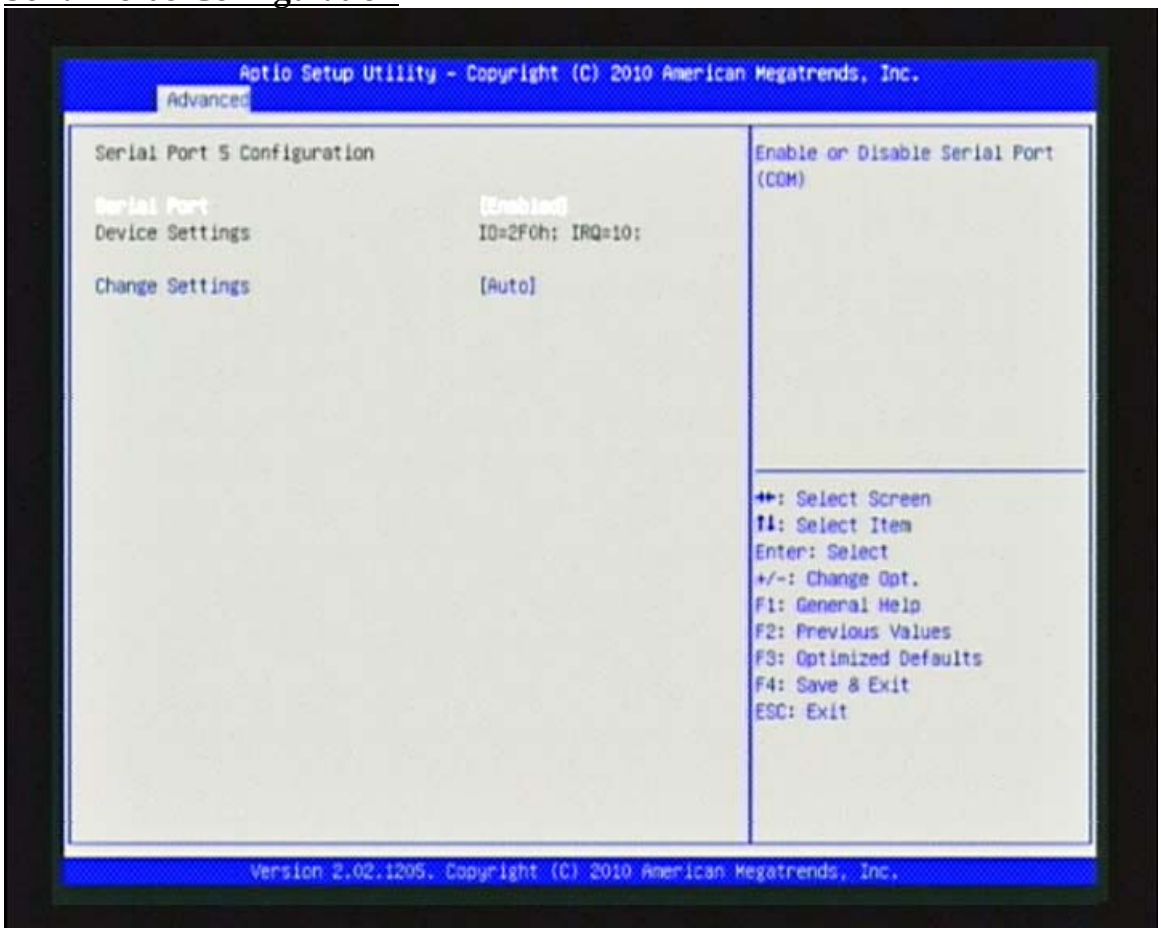
Serial Port 4 Configuration



Serial Port
Choices: Disabled, Enabled

Change Setting
Choices: Auto,
IO=2F8h; IRQ=3;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

Serial Port 5 Configuration



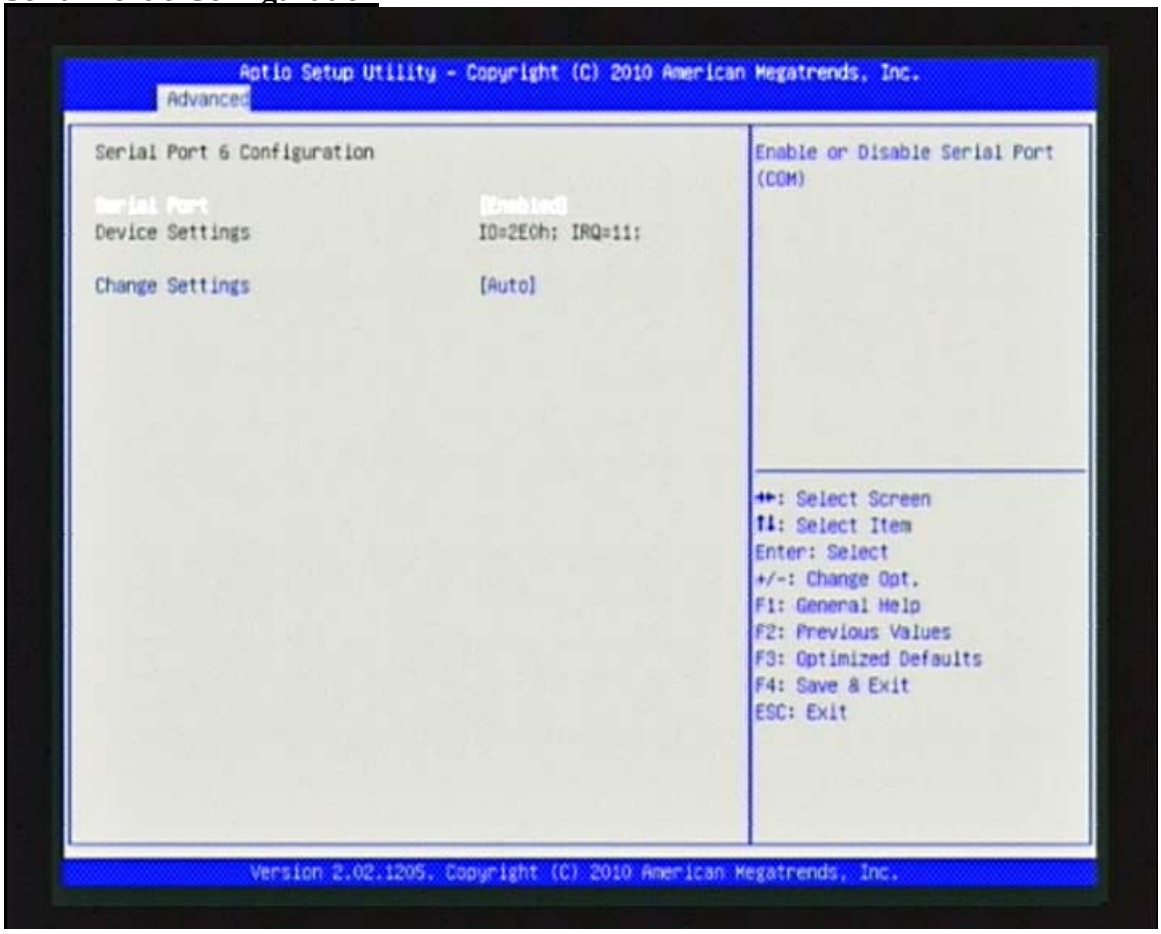
Serial Port

Choices: Disabled, Enabled

Change Setting

Choices: Auto,
IO=3E8h; IRQ=3;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

Serial Port 6 Configuration



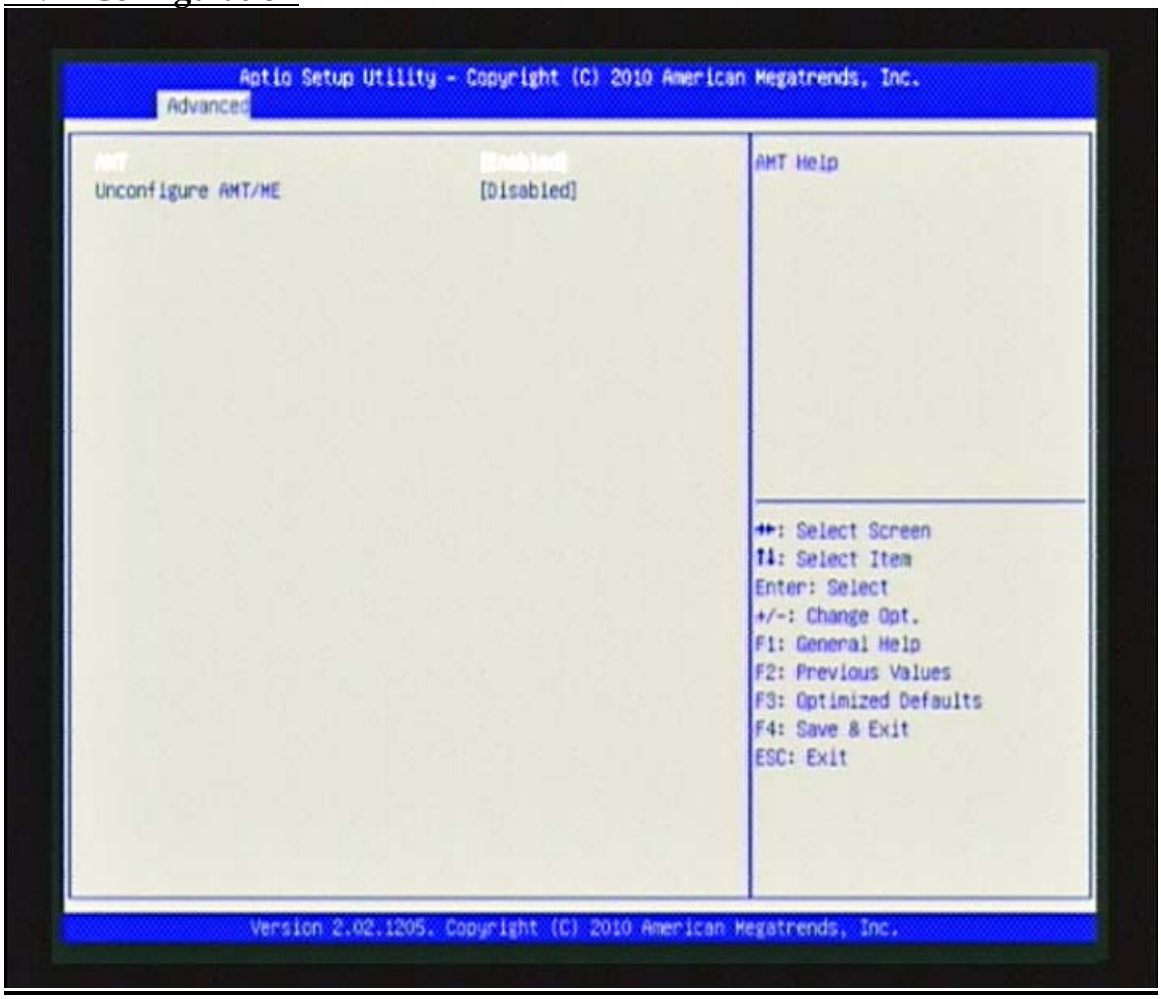
Serial Port

Choices: Disabled, Enabled

Change Setting

Choices: Auto,
IO=2E8h; IRQ=3;
IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

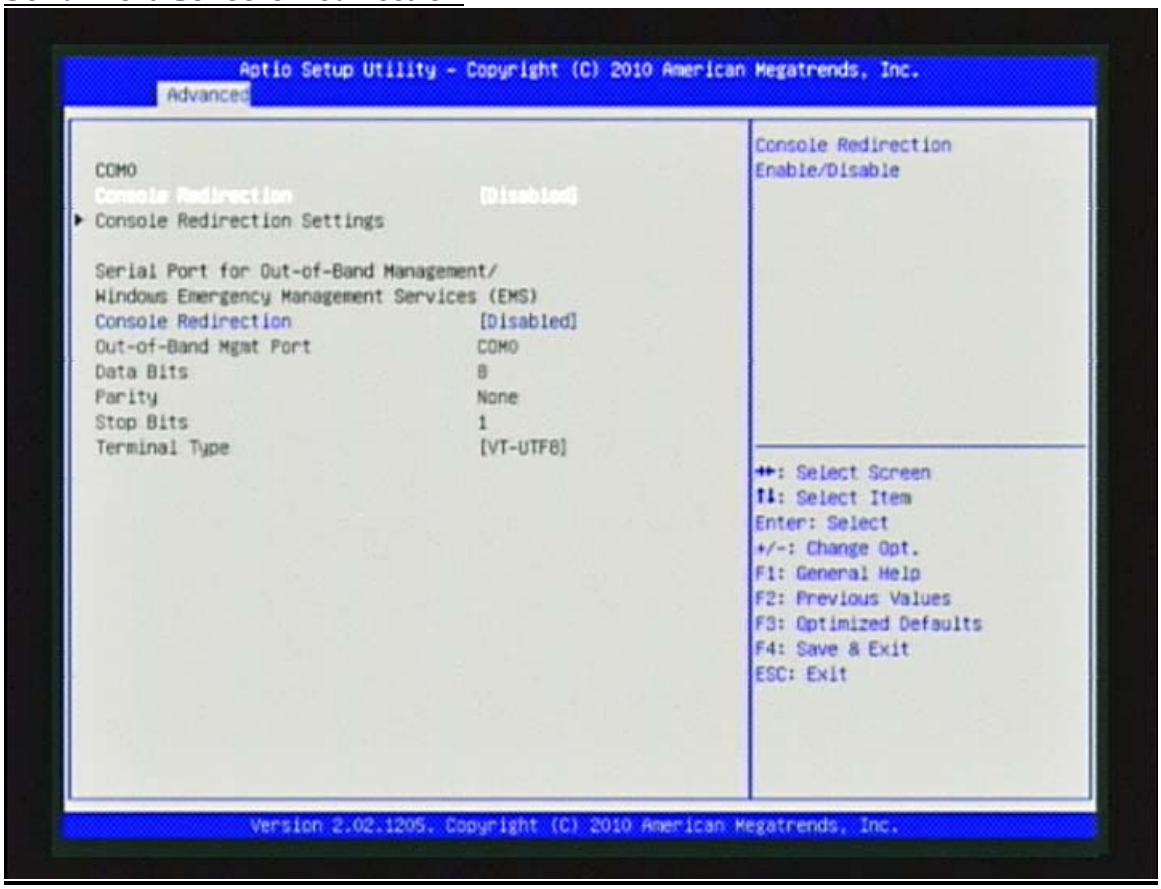
AMT Configuration



AMT
Choices: Disabled, Enabled

Unconfigure AMT/ME
Choices: Disabled, Enabled

Serial Port Console Redirection

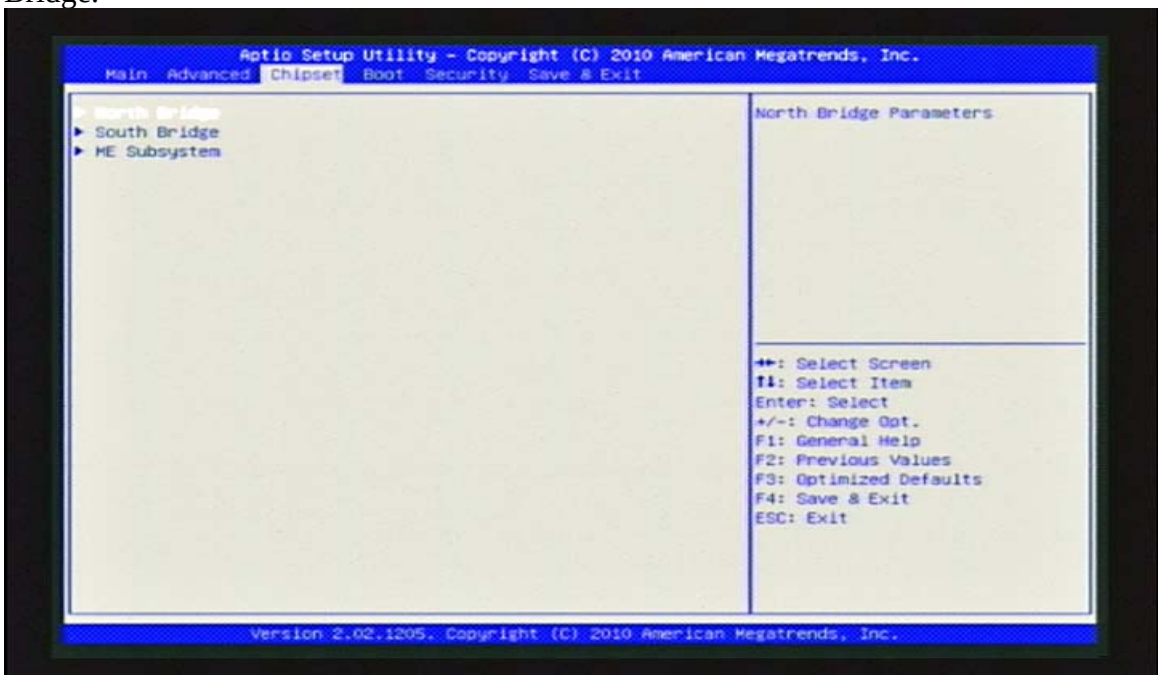


Console Redirection

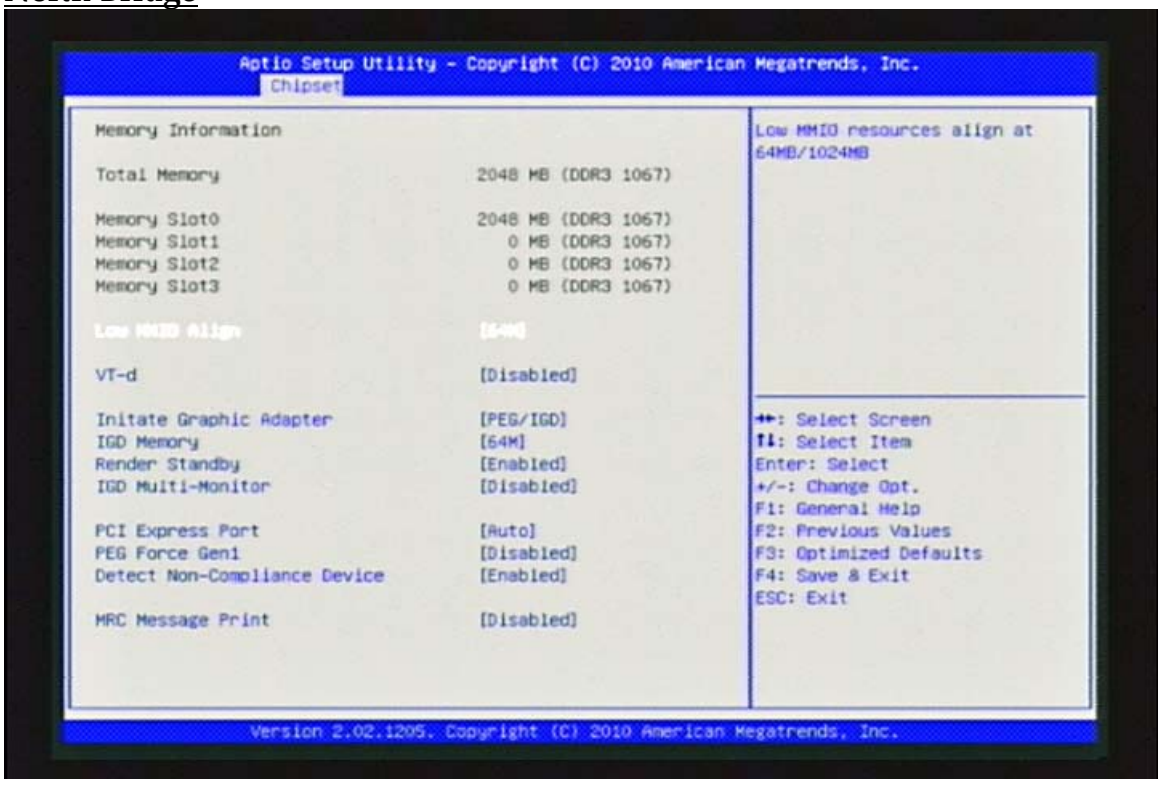
Choices: Disabled, Enabled

4.4 Chipset

This menu controls the advanced features of the onboard Host Bridge and South Bridge.



North Bridge



Low MMIO Align
Choices: 64M, 1024M

VT-D
Choices: Disabled, Enabled

Intate Graphic Adapter
Choices: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI

IGD Memory
Choices: Disable, 32M, 64M,128M

Render Standby
Choices: Disabled, Enabled

IGD Multi-Monitor
Choices: Disabled, Enabled

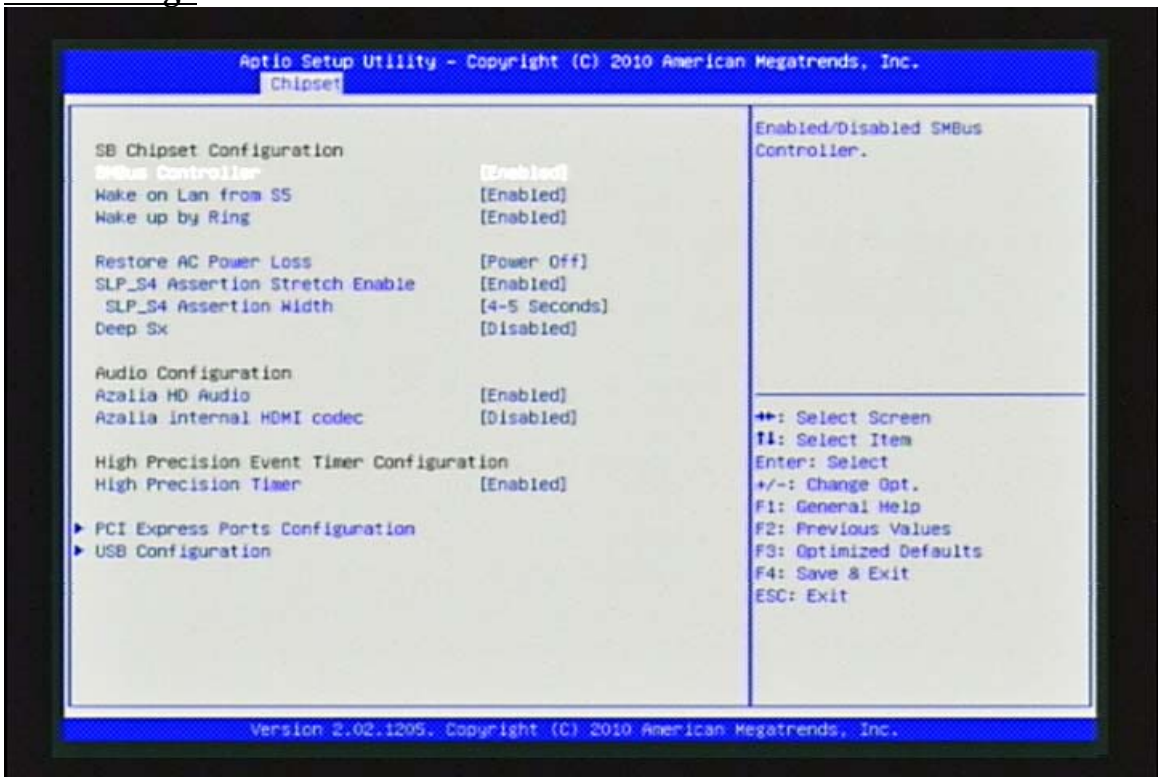
PCI Express Port
Choices: Disabled, Enabled, Auto

PEG Force Gen1
Choices: Disabled, Enabled

Detect Non-Compliance Device
Choices: Disabled, Enabled

MRC Message Print
Choices: Disabled, Enabled

South Bridge



SMbus Controller
Choices: Disabled, Enabled

Wake On Lan from S5
Choices: Disabled, Enabled

Wake up by Ring
Choices: Disabled, Enabled

Restore AC Power Loss
Choices: Power off, Power on, Last State

SLP_S4 Assertion Stretch Enable
Choices: Disabled, Enabled

SLP_S4 Assertion Width
Choices: 1-2, 2-3, 3-4, 4-5 Seconds

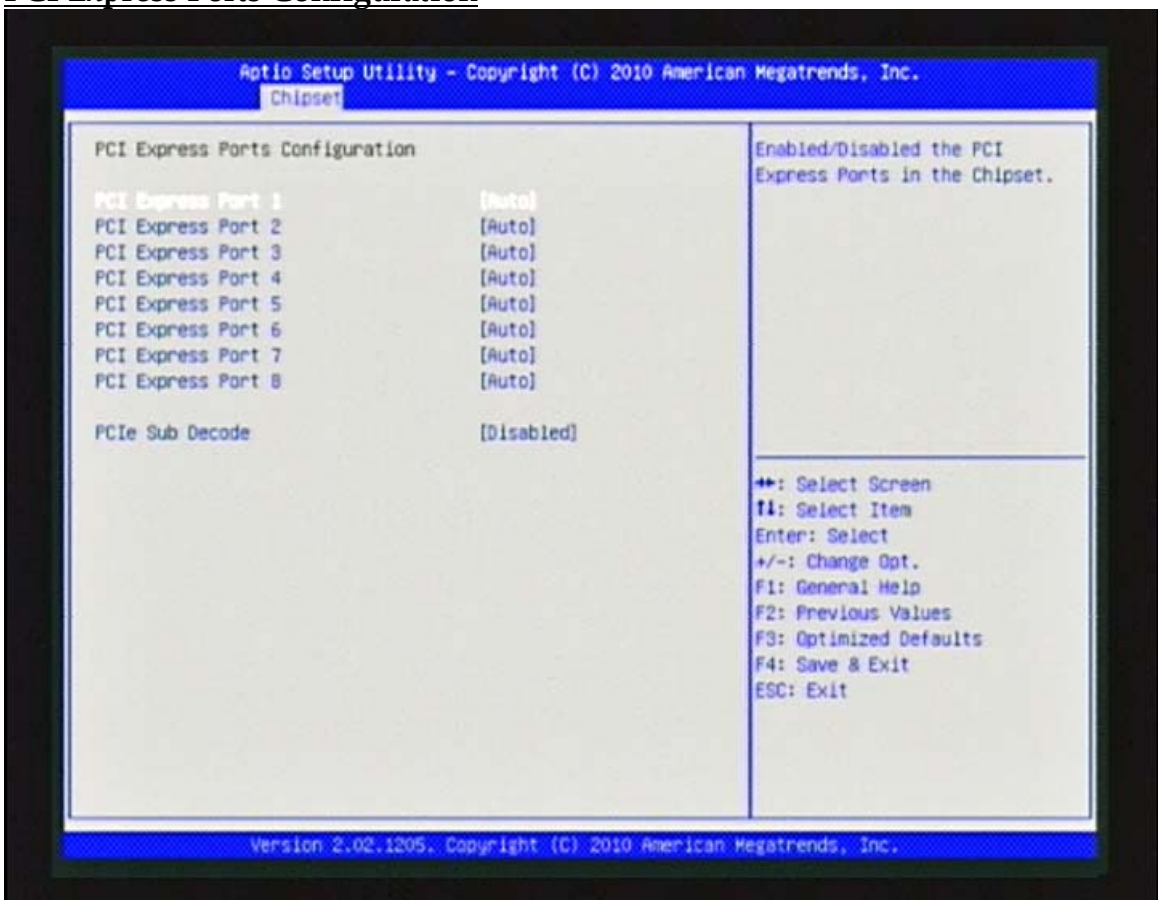
Deep Sx
Choices: Disabled, Enable in S5(Battery), Enable in S5, Enable in S4 and S5(Battery), Enable in S4 and S5

Azalia HD Audio
Choices: Disabled, Enabled

Azalia Internal HDMI codec
Choices: Disabled, Enabled

High Precision Timer
Choices: Disabled, Enabled

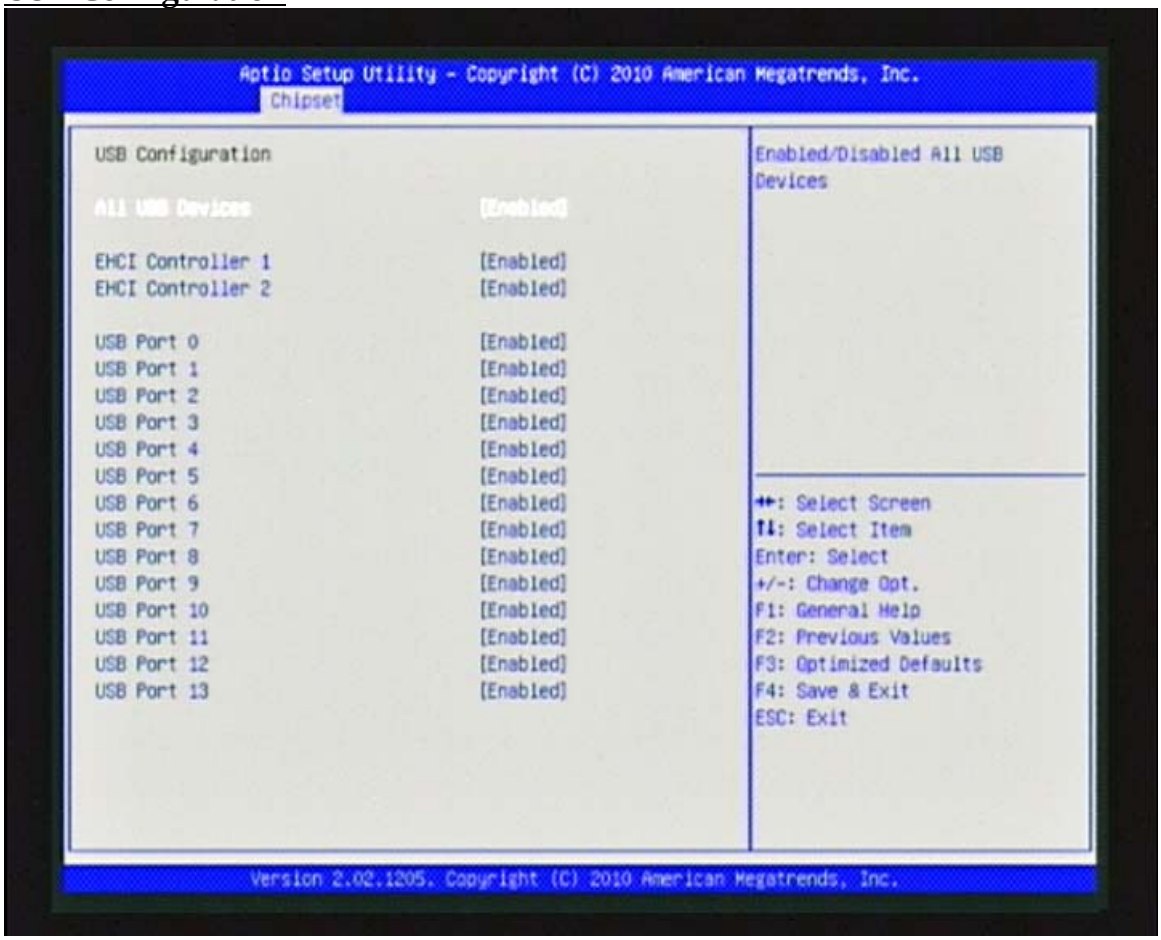
PCI Express Ports Configuration



PCI Express Port 1~8
Choices: Disabled, Enabled, Auto

PCIe Sub Decode
Choices: Disabled, Enabled

USB Configuration



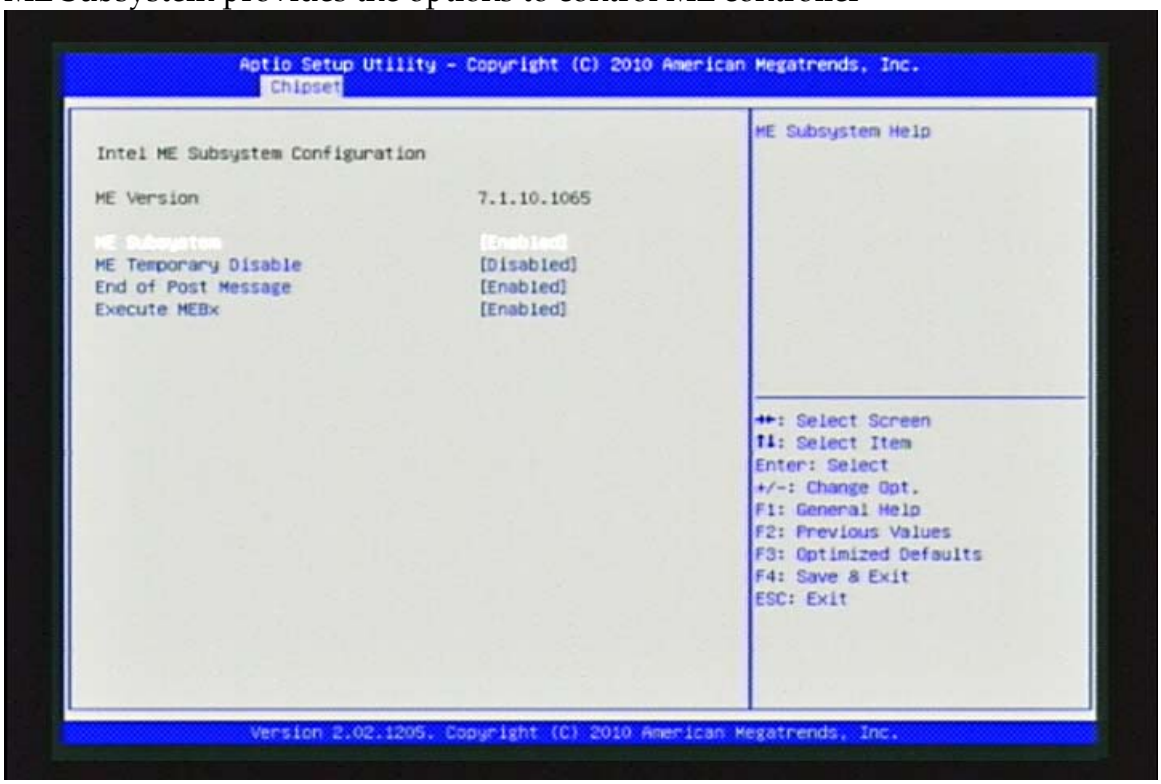
All USB Devices
Choices: Disabled, Enabled

EHCI Controller 1~2
Choices: Disabled, Enabled

USB Port 0~13
Choices: Disabled, Enabled

ME Subsystem

ME Subsystem provides the options to control ME controller



ME Subsystem

Choices: Disabled, Enabled

ME Temporary Disable

Choices: Disabled, Enabled

End of Post Message

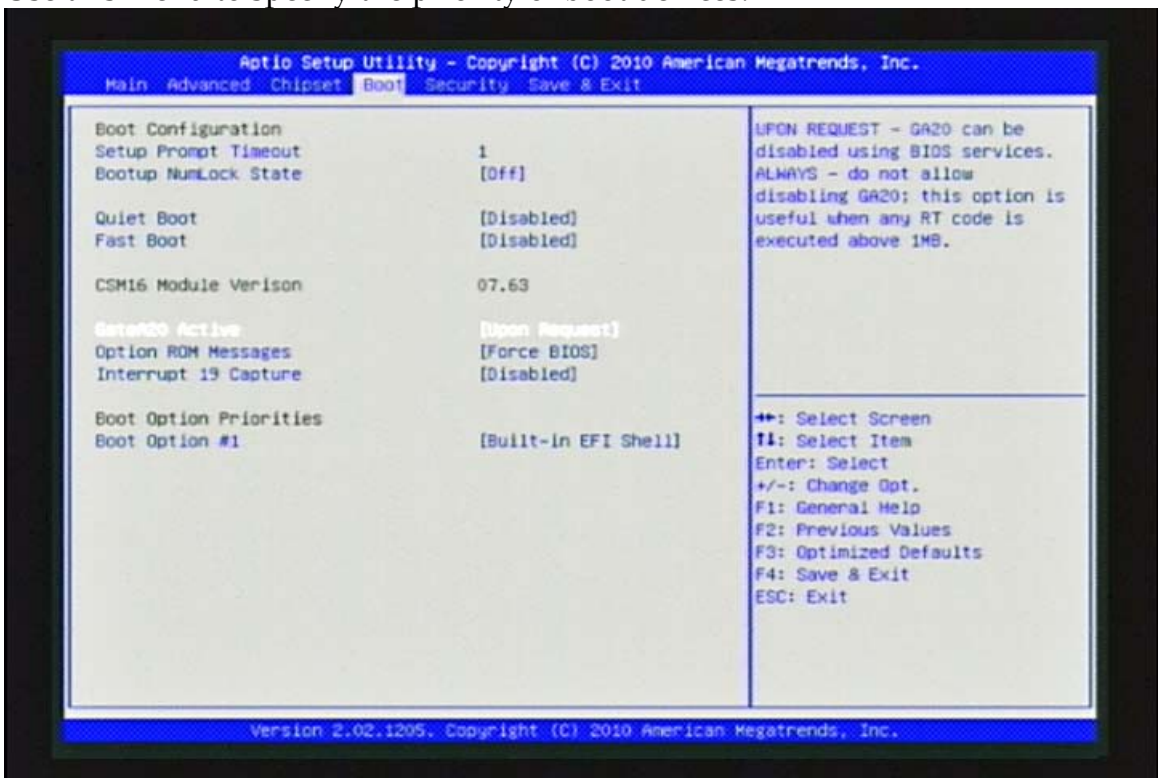
Choices: Disabled, Enabled

Execute MEBx

Choices: Disabled, Enabled

4.5 Boot

Use this menu to specify the priority of boot devices.



Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

Choices: Disabled, Enabled.

Fast Boot

Enabling this setting will cause the BIOS POST routine to skip some of its tests during boot up for faster system boot.

Choices: Disabled, Enabled.

Boot Up Num-Lock State

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

Choices: On, Off.

GateA20 Active
Choices: Upon Request, Always

Option ROM Messages
This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

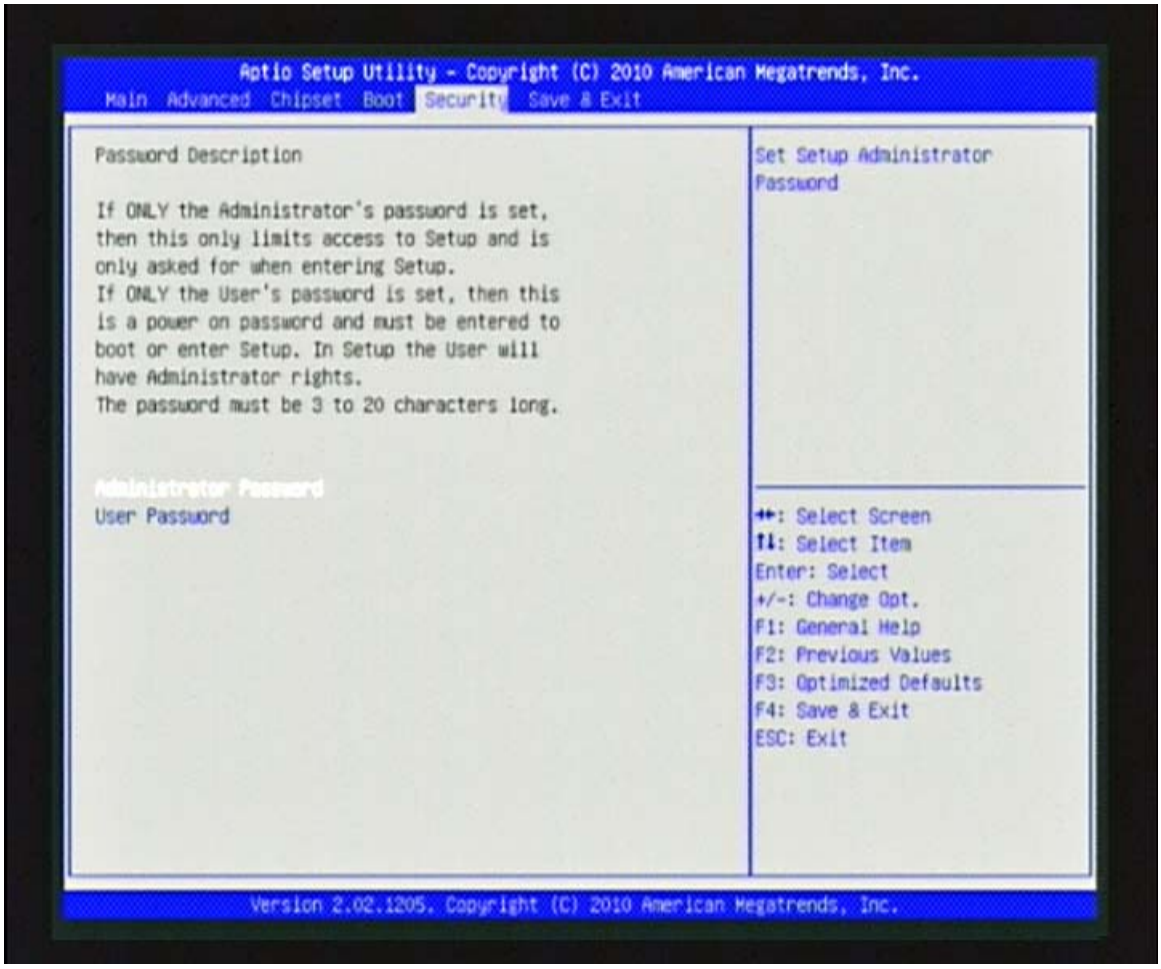
Choices: Force BIOS, Keep Current.

Interrupt 19 Capture
Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.
When it is disabled, the ROM BIOS of these host adaptors will not be able to "capture" the Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

Choices: Disabled, Enabled.

4.6 Security

Use this menu to set supervisor and user passwords.

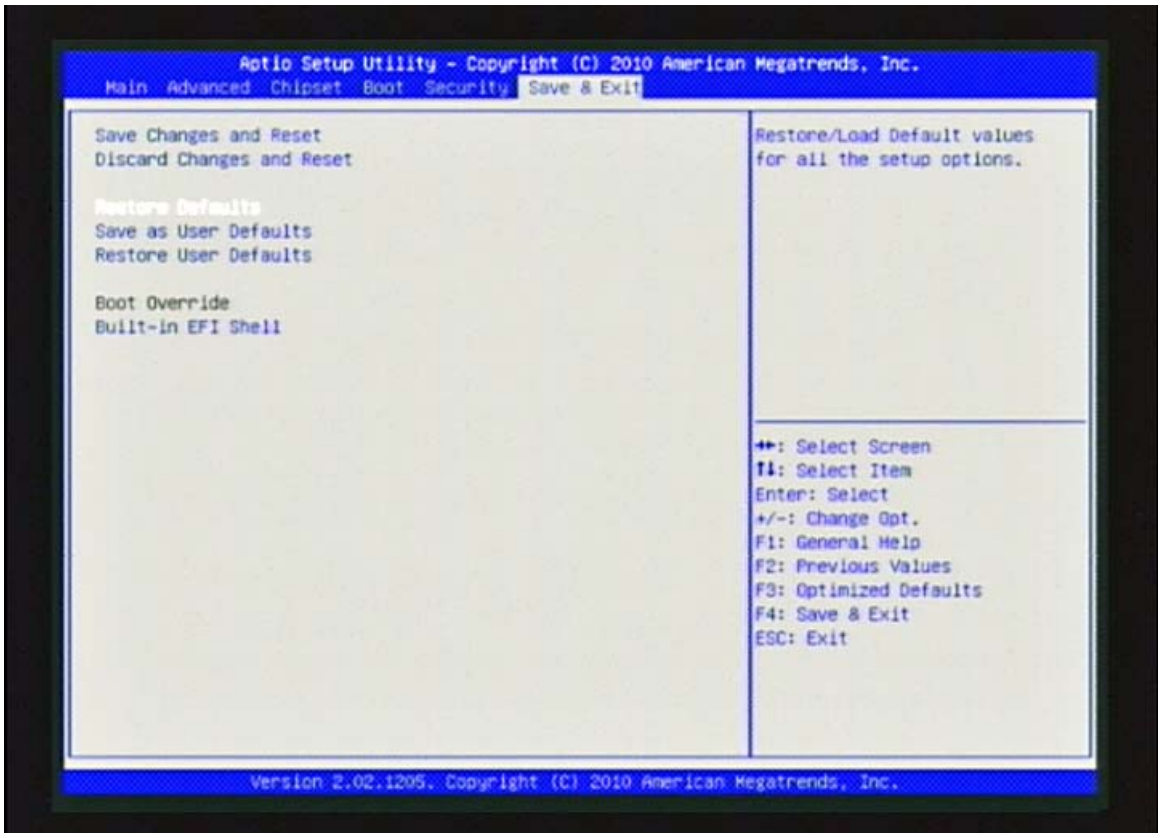


Administrator Password
Administrator Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password
User Password controls access to the system at boot. These settings allow you to set or change the user password.

4.7 Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Discard Changes and Exit
Abandon all changes and exit the Setup Utility.

Save Changes and Reset
Exit System Setup and save your changes to CMOS then reboot.

Discard Changes and Reset
Abandon all changes and exit the Setup Utility then reboot

Restore Defaults
Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Save as User Defaults
Save all changes and considers as User's default.

Restore User Default
Restore the setting according to User's default

Launch EFI Shell from filesystem device

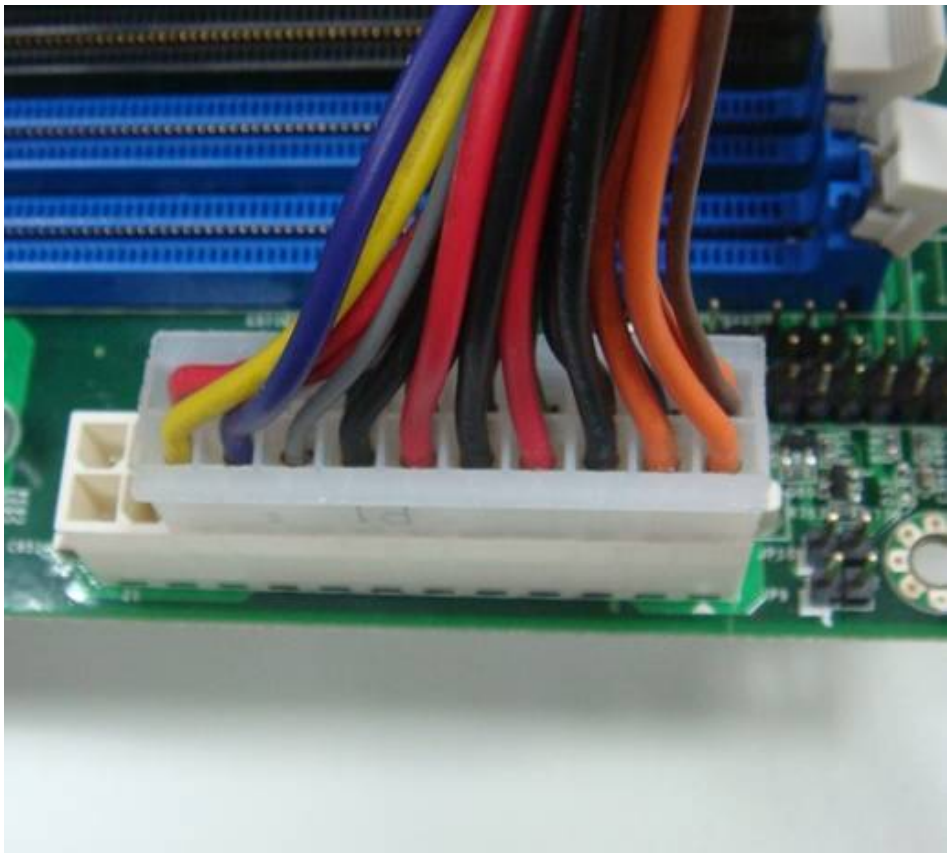
To enter the Built-in EFI shell for further modification such as upgrade BIOS.

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get RUBY-D711/D712 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

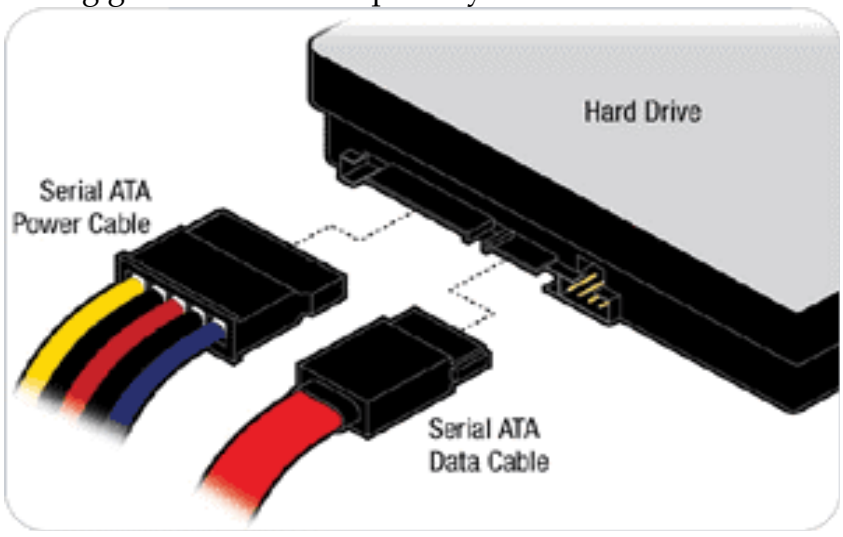


RUBY-D711/D712 supports ATX. Therefore, there is no other setting that really needs to be
set up. However, there are only two connectors that must be connected—J7 (4 pins
CPU +12V main power connector) & J36 (20 pins ATX Power Connector)

ATX Power Connector
4-Pins CPU Main Power Connector

Serial ATA Hard Disk Setting for IDE/RAID/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total six connectors, SATA1~6 port. The installation of Serial ATA is
simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1/5/10) and AHCI application for system, please follow up
setting guide in BIOS setup utility



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 204-pin DDR3 memory, keyboard, mouse, floppy drive, SATA hard disk, DVI-I connector, but it only can use on DVI-D function, doesn't support DVI-I function, device power cables,
ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible
to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with RUBY-D711/D712, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting
When prompted with the main setup menu, please scroll down to "Load Optimal
Defaults", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to
do this so you can be sure the system is running with the BIOS setting that Portwell
has highly endorsed. As a matter of fact, users can load the default BIOS setting any
time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks
In the BIOS => Standard CMOS setup menu, pick up any one from
Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected
IDE port and its access mode to "Auto". This will force system to automatically pick
up the IDE devices that are being connected each time system boots up.

Improper disable operation
There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/

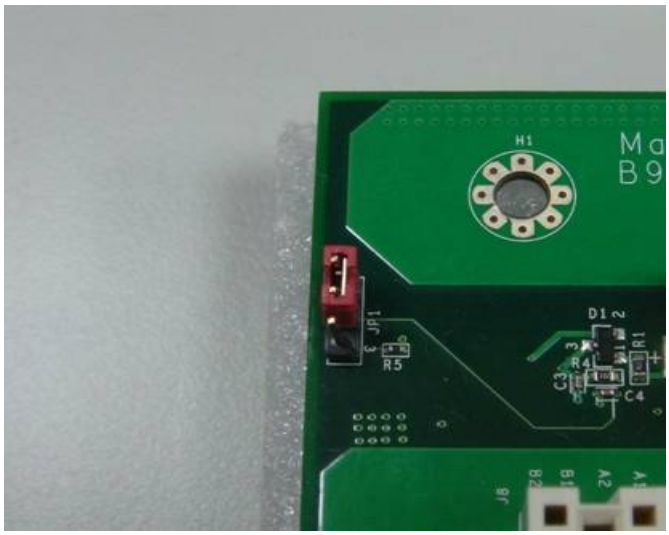
COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are
Disable COM1 serial port to release IRQ #4
Disable COM2 serial port to release IRQ #3
Etc…

A quick review of the basic IRQ mapping is given below for your reference.
IRQ #0 System Timer
IRQ #1 Keyboard Event
IRQ #2 Usable IRQ
IRQ #3 COM2
IRQ #4 COM1
IRQ #5 Usable IRQ
IRQ #6 Diskette Event
IRQ #7 Usable IRQ
IRQ #8 Real-Time Clock
IRQ #9 Usable IRQ
IRQ #10 Usable IRQ
IRQ #11 Usable IRQ
IRQ #12 IBM Mouse Event
IRQ #13 Coprocessor Error
IRQ #14 Hard Disk Event
IRQ #15 Usable IRQ
It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FQA

Installation Problem
Question: I forget my password of system BIOS, what am I supposed to do?
Answer: You can simply short JP1 pin 2-3 to reset your password.



Question: How to update the BIOS file of the RUBY-D711/D712?
Answer:
Please visit web site of the Portwell download center as below hyperlink and registeran account. http://www.portwell.com.tw/support/ Input your User name and password to log in the download center. Select the "Search download" to input the keyword "WADE-8020". Find the "BIOS" page to download the ROM file and flash utility.

Execute the zip file to root of the bootable USB Pen drive.
Insert your bootable USB Pen drive in WADE-8020 board and power-on.
Input the "FPT /f XXXXX.ROM /BIOS" to start to update BIOS. (“XXXXX” is the file name of the ROM file.)

Switch "Off" the Power Supply when you finished the update process.
To short the JP1 2-3 jumper for 5 seconds then set back to normal. (Clear CMOS)

Switch "ON" the Power Supply then press the "del" key to BIOS to load "Restore Defaults" then save them to exit.

Note:
Please visit our technical web site at http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can
mail to tsd@mail.portwell.com.tw or to our sales for further assistance. Thank you.