LABORATORY EXPERIMENTS

DIGITAL COMMUNICATION

INDEX

EXPERIMENT NO. 1: **Pulse Amplitude Modulation**

AIM: To study PAM generator and detector and observe the waveforms.

THEORY:

Pulse Modulation may be used to transmit analoginformation, such as continuous speech or data. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times, together with any information Pulse that may be required. At the receiving end, the original waveforms may be reconstructed from the information regarding the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation and frequency modulation, the resulting receiver output can have negligible distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be infinitely variable, while in the latter a code which indicates the sample Amplitude to the nearest predetermined level is sent.Pulse Amplitude modulation (PAM) is an analog communication whichis discussed in the following section.

In PAM we have a fixed width of each pulse, but the amplitude of each pulse is made proportional to the amplitude of the modulating signal at that instant. Pulse Amplitude Modulation generation circuit is shown in Fig. (Panel layout diagram). Sampling clock is applied to the base of the Transistor Modulating signal is given in the collector of the transistor. So that the output of the transistor (collector current) varies according to the modulating signal voltage. Sampling clock given at the base of the transistor will appear at the collector (same frequency of clock) but its amplitude is proportional to the modulating voltage. This is Pulse Amplitude Modulation output.

The Demodulation of the Pulse Amplitude Modulation is quite a sample process. Pulse Amplitude Modulation is fed to an integration RC circuit (Low Pass Filter) from which the Demodulating signal emerges, whose amplitude at any time is proportional to the pulse amplitude modulation at that time. This signal is given to an inverting amplifier to amplify its level. So that the demodulated output is having almost equal amplitude with the modulating signal but it is having some phase difference.

APPRATUS REQUIRED:

1. **Modulating signal generator using TL084/LM324**: The TL084 is a quadruple operational amplifier fabricated on a signal modulation. It is specified over a temperature range from -40°C to +85°C. They have finite differential inputs and remain in the linear mode with an input common - mode voltage of 0V dc. Both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers.
   Application areas include AC amplifiers, RC active filters, low frequency triangle, square wave and pulse waveform generation circuits, techno meters and low speed high voltage digital logic gates. Fig. 1 shows the pin out diagram of the IC TL084.

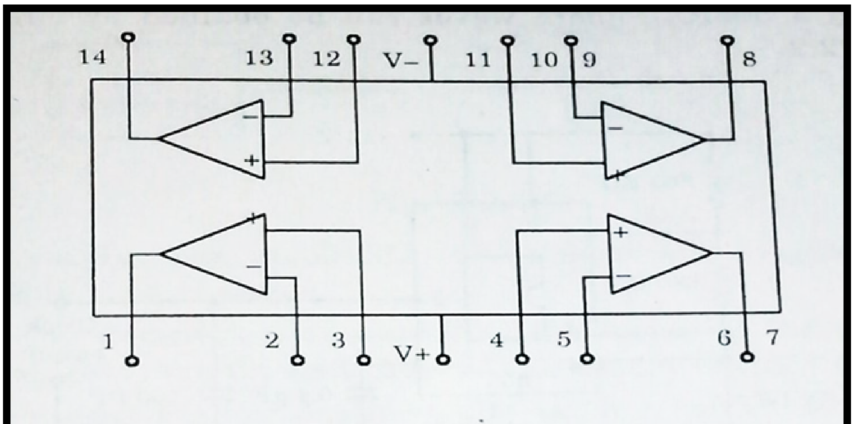


Fig. P2.1

PRINCIPAL FEATURES

- Internally frequency Compensated for unity gain/wide band width (unity gain) is 1 MHz
- Power supply range supply 3 - 26 volts
- Low input offset voltage of 2 milli volts
- Input common mode voltage range includes ground.

The solution is represented by sinusoidal oscillation of frequency:

$$f = 1/2\pi RC$$

In practice the resistor $R_1$is made slightly larger than the other resistor to ensure a sufficient positive feedback for oscillations. The Zener Diodes V_2, used to bound the output of the inverting integration integrator, serve to stabilize the amplitude of oscillations.

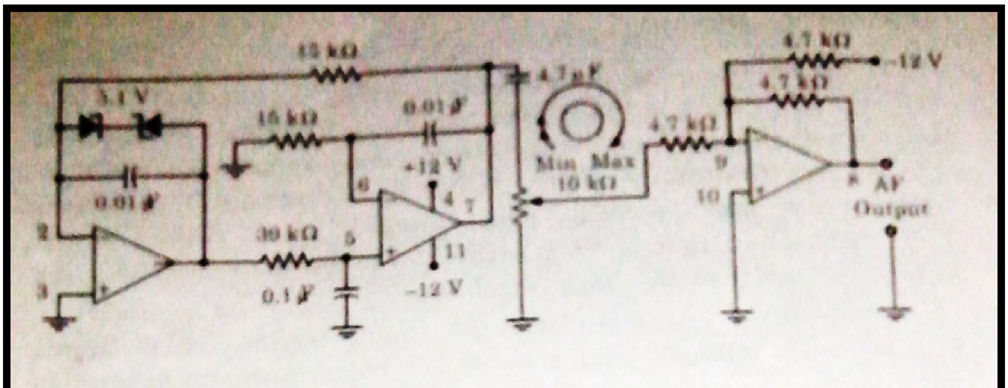


Fig. P2.2

2. **Clock generator using 555 IC:** A conventional astable circuit using a 555 IC. Square wave can be obtained by circuit shown in Fig. P2.2.

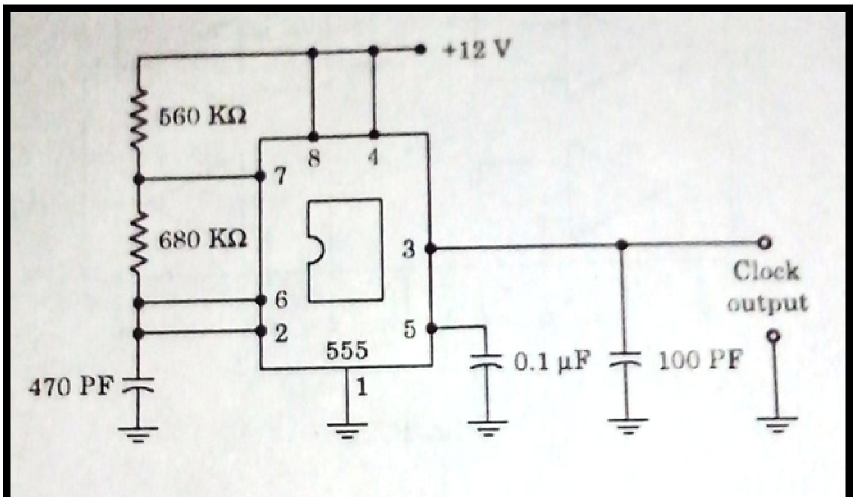


Fig. P2.3

The asymmetry of a conventional astable circuit is a result of the fact that charging and discharging times are not equal. In fig. 2 capacitor C, is charged through $R_1$and R_2while discharged through R_2. If $R_1$is made very small compared to R_2then both time constant will be reduced so that they essentially depend on C_2 and C_1. The frequency of operation (f) is approximately $0.7/R_2C_1$The frequency is of course independent to the supply voltage.

3. PAM Modulation circuit arrangement
4. PAM Demodulator circuit arrangement
5. Circuit arrangement
6. AFD Signal Generator
7. Built in DC Power supply +/- 12 V @350mA
8. Set of Patch chords and User's Manual

PROCEDURE:

1. Switch on experimental kit.
2. Observe the AF signal and carrier clock generators outputs.
3. Adjust the AF signal generator O/P to 1 Vp-p amplitude.
4. Apply the AF signal generator output and clock generators output to the PAM modulator.
5. Following figure P2.4 shows the testing procedure.

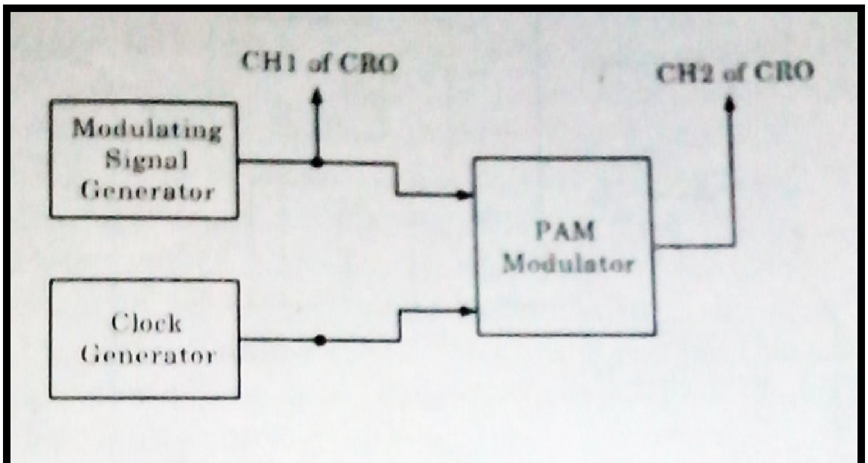


Fig. P2.4

6. By varying the amplitude of the modulating signal depth of modulation changes
7. During demodulation, connect PAM output to the input of the PAM demodulator and observe the output of PAM demodulator
8. Following Fig. P2.5 shows the testing procedure

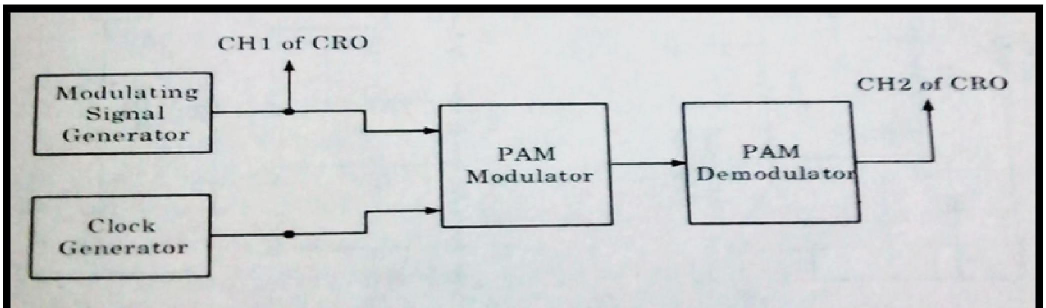
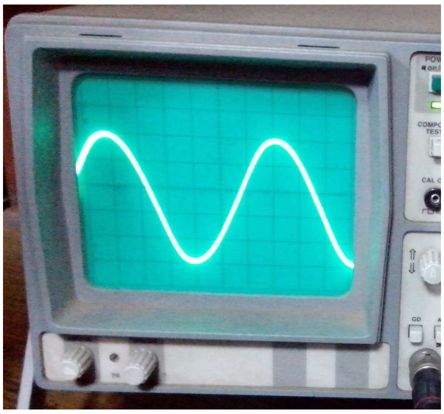
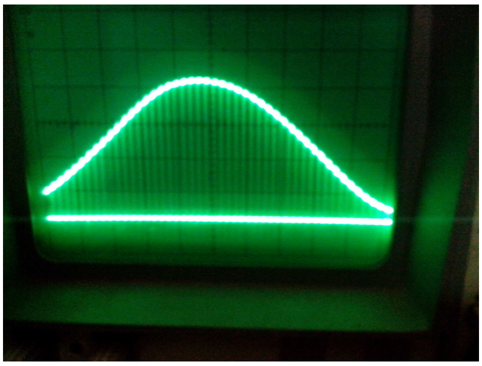
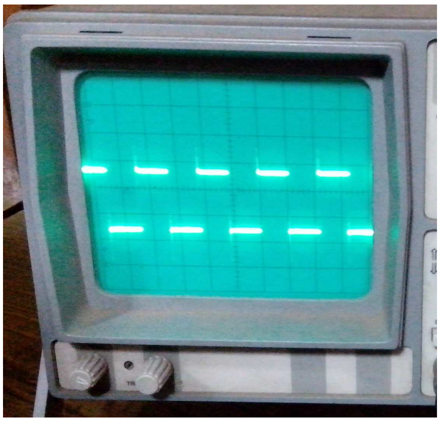
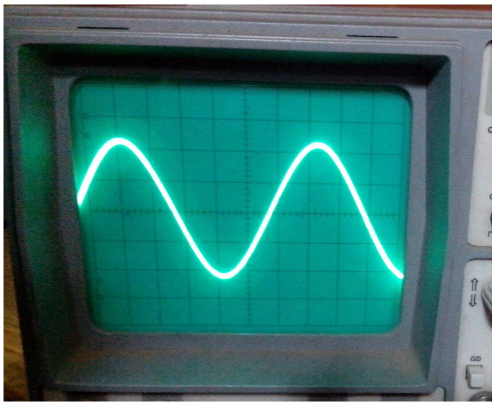
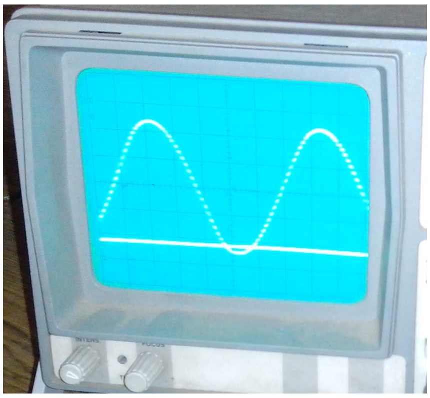


Fig. P2.5

RESULT

PAM Modulation	PAM Demodulation
 **Modulating Signal**	 **PAM Modulated Signal**
 **Carrier Pulse Signal**	 **PAM Demodulated Signal**
 **PAM Modulated Signal**	

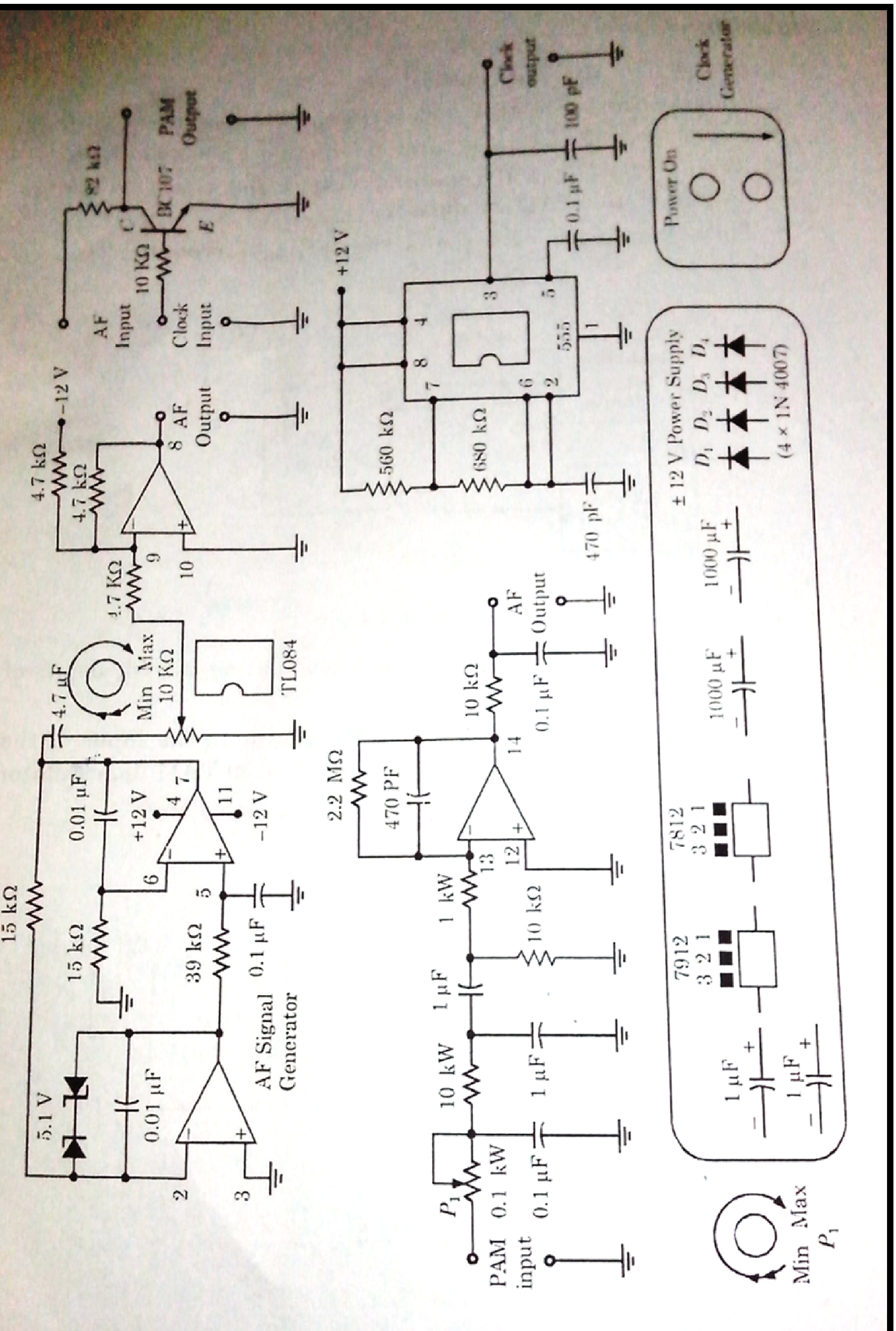


Fig. P2.6 *Circuit Diagram*

EXPERIMENT NO. 2: Pulse Width Modulation (PWM)

AIM: To study PWM modulator and demodulator and observe the waveforms.

THEORY:

A monostable multivibrator, often called a one-shot multivibrator, is a Pulse-generating circuit in which the duration of the pulse is determined by the R_C network connected externally to the 555 timer. In a stable or stand by state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go high (= V_{CC}). The time the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The mono stable circuit has only one stable state (output low), hence the name mono stable. Normally the output of the mono stable multivibrator is low.

The demodulation of the pulse width modulation is quite simple process. PWM output is given to a two state RC integrator (low pass filter) and amplified to get the voltage level equal to the AF signal given to the PWM modulator.

APPARATUS REQUIRED:

1. PWM Modulator
2. PWM Demodulator
3. Clock generator
4. AF signal generator (Variable amplitude)
5. ±12V @ 350 mA fixed dc power supply
6. PWM Modulation and Demodulation kit (Trinity Micro systems or any other kit)
7. Dual trace oscilloscope
8. Variable RPS power supply

PROCEDURE:

1. Switch ON the experiment kit shown in Fig. P3.1.
2. Observe the clock generator output and AF signal outputs.
3. Connect clock generator output to the clock input point of PWM modulator and observe the same clock on channel 1 of a dual trace CRO.
4. Trigger the CRO with respect to CHI.
5. Apply a variable DC voltage of 8 to 12 volts from any external regular power supply.
6. Observe the PWM output on CH2.
7. If we observe the PWM output, its width varies according to the DC input voltage.
8. A variable amplitude AF signal is given to observe how the PWM signals are varying for AC modulation voltages.
9. For this observe AF signal on CHI and PWM output on CH2.

NOTE: Generally we have to store PWM signals with respect to the modulating signals to get better results. Real time CRO also useful but triggering for AC modulating voltages is difficult.

10. During the demodulation, apply PWM signal to the output of demodulator and observe its output.
11. Output of the demodulator almost coincides with the modulating signal but having some phase difference due to RC networks and amplifier are in the demodulator.

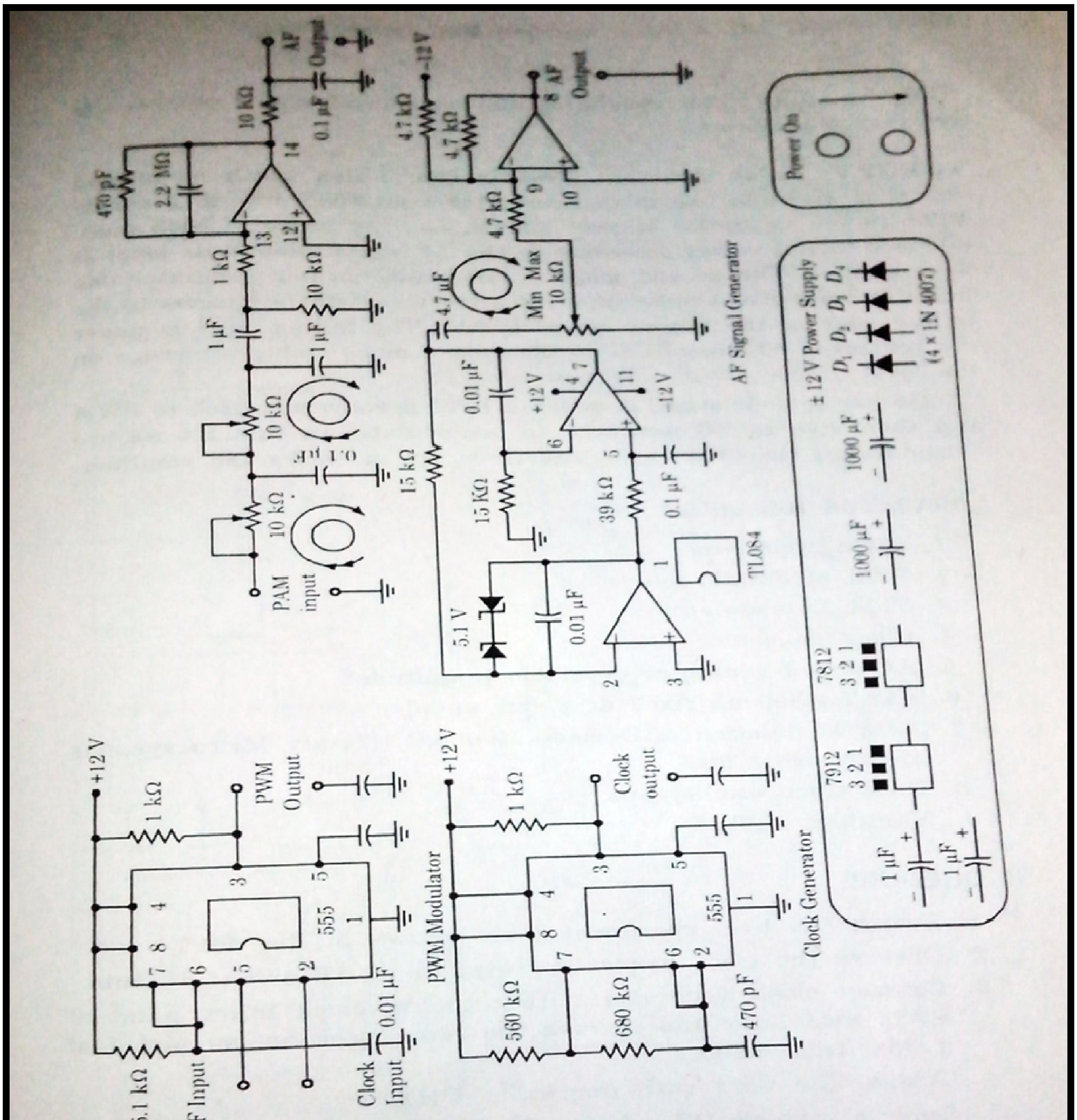
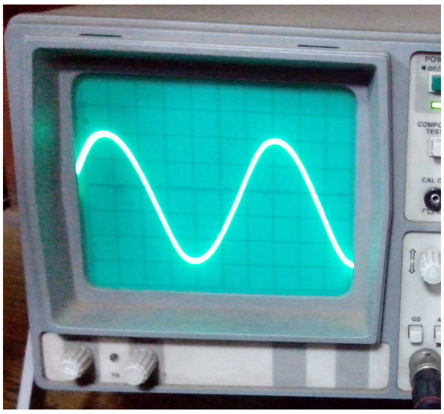
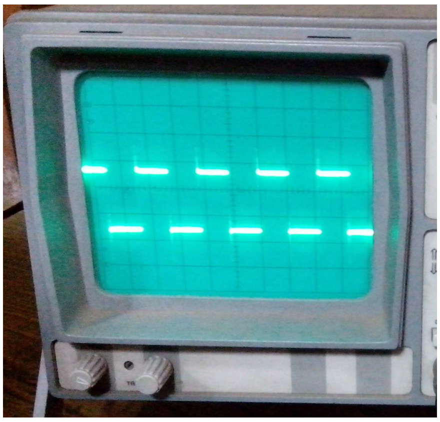
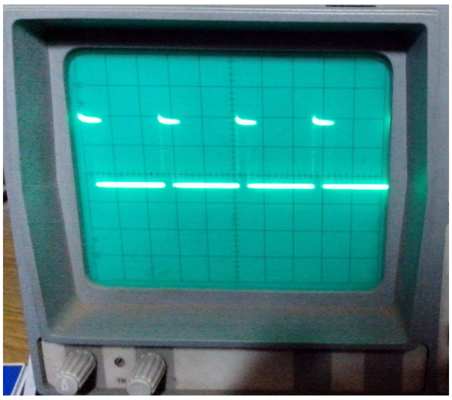
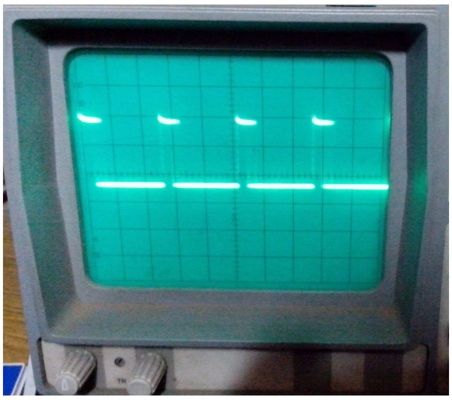
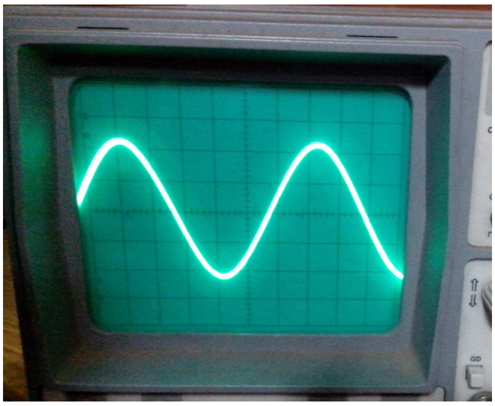


Fig. P3.1 *Circuit Diagram of PWM Modulation/Demodulation (Trinity Microsystems kit)*

RESULT

PWM Modulation	PWM Demodulation
 **Modulating Signal**  **Carrier Pulse Signal**  **PWM Modulated Signal**	 **PWM Modulated Signal**  **PWM Demodulated Signal**

EXPERIMENT NO. 3: Pulse Position Modulation (PPM)

AIM: To study PPM modulation and demodulation and observe the relevant waveforms.

THEORY:

Pulse width modulated signal is given to one more mono stable multivibrator to generate PPM signal. Operation is very simple, i.e., the width of each pulse of PWM signal varies according to the AF signal amplitude level at that instant. The second mono stable multivibrator generates one pulse for each PWM pulse input. But the mono stable triggers to the falling edge of the trigger signal (PWM- the falling edge is under the control of AF signal i.e. so the second mono stable generates on the level of the AF signal input).

During demodulation, in general, PPM is converted back to PWM and then gives to RC networks to demodulate. In this kit we are demodulating the PPM signal directly by RC networks and amplifier.

APPARATUS REQUIRED:

1. PWM Modulator
2. PPM Modulator
3. PPM Demodulator
4. Clock generator
5. AF signal generator (Variable amplitude)
6. ± 12 V @350 mA fixed dc power supply.
7. PPM Modulation & Demodulation kit. (Trinity Micro systems or any other kit).
8. Dual trace oscilloscope.
9. Variables RPS.

PROCEDURE:

1. Switch ON the experimental kit, shown in Fig. P4.1
2. Observe the clock generator output and AF signal outputs.
3. Connect clock generator output to the clock input point of PWM modulator and observe the same clock on channel 1 of a dual trace CRO.
4. Trigger the CRO with respect to CHI.
5. Apply a variable DC voltage of 8 to 12 volts from any external regulated power supply.
6. Observe the PWM output on CH2.
7. If we obtain the PWM output, its width varies according to the DC input voltage.
8. Now observer PPM output on CH2, its position changes according to the DC input voltage.
9. A variable amplitude AF signal is given to observe how the PWM signals are varying for AC modulating voltages.
10. For this observe AF signal on CH1 and PWM output on CH2.
11. Observe PPM on CH2.

Note: Generally we have to store PWM and PPM signals with respect to the modulating signals to get better results. Real time CRO also useful but triggering for AC modulating voltages is difficult.

12. During the demodulation, apply PWM and PPM signal to the input of demodulator and observe its output.

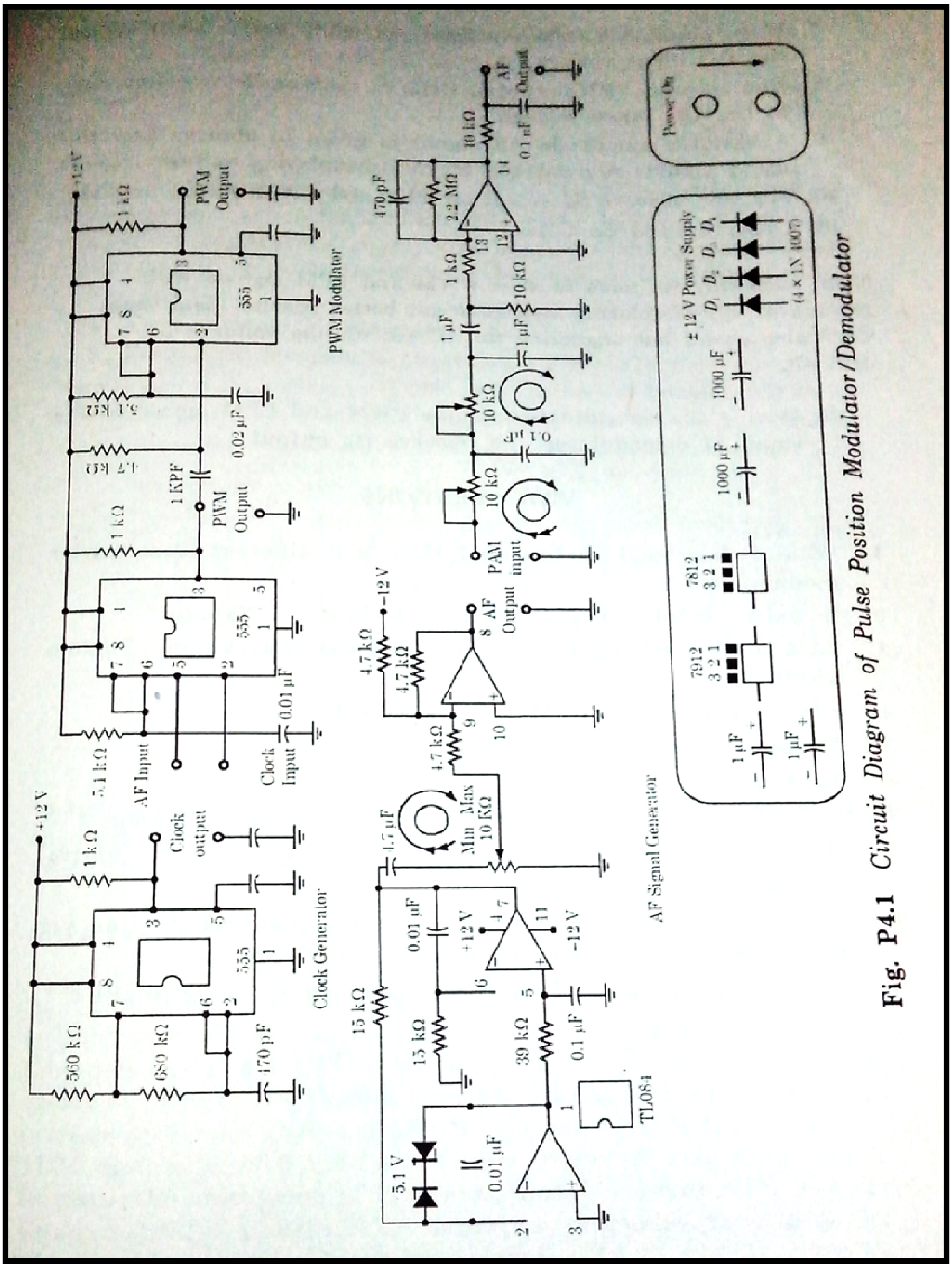


Fig. P4.1 *Circuit Diagram of Pulse Position Modulator/Demodulator*

EXPERIMENT NO. 4: Pulse Code Modulation and Demodulation

AIM: To study PCM modulation and demodulation and observing the waveforms.

THEORY:

Pulse Code Modulation (PCM) is different from Amplitude Modulation (AM) and Frequency Modulation (FM) because, those two are continuous forms of modulation. Pulse Code Modulation (PCM) is used to convert analog signals into binary form. In the absence of noise and distortion it is possible to completely recover continuous analog modulated signals. But in real time they suffer from transmission distortion and noise to an appreciable extent. In the PCM system, groups of pulses or codes are transmitted which represent binary number corresponding to Modulating Signal Voltage levels. Recovery of the transmitter information does not depend on the height, width, or energy content of the individual pulses, but only on their presence or absence. Since it is relatively easy to recover pulses under these conditions, even in the presence of large amounts of noise and distortion, PCM systems tend to be very immune to interference and noise. Regeneration of the pulse enroute is also relatively easy, resulting in system that produces excellent result for long-distance communication.

The decoding process reshapes the incoming pulses and eliminates most of the transmission noise. A serial to parallel circuit passes the bits in parallel groups to a digital to analog converter (D/A) for decoding. Thus decoded signal passes through a sample and hold amplifier which maintains the pulse level for the duration of the sampling period, recreating the staircase waveform approximation of the modulating signal. A low-pass filter may be used to reduce the quantization noise.

APPARATUS REQUIRED:

1. **ADC 0800(U1):** ADC 0800 is 8-bit monolithic Analog to Digital converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog switches. When the approximate tie point approximation technique where the unknown analog switches. When the appropriate tie point voltage matches the unknown voltage conversion is complete and the digitaloutputs containa 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE to permit bussing on common data lines.

   The ADC 0800 PD is specified over 55C to +125Cand the ADC 0800 PCD is specified over 0 C to 70 C.

FEATURES

- Low cost
- ±10V
- No Missing Codes
- Ratio meter conversion
- Tri-State outputs
- Fast (T_c = 50μs)
- Contains output latches

- TTL compatible
- Supply voltages (5 VDC and -12 VDC)
- Resolution (8-Bits)
- Linearity (±1 LSB)
- Conversion speed (40 Clock periods)
- Clock Range (50 to 800 kHz)

2. **74163(U8) Synchronous pre-settable binary counter:** The74161 and 74163 are high speed synchronous modulo-16 binarycounters. They are synchronously pre-settable for application in programmable dividers and have two types of count. Enable inputsplus a terminal count output for versatility in forming synchronous multistage counters. The 161 has an asynchronous multistage MasterReset input that overrides all other inputs and forces the outputsLOW. The 163 has a synchronous Reset input that overrides countingand parallel loading and allows the outputs to be simultaneously reseton the rising edge of the clock.

3. **74164(U3) (serial in parallel out shift register):** The 74164 is a high speed 8-bit serial in parallel out shift register. Serial data is entered through a 2 inputs and gate synchronous with the LOW-to-HIGH transition of the clock. The device features as asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the schottky diode clamped process to achieve high speeds.

4. **74165(U2) (8-Bit parallel-to-Serial Converter):** 74165 is an 8-bit parallel load or serial in register with complementary outputs available from the last stage. Parallel inputting occurs asynchronously when the parallel load (PL) input is LOW. With PL HIGH, serial shifting occurs on the rising edge of the clock, new data enters via the serial DATA (Ds) input. The 2-input outlock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

5. **8038 (U7) (Waveform Generator):** ICL 8038 waveform generator is monolithic integrated circuit capable of producing high accuracy since wave forms with a minimum of external components. The frequency can be selected externally from .001Hz to more than 300KHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage, the ICL 8038 is fabricated with advanced monolithic technology using schottky barrier diode and thin film resistors, and the output is stable over a wide range of temperature and supply variations as shown in fig. 2.

6. **74LS374 (U4) (OCTAL Transparent latch):** These 8-bit registers feature totem-pole TRI-STATE output designed specifically for driving highly capacitive or relatively low-impedance loads. The high impedance state and increased high logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus organised without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

The eight flip-flops of the LB374 are edge triggered D typeflipflops. On the positive transition of the clock, the Q output will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the output neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

7. **741 IC (U6) Operational Amplifier:** The mA 141 is a high performance monolithic operational Amplifier connected using the Fair child planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of ‘latch up' tendencies make the mA 741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance integrator, summing amplifier and general feedback applications.

   - No frequency compensation required
   - Short circuit protected
   - Offset voltage null capability
   - Large common mode and differential voltage ranges
   - Low power consumption
   - No latch up

8. **DAC 08(u5) (5-bit digital-to-analog converter):** DAC 0800 (TJ5) series are monolithic 8-bit high speed current output digital to analog converters (DAC) featuring typical setting times of 100ns. When used as 4 multiplying DAC, monolithic performance over a 40 to 1 reference current range is possible. The DAC 0800 series also features high compliance complementary current outputs to allow differential output voltages of 20Vp-p with simple resistor loads.

   The reference to full scale current matching of better than ± 1 LSB eliminates the need for full scale trims in most applications while the non linearity's of better than ±0.1% over temperature minimizes system error accumulations.

   The noise immune inputs of the DAC 0800 series will accept TL levels with the logic threshold pin, VLC potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially uncharged over the full ±4.5V to ± 18 V power supply range; power dissipation is only 33mW with the + 5 V supplied and is independent of the logic input states.

   The DAC 0800/DAC, 0808/DAC, 0800C/DAC, 0801C and DAC 0802C are a direct replacement for DAC 08, DAC 08A, DAC 08A, DAC 08E and DAC 08H, respectively.

PROCEDURE:

STEP-1: PCM MODULATION WITH D.C. INPUT

1. ‘Switch ON’ the experimental kit.
2. Observe the Basic clock generator output and sampling pulse output.
3. Connect the sampling pulse generator output to the CHI of the CRO and trigger CRO w.r.t. CH1 only.
4. Observe the output of the parallel to serial converter output (PCM data) on the CH2 of the CRO.
5. Make sure that CRO is triggered with the positive going edge of the sample pulse generator.
6. Now connect the variable DC output to the input of the PCM Modulator.
7. Adjust the Time/div Switch of the CRO such that two samples can be seen at a time on the screen.
8. Now vary the D.C. voltage from its minimum to the maximum.
9. At each step observe the parallel data displayed by the LEDsat the ADC output and compare the PCM output (Parallel to serial converter), which is the same ofthe ADC output but is in serial form.

Note: Between two samples, 8-bit serial data will be transmitted.

STEP-2: PCM DEMODULATION WITH DC INPUT

1. Connect the PCM output to the input of the PCM demodulator.
2. Output of the serial to parallel converter displayed by the LEDs is the same with is displayed by the ADC output LEDs.
3. Observe the output of the D/A converter.
4. Observe the output of the low pass filter and adjust the potentiometer such that the output D.C. voltage is equal to the D.C. input at the PCM modulator.

Note: Output D.C. output is 180° out of phase to the input because D to A converter introduces 180° out of phase and low pass filter also introduces some delay, because in all practical PCM systems negative logic is used to reduce the noise in transmission.

STEP-3: PCM MODULATION WITH AC INPUT

1. Now remove DC and connect the AC voltage to the input of the PCM modulator.
2. Observe the PCM output with follows the sequence of the AC input.
3. Here one has to make sure that like DC input, we cannot see the stable digital output at the PCM modulator output. Because this is a dynamic process and with the AC input, we cannot send same PCM data between successive samples. But in the DC input case at any sample same data will transmitted because at any sample same voltage is available not like AC input.

RESULT

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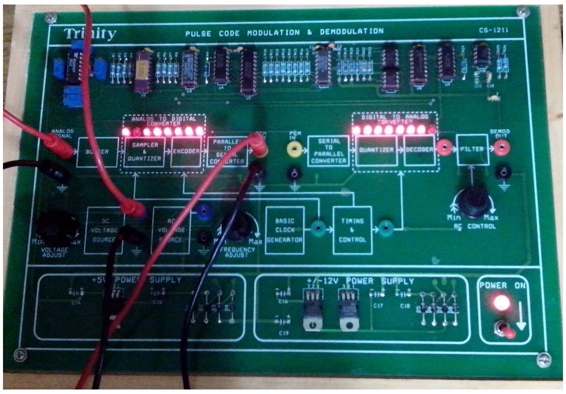
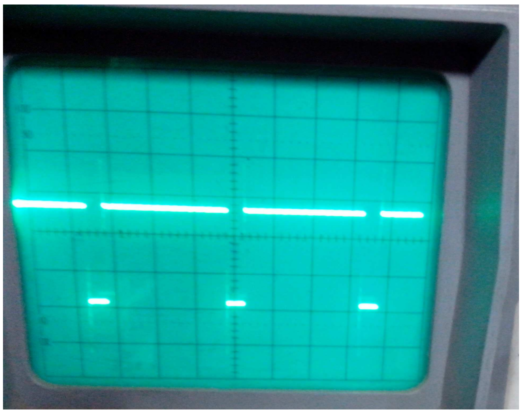
<tr><th>PCM Modulation with DC Input</th><th>PCM Modulation with AC Input</th></tr>
<tr>
<td>




<u>PCM Output Signal</u>
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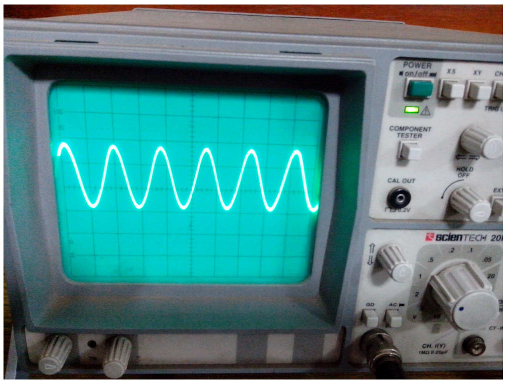
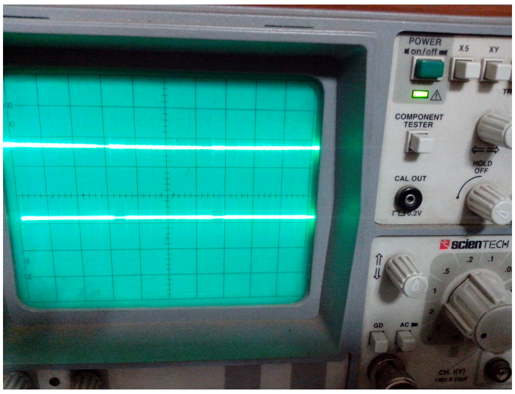
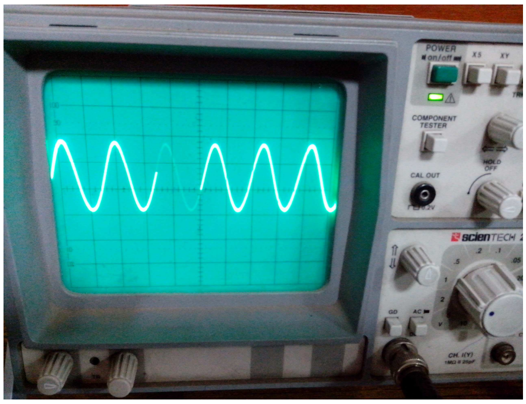


<u>PCM Modulating Signal</u>



<u>PCM Output Signal</u>



<u>PCM Demodulated Signal</u>
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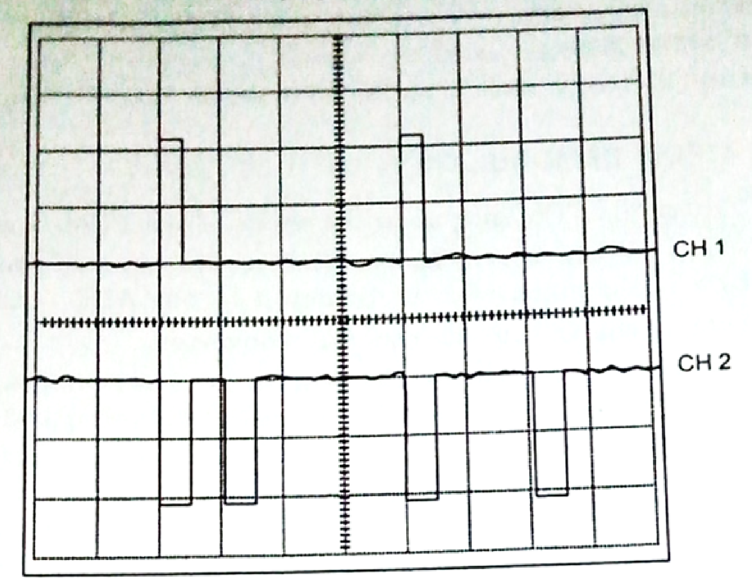
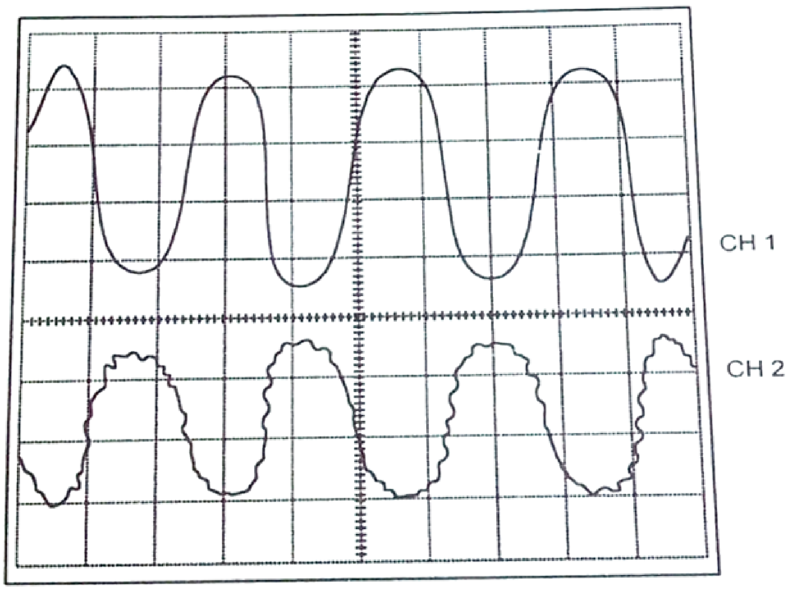
Sampling Frequency



PCM Output for sine wave I/P

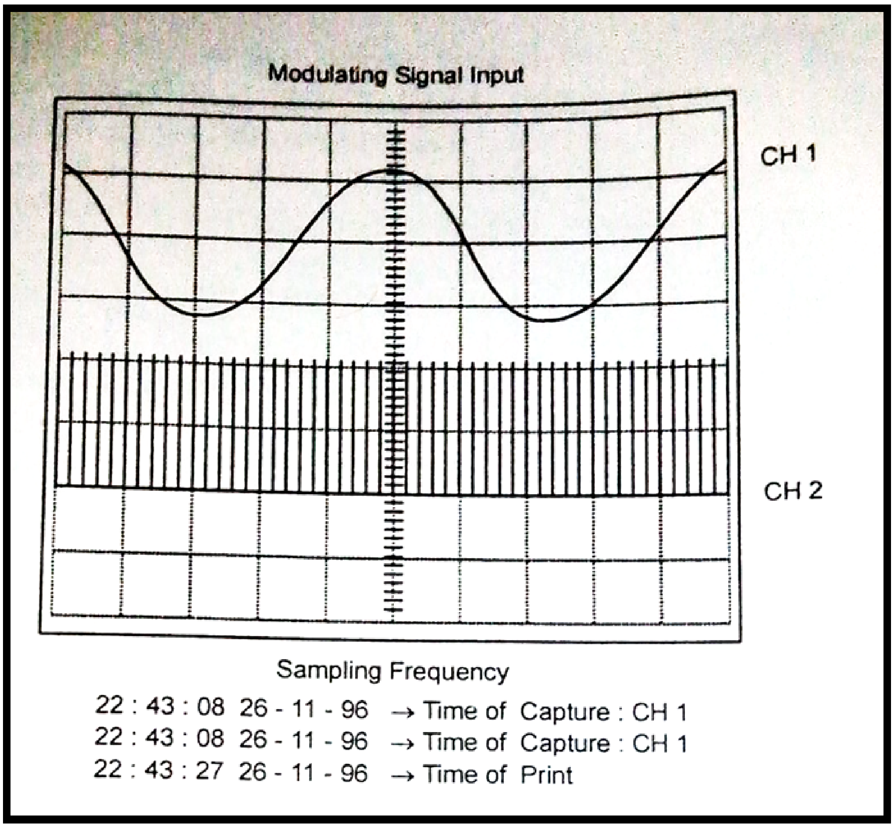
22 : 13 : 36 26 – 11 – 96 → Time of capture : CH 1
22 : 13 : 36 26 – 11 – 96 → Time of capture : CH 2
22 : 25 : 11 26 – 11 – 96 → Time of print

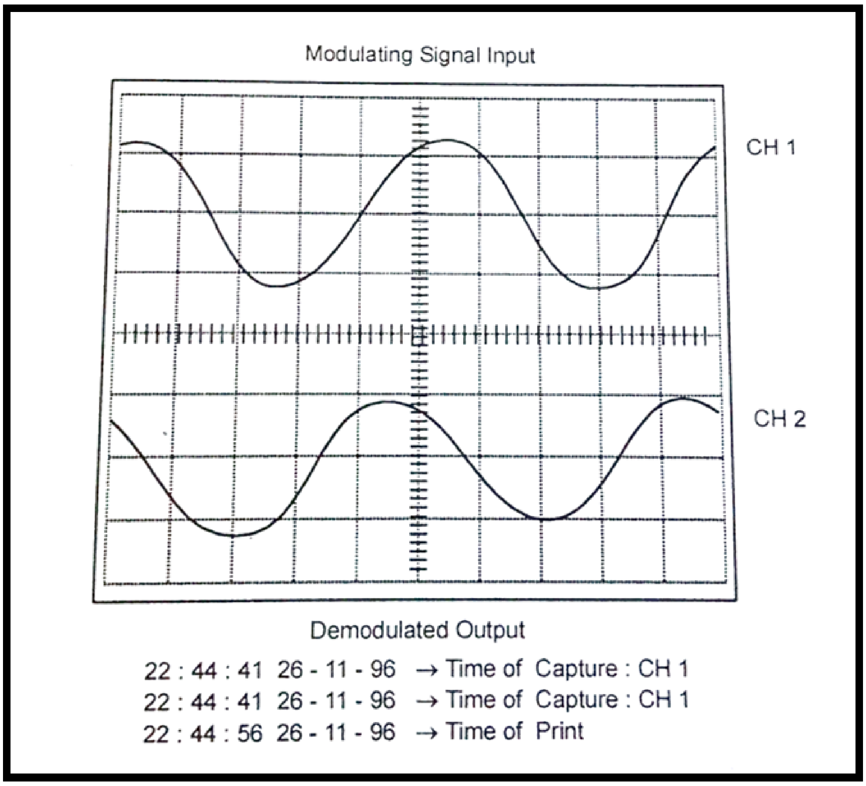
Input lating signal

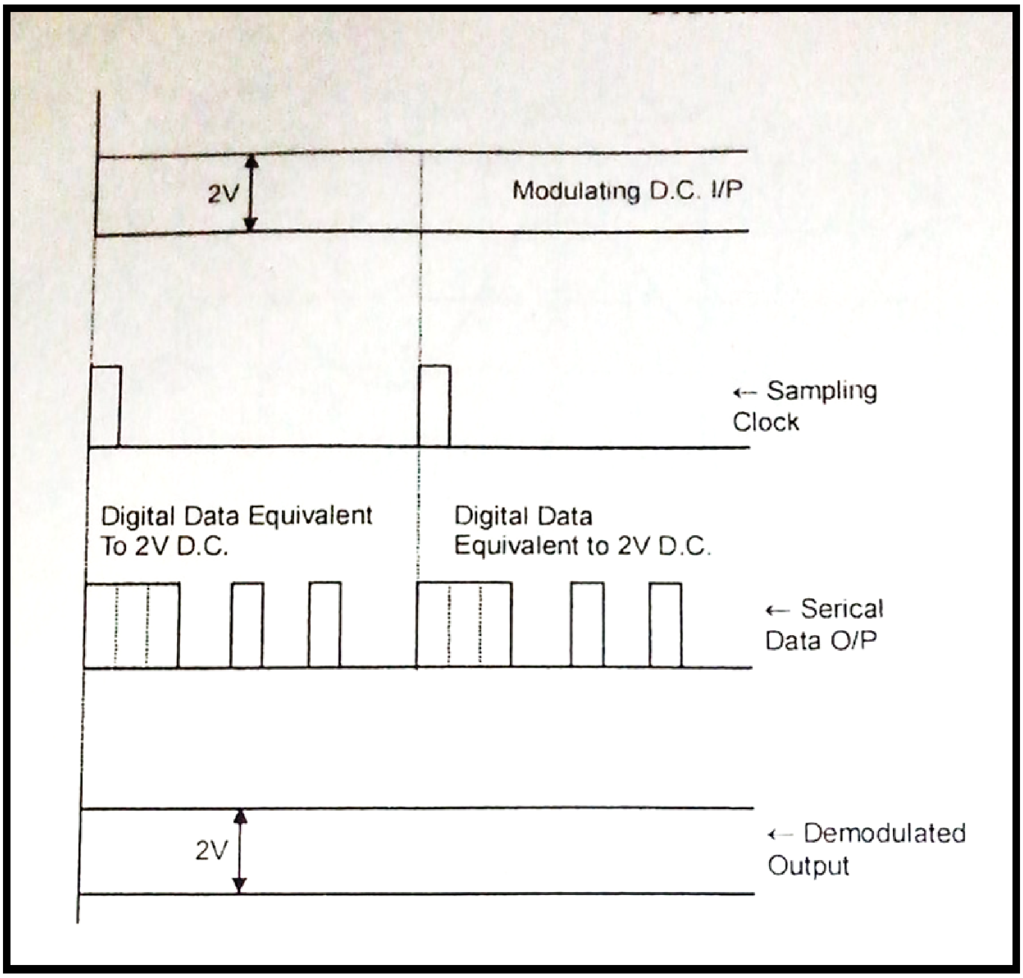


D + TO – A Converter Cutput

22 : 30 : 40 26 – 11 – 96 → Time of capture : CH 1
22 : 30 : 40 26 – 11 – 96 → Time of capture : CH 2


Modulating Signal Input
CH 1
CH 2
Sampling Frequency
22 : 43 : 08 26 - 11 - 96 → Time of Capture : CH 1
22 : 43 : 08 26 - 11 - 96 → Time of Capture : CH 1
22 : 43 : 27 26 - 11 - 96 → Time of Print


Modulating Signal Input
CH 1
CH 2
Demodulated Output
22 : 44 : 41 26 - 11 - 96 → Time of Capture : CH 1
22 : 44 : 41 26 - 11 - 96 → Time of Capture : CH 1
22 : 44 : 56 26 - 11 - 96 → Time of Print



2V
Modulating D.C. I/P
← Sampling
Clock
Digital Data Equivalent
To 2V D.C.
Digital Data
Equivalent to 2V D.C.
← Serical
Data O/P
2V
← Demodulated
Output

EXPERIMENT NO. 5: Amplitude Shift Keying

AIM: To study Amplitude Shift Keying modulation and demodulation.

APPARATUS:

SI. No.	Apparatus	Range	Quantity
1.	IC 741		1
2.	Transistor SI 100		1
3.	Diode OA79		1
4.	Resistors	100 kΩ 22 kΩ 2.2 kΩ	Each 1
5.	POT	10 kΩ	1
6.	Capacitor	0.01 uF	1

PROCEDURE:

1. Connections are made as shown in the circuit diagrams shown in Fig. P9.1.
2. Apply a square wave modulating signal of 500 Hz (1000 bits/ sec) and 0V peak to peak amplitude.
3. Apply a sine wave carrier signal of 50 kHz of 5V peak-to-peak amplitude.
4. Observe ASK waveform at point A.
5. Demodulate the ASK signal using the envelope detector.
   {The error in the demodulated wave form can be minimized by adjusting the V_{ref} using 10 KΩ POT}
6. To find minimum frequency of carrier signal for proper detection.
   i. After step No. 5, start reducing the freq2uency of the sine wave carrier signal from 50 kHz gradually.
   ii. At a particular frequency of the carrier signal, the demodulated signal does not tally with the modulating square wave signal.

The minimum frequency of the carrier sine wave signal is that frequency, when demodulated signal tally with the modulating signal for the first time.

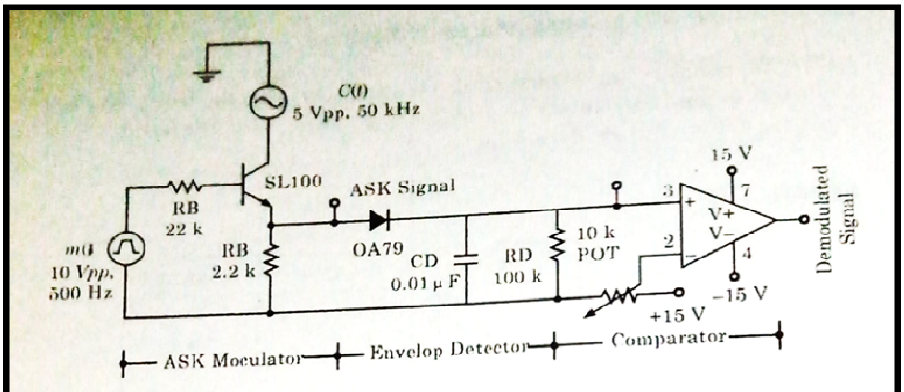


Fig. P9.1

Design:

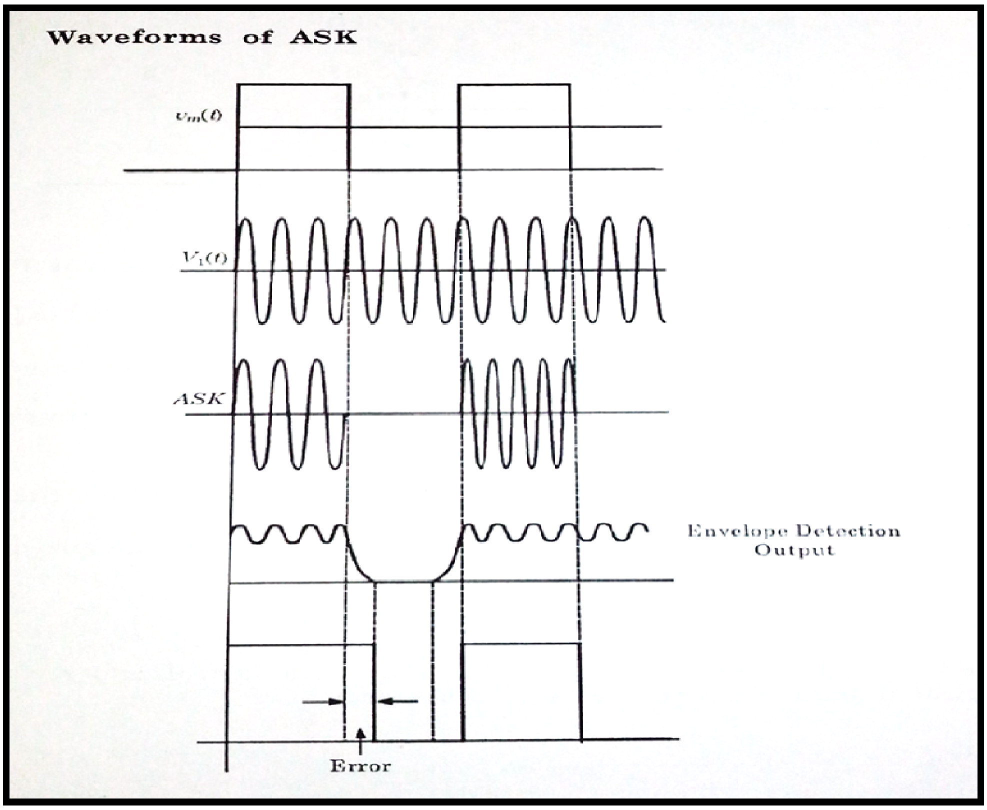
Specification: $V_C = 5V_{pp}$, $V_m = 10V_{pp}$, $f_m = 500Hz$ and $f_c = 50KHz$

Assume:
$h_{fe} = 30$
V_{BE} sat = 0.7V
V_{CE} sat = 0.3V
$I_C = 1mA$, $I_E = I_C$

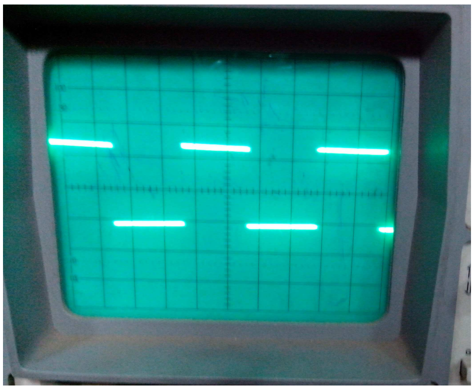
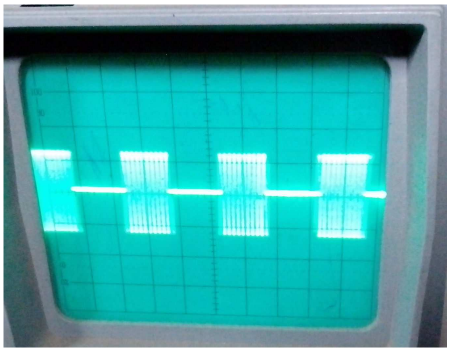
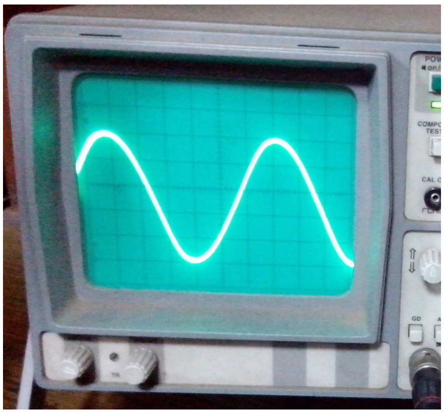
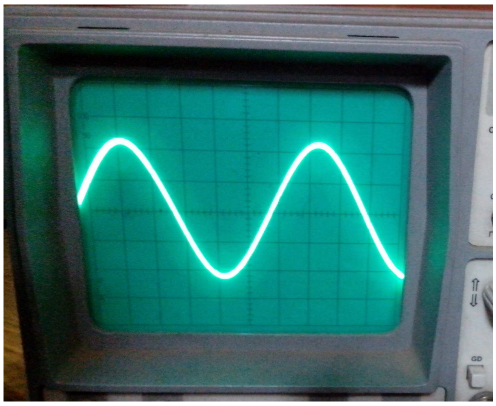
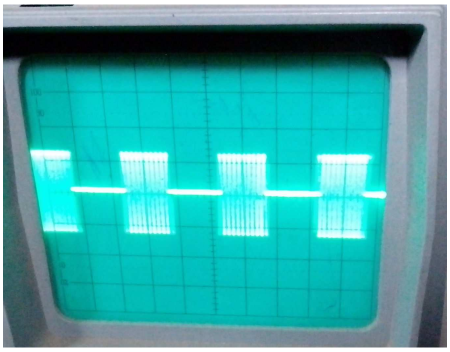
Biasing:
$V_{cpeak} = V_{CE\,sat} + I_E R_E$
1.5.1 $= 0.3 + 1mA\,R_E$, therefore, $R_E = 2.2K\Omega$
$V_{mpeak} = R_B I_B + V_{BE\,sat} + I_E R_E$
$5 = R_B I_B + 0.7 + 2.2$
Then $R_{Bmax} = 63K\Omega$, choose $R_B = 22K\Omega$

Envelope Detector:
$1/f_m > R_D C_D > 1/fc$
$5ms > R_D C_D > 20\mu s$
Let $R_D C_D = 500/f_c = 1ms$
Assume $C_D = 0.01\mu F$, then $R_D = 100K\Omega$ choose $R_D = 100K\Omega$
$R_D = 100K\Omega$, $R_B = 22K\Omega$, $R_E = 2.2K\Omega$, $C_D = 0.01\mu F$

Check Points:
1. Check the OP AMP. Transistor and Diodes.
2. V_{ref}.



RESULT

ASK Modulation	ASK Demodulation
 **Modulating Signal**	 **ASK Modulated Signal**
 **Carrier Signal**	 **ASK Demodulated Signal**
 **ASK Modulated Signal**	

EXPERIMENT NO. 6: Phase Shift Keying

AIM: To study Phase Shift Keying Modulation and Demodulation.

APPRATUS:

SI. No.	Apparatus	Range	Quantity
1.	IC 1548		2
2.	Transistor SL 100		2
3.	Diode OA79		1
4.	Resistors	100 kΩ, 22KΩ 2.2kΩ, 10kΩ	1,2, 2,8
5.	POT	10 kΩ	2
6.	Capacitor	0.01 uF 0.1 uF	1 2

PROCEDURE:

1. Connections are made as shown in the circuit diagram, as in Fig. P11.1.
2. Apply a square wave modulating signal of 500 Hz 1 kHz 100 kHz bits a 5 V peak to peak amplitude.
3. Apply a sine wave carrier signal of 50 kHz of 5V peak to peak amplitude.
4. Observe BPSK wave form at point A.
5. Demodulate, the BPSK signal using the coherent detection (Adder + Envelope Detector).
   {The error in the demodulated wave form can be minimized by adjusting the V_{ref} using 10 kΩ POT}

Design

Specification:

$V_C = 5V_{pp}$, $V_m = 10V_{pp}$, $f_m = 500Hz$ and $f_c = 50KHz$

Assume:

$h_{fe} = 30$

$V_{BE}\,sat = 0.7V$

$V_{CE}\,sat = 0.3V$

$I_C = 1mA$, $I_E = I_C$

Biasing:

$V_{c\,peak} = V_{CE\,sat} + I_E R_E$

$1.5 = 0.3 + 1mA\ R_E$, therefore, $R_E = 2.2K\Omega$

$V_{m\,peak} = R_B I_B + V_{BE\,sat} + I_E R_E$

$5 = R_B I_B + 0.7 + 2.2$

Then $R_{Bmax} = 63K\Omega$, choose $R_B = 22K\Omega$

Envelope Detector:

$1/f_m > R_D C_D > 1/fc$

$5ms > R_D C_D > 20\mu s$

Let $R_D C_D = 500/f_c = 1ms$

Assume $C_D = 0.01\mu F$, then $R_D = 100K\Omega$ choose $R_D = 100K\Omega$

$R_D = 100K\Omega$, $R_{B1} = R_{B2} = 22K\Omega$, $R_{E1} = R_{E2} = 2.2K\Omega$, $C_D = 0.01\mu F$, $C_C = 0.01\mu F$

CHECK POINT

1. Check the OP AMP, Transistors and Diodes.
2. V_{ref} should be between the voltage swings of envelope detector output at point A.

Design

Specification: $V_C = 5V_{pp}$, $V_m = 10V_{pp}$, $f_m = 500Hz$ and $f_{c1} = 50KHz$, $f_{c2} = 50KHz$

Assume: $h_{fe} = 30$, V_{BE} sat $= 0.7V$, V_{CE} sat $= 0.3V$, $I_C = 1mA$, $I_E = I_C$

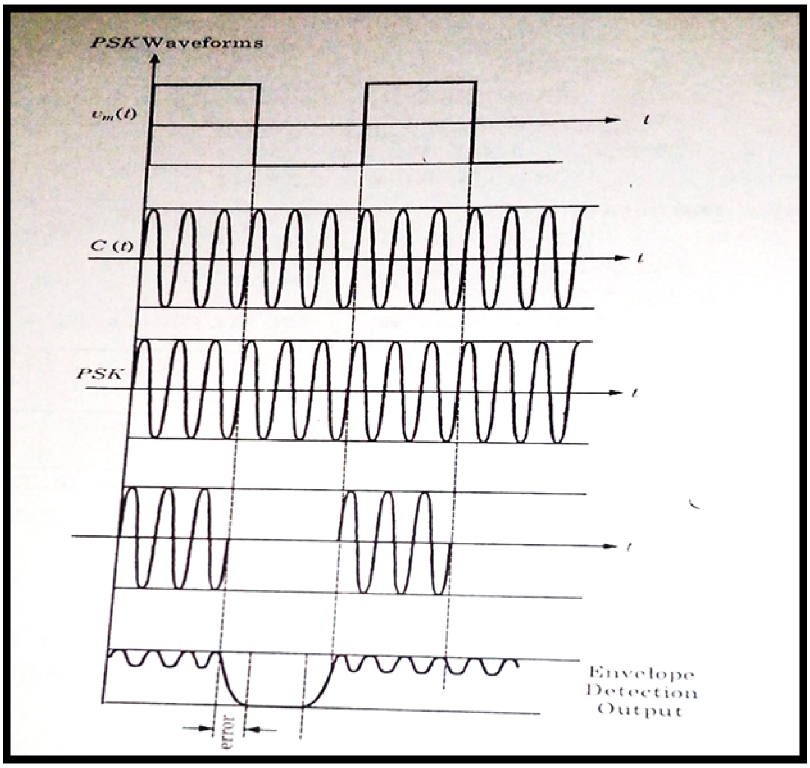
Biasing: $V_{c\,peak} = V_{CE\,sat} + I_E R_E$

$2.5 = 0.3 + 1mA\ R_E$, therefore, $R_E = 2.2K\Omega$

$V_{m\,peak} = R_B I_B + V_{BE\,sat} + I_E R_E$

$5 = R_B I_B + 0.7 + 2.2$

Then $R_{B\,max} = 63K\Omega$, choose $R_B = 22K\Omega$



Envelope Detector:

$1/f_m > R_D C_D > 1/fc$

$5ms > R_D C_D > 20\mu s$

Let $R_D C_D = 500/f_c = 1ms$

Assume $C_D = 0.01\mu F$, then $R_D = 100K\Omega$ choose $R_D = 100K\Omega$

$R_{B1} = R_{B2} = 22K\Omega$, $R_{E1} = R_{E2} = 2.2K\Omega$, $C_D = 0.01\mu F$, $C_C = 0.01\mu F$

CHECK POINT

1. Check the OP AMP, Transistors and Diodes.
2. V_{ref} should be between the voltage swings of envelope detector output at point A.

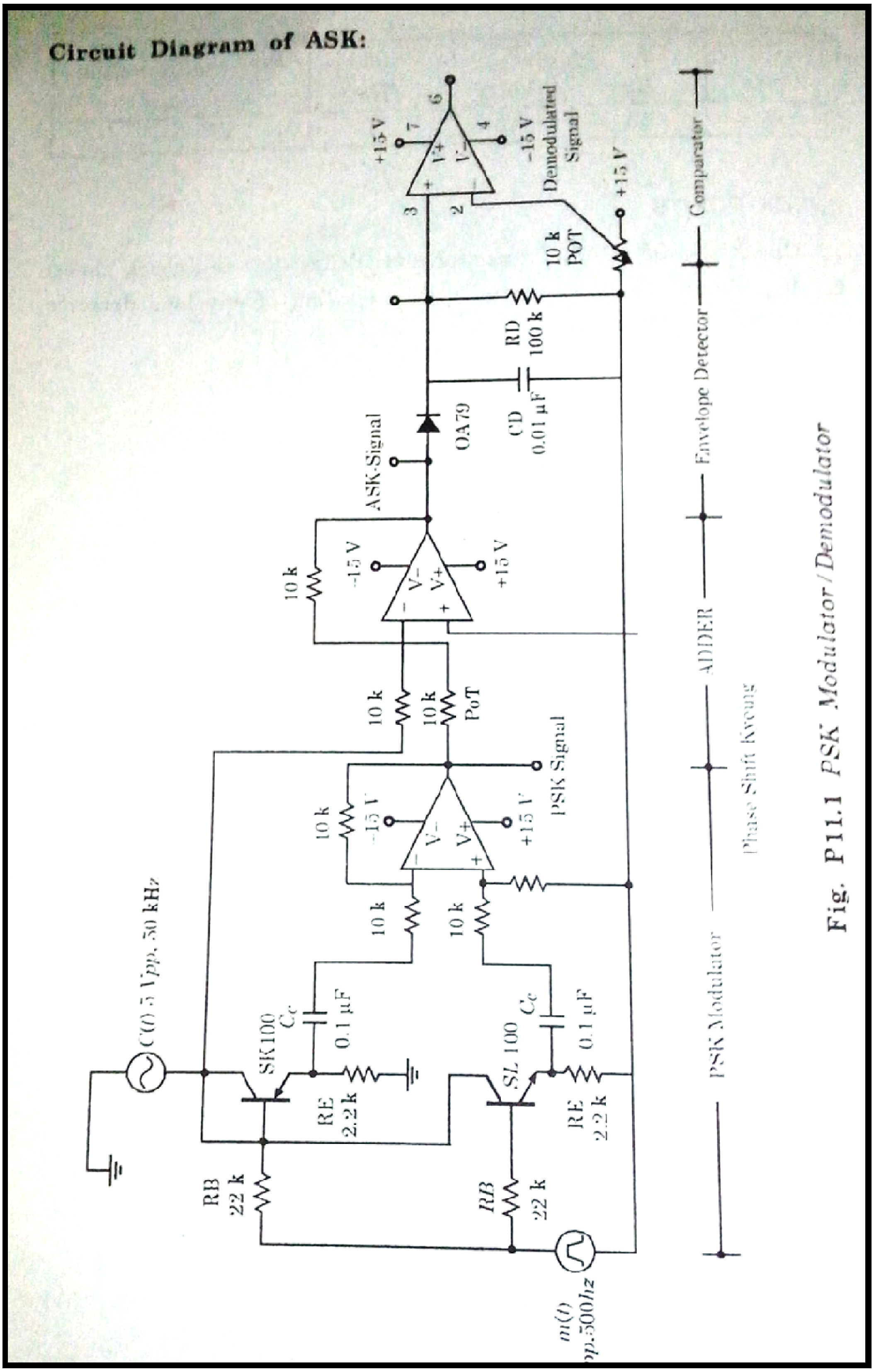
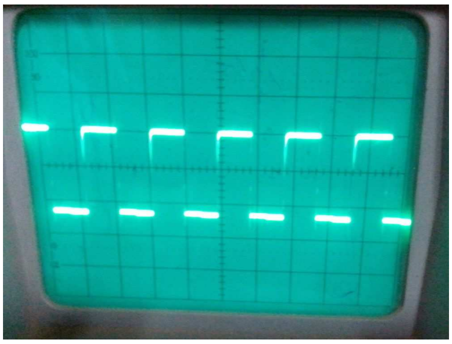
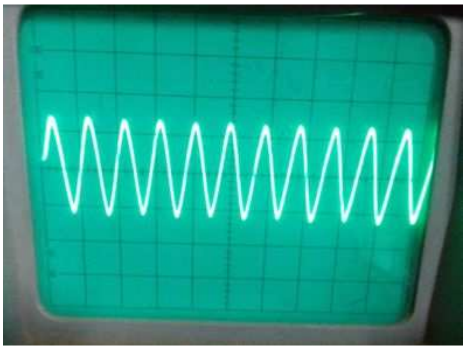
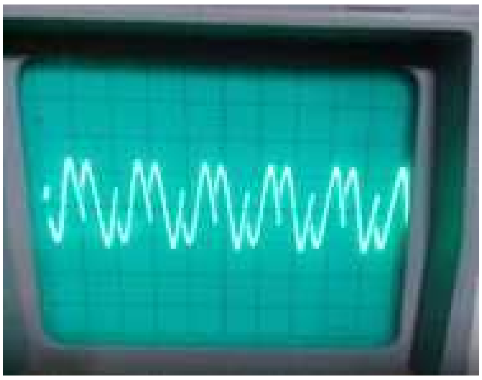
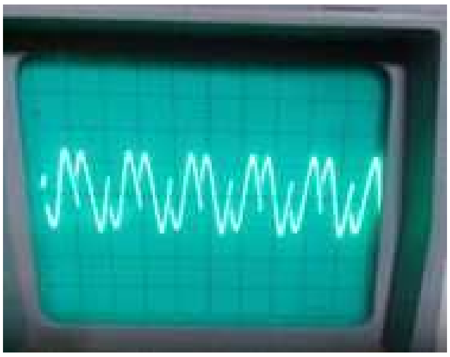
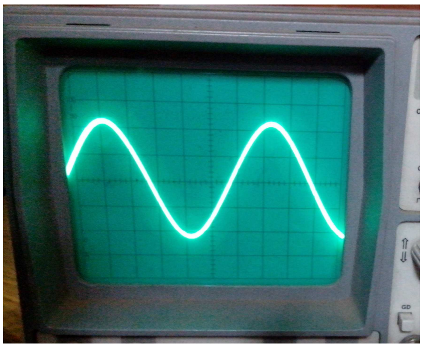


Fig. P11.1 PSK Modulator/Demodulator

RESULT

PSK Modulation	PSK Demodulation
 **Modulating Signal**  **Carrier Signal**  **PSK Modulated Signal**	 **PSK Modulated Signal**  **PSK Demodulated Signal**