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RTOS Based Dynamic Scheduler in Power Quality Applications

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Abstract — In this modern world, there has been a great deal of focus on power quality management in industrial applications. The embedded software application requires performing a task which is efficiently achieved by dividing the global task into many smaller subtasks. Each subtask apart from executing its own task, services a part of the global task.RTX is the RTOS that powers more than one billion real-time systems across the globe, from small consumer products to commercial airliners. When the consequences for failure are expensive or worse, life threatening, RTX RTOS is the only choice. The concept of dynamic assignment of priorities to interrupts is used which reduces the time delay for a lower priority task under some circumstances becomes a higher priority task. Slicing of interrupt timings improves the performance. The highest priority task is serviced more number of times than the lesser time period. Voltage sensor and current sensor are interfaced to microcontroller, the capacitor bank is powered and the power factor produced from the location is gathered and depending on the particular criteria, The capacitor banks are switched ON to a controllable and variable amount of reactive power according to the requirements of load such that the power factor is improved and the uninterrupted working is done.

***Keywords*-ARM controller, Switched capacitor bank, SPI protocol, Round robin, Power factor correction, Task scheduling.**

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I. Introduction

Interactive Power management tool helps track power usage, identify wastage and benchmark energy consumption per unit of output against industry norms.The main objective is to increases the productivity of the existing system and efficient power management thereby enhancing the flexibility of the system. The goal of any load-management program is to maintain, as nearly as possible, a constant level of load, thereby allowing the system load factor to approach 100%. The important benefits of load management are reduction in maximum demand, reduction in power loss, better equipment utilization and saving through reduced maximum demandcharges. It is a powerful superset of mere Energy Recording is excellent for overall automation of production systems andthat difference is vital in bringing energy centers where line capacities have energy constraints.

II. System Overview

The basic characteristics of the system

1) Easiness of implementation.
2) Low-cost implementation.
3) Easiness of implementation ofredundant routines (security) and portability/versatility.

Voltage sensor and current sensor reading are given to SPI protocol IC it is interfaced to microcontroller. The measured reading is transmitted through the Zigbee given in the fig 1.

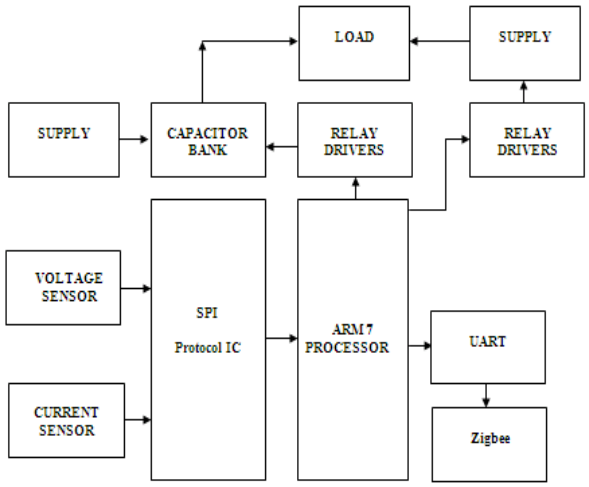


Fig 1. Block diagram of transmitter

. TheARM controller to monitor& controlling the corresponding parameters, if there is any variation or unbalanced condition of load, ARM will switch on the capacitor through the relay drivers.The capacitor banks balance the load. The capacitor bank ispowered and the power factor which produces from the industry is gathered first and depending upon that one. The capacitorbanks are used to power the power plant to the uninterrupted working of the industries. the harmonics are reduced.

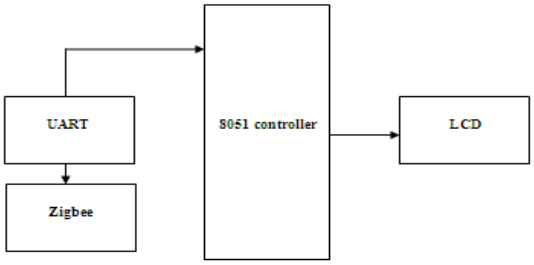


Fig 2. Block diagram of receiver

Then the received by another controller and it is displayed through LCD. Given in the Fig 2.

III. Electroletic Capacitor Bank

Our system is required to switch capacitor bank to keep the power factor of the grid within the limits set by the user using the human machine interface(HMI).the capacitor bank is switched ON/OFF using the relay drivers. The RTOS scheduling algorithm is based on static reactive power (Q) compensation of PFC controllers. The dynamic Scheduler algorithm to scheduling the parameters like power factor, Voltage stability, current and frequency for the CS5467 SPI protocol. Power factor correction is a technique of counteracting the undesirable effects of electric load that create a power factor that isless than one which can improve the stability and efficiency of the load.

Power factor = Actual power/apparent power

In AC circuits P average = VI COSΦ

Where Φ is the phase angle between the voltages

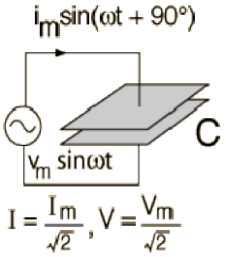
A. Capacitor Selection

Static power factor correction must neutralize no more than 80% of the magnetizing current of motor. If the correction which can result in equipment failure with several damage to the motor and capacitor. Unfortunately, the magnetizing current of induction motor varies considerably between different motor design. The magnetizing current is almost always higher than 20%of the rated full load current of the motor.

B. Phasor Diagram of Capacitor

The capacitor with AC supplies Fig 3. and its phasor diagram is shown in the Fig 4.

This shows the phase angle between current and voltage. In case of capacitor voltage lags current by 90o. The voltage across a capacitor lags the current because the current must flow to build up charge and voltage is proportional to the charge which is build up on the capacitorplates.



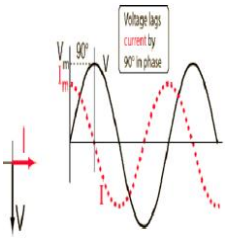


Fig 3.Capacitor **Fig 4.phasor diagram& phase angle**

IV. Power Factor Correction

The power factor of an AC electrical power system is defined as the ratio of the real power flowing to the load to the apparent power in the circuit, and is a dimensionless number between 0 and 1. Real power is the capacity of the circuit forperforming work in a particular time. Apparent power is the product of the current and voltage of the circuit. Due to energystored in the load and returned to the source, or due to a non-linear load that distorts the wave shape of the current drawnfrom the source, the apparent power will be greater than the real power. Instead of using a set of switched capacitors, anunloaded synchronous motor can supply reactive power. The reactive power drawn by the synchronous motor is a function of its field excitation. This is referred to as a synchronous condenser. It is started and connected to the electrical network. Itoperates at a leading power factor and puts vary onto the network as required to support a system's voltage or to maintain the system power factor at a specified level. In an electric power system, aload with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. The higher currents increase the energy lost in the distribution system, and require larger wires and other equipment. Because of the costs of larger equipment and wasted energy, electrical utilities will usually charge a higher cost to industrial or commercial customers where there is a low power factor.Linear loads with low power factorsuch as induction motorscan be corrected with a passive network of capacitors.

A. Power Factor Correction of Linear Loads

A high power factor is generally desirable in a transmission system to reduce transmission losses and improve voltage regulation at the load.

It is often desirable to adjust the power factor of a system to near 1.0. When reactive elements supply or absorb reactive power near the load, the apparent power is reduced. Power factor correction may be applied by an electrical power transmission utility to improve the stability and efficiency of the transmission network.

Individual electrical customers who are charged by their utility for low power factor may install correction equipment

to reduce those costs. Power factor correction brings the power factor of an AC power circuit closer to 1 by supplying reactive power of opposite sign, adding capacitors or inductors that act to cancel the inductive or capacitive effects of the load, respectively. For example, the inductive effect of motor loads may be offset by locally connected capacitors. If a load had a capacitive value, inductors (also known as reactors in this context) are connected to correct the power factor. In the electricity industry, inductors are said to consume reactive power and capacitors are said to supply it, even though the energy is just moving back and forth on each AC cycle. The reactive elements can create voltage fluctuations and harmonic noise when switched on or off. They will supply or sink reactive power regardless of whether there is a corresponding load operating nearby, increasing the systems no-load losses. In the worst case, reactive elements can interact with the system and with each other to create resonant conditions, resulting insystem instability and severe overvoltage fluctuations. As such, reactive elements cannot simply be applied without engineering analysis. An automatic power factor correction unit consists of a number of capacitors that are switched by means of contactors. These contactors are controlled by a regulator that measures power factor in an electrical network. Depending on the load and power factor of the network, the power factor controller will switch the necessary blocks of capacitors in steps to make sure the power factor stays above a selected value. Instead of using a set of switched capacitors, an unloaded synchronous motor can supply reactive power. The reactive power drawn by the synchronous motor is a function of its field excitation.

V. Four Channel Power To Energy Ic

The CS5467 is an integrated power measurement device which combines four ΔΣ analog to digital converters, power calculationengine, energy to frequency converter anda serial interface on a single chip. The CS5467 analog inputs are structured withtwo current channels and two voltage channels, and optimized to simplify interfacing to sensing elements. The voltage sensingelements introduces a voltage waveform on the voltage channel input VIN+, VIN-, which is subjected to a gain of 10x. A secondorder delta sigma modulator samples the amplified signal for digitization.

The current sensing elements introduces a currentwaveform on the current channel input IIN+,IIN-, which is subjected to a gain of 10x. A fourth order delta sigma modulatorsamples the amplified signal for digitization. The over sampling provides a wide dynamic range and simplified anti aliasfilter design.

VI. ARM7 LPC2148

The 32-bit ARM7 TDMI-S microcontroller in a tiny LQFP64 package. 40 kb of on-chip static RAM and 512 kb of on-chip flash memory.128-bit wide interface accelerator enables high-speed 60 MHz operation.In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot loader software. Single flash sector or full chiperase in 400 ms and programming of 256 bytes in 1 ms .Embedded ICE RT and Embedded Trace interfaces offer real-time debugging with the on-chip Real Monitor software and high-speed tracing of instruction execution.USB 2.0 Full-speed compliant devicecontroller with 2 kb of endpoint RAM. In addition, the LPC21/48 provides 8 kb of on-chip RAM accessible to USB by DMA. One ortwo (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of 6/14 analog inputs, with conversion times as low as 2.44 μsper channel. Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only).Two 8-bit timers/external eventcounters (with four capture and four Compare channels each), PWM unit (six outputs) and watchdog. Low power Real-Time Clock(RTC) with independent power and 8 kHz clock input. Multiple serial interfaces including two UARTs (16C550), two Fast I2C-bus(400 Kbit/s), SPI and SSP with buffering and variable data length capabilities.60MHz maximum CPU clock available fromprogrammable on-chip PLL with settling time of 100 μs. On-chip integrated oscillator operates with an external crystal from 1MHz to 25 MHz.

VII. Features Of RTOS Kernel

One chooses a Real time operating system (RTOS) when certain operations are critical and must be completed correctly andwithin a certain amount of time. The physical parameters like voltage, current, Power factor and frequency are monitored bythe use of multitasking RTX kernel RTOS[9].Traditionally Developers of small embedded applications have to write virtuallyall the code that runs on the microcontroller. Typically this is in the form of interrupt handler with a main backgroundscheduling loop.The Keil RTX is a royalty-free, deterministic Real-Time Operating System designed for microcontrollers basedon ARM7™TDMI, ARM9™, and Cortex™-M CPU cores. It runs quickly and takes the minimum of MCU resources with a memory footprintas small as 5KB (ROM).

The RTX kernel can be used for creating applications that perform multiple functions or taskssimultaneously. It allows you to create programs that simultaneously perform multiple functions and helps to createapplications which are better structured and more easily maintained. While it is certainlypossible to create real-timeapplications without an RTOS (by executing one or more tasks in a loop), there are

numerous scheduling, maintenance, andtiming issues that can be solved better with an RTOS.

For example, an RTOS enables flexible scheduling of system resourceslike CPU and memory, and offers methods to communicate between tasks. An advanced RTOS, such as the Keil RTX, deliversserious benefits like, task scheduling, multitasking, inter task communication, shorter ISR system management.The Fig 5. RTX kernel provides basic functionality to start and stop concurrent tasks (processes). RTX consists of ascheduler that supports round-robin, pre-emptive, and cooperative multitasking of program tasks, as well as time and memorymanagement services. Additional RTOS services include time and memory management and interrupt support.

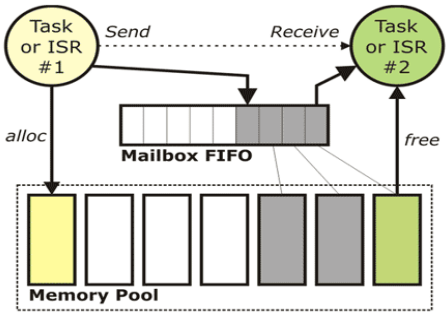


Fig 5. RTX kernel

The RTX kernel provides several ways for inter-process communication. These are:Event flags, mailbox, mutexes, semaphores.

A. Round-Robin Scheduling Algorithm

It is one of the oldest, simplest, and fairest and most widely used scheduling algorithms, designed especially fortime-sharing systems. A small unit of time, called time slices or quantum is defined. All runnable processes are kept in acircular queue. The CPU scheduler goes around this queue, allocating the CPU to each process for a time interval of onequantum. New processes are added to the tail of the queue .The CPU scheduler picks the first process from the queue, sets atimer to interrupt after one quantum, and dispatches the process. If the process is still running at the end of the quantum,the CPU is preempted and the process is added to the tail of the queue. If the process finishes before the end of thequantum, the process itself releases the CPU voluntarily. In either case, the CPU scheduler assigns the CPU to the nextprocess in the ready queue. Every time a process is granted the CPU, a context switch occurs, which adds overhead totheprocess execution time.

If there are n processes in the ready queue and the time slice is q, then each process ideallywould get 1/n of the CPU time in chunks of q time units, and each process would wait no longer than nq time units until itsnext quantum. A more realistic formula would be n(q+o), where o is the context switch overhead. So, for practical purposes,it is desirable that the context switch be negligible compared to the time slice.

The performance of the Round-Robin algorithm depends heavily on the size of the quantum.

If the quantumis very large, theRound-Robin algorithm is similar to theFirst-Come, First-Served algorithm as shown in Fig 6. If the quantum is very small,the Round-Robin approach is called processor sharing.

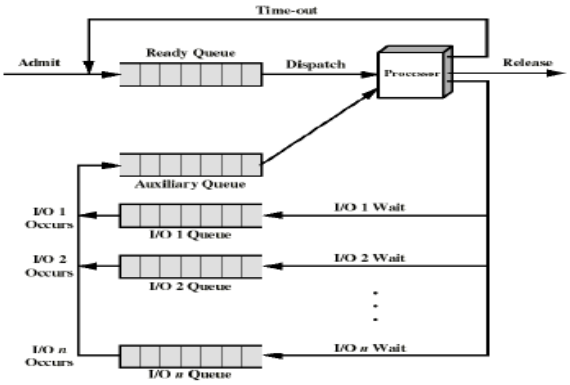


Fig 6. Virtual Round Robin Queue

B. Data Packet Scheduling

In best-effort packet switching and other statistical multiplexing, round-robin scheduling can be used as an alternative to first-come first-served queuing.A multiplexer, switch, or router that provides round-robin scheduling has a separate queue for every data flow, where a data flow may be identified by its source and destination address. The algorithm lets every active data flow that has data packets in the queue to take turns in transferring packets on a shared channel in a periodically repeated order. The scheduling is work-conserving, meaning that if one flow is out of packets, the next data flow will take its place. Hence, the scheduling tries to prevent link resources from going unused.Round-robin scheduling results in max-min fairness if the data packets are equally sized, since the data flow that has waited the longest time is given scheduling priority. It may not be desirable if the size of the data packets varies widely from one job to another. A user that produces large packets would be favored over other users. In that case fair queuing would be preferable.If guaranteed or differentiated quality of service is offered, and not only best-effort communication, deficitround-robin (DRR) scheduling,weighted round-robin (WRR) scheduling, or weighted fair queuing (WFQ) may be considered.

In multiple-access networks, where several terminals are connected to a shared physical medium, round-robin scheduling may be provided by token passing channel access schemes such as token ring, or by polling or resource reservation from a central control station.In a centralized wireless packet radio network, where many stations share one frequency channel, a scheduling algorithm in a central base

station may reserve time slots for the mobile stations in a round-robin fashion and provide fairness. However, if link adaptation is used, it will take a much longer time to transmit a certain amount of data to "expensive" users than to others since the channel conditions differ.

It would be moreefficient to wait with the transmission until the channel conditions are improved, or at least to give scheduling priority to less expensive users. Round-robin scheduling does not utilize this. Higher throughput and system spectrum efficiency may be achieved by channel-dependent scheduling, for example a proportionally fair algorithm, or maximum throughput scheduling. Note that the latter is characterized by undesirable scheduling starvation.

VIII. Slicing Of Interrupt Timings By The Priority Manager

Fig7. Interrupt timer flag switching in case of slicing by the priority manager job that priority manager can do is significantly slicing the timings for the interrupts, which is chosen according to the configuration of UART/I2C. This way, the highest priority task is serviced more number of times and with lesser time period. Hence it need not wait for the slack time of other previously higher priority interrupts. Consider the case at 250ms Since I2C is higher in priority but does not require servicing at this moment; the highest priority is dynamically assigned to UART. This implies, now instead of I2C, UART will get executed first processing 1 byte, but it again has to wait 50ms to process the next byte. In order to speed up the process, the interrupt timing for UART is significantly slashed.The revised timing (after slicing) for the interrupt which is to be given highest priority (either I2C or UART) is very critical. If the timing is kept lesser than the minimum time required to service the interrupt once, then the integrity of data is lost and if the timing is much more than what is required, the concept of slicing becomes less effective. TheUART is configured for 115200 baud, which implies to send a byte (8 bits) at a time plus a cushion of let's say 2 bits the time taken to perform a transmit/receive task comfortably, will be as shown in the following equation…

$$t_{10}=1/115200X10=868\mu s$$

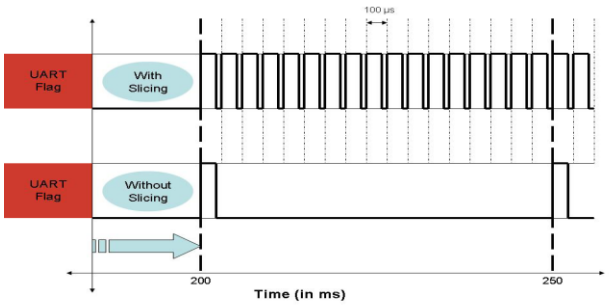


Fig7. Interrupt timer flag switching in case of slicing by the priority manager

To be on the safer side, the timer is configured for 100µs. It can also be seen that, it is almost guaranteed that at every interrupt of 100µs, the data operation is ready and can be performed immediately.

This makes the checking of flag (byte received) a redundant process and hence can be Avoided by directly reading the register value without any Check thereby reducing the number of instructions to be Executed. Since the interrupt latency based on context switching is approximately 400ns, which is acceptable for such a kind of application we would utilize this to let the data-bits be sent during this time. Once all the data is read, the priorities go back to the normal operation and the priority manager will restore its highest priority.

IX. Zigbee Transceiver

Zigbeeis a specification for a suite of high level communication protocols using small, low-power digital radios based on the ieee 802.15.4-2003 standard for wireless personal area networks (wpans), such as wireless headphones connecting with cell phones via short-range radio. The technology defined by the zigbee specification is intended to be simpler and less expensive than other wpans, such as Bluetooth. Zigbee is targeted at radio-frequency (RF) applications that require a low data rate, long battery life, and secure networking.

X. CONCLUSION

The proposed system "RTOS BASED DYNAMIC SCHEDULER IN POWER QUALITY APPLICATIONS" for monitoring, controlling and multitasking in industrial load .With help of ARM7 controller monitoring and controlling the industrial parameters such as power factor, voltage, current and frequency. RTX RTOS is a part of ARM7. RTX service is to provide priority scheduling for Power factor by using Round robin scheduling. Capacitor bank to provide power to load for unbalanced condition.

XI. FUTURE WORK

The Round robin algorithm, business logic and scheduling was tested in the test panel. The future work includes using DMA peripherals of advanced microcontrollers and some other multi-tasking RTOS kernel for multiple load applications.

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