



USER'S MANUAL

MCA-E2701

Product Model: CBI-2701

Ver. 1.2



Notes to Users

The specifications of the product are under continuous improvement and while every effort is made to keep this manual up-to-date, we reserve the right to update the contents of this user's manual without prior notice. Therefore, you should thoroughly read this user's manual even if you have often purchased this product before.

Using this product requires technical knowledge of hardware and software.

Use this product only under the specified conditions such as power supply, voltage, temperature, and humidity range. Interface Corporation's products are not designed with components intended to ensure a level of reliability suitable for use under conditions that might cause serious injury or death.

Please consult our Technical Support Center if you intend to use our products for special purpose, such as use for moving vehicles, medical treatment, aerospace engineering, controlling nuclear power, submerged translators and so on. This product is made under strict quality management, however, when using this product for the purposes that may result in any damages, lost profits, or any other incidental or consequential damages resulting from breakdown of this product, the user is required to take adequate and appropriate measures, such as installing safety devices to avoid possible serious accidents.

Conventions Used in This Manual

<u> Î</u>	This icon denotes a warning, which advises you of precautions to take to avoid injury, data loss, or system crash.
7	This icon denotes a note, caution, or warning.

Indemnification

Interface Corporation makes no warranties regarding damages resulting from installation or use of this product, whether hardware or software, and assume that such risk reverts to the user.

Interface Corporation shall not be liable for any incidental or consequential damages, including damages or other costs resulting from defects which might be contained in the product, product supply delay or product failure, even if advised of the possibility thereof. Customer's right to recover damages caused by fault or negligence on the part of Interface Corporation shall be limited to the amount paid by the customer for that product.

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Interface Corporation products are warranted for a period of either one year or two years from the date of shipment, as evidenced by receipts or other documentation. This warranty does not apply to the software products and expendable supplies such as batteries.

Note: You can determine the warranty period at our Web site by the serial number of your product. Those without Internet access should contact the Sales Information Center.

During the warranty period Interface Corporation will, as a general rule, replace or recondition the defective product without charge, in which case the user will be required to pay the shipping costs, except as set forth below.

The Warranty provided herein does not cover expendable supplies such as batteries and damages, defects, malfunctions, or failures caused by impact during transportation while under owner's responsibility; owner's failure to follow the instructions and the precautions contained in this manual; modification and/or repair of the product by other than Interface Corporation, trouble caused by use with peripherals not specified by Interface Corporation, power failure or surges, fire, earthquake, tidal wave and/or flood.

This warranty applies only when the product is used in Japan.

Interface Corporation warrants its repairs for six months, and will again repair the same defective part without additional charge provide the product is economically repairable. In that case, the user should attach a copy of the most recent repair report to the repair request form. If no repair report is attached, it will be considered as a new repair request.

Before You Export Interface Products

The foreign exchange and foreign trade law of Japan controls the export of this product, due to its possible use as a STRATEGIC MATERIAL. Therefore, before you export this product, you must secure an export permit from the Ministry of Economy, Trade and Industry of Japan.

Revision History

Version	Date	Comments		
1.0	October 2003	User's manual MCA-E2701 published.		
1.1	October 2003	Manual revised:		
		The model of user's manual MCA-E2701 changed from the CBI-2701 and CBI-2702 to the CBI-2701.		
1.2	December 2003	Manual revised:		
		Section 3.1 Hardware Specifications		
		Low-level input current changed from		
		$I_{\rm IL}$ = -0.6 mA (max.) to $I_{\rm IL}$ = -1.1 mA (max.).		
		High-level input current changed from		
		$I_{IH} = +40 \mu\text{A} (\text{max.}) \text{ to } I_{IH} = +11 \mu\text{A} (\text{max.}).$		
		Low-level output voltage added.		
		Chapter 6 Address Assignment added.		
		Section 8.1 Checkpoints		
		A problem and solution added.		

Due to constant product improvements, the information in this user's manual is subject to change without prior notice.

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Chapter 1 Introduction

1.1 Summary

The CBI-2701 is a multifunction digital input/output card for CardBus-based computers. It provides 48 CMOS gated high-voltage digital input and 48 TTL open-collector output channels. This card includes a timer/counter circuit. This timer/counter circuit can be used as an interval timer. This card does not require an external power supply because the input circuit is CMOS gated high-voltage input. External reset signal input is supported by a connector.

1.1.1 Features

- TTL open-collector output channels (+5 Vdc to +24 Vdc)
 Output circuits on the CBI-2701 have TTL open-collector buffers. This feature provides up to +40 mA (max.) of current.
- 2. CMOS gated high-voltage input channels (0 Vdc to \pm 24 Vdc) Input circuits have protection diode, so this product inputs \pm 30 Vdc (max.). It can also input TTL level signal because of 4.7 k Ω pull-up resistor.
- 3. External reset input (RSTIN)

 The RSTIN signal resets this card. This signal can also be configured as one of the interrupt sources.
- 4. Built-in timer/counter

The CBI-2701 has a timer/counter circuit that can be used as an interval timer as mentioned above. A software selectable clock period of $10~\mu s$, $100~\mu s$, 1~ms, 10~ms, and 100~ms and a software programmable frequency divisor in the range of 1 through 15 are supported. The output of the built-in timer/counter circuit can be used as interrupt sources.

- Software configurable interrupt source
 Software configurable interrupt sources are supported. Each interrupt can be masked or unmasked individually.
- Cable
 The JKC-0124 cable is included with the CBI-2701. You can modify one side as desired.

1.2 Optional Products

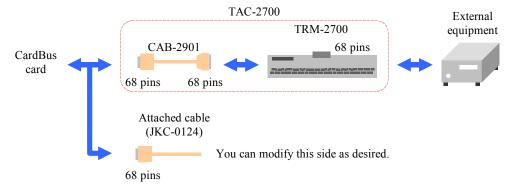
1.2.1 Accessories

Part Number	Description
TAC-2700	The TAC-2700 is composed of a cable and terminal block. The CAB-2901 straight
Cable: CAB-2901	cable converts a PC Card 68-pin male connector to 68-pin half-pitch female
Terminal block: TRM-2700	connector. The cable length is 1.5 m. The TRM-2700 terminal block has 68 screw
	terminals for easy connection of field signals. It has a 68-pin half-pitch male
	connector. It also includes hardware for mounting on a standard DIN rail.
BPA-0507 (Japanese)	The BPA-0507 software controls Interface digital input/output boards from your
	application running on Windows XP, Windows 2000, Windows Me, or Windows 98.
BPC-0506 (Japanese)	This software provides VI (diagram) for Interface digital input/output card on
	LabVIEW of National Instruments Corporation.
BPD-0805 (Japanese)	This software retrieves the configuration registers for MS-DOS and PC DOS.
GPC-2000 (Japanese)	Digital input/output driver software for Windows XP/2000/Me/98.
GPF-2000 (English)	Digital input/output driver software for Windows XP/2000/Me/98.
GPD-2000 (Japanese)	Digital input/output driver software for MS-DOS and PC DOS.
GPG-2000 (Japanese)	Digital input/output driver software for Linux and RTLinux.
GPH-2000 (English)	Digital input/output driver software for Linux and RTLinux.

Refer to our Web site for the latest information and prices of optional products.

Note: You may download software drivers from our Web site free of charge. We also provides software drivers on CD-ROM for a nominal fee.

Connection Diagram



Chapter 2 Signal Definitions

2.1 Cable Connector Pin Assignments



Note: For prevention of incorrect insertion, the card frame and contraction tube of the attached cable are the same color. Check if they are the same color when you connect the cable with the card.

2.2 Signals

Signal Description

Signal	Pin Number	Direction		Description
IN/OUT1	3	Input/output	Digital input/output	General purpose digital input/output Interrupt input signal 1
IN/OUT2	4	Input/output	signal (bi-direction)	General purpose digital input/output Interrupt input signal 2
IN/OUT3	5	Input/output		General purpose digital input/output Interrupt input signal 3
IN/OUT4	6	Input/output		General purpose digital input/output Interrupt input signal 4
IN/OUT5 through IN/OUT48	7 through 18, 27 through 34, 37 through 52, 59 through 66	Input/output		General purpose digital input/output
RSTIN	57	Input	External reset signal	This is a reset signal input. An external circuit can reset this CardBus card by asserting this signal, and an external circuit can request service from the computer.

Use corresponding pins for ground.

Ground Pin Selection*1

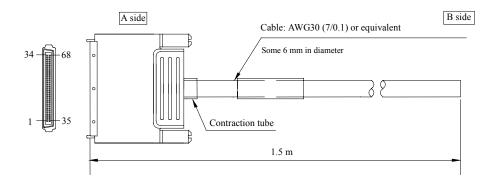
Signal	Pin Number	Ground
IN1 through IN16	1, 2	-COM1
IN17 through IN32	35, 36	-COM2
IN33 through IN48	67, 68	-COM3
RSTIN	58	-FCOM

Note: *1 -COM1, -COM2, -COM3, and -FCOM are connected inside the CardBus card.

2.3 Attached Cable

The JKC-0124 cable is included with the CBI-2701. This cable has a single 68-pin half-pitch female on the A side. You can modify the B side as desired. The cable length is 1.5 m.

2.3.1 Dimensions of the Connector



2.3.2 Wire Connection

CN1	Color of Wire Cover	Dot Mark . Color
1	gray	rec
2	gray	black
3	orange	rec
4	orange	black
5	gray	rec
6	gray	black
7	white	rec
8	white	blacl
9	yellow	rec
10	yellow	black
11	pink	rec
12	pink	blacl
13	orange	rec
14	orange	blacl
15	gray	rec
16	gray	— — black
17	white	rec
18	white	— blacl
19	pink	rec
20	pink	b lacl
21	gray	rec
22	gray	b lacl
23	white	rec
24	white	blace
25	orange	rec
26	orange	blace
27	yellow	— rec
28	yellow	— blacl
29	pink	— rec
30	pink	— blacl
31	orange	rec
32	orange	blacl
33	gray	rec
34	gray	black

CN1	Color of Wire Cover	Dot Mark . Color	
35	white		red
36	white		black
37	white		red
38	white		black
39	yellow		red
40	yellow		black
41	pink		red
42	pink		black
43	orange		red
44	orange		black
45	orange		red
46	orange		black
47	gray		red
48	gray		black
49	white		red
50	white		black
51	yellow		red
52	yellow		black
53	orange	(*1)	red
54	orange	 (*1)	black
55	yellow		red
56	yellow		black
57	pink		red
58	pink		black
59	gray	(*1)	red
60	gray	 (*1)	black
61	white	(*1)	red
62	white	(*1)	black
63	yellow	(*1)	red
64	yellow	 (*1)	black
65	pink	(*1)	red
66	pink	 (*1)	black
67	yellow		red
68	yellow		black

Notes:

- *1 These dot marks are printed in straight succession.
- The heavy line indicates twisted-pair wires.
- The braided shield is connected to the ground of CN1.

Chapter 3 Specifications

3.1 Hardware Specifications

General Purpose Digital Input Circuits

Parameter	Specification
Input signals	IN1 through IN48 (bi-direction), RSTIN
Input configurations	CMOS gated high-voltage input
	(with 4.7 k Ω pull-up resistor and protection diode, able to connect to TTL
	level output)
	74VHC14 or equivalent
Input logic	1 ← Low
	$0 \leftarrow \text{High}$
Maximum voltage rating	+30 Vdc
Input voltage range	0 Vdc to +24 Vdc
Input impedance	$4.7 \text{ k}\Omega$ pull-up resistor
Low-level input current	$I_{IL} = -1.1 \text{ mA (max.)}$
High-level input current	$I_{IH} = +11 \mu\text{A} (\text{max.})$
Low-level input voltage	$V_{IL} = +0.7 \text{ V (max.)}$
High-level input voltage	$V_{IH} = +3.1 \text{ V (min.)}$
Input response time	$T_{RON} = 0.1 \mu s (typ.)$
	$T_{ROFF} = 0.1 \mu s (typ.)$

General Purpose Digital Output Circuits

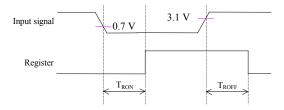
Parameter	Specification
Output signals	OUT1 through OUT48 (bi-direction)
Output configurations	TTL open-collector output (with 4.7 kΩ pull-up resistor)
	TD62597AFN or equivalent
Output logic	$1 \rightarrow \text{Low}$
	$0 \rightarrow \text{High}$
Maximum voltage rating	+30 Vdc
Applied voltage range	+5 Vdc to +24 Vdc
Output voltage range	0 Vdc to the applied voltage
Maximum output current	$I_{OL} = +40 \text{ mA}$
Low-level output voltage	$V_{OL} = +0.2 \text{ V (max.)} (I_{OL} = +10 \text{ mA})$
	$V_{OL} = +0.5 \text{ V (max.)} (I_{OL} = +40 \text{ mA})$
Output response time	$T_{RON} = 1.0 \mu s$ (typ.) (with the maximum load)
	$T_{ROFF} = 1.0 \mu s$ (typ.) (with the maximum load)
	(Low-to-high transition time varies depending on the load impedance.)

Basic Specifications

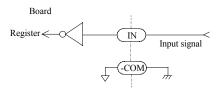
Parameter	Specification
Isolation	No-isolation
Interrupt sources	6 sources (IN1, IN2, IN3, IN4, interval timer, and RSTIN)
	One IRQ required (automatically assigned by the Plug and Play system)
Wiring requirements	Approximately 1.5 m or less (depending on the wiring environment)
Number of slots required	1 slot
Number of I/O ports	16 ports (automatically assigned by the Plug and Play system)
Power consumption	+3.3 Vdc: 175 mA (typ.)
Bus requirements	PC Card Standards-Based CardBus
Card size	PCMCIA/JEITA Type II
Environmental conditions	Operating temperature: 0 °C to 50 °C
	Relative humidity: 20% to 90% (non-condensing)
Acceptable cable connector	CN1: HDRA-E68FT2-SL (68-pin PC Card connector)
	(Honda Tsushin Kogyo Co., Ltd.) or equivalent

• Input Response Time

We define the input response time as required for the input data to travel to the CardBus card register. The input response time includes propagation delays of input buffer ICs. The following figure shows an input waveform and the corresponding CardBus card register timing chart.

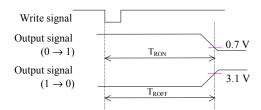


The following figure shows the test circuit for the input response time.

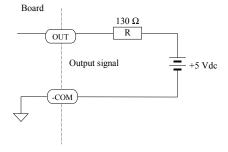


• Output Response Time

We define the output response time as required for the output data to travel to an output pin on the CardBus card after a CBI write command is issued. The output response time includes CBI write cycle duration and propagation delays of output buffer ICs. The following figure shows a CBI write signal and output waveforms.

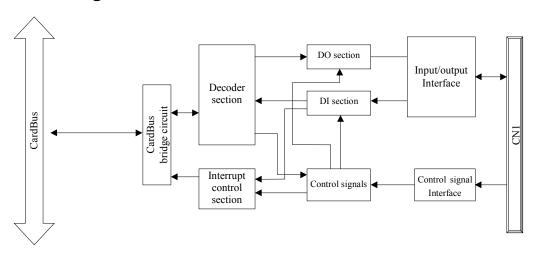


The following figure shows the test circuit for the output response time.



Note: The input response time and the output response time do not include the processing time of the computer.

3.2 Circuit Diagram

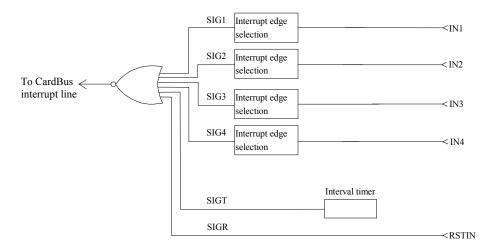


3.3 Interrupt Sources

This board can	generate interrupts	s to the compute	er with the fo	llowing courses
Tills board call	echciale interrupe	Տ ւՕ ւне сонношк	a willi liic id	mowing sources.

Interrupt Source	Description
SIG1	Input signal from IN1
SIG2	Input signal from IN2
SIG3	Input signal from IN3
SIG4	Input signal from IN4
SIGT	Interval timer interrupt
SIGR	External reset input (RSTIN)

The interrupt circuit consists of the interrupt edge selection circuit blocks and the interrupt source selection circuit blocks.



Interrupt requests are cleared under the following conditions:

- SIG1, SIG2, SIG3, SIG4
 - When the software deasserts the request explicitly.
 - When you change the settings of the interrupt edge selection, the interrupt source selection, or the interrupt mask. (Only the corresponding interrupt source)
 - When the CardBus reset occurs.
 - When the RSTIN signal is asserted.
- SIGT
 - When the software deasserts the request explicitly.
 - When you change the interrupt mask. (Only the corresponding interrupt source)
 - When the CardBus reset occurs.
 - When the RSTIN signal is asserted.
 - When the interval timer is reset.
- SIGR
 - When the software deasserts the request explicitly.
 - When you change the interrupt mask. (Only the corresponding interrupt source)
 - When the CardBus reset occurs.

When the board is turned on, all interrupt requests are cleared.

3.3.1 Interval Timer

The interval timer can be used to generate an interrupt to the host computer every timer cycle period. The timer cycle period is given by the following equation:

$$T = RATE \times CLK$$

T: Timer cycle period

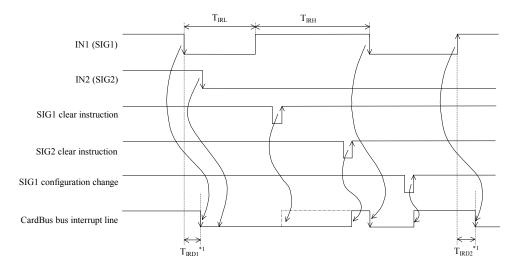
RATE: integer 1 through 15

CLK: 10 µs, 100 µs, 1 ms, 10 ms, 100 ms

This timer begins counting immediately after both *RATE* and *CLK* are programmed, and it will keep counting until a stop instruction is issued. It is recommended that you use an interrupt timer interval greater than or equal to 10 ms. Windows XP, Windows 2000, Windows NT 4.0, Windows Me, and Windows 98 cannot handle a large number of interrupts within a short time period. In such a case, Windows may hang up or freeze.

3.3.2 Timing Chart for Interrupt Signals

Where we assume that IN1 and IN2 are selected as interrupt sources for SIG1 and SIG2, respectively and the falling edge of each signal is selected as an interrupt edge.

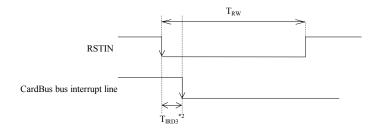


The computers accept interrupt requests when the CardBus bus interrupt signal is low level.

Switching Characteristics for IN1, IN2, IN3, IN4

Symbol	Parameter	Min.	Тур.	Unit
T_{IRL}	Low-level time	600		ns
T_{IRH}	High-level time	1.5	_	μs
T_{IRDI}^{*1}	High-to-low transition to interrupt request delay time	_	500	ns
T_{IRD2}^{*1}	Low-to-high transition to interrupt request delay time	_	1	μs

Note: *1 The delay time T_{IRD1} and T_{IRD2} are the interval between the instant when input signals go from high-level to low-level or from low-level to high-level and the instant when the card requests an interrupt on the CardBus bus, not when the computer begins to process the interrupt request.



Switching Characteristics for RSTIN

Symbol	Parameter	Min.	Тур.	Unit
T_{RW}	RSTIN low-level time	10		μs
T_{IRD3}^{*2}	High-to-low transition of RSTIN to interrupt request delay time ^{*3} (clear delay time for output flip-flop and internal registers)	_	5	μs

Notes:

- *2 In another aspect, T_{IRD3} is the delay time for output flip-flops and internal registers to be cleared after RSTIN is asserted. Output pins require a response time of 0.5 μ s plus T_{IRD3} to be cleared to high-level.
- \bullet *3 The delay time T_{IRD3} is the interval between when RSTIN goes from high-level to low-level and when the card requests an interrupt on the CardBus bus, not when the computer begins to process the interrupt request.

Chapter 4 External Connections

Keep these important points in mind when connecting the card with external equipment.

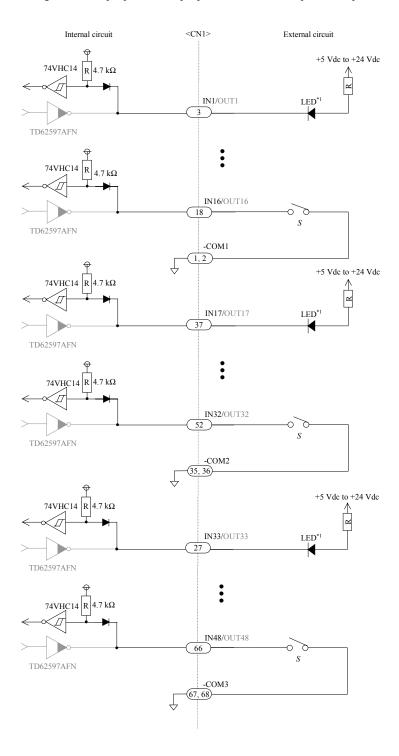
FAILURE TO OBSERVE THESE IMPORTANT SAFETY PRECAUTIONS MIGHT RESULT IN EXCESSIVE VOLTAGE IN THE CARDBUS CARD CIRCUITS, CAUSING AN ELECTRICAL FIRE, WITH POSSIBLE OPEN FLAME AND SMOKE.

! Never connect an output signal to other output signals except open-collector outputs that are capable of
wire-OR connection.
! Never short-circuit an output signal to external power supply anodes.
! The maximum voltage rating of output cirtcuit is +30 Vdc.
! The maximum output current of each general purpose digital output channel is +40 mA.
! The maximum voltage rating of input cirtcuit is +24 Vdc.
! Double-check that polarities are correct before connecting external power supplies.
! Keep the signal cable away from other equipment as far as possible to avoid electromagnetic
interference.

4.1 Example Connections

4.1.1 General Purpose Digital Inputs/Outputs (IN1/OUT1 through IN48/OUT48)

The digital input/output circuit has 48 inputs/outputs, numbered from IN1/OUT1 through IN48/OUT48. Each pin can be configured as an input pin or an output pin. The maximum output current per channel is +40 mA.



1. Digital input

Programs can read data from the input pins by issuing the IN instructions to the corresponding I/O port addresses.

Input Data	INxx	External Circuit
1	Low	Closed (S: on)
0	High	Open (S: off)

2. Digital output

Programs can write data to output pins by issuing the OUT instructions to the corresponding I/O port addresses.

Output Data	OUTxx	External Circuit
1	Low	Closed (LED: on)
0	High	Open (LED: off)

Notes:

- Data 0 must be previously output to the pin before using it as an input. Data 0 is output when the CardBus card is
 powered up or reset.
- *1 The following description shows how to determine resistance of the currrent limiting resistor. Where $I_{\text{LED}}(A)$ is the LED operating current, $V_{\text{LED}}(V)$ is the LED forward bias, $V_{\text{OL}}(V)$ is the low-level output voltage of the output pin, and $V_{\text{DD}}(V)$ is the supply voltage, the current limiting resistance $R(\Omega)$ is obtained by the following equation:

$$R = (V_{DD} - V_{LED} - V_{OL}) / I_{LED}$$
.

Use appropriate resistors to meet the operating conditions of the LED and supply voltage.

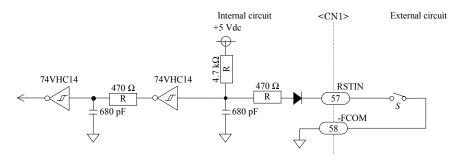
Power consumption P (W) of the resistor is obtained by the following equation:

$$P = I_{\text{LED}}^2 \times R$$
.

Power consumption of the resistor must be less than the power rating of the resistor.

4.1.2 Reset Input (RSTIN)

A signal on the pin 57 of CN1 is an external reset signal. When this signal is asserted, an interrupt occurs to your computer. This signal can be masked or unmasked. To be recognized as a valid reset signal, a $10 \,\mu s$ minimum assertion of the RSTIN signal is required.



Board Status	RSTIN	External Circuit
Reset	On	Closed (S: on)
Operating	Off	Open (S: off)

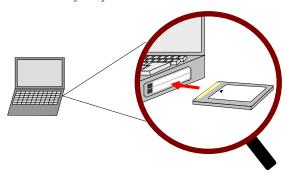
Chapter 5 Installation

BE SURE TO ELIMINATE STATIC ELECTRICITY OF YOUR BODY BEFORE YOU INSTALL OR REMOVE THIS PRODUCT.

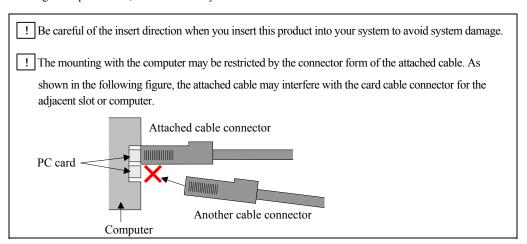
5.1 Card Installation

When you install this product in your system, read the manual of your system which refers to the PC card slot.

- Make sure that the system is turned off and the power cable is unplugged.
 (This card corresponds to Hot Swap. You can insert this card when the system turns on.)
- 2. Insert the card into the PC card slot in your system.



3. Plug in the power cord, and turn on the system.



5.2 Driver Software Installation

Refer to our Web site for the Help of each optional software when you install and use it.

5.3 Card Uninstallation

The method of removing PC card from your system differs depending on each system. Please read the manual of your system.

! Do not remove this product when accessing to the external equipment. Your system may not operate correctly.

Chapter 6 Address Assignment

6.1 Configuration Register

The following table describes the configuration space register.

Offset	3h	2h	1h	0h				
00h	Device ID		Vendor ID					
OOH	0A8D (CBI-2701)		1147h (Interface)					
04h	Status		Command					
0411	00000010000000000	b	000000000000000000000000000000000000000					
08h	Class Code			Revision ID				
oon	FF0000h (Other De		T	01h				
0Ch	BIST	Header Type	Latency Timer	Cache Line Size				
oen_	00h	00h	00h	00h				
	Base Address Regis							
10h	Card control address							
1 41	?????????????????							
14h		0000000000000000b						
18h		00000000000000000000000000000000000000						
1Ch		0000000000000000b						
20h		00000000000000000000000000000000000000						
24h		0000000000000000b						
28h	Card bus CIS Pointe 00000000h	er						
2Ch	Subsystem ID		Subsystem Vendor	ID				
2CII	0201h (CBI-2701)		1147h (Interface)					
30h	Expansion ROM Base Address							
	00000000h							
34h	00000000h							
38h	00000000h							
3Ch	MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line				
<i>J</i> CII	00h	00h	01h (INTA#)	??h				
40h through DFh	CIS							
F0h through FFh	Reserved							

Notes:

- The above values are described as follows:
 - >> h: hexadecimal form
 - >> b: binary form
 - >> ?: configured by the Plug and Play system
- Refer to PC Card Standard for more details of registers.

6.1.1 Vendor ID Register

Offset	Direction	Description									
		D.	1.5	1.4	12	10	11	10	0		
	+01h Input	Bit	15	14	13	12	11	10	9	8	
+01h		Mnemonic	VEN	VEN	VEN	VEN	VEN	VEN	VEN	VEN	
· OIII		Milemonic	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	
		Default value	0	0	0	1	0	0	0	1	
		Bit	7	6	5	4	3	2	1	0	
+00h	Input	Mnemonic	VEN	VEN	VEN	VEN	VEN	VEN	VEN	VEN	
+00II II	при	Millemonic	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
		Default value	0	1	0	0	0	1	1	1	

VENID15 through VENID0:

Indicates the vendor (manufacturer).

(Vendor ID register)

6.1.2 Device ID Register

Offset	Direction	Description									
+03h Input		Bit	15	14	13	12	11	10	9	8	
	Input	Mnemonic	DEV ID15	DEV ID14	DEV ID13	DEV ID12	DEV ID11	DEV ID10	DEV ID9	DEV ID8	
		Default value	0	0	0	0	1	0	1	0	
		Bit	7	6	5	4	3	2	1	0	
+02h	Input	Mnemonic	DEV ID7	DEV ID6	DEV ID5	DEV ID4	DEV ID3	DEV ID2	DEV ID1	DEV ID0	
		Default value	1	0	0	0	1	1	0	1	

DEVID15 through DEVID0: (Device ID register)

Indicates the device ID (manufacturer).

6.1.3 Command Register

Offset	Direction	Description								
		Bit	15	14	13	12	11	10	9	8
+05h	Input	Mnemonic	-	-	-	-	-	-	•	-
		Default value	0	0	0	0	0	0	0	0
		Bit	7	6	5	4	3	2	1	0
+04h	Input/Output	Mnemonic	-	1	1	1	1	-	-	I/O Space
		Default value	0	0	0	0	0	0	0	?

I/O Space:

(I/O space control)

Indicates that the board can respond to I/O accesses when bit0 is 1. The value 1 is written to bit0 when the Plug and Play system allocates I/O space.

6.1.4 Status Register

Offset	Direction	Description									
		Bit	15	14	13	12	11	10	9	8	1
+07h	Input	Mnemonic	-	1	-	-	-	Devsel1	Devsel0	-	
		Default value	0	0	0	0	0	0	1	0	
+06h	Input	Reserved					-	•			_

Devsel1, Devsel0: (DEVSEL timing register)

Indicates the timing which encodes the DEVSEL# signal. The value 01 identifies a target board that provides medium-speed response.

6.1.5 Revision ID Register

Offset	Direction	Description								
		Bit	7	6	5	4	3	2	1	0
+08h	Input	Mnemonic	REV ID7	REV ID6	REV ID5	REV ID4	REV ID3	REV	REV ID1	REV ID0
		Default value	0	0	0	0	0	0	0	1

REVID7 through REVID0: (Revision ID register)

Indicates the revision of the device. The revision ID will be changed with changes such as function, or specification of the device.

6.1.6 Base Address Register 0

Offset	Direction	Description									
		Bit	31	30	29	28	27	26	25	24	1
		Бц	BA0	1							
+13h	Input/Output	Mnemonic	31	30	29	28	27	26	25	24	
		Default value	?	?	?	?	?	?	?	?	1
		Bit	23	22	21	20	19	18	17	16	
+12h	Input/Output	Mnemonic	BA0								
	T T		23	22	21	20	19	18	17	16	4
		Default value	?	?	?	?	?	?	?	?]
		D:4	1.5	1.4	12	10	11	10	9	8	1
		Bit	15	14	13	12	11	10			4
+11h	Input/Output	Mnemonic	BA0 15	BA0 14	BA0 13	BA0 12	BA0 11	BA0 10	BA0 09	BA0 08	
		Default value		7	7	7	7	7	7	?	1
		Delault value	÷	•	•		•	•	•	•	
		Bit	7	6	5	4	3	2	1	0	1
+10h	Input/Output	Mnemonic	BA0	BA0	BA0					_	1
1011	input output		07	06	05	_					
		Default value	?	?	?	0	0	0	0	1]

BA031 through BA005: (Board control base address register)

Indicates board control I/O space.

6.1.7 Interrupt Line Register

Direction	Description									
	Bit	7	6	5	4	3	2	1	0	
Input/Output	Mnemonic	ILIN7	ILIN6	ILIN5	ILIN4	ILIN3	ILIN2	ILIN1	ILIN0	
	Default value	?	?	?	?	?	?	?	?	
		Bit Input/Output Mnemonic	Bit 7 Input/Output Mnemonic ILIN7	Input/Output Bit 7 6 Mnemonic ILIN7 ILIN6	Bit 7 6 5	Bit 7 6 5 4	Bit 7 6 5 4 3	Bit 7 6 5 4 3 2 2 2 2 2 2 2 2 2	Bit 7 6 5 4 3 2 1	

ILIN7 through ILIN0: (Interrupt line register)

Indicates the interrupt line of the device. The Plug and Play system automatically assigns the line.

6.2 Board Control Register (Base Address 0)

The following table describes the board control registers. When the CardBus reset or on-card power-on reset is asserted, each register is set to default value.

Offset	Direction	Description
+001- 41-man-al- +051-	Input	General purpose digital input register
+00h through +05h	Output	General purpose digital input register
+06h through +09h	Input	Reserved
+0011 tillough +09fi	Output	Reserved
+0Ah	Input	Interval timer register
⊤UAII	Output	Interval timer register
+0Bh	Input	Reserved
⊤UDII	Output	Reserved
+0Ch	Input	Interrupt source flag register
+0CII	Output	Interrupt source flag register
+0Dh	Input	Interrupt mask register
⊤0DII	Output	Interrupt mask register
+0Eh	Input	Interrupt edge selection register
TOEII	Output	Interrupt edge selection register
+0Fh	Input	Reserved
TOFII	Output	Reserved

6.2.1 General Purpose Digital Input/output Register

Offset	Direction	Description								
		Bit	47	46	45	44	43	42	41	40
	Input	Mnemonic	IN48	IN47	IN46	IN45	IN44	IN43	IN42	IN41
	Input	Default value	IN48	IN47	IN46	IN45	IN44	IN43	IN42	IN41
+05h		Bolault value	11110	11117	11110	11113	11111	11113	11112	11111
		Bit	47	46	45	44	43	42	41	40
	Output	Mnemonic			_		OUT44			
	,	Default value	0	0	0	0	0	0	0	0
-										
		Bit	39	38	37	36	35	34	33	32
	Input	Mnemonic	IN40	IN39	IN38	IN37	IN36	IN35	IN34	IN33
		Default value	IN40	IN39	IN38	IN37	IN36	IN35	IN34	IN33
+04h									•	
		Bit	39	38	37	36	35	34	33	32
	Output	Mnemonic	OUT40			OUT37		OUT35	OUT34	OUT33
		Default value	0	0	0	0	0	0	0	0
		E.	2.1	20	20	20	27	2.	2.5	
	Incert	Bit	31	30	29	28	27	26	25	24
	Input	Mnemonic	IN32	IN31	IN30	IN29	IN28	IN27	IN26	IN25
+03h		Default value	IN32	IN31	IN30	IN29	IN28	IN27	IN26	IN25
+0311		Bit	31	30	29	28	27	26	25	24
	Output	Mnemonic								
	Output	Default value	00132	00131	00130	00129	0	00127	0	0
		Delauit value	U	U	U	U	U	U	U	U
		Bit	23	22	21	20	19	18	17	16
	Input	Mnemonic	IN24	IN23	IN22	IN21	IN20	IN19	IN18	IN17
		Default value	IN24	IN23	IN22	IN21	IN20	IN19	IN18	IN17
+02h										
		Bit	23	22	21	20	19	18	17	16
	Output	Mnemonic	OUT24	OUT23	OUT22	OUT21	OUT20	OUT19	OUT18	OUT17
		Default value	0	0	0	0	0	0	0	0
					1	1	1	1		
		Bit	15	14	13	12	11	10	9	8
	Input	Mnemonic	IN16	IN15	IN14	IN13	IN12	IN11	IN10	IN9
+01h		Default value	IN16	IN15	IN14	IN13	IN12	IN11	IN10	IN9
+01II		D:4	1.5	1.4	12	12	11	10	0	0
	Output	Bit Mnemonic	15	14	13	12	11	10	9 OUT10	8
	Output	Default value	00116	0	00114	00113	00112	0	OUT10 0	OUT9 0
		Delaunt value		L ⁰	U	L	J 0	L		U
		Bit	7	6	5	4	3	2	1	0
	Input	Mnemonic	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
		Default value	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
+00h										
		Bit	7	6	5	4	3	2	1	0
	Output	Mnemonic	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1
		Default value	0	0	0	0	0	0	0	0
	j				,		,		,	

IN48 through IN1: Indicates the status of IN/OUT1 through IN/OUT48.

(General purpose digital input) 0: High 1: Low

OUT48 through OUT1: Indicates the status of IN/OUT1 through IN/OUT48.

(General purpose digital output) 0: High 1: Low

6.2.2 Interval Timer Register

Offset	Direction	Description									
		Bit	7	6	5	4	3	2	1	0	
	Input	Mnemonic	-	-	-	-	TD4	TD3	TD2	TD1	
		Default value	0	0	0	0	0	0	0	0	
+0Ah											
		Bit	7	6	5	4	3	2	1	0	
	Output	Mnemonic	ı	SCK3	SCK2	SCK1	TCTRL4	TCTRL3	TCTRL2	TCTRL1	
		Default value	0	0	0	0	0	0	0	0	

TD4 through TD1: Reads the timer count value of the interval timer.

(Timer count reading)

TCTRL4 through TCTRL1: Sets the frequency divisor of the interval timer.

(Timer count setting)

SCK3 through SCK1: Sets the base clock frequency of the interval timer.

(Timer count setting)

The following table describes the interval timer period.

			SCK3		()			1	1	
	_		SCK2	(0		1)	1	1
TCTRL4	TCTRL3	TCTRL2	SCK1 TCTRL1	0	1	0	1	0	1	0	1
		. 0	0	Stop	Stop	Stop	Stop	Stop	-	ı	ı
	0	U	1	10 μs	100 μs	1 ms	10 ms	100 ms	-	1	ı
	U	1 1	0	20 μs	200 μs	2 ms	20 ms	200 ms	-	-	-
0		1	1	30 µs	300 μs	3 ms	30 ms	300 ms	-	-	-
U		. 0	0	40 μs	400 μs	4 ms	40 ms	400 ms	-	-	-
	1	U	1	50 μs	500 μs	5 ms	50 ms	500 ms	-	-	1
	1	1	0	60 µs	600 μs	6 ms	60 ms	600 ms	-	-	-
		1	1	70 µs	700 μs	7 ms	70 ms	700 ms	-	-	-
		0	0	80 µs	800 µs	8 ms	80 ms	800 ms	-	-	-
	0	0	1	90 μs	900 μs	9 ms	90 ms	900 ms	-	-	-
	0	1	0	100 μs	$1000\mu s$	10 ms	100 ms	1000 ms	-	-	-
1		1	1	110 µs	1100 µs	11 ms	110 ms	1100 ms	-	-	-
1		0	0	120 µs	1200 µs	12 ms	120 ms	1200 ms	-	-	-
	1	0	1	130 µs	1300 µs	13 ms	130 ms	1300 ms	-	-	-
	1	1	0	140 μs	1400 μs	14 ms	140 ms	1400 ms	-	-	-
		1	1	150 μs	1500 μs	15 ms	150 ms	1500 ms	-	-	-

6.2.3 Interrupt Source Flag Register

Offset	Direction		Description									
.001	Input	Bit Mnemonic Default value	7 - 0	6 SIGRR SIGRR	5 SIGR 0	4 SIGT 0	3 SIG4 0	2 SIG3 0	1 SIG2 0	0 SIG1 0		
+0Ch	Output	Bit Mnemonic Default value	7 - 0	6 - 0	5 SIGR 0	4 SIGT 0	3 SIG4 0	2 SIG3 0	1 SIG2 0	0 SIG1 0		

SIGRR Indicates the status of RSTIN.

0: High 1: Low

SIGR: <Input>

Inidicates the status of interrupt from RSTIN.

0: Interrupt did not occur.1: Interrupt occurred.

<Output>

Clears the status of interrupt from RSTIN.

0: Not clear 1: Clear

SIGT: <Input>

Indicates the status of the interval timer interrupt.

0: Interrupt did not occur.1: Interrupt occurred.

<Output>

Clears the status of the interval timer interrupt.

0: Not clear 1: Clear

SIG4 through SIG1: <Input>

Indicates the status of the interrupt input signals 1 through 4.

0: Interrupt did not occur.1: Interrupt occurred.

<Output>

Clears the status of the interrupt input signals 1 through 4.

0: Not clear 1: Clear

6.2.4 Interrupt Mask Register

Offset	Direction	Description									
		Bit	7	6	5	4	3	2.	1	0	[
+0Dh	Input/Output	-		-	SIGR	SIGT	SIG4	SIG3	SIG2	SIG1	1
	-	Default value	0	0	0	0	0	0	0	0	
		•									•

SIGR: Indicates the RSTIN interrupt mask.

0: Mask (ed) 1: Unmask (ed)

SIGT: Indicates the interval timer interrupt mask setting.

0: Mask (ed) 1: Unmask (ed)

SIG4 through SIG1: Indicates the mask setting of interrupt input signals 1 through 4.

0: Mask (ed) 1: Unmask (ed)

6.2.5 Interrupt Edge Selection Register

Offset	Direction	Description									
		7 .		_						_	7
		Bit	7	6	5	4	3	2	l	0	
+0Eh	Input/Output	Mnemonic	EDS4	EDS3	EDS2	EDS1	-	-	-	-	
		Default value	0	0	0	0	0	0	0	0	1
		'									-

EDS4: Indicates the interrupt edge selection of SIG4.

0: Interrupts occur (ed) when SIG4 goes from high to low. 1: Interrupts occur (ed) when SIG4 goes from low to high.

EDS3: Indicates the interrupt edge selection of SIG3.

0: Interrupts occur (ed) when SIG3 goes from high to low. 1: Interrupts occur (ed) when SIG3 goes from low to high.

EDS2: Indicates the interrupt edge selection of SIG2.

0: Interrupts occur (ed) when SIG2 goes from high to low. 1: Interrupts occur (ed) when SIG2 goes from low to high.

EDS1: Indicates the interrupt edge selection of SIG1.

0: Interrupts occur (ed) when SIG1 goes from high to low. 1: Interrupts occur (ed) when SIG1 goes from low to high.

Chapter 7 Notes for Users

For your safety, follow all warnings and instructions described in this manual.

7.1 Cautions, Periodic, Inspections, and Storage

Failure to follow this warning may result in electric shock, burns, serious injury, and in some cases, even cause death.



Use this product only under the conditions as shown below.

Environmental Specifications

Parameter	Specification
Temperature Range	0 °C to 50 °C
Relative Humidity Range	20% to 90% (non-condensing)
Dust	Typical office environment
Corrosive Gas	None
Noise	Far from power source and its wiring
Voltage Requirements	CardBus specification (+3.3 Vdc (+/-3 V))

The following inspections should be carried out on this card periodically.

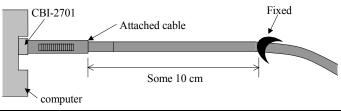
Periodic Inspections

Item	Checkpoint
Cable Connections	Be sure that all connectors and cables are installed correctly.
Connector Contacts	Check for dirt or corrosion.

TO AVOID DAMAGE TO THE BOARD AND POSSIBLE INJURY, TAKE APPROPRIATE PRECAUTIONS AS DESCRIBED BELOW WHEN HANDLING IT.

Caution!

- ! This board should be stored exactly the same way as when it was received. Proceed as follows:
 - 1. Put the board back in its electro-conductive bag.
 - 2. Wrap the board with the original packing material.
 - 3. Avoid excessive humidity.
 - 4. Do not expose the board to the direct rays of the sun.
 - 5. Store the board at room temperature.
- ! Do not modify the card. Interface Corporation assumes no liability for any malfunctions resulting from users' unauthorized modification of the card.
- ! Take measures to avoid and minimize shock, vibration, magnetic fields, and static electricity in the storage or operating environment of this card.
- ! Make sure that the card is disconnected from the cable before inserting or removing any cards.
- ! Please keep the attached cable in a horizontal position for approximately 10 cm from the card connection part as below, and fix it not to move, even if stress starts.



Chapter 8 Troubleshooting

8.1 Checkpoints

Problem	Solution
Data cannot be	Double-check all cable connections.
transferred correctly.	Set up your equipment to meet the timing characteristics of this board, such as data setup time, input/output response time.
	If the power requirements exceed the system power budget, the circuits on the card or connected external circuits cannot be driven properly. Prepare an external power supply for your CardBus card.
Interrupts do not occur.	Set up the card interrupt configuration such as edge selection or sources to be consistent with your application and external circuits.
	If the interrupt configuration is correct, but the interrupt is masked, the interrupt will not occur. Unmask the interrupt that you want to use.
The computer does not recognize this card.	Use the PCI device viewer (BPF-0801) to examine the CardBus cards on your computer after downloading it from our Web site. Please send the result to our Technical Support Center by fax or e-mail. The PCI device viewer may be downloaded from our Web site free of charge.
The computer does not response after Standby mode. (Input and output are disabled.)	Set the System standby setting to "Never".

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For Assistance:

Please visit our Web site (www.interface.co.jp) or send a fax (0120-621553(in Japan)) or e-mail (support@interface.co.jp) to the Technical Support Center.

We recommend you to ask questions from our Web site to shorten the answering time.

If the problem is urgent, please consult the Sales Information Center.

When you contact us, we need the information on the **Technical Support Form** provided with this manual plus the information listed below so we can answer your questions as quickly as possible.

Computer Environment	Computer brand and model, specific operating system, software configuration, other interface boards installed if any.
Description of The Problem	Situations where the product was used.

Technical support is available during business hours.

We provide a product rental service so you can evaluate our product prior to purchase.

Inquiries	Refer to	Phone	FAX
Product Rental Service	Technical Support Center	082-262-1630 (in Japan)	082-262-1552 (in Japan)
Distributors, Shipping Date,	Sales Information Center	0120-447213 (in Japan)	0120-458257 (in Japan)
Prices, Others		E-mail : sales@	interface.co.jp

Repair and Maintenance

The company will, at its option, replace its product, which the company, upon inspection, shall determine to be defective in material and/or workmanship. If the product is obviously damaged or defective, please return it using procedures outlined below.

- 1. Fill out the **Repair Request Form**. Describe hardware configurations of the board and malfunction in detail.
- 2. Fax the **Repair Request Form** to the Technical Support Center.
- 3. We will send you a repair quotation by return fax.
- 4. Carefully repack the damaged product, enclosing the **Repair Request Form**, and forward it (shipping prepaid) to the repair group, at our Oita Plant (address shown below).

When the damage or defect is not obvious, please contact the Sales Information Center or our Technical Support Center.

Be aware that depending on the extent and type of damage, the unit may not be economically repairable. If so, we will notify you immediately.

will fictify you minitediately	•
Receiver's Address	Repair Group, Oita Plant, Interface Corporation 1428, Shimobaru, Aki-machi, Higashikunisaki-gun, Oita, 873-0231 Japan
Contact Information	Technical Support Center Phone: 082-262-1630 (Available during business hours) FAX: 082-262-1552

Visit our Web site (www.interface.co.jp) for:

Technical Support	Frequently asked questions, related technical terminology
Product Information	The latest information about our products; specifications, product selection guides, etc
Useful Information	Discount information, rental information, distributors
Downloads Service	Drivers, technical documents such as I/O port maps, sample programs, and user's
	manual data.

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