User's Manual

ELPIDA

HOW TO USE DDR SDRAM

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INTRODUCTION

This manual is intended for users who design application systems using double data rate synchronous DRAM (DDR SDRAM). Readers of this manual are required to have general knowledge in the fields of electrical engineering, logic circuits, as well as detailed knowledge of the functions and usage of conventional synchronous DRAM (SDRAM).

Purpose

This manual is intended to give users understanding of basic functions and usage of DDR SDRAM. For details about the functions of individual products, refer to the corresponding data sheet. Since operation examples that appear in this manual are strictly illustrative, numerical values that appear are not guaranteed values. Use them only for reference.

Conventions

Caution: Information requiring particular attention
Note: Footnote for items marked with Note in the text
Remark: Supplementary information

Related Documents

Related documents indicated in this manual may include preliminary versions, but they may not be explicitly marked as preliminary.

Document Name	Document Number
EDD1204ALTA, EDD1208ALTA, EDD1216ALTA DATA SHEET	E0136E
HOW TO USE SDRAM USER'S MANUAL	E0123N

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CHAPTER 1 DIFFERENCES BETWEEN SDRAM AND DDR SDRAM

DDR SDRAM (double data rate synchronous DRAM) is a type of DRAM that realizes twice the data transfer rate of conventional SDRAM (here after in this document, conventional SDRAM is referred to as SDR SDRAM (single data rate synchronous DRAM) in contrast with DDR SDRAM).

This chapter explains the differences between DDR SDRAM and SDR SDRAM in the following areas.

(1) Differences in functions and specifications
(2) Differences in commands
(3) Differences in operation timing

1.1 Differences in Functions and Specifications

DDR SDRAM is a type of SDRAM that inherits technologies from SDR SDRAM and realizes faster operation and lower power consumption. It shares many common aspects with SDR SDRAM, which enables easy transition to DDR SDRAM.

This section explains the differences in functions and specifications between DDR SDRAM and SDR SDRAM.

Table 1-1. Differences in Functions and Specifications

Item	DDR SDRAM	SDR SDRAM
Data transfer frequency	Twice the operation frequency	Same as the operation frequency
Data rate	$2/t_{CK}$	$1/t_{CK}$
Clock input	Differential clock	Single clock
Data strobe signal (DQS)	Essential	Not supported
Interface	SSTL_2	LVTTL
Supply voltage	2.5 V	3.3 V
/CAS read latency	2, 2.5	2, 3
/CAS write latency	1	0
Burst length	2, 4, 8	1, 2, 4, 8, full-page (256) Note
Burst sequence	Sequential/Interleave	Sequential/Interleave
Use of DLL	Essential	Option
Data mask	Write mask only	Write mask/Read mask

Note Full-page (256) burst of SDR SDRAM is an option.

Remark t_{CK}: Clock cycle time

1.1.1 Data transfer frequency, data rate

DDR SDRAM achieves a data transfer rate that is twice the clock frequency by employing 2-bit prefetch architecture.

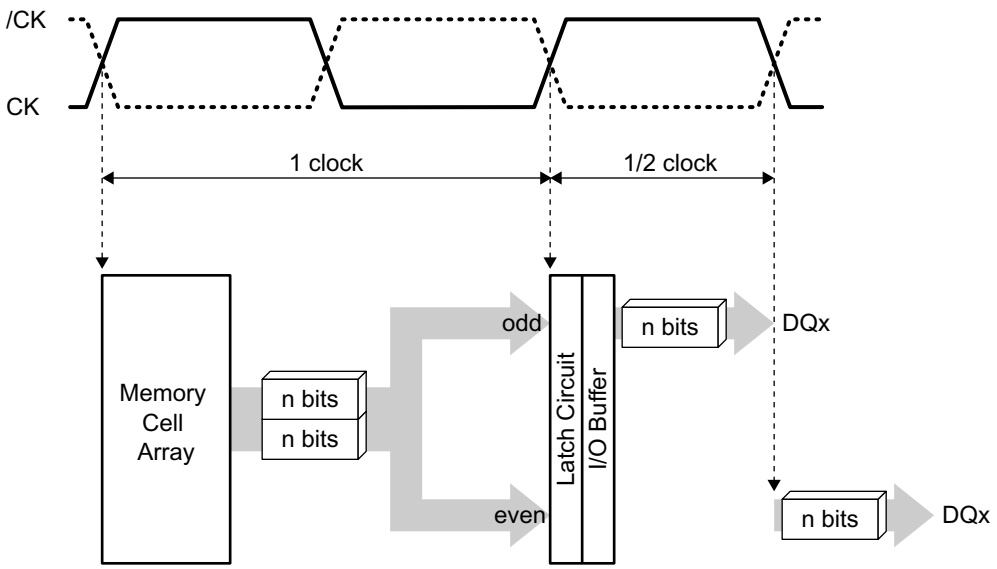
The 2-bit prefetch architecture is explained here using the read cycle as an example.

In this architecture, 2n bits of data are transferred from the memory cell array to the I/O buffer every clock. Data transferred to the I/O buffer is output n bits at a time every half clock (both rising and falling edges of the clock (CK)).

As the internal bus width is twice the external bus width, DDR SDRAM achieves a data output rate that is twice the data rate of the internal bus.

Because data is accessed in 2-bit pairs, only burst lengths of 2, 4, and 8 are supported for DDR SDRAM.

Figure 1-1. 2-Bit Prefetch Architecture



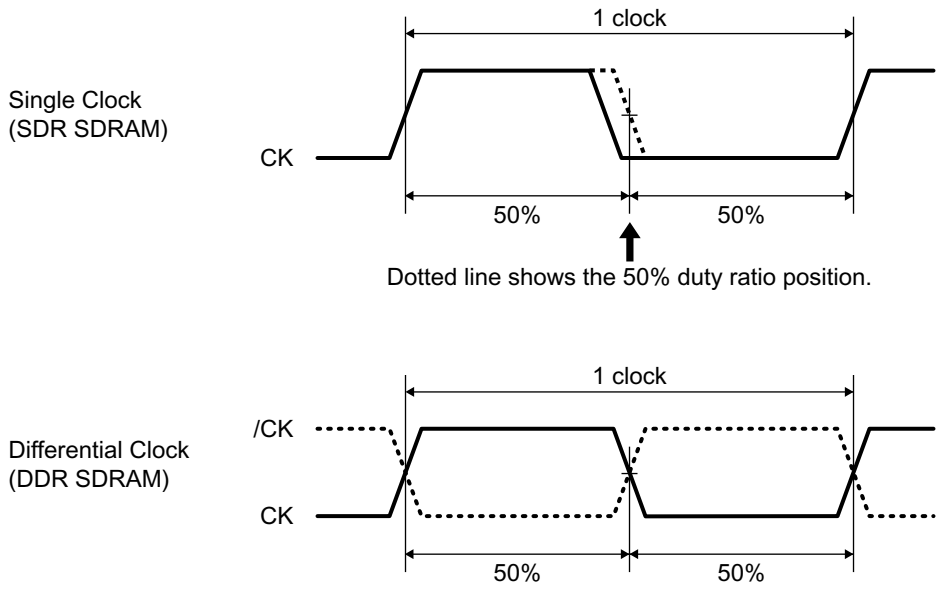
1.1.2 Clock input

Due to the influence of various factors, the high-level period and low-level period of the clock input may not be the same (the duty ratio may not be 50%).

In the case of SDR SDRAM, for which data input/output is only synchronized with the rising edges of the clock, there is some margin in the timing. However, in the case of DDR SDRAM, for which data input/output is synchronized with both the rising and falling edges of the clock, it is difficult to accurately control the data input/output timing based on the conventional single clock.

Therefore, DDR SDRAM adopts a differential clock scheme that enables accurate memory control.

Figure 1-2. Clock Input



/CK is an input signal that has the same clock period but the reverse phase of CK. The high-level period and low-level period can be made equal by using the intersection of CK and /CK as an input reference level. In the case of DDR SDRAM, data input/output is synchronized with both the rising and falling edges of the data strobe signal (DQS), which has the same period as clock input CK.

Employing a differential clock scheme enables DDR SDRAM to support a higher clock frequency and limit the negative influence of noise and other factors.

1.1.3 Data strobe signal (DQS)

Similarly to SDR SDRAM, DDR SDRAM is controlled by command input at the rising edge of the clock (CK), but the data input/output timing differs from that of SDR SDRAM. To achieve high-speed data transfer, DDR SDRAM adopts a data strobe signal (DQS). DQS is output from the device and received by the receiver, which adjusts the data (DQ) capture timing using DQS. For details, refer to **CHAPTER 9 DATA STROBE SIGNAL (DQS) CONTROL OPERATION**.

1.1.4 Interface

DDR SDRAM employs the JEDEC-compliant SSTL_2 (Stub Series Terminated Logic for 2.5V) interface to eliminate the signal degradation caused by noise and reflection produced as a result of a high operating frequency.

SSTL-2 is a low-voltage (2.5V), small-amplitude and high-speed interface that reduces the effect of reflection by connecting series resistance between the signal branch point from the bus (stub) and the memory.

(1) Stub resistance

A stub resistance of approximately 25Ω (22Ω is generally used for DIMMs (Dual In-Line Memory Modules)) is connected in series to the output pin (V_{OUT}), providing impedance matching between the transmission line and device output.

(2) Termination voltage

The V_{TT} line is terminated with a resistance of approximately 25Ω (27Ω is generally used for DIMMs). This termination suppresses signal reflection in the transmission line and also reduces voltage spikes, enabling high-speed data transmission.

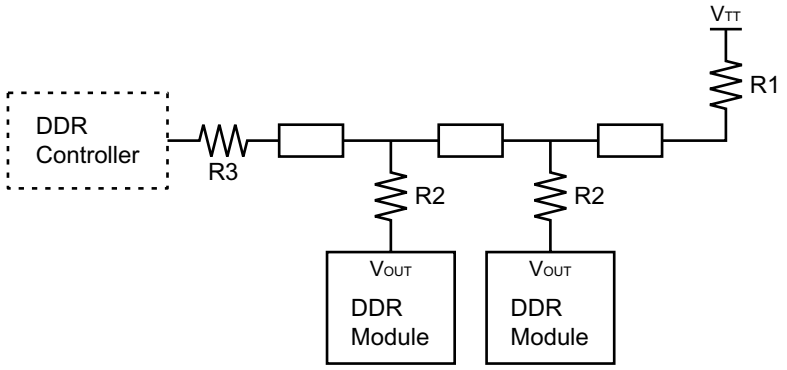
(3) Reference voltage

The SSTL_2 interface is symmetrical with respect to high-level and low-level output. V_{REF} is used as a reference voltage to detect high and low levels.

(4) Interface specification

DDR SDRAM generally uses the SSTL_2 interface with termination at one end.

Figure 1-3. SSTL_2 Interface (case of DIMM)



R1: Termination resistance (27Ω)
R2: Stub resistance (22Ω) (Mounted on DIMM)
R3: (22Ω)
V_{TT} = 1/2 $V_{DD}Q$

Table 1-2. SSTL_2 Interface Specifications

Item	Symbol	MIN.	TYP.	MAX.	Unit
Power supply	V_{DD}	2.3	2.5	2.7	V
DQ power supply	$V_{DD}Q$	2.3	2.5	2.7	V
SSTL_2 reference voltage	V_{REF}	0.49 $V_{DD}Q$	0.5 $V_{DD}Q$	0.51 $V_{DD}Q$	V
Termination voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
High-level input voltage (DC specifications)	V_{IH} (DC)	V_{REF} + 0.18		V_{REF} + 0.30	V
Low-level input voltage (DC specifications)	V_{IL} (DC)	-0.30		V_{REF} – 0.18	V
High-level input voltage (AC specifications)	V_{IH} (AC)	V_{REF} + 0.35			V
Low-level input voltage (AC specifications)	V_{IL} (AC)			V_{REF} – 0.35	V

Remark These specifications may differ depending on the product. For details, refer to the corresponding data sheet of each DDR SDRAM.

1.1.5 Power supply

Compared to the 3.3V power supply of SDR SDRAM, the power supply of DDR SDRAM is 2.5V. This reduction in power supply voltage reduces the power consumption of the DDR SDRAM circuits.

1.1.6 /CAS read latency, /CAS write latency, burst length, and burst sequence

Similarly to SDR SDRAM, DDR SDRAM has mode register set commands for the latency, burst length, and burst sequence. Refer to **CHAPTER 5 MODE REGISTER SET**.

1.1.7 Use of DLL

DDR SDRAM is provided with a DLL (Delay Locked Loop) circuit. The DLL circuit is designed to realize a fast access time and high operation frequencies by controlling and adjusting the time lag between the external clock and internal clock. Refer to **2.3 Block Diagram**.

1.1.8 Data mask

DDR SDRAM uses a DQ write mask enable signal (DM) which masks write data. SDR SDRAM can mask both read and write data, but the read mask is not supported by DDR SDRAM. For details about the DM control operation, refer to **CHAPTER 10 DQ WRITE MASK ENABLE SIGNAL (DM) CONTROL OPERATION**.

1.2 Differences in Commands

Similarly to SDR SDRAM, DDR SDRAM is controlled by commands, but the commands supported by DDR SDRAM differ from those supported by SDR SDRAM.

Table 1-3. Differences in Commands

Item	DDR SDRAM	SDR SDRAM
Clock suspend	Invalid	Valid
Full-page burst	Invalid	Valid
Burst stop	Valid only for read operation	Valid
Single write after burst read	Invalid	Valid

1.2.1 Clock suspend

In the case of SDR SDRAM, operation can be suspended by making the clock enable signal (CKE) low during a read or write operation, but in the case of DDR SDRAM, clock suspend is not supported.

1.2.2 Full-page burst

The burst lengths of DDR SDRAM are 2, 4, and 8. Full-page burst is not supported.

1.2.3 Burst stop

In the case of DDR SDRAM, data output is suspended by the burst stop command during a burst read operation, but the burst stop command is not available for a write operation. Instead write data can be masked using the DQ write mask enable signal (DM) during a burst write operation, but read data cannot be masked during a burst read operation.

1.2.4 Single write after burst read

DDR SDRAM does not support single write after burst read. This is because, whereas command input is synchronized only with the rising edge of the clock, data input/output is synchronized with both the rising and falling edges and thus the operation frequency is twice as high.

For details about the commands of DDR SDRAM, refer to **3.2 Command Control** and **CHAPTER 7 COMMAND OPERATIONS**.

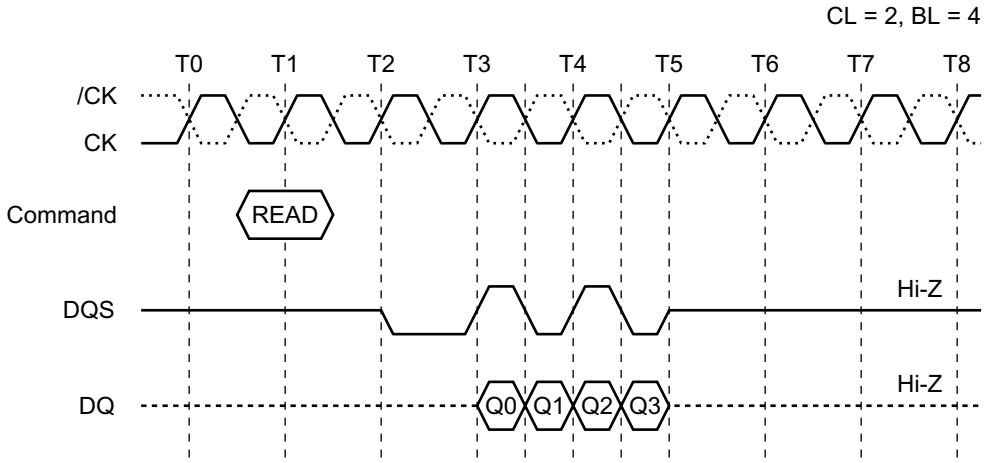
1.3 Differences in Operation Timing

Similarly to SDR SDRAM, DDR SDRAM is controlled by inputting commands at the rising edge of the clock (CK). However, the data input/output timing of DDR SDRAM differs from that of SDR SDRAM.

DDR SDRAM employs a differential clock (CK, /CK) and data strobe signal (DQS) to realize high-speed data transfer. DQS is synchronized with CK, and data input/output (DQ) is synchronized with both the rising and falling edges of DQS.

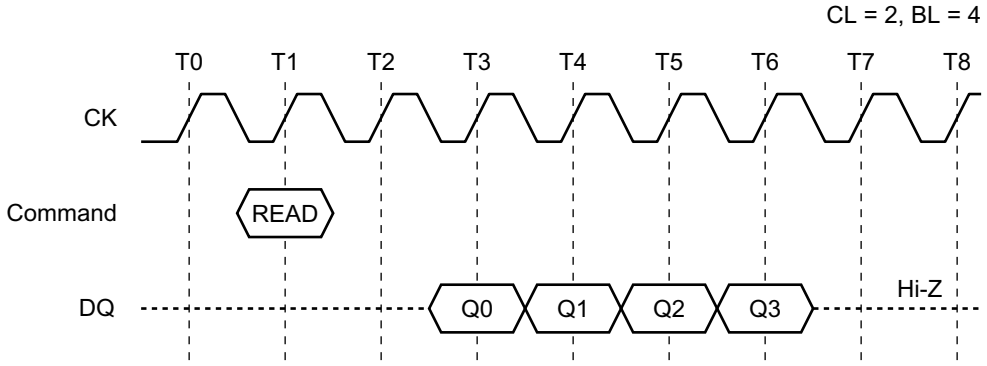
The following examples show the relationship between the clock input of DDR SDRAM/SDR SDRAM, their control signals (commands), and the data input/output timing.

Figure 1-4. DDR SDRAM Read Cycle Timing



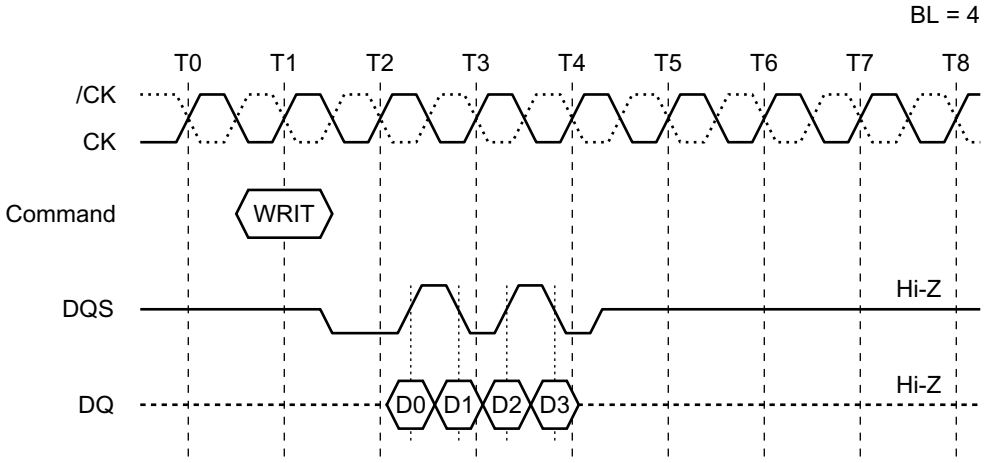
Remark CL: /CAS latency, BL: Burst length

Figure 1-5. SDR SDRAM Read Cycle Timing



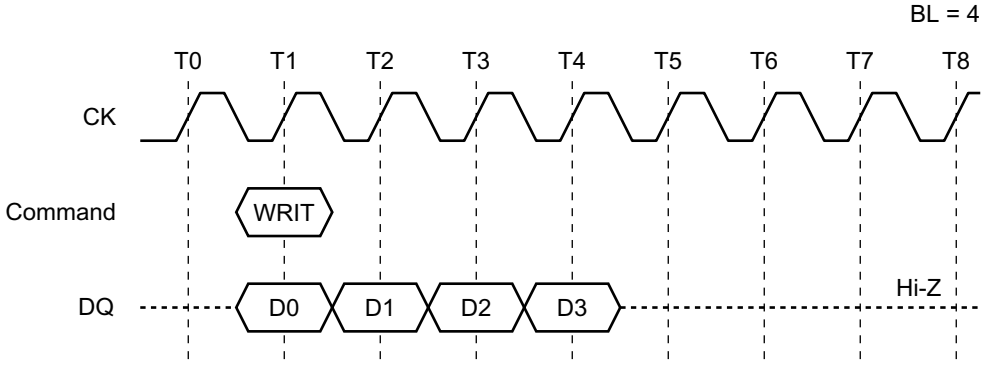
Remark CL: /CAS latency, BL: Burst length

Figure 1-6. DDR SDRAM Write Cycle Timing



Remark BL: Burst length

Figure 1-7. SDR SDRAM Write Cycle Timing



Remark BL: Burst length

CHAPTER 2 PRODUCT OUTLINE

This chapter provides an outline of DDR SDRAM products, taking the EDD1216ALTA 128M bit DDR SDRAM (2M words × 16 bits × 4 banks) as an example. Unless otherwise specified, all the examples use EDD1216ALTA throughout this manual.

2.1 Pin Configurations

This section shows the pin configurations and the pin names of the 128M bit, 256M bit, and 512M bit DDR SDRAM.

Figure 2-1. Pin Configuration of 128M bit DDR SDRAM

x16 (128M bits)	x8 (128M bits)	x4 (128M bits)			x4 (128M bits)	x8 (128M bits)	x16 (128M bits)
V_{DD}	V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}	V_{SS}
DQ0	DQ0	NC	2	65	NC	DQ7	DQ15
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	3	64	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
DQ1	NC	NC	4	63	NC	NC	DQ14
DQ2	DQ1	DQ0	5	62	DQ3	DQ6	DQ13
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	6	61	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
DQ3	NC	NC	7	60	NC	NC	DQ12
DQ4	DQ2	NC	8	59	NC	DQ5	DQ11
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	9	58	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
DQ5	NC	NC	10	57	NC	NC	DQ10
DQ6	DQ3	DQ1	11	56	DQ2	DQ4	DQ9
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	12	55	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
DQ7	NC	NC	13	54	NC	NC	DQ8
NC	NC	NC	14	53	NC	NC	NC
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	15	52	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
LDQS	NC	NC	16	51	DQS	DQS	UDQS
NC	NC	NC	17	50	NC	NC	NC
V_{DD}	V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}	V_{REF}
NC	NC	NC	19	48	V_{SS}	V_{SS}	V_{SS}
LDM	NC	NC	20	47	DM	DM	UDM
/WE	/WE	/WE	21	46	/CK	/CK	/CK
/CAS	/CAS	/CAS	22	45	CK	CK	CK
/RAS	/RAS	/RAS	23	44	CKE	CKE	CKE
/CS	/CS	/CS	24	43	NC	NC	NC
NC	NC	NC	25	42	NC	NC	NC
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10, AP	A10, AP	A10, AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}	V_{SS}

CK, /CK	: Clock inputs
CKE	: Clock enable input
/CS	: Chip select input
/RAS	: Row address strobe input
/CAS	: Column address strobe input
/WE	: Write enable input
A0 to A11	: Address inputs
BA0, BA1	: Bank address inputs
DQ0 to DQx	: Data inputs/outputs
DQS, LDQS, UDQS	: Date strobe inputs/outputs
DM, LDM, UDM	: DQ write mask enable inputs
V_{DD}	: Power supply (for the intermal circuit)
V_{SS}	: Ground (for the intemal circuit)
$V_{DD}Q$	: DQ power supply
$V_{SS}Q$	: DQ ground
V_{REF}	: Referential voltage
NC	: No connection

Remark /xxx indicates active low signal.

Figure 2-2. Pin Configuration of 256M/512M bit DDR SDRAM

x16	x8	x4		x4	x8	x16
V_{DD}	V_{DD}	V_{DD}	1	66	V_{SS}	V_{SS}	V_{SS}
DQ0	DQ0	NC	2	65	NC	DQ7	DQ15
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	3	64	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
DQ1	NC	NC	4	63	NC	NC	DQ14
DQ2	DQ1	DQ0	5	62	DQ3	DQ6	DQ13
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	6	61	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
DQ3	NC	NC	7	60	NC	NC	DQ12
DQ4	DQ2	NC	8	59	NC	DQ5	DQ11
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	9	58	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
DQ5	NC	NC	10	57	NC	NC	DQ10
DQ6	DQ3	DQ1	11	56	DQ2	DQ4	DQ9
$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$	12	55	$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$
DQ7	NC	NC	13	54	NC	NC	DQ8
NC	NC	NC	14	53	NC	NC	NC
$V_{DD}Q$	$V_{DD}Q$	$V_{DD}Q$	15	52	$V_{SS}Q$	$V_{SS}Q$	$V_{SS}Q$
LDQS	NC	NC	16	51	DQS	DQS	UDQS
NC	NC	NC	17	50	NC	NC	NC
V_{DD}	V_{DD}	V_{DD}	18	49	V_{REF}	V_{REF}	V_{REF}
NC	NC	NC	19	48	V_{SS}	V_{SS}	V_{SS}
LDM	NC	NC	20	47	DM	DM	UDM
/WE	/WE	/WE	21	46	/CK	/CK	/CK
/CAS	/CAS	/CAS	22	45	CK	CK	CK
/RAS	/RAS	/RAS	23	44	CKE	CKE	CKE
/CS	/CS	/CS	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10, AP	A10, AP	A10, AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
V_{DD}	V_{DD}	V_{DD}	33	34	V_{SS}	V_{SS}	V_{SS}

x4 (256M/512M bits)

x8 (256M/512M bits)

x16 (256M/512M bits)

CK, /CK	: Clock inputs
CKE	: Clock enable input
/CS	: Chip select input
/RAS	: Row address strobe input
/CAS	: Column address strobe input
/WE	: Write enable input
A0 to A12	: Address inputs
BA0, BA1	: Bank address inputs
DQ0 to DQx	: Data inputs/outputs
DQS, LDQS, UDQS	: Date strobe inputs/outputs
DM, LDM, UDM	: DQ write mask enable inputs
V_{DD}	: Power supply (for the intermal circuit)
V_{SS}	: Ground (for the intemal circuit)
$V_{DD}Q$	: DQ power supply
$V_{SS}Q$	: DQ ground
V_{REF}	: Referential voltage
NC	: No connection

Remark /xxx indicates active low signal.

2.2 Pin Functions

This section explains the pin functions of DDR SDRAM.

2.2.1 Clock input (CK, /CK)

Clock input (CK, /CK) for memory operation. /CK has the same period but the reverse phase of CK.

All input signals except data input/output (DQ), data strobe (DQS), and DQ write mask enable (DM), are synchronized with the rising edge of CK. The intersection of CK and /CK is used as the reference timing for input/output.

2.2.2 Clock enable input (CKE)

The clock enable signal (CKE) determines whether the clock (CK) is valid or not. If CKE is high at the rising edge of a given CK, the next rising edge of CK is valid. Otherwise, the next rising edge of CK is invalid.

(1) Self refresh mode

When the device is in the idle state, self refresh mode is set by issuing the self refresh command (CKE is low). In this mode, CKE must be kept low. For details about self refresh mode control by CKE, refer to **11.2.3 Clock enable signal (CKE) command truth table (128M bit DDR SDRAM (EDD1216ALTA))**.

(2) Power down mode

When the device is in the idle or bank active state, power down mode is set by setting CKE low. In this mode, CKE must be kept low. As refresh is not performed automatically in power down mode, the power down mode period needs to be shorter than the device refresh cycle. For details about power down mode control by CKE, refer to **11.2.3 Clock enable signal (CKE) command truth table (128M bit DDR SDRAM (EDD1216ALTA))**.

2.2.3 Chip select input (/CS)

When the chip select (/CS) is low, command input is valid.

When /CS is high, commands are ignored but the operation continues.

2.2.4 Row address strobe input (/RAS), Column address strobe input (/CAS), Write enable input (/WE)

The row address strobe (/RAS), column address strobe (/CAS), and write enable (/WE) functions are same as those used for SDR SDRAM. Each combination of /RAS, /CAS and /WE in conjunction with chip select (/CS) at the rising edge of the clock (CK) determines the DDR SDRAM operation. For details, refer to **7.1 DDR SDRAM Command Truth Table**.

2.2.5 Address input (A0 to Ax)

(1) Row address

Determined by addresses (A0 to Ax) when an active command is issued.

(2) Column address

Determined by addresses (A0 to Ax) when a read or write command is issued.

(3) Precharge mode select address (AP)

The function differs depending on the input level of the precharge mode select pin (AP) when a precharge or read/write command is issued.

When precharge command is issued

AP	Function
High level	Precharge all banks.
Low level	Precharge only one bank selected by bank addresses (BA0, BA1).

When read/write command is issued

AP	Function
High level	Auto precharge after read/write burst.
Low level	Precharge command is necessary to start precharge.

Table 2-1. Address Pins of 128M bit DDR SDRAM

Part Number	Organization (words x bits x banks)	Address Pins	Row Address	Column Address	AP
EDD1204ALTA	8M x 4 x 4	A0 - A11	A0 - A11	A0 - A9, A11	A10
EDD1208ALTA	4M x 8 x 4	A0 - A11	A0 - A11	A0 - A9	A10
EDD1216ALTA	2M x 16 x 4	A0 - A11	A0 - A11	A0 - A8	A10

2.2.6 Bank Address input (BA0, BA1)

The bank to be selected differs depending on the input level of the bank addresses (BA0, BA1) when a command is input. Read/write or precharge is applied to the bank selected by BA0 and BA1.

Table 2-2. Bank Address and Selected Bank

Selected Bank	BA0	BA1
Bank A	L	L
Bank B	H	L
Bank C	L	H
Bank D	H	H

2.2.7 Data input/output (DQ0 to DQx)

The data input/output (DQ0 to DQx) functions are the same as those used for SDR SDRAM.

2.2.8 Data strobe input/output (DQS, LDQS, UDQS)

Data strobe signals (DQS, LDQS, UDQS) are used to control the I/O buffer. All data input/outputs are synchronized with the rising and falling edges of these signals. x16-bit products use LDQS and UDQS for the lower byte and upper byte respectively.

2.2.9 DQ write mask enable input (DM, LDM, UDM)

DQ write mask enable signals (DM, LDM, UDM) mask write data at both the rising and falling edges of the data strobe signal (DQS). For x16-bit products, LDM and UDM are used to control the lower byte and upper byte respectively.

If DM is high during a write operation, write data is masked. Unlike the DQ mask enable signal used for SDR SDRAM, these signals are not used to control read operations.

2.2.10 Power supply (for the internal circuit) (V_{DD}, V_{SS})

V_{DD} and V_{SS} are power supply pins for the internal circuit.

2.2.11 Power supply (for DQ) ($V_{DD}Q$, $V_{SS}Q$)

$V_{DD}Q$ and $V_{SS}Q$ are power supply pins for the I/O buffer.

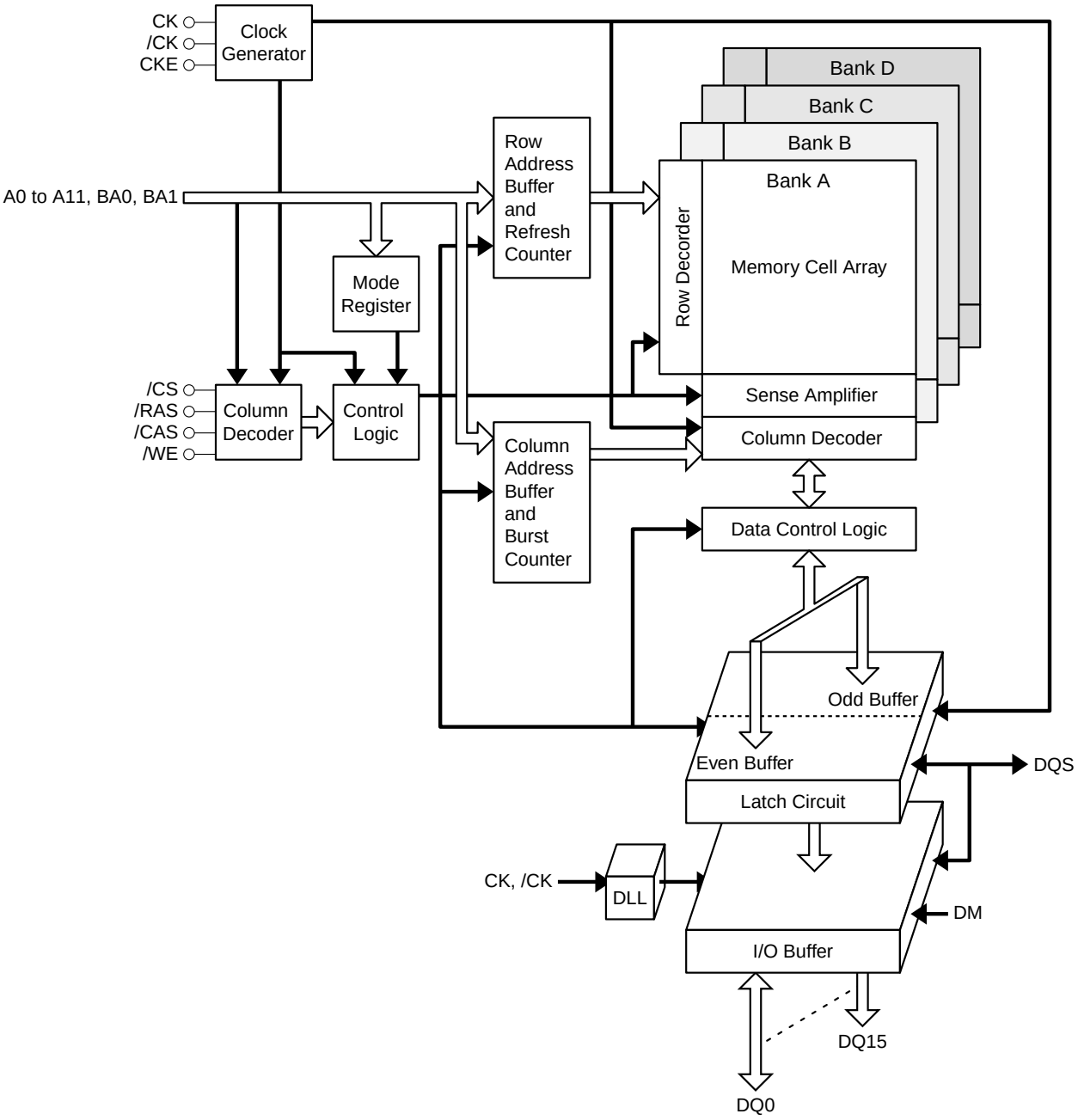
2.2.12 Referential voltage (V_{REF})

V_{REF} is the reference voltage supply pin for the SSTL_2 interface.

2.3 Block Diagram

Following figure shows the block diagram of 128M bit DDR SDRAM (EDD1216ALTA).

Figure 2-3. Block Diagram of 128M bit DDR SDRAM (EDD1216ALTA)

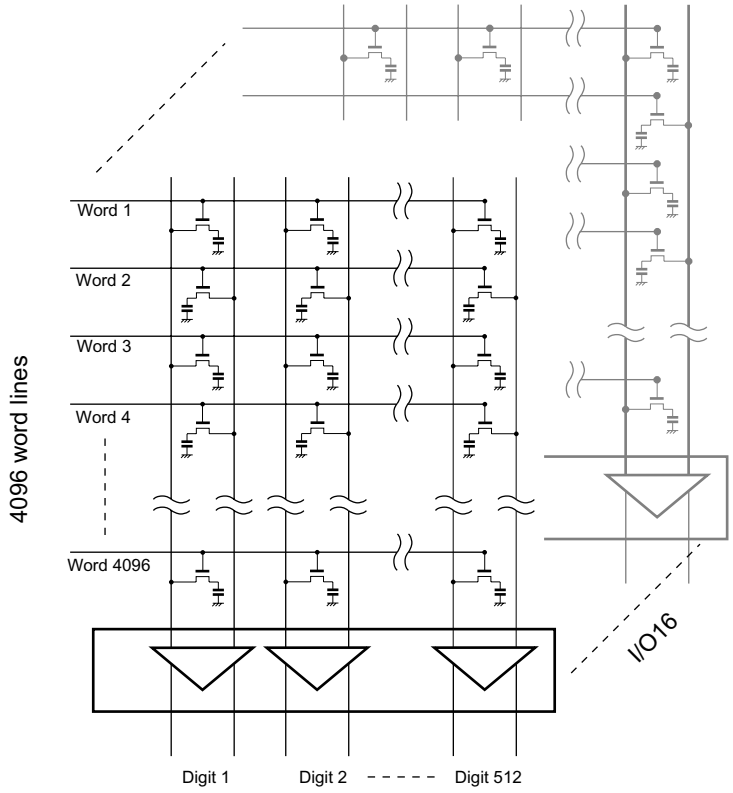


2.3.1 Memory cell array of 128M bit DDR SDRAM (EDD1216ALTA)

A DDR SDRAM memory cell consists of one transistor and one capacitor, like SDR SDRAM.

DDR SDRAM (EDD1216ALTA) has a total capacity of 128M bits and consists of 4096 word lines × 512 digit pairs × 16 I/O lines × 4 banks.

Figure 2-4. Memory Cell Array of 128M bit DDR SDRAM (EDD1216ALTA) (Bank A)



Note The above figure is a conceptual diagram. It may differ from the layout of actual products.

2.3.2 Address decoder (Row address decoder, Column address decoder)

Similar to SDR SDRAM, DDR SDRAM employs the address multiplex method. First, a bank address and a row address are loaded with an active command, and the corresponding word line is selected. Next, a bank address and a column address are loaded with a read or write command, and the corresponding digit line is selected.

2.3.3 I/O buffer

Buffer for data input/output.

2.3.4 Refresh counter

This counter automatically generates row addresses internally.

2.3.5 DLL (Delay Locked Loop)

DDR SDRAM is provided with a DLL (Delay Locked Loop) circuit. The DLL circuit is designed to realize fast access and high operation frequencies by controlling and adjusting the time lag between external and internal clock signals. By employing DLL, timing skew between the clock (CK, /CK) and DQ/DQS is minimized.

CHAPTER 3 PRODUCT FEATURES

Elpida Memory's DDR SDRAM is a JEDEC-compliant 2.5V device with a 133MHz clock frequency (next generation DDR SDRAM supports clock frequencies of 167MHz or more).

This chapter explains following features of DDR SDRAM.

(1) Synchronous operation
(2) Command control
(3) Multibank operation
(4) Burst operation
(5) Access time

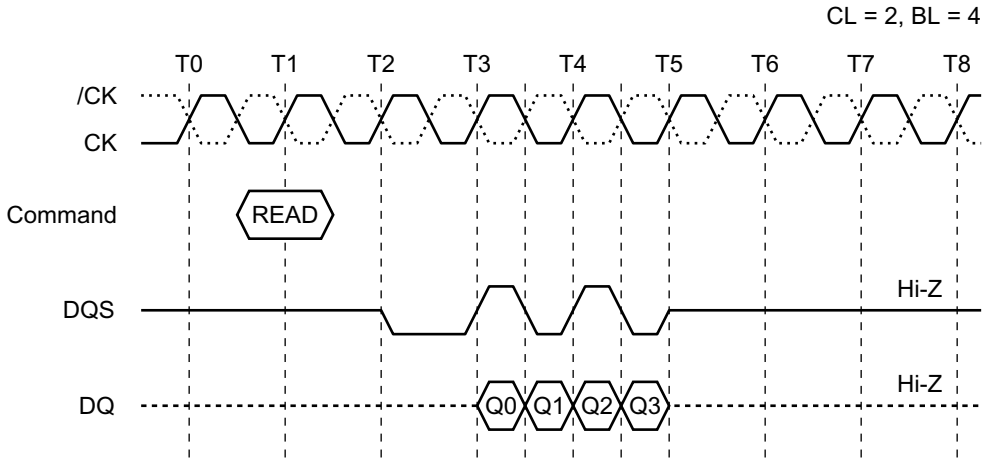
3.1 Synchronous Operation

Each control signal (command) is latched at the rising edge of the clock (CK). Input/output data (DQ) is transmitted along with the data strobe signal (DQS) and captured by the receiver at the rising and falling edges of DQS, thus making it easy to perform high-speed operation.

The following examples show the relationship between the clock input of DDR SDRAM, various control signals, and the data input/output timing.

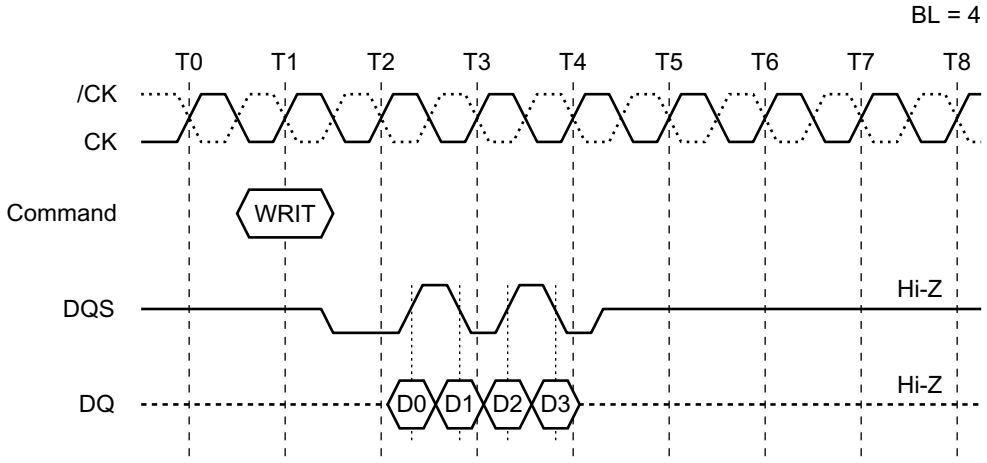
For details about the clock input of DDR SDRAM, refer to **1.1.2 Clock input**, and for details about DQS, refer to **CHAPTER 9 DATA STROBE SIGNAL (DQS) CONTROL OPERATION**.

Figure 3-1. DDR SDRAM Read Cycle Timing



Remark CL: /CAS latency, BL: Burst length

Figure 3-2. DDR SDRAM Write Cycle Timing



Remark BL: Burst length

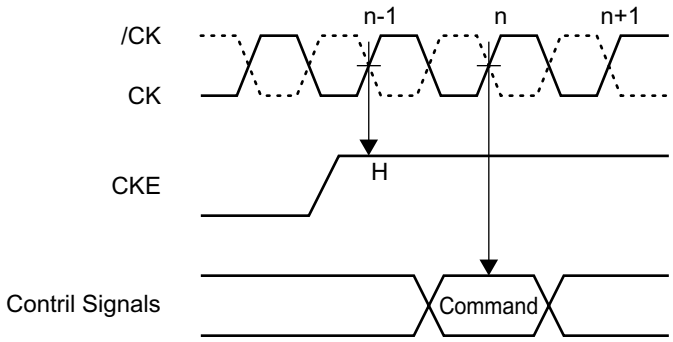
3.2 Command Control

Similar to SDR SDRAM, DDR SDRAM is controlled by commands (combinations of logic levels of control signals). Typical commands include the active command, read command, write command, and precharge command. For further details about the commands of the 128M bit DDR SDRAM, refer to **CHAPTER 7 COMMAND OPERATIONS**.

3.2.1 Command input timing

All the commands are latched in synchronization at the intersection of the rising edge of the clock (CK) and the falling edge of the clock (/CK). A clock enable signal (CKE) is provided as a signal to activate the clock. To input a command at the rising edge of CK "n", CKE must be high 1 cycle before the command input (high at CK " n - 1").

Figure 3-3. Command Input Timing



3.2.2 DDR SDRAM command table

The commands of 128M bit DDR SDRAM are listed below.

Table 3-1. 128M bit DDR SDRAM (×4/×8/×16-bit Organization) Command List

Command	Symbol	Operation
Device deselect	DESL	Device deselect. Current operation continues.
No operation	NOP	No operation. Current operation continues.
Burst stop	BST	Terminate burst read operation.
Read	READ	Start burst read.
Read with auto precharge	READA	Start burst read. After burst read is finished, precharge starts automatically.
Write	WRIT	Start burst write.
Write with auto precharge	WRITEA	Start burst write. After burst write is finished, precharge starts automatically.
Bank active	ACT	Open (or activate) a row in a particular bank for a subsequent access.
Precharge	PRE	Precharge selected bank.
Precharge all banks	PALL	Precharge all banks.
Mode register set	MRS	Mode register set for latency, burst suquence, burst length and DLL reset.
Extended mode register set	EMRS	Select DLL enable/disable.
CBR (auto) refresh	REF	Start CBR (auto) refresh.
Self refresh entry	SELF	Start self refresh.
Self refresh exit	SREX	Exit self refresh.
Power down entry	PWDN	Enter power down mode.
Power down exit	PDEX	Exit power down mode.

Remark Each operation is valid when the current state satisfies the command execution condition. Refer to **6.1 Simplified State Diagram of DDR SDRAM** and **7.2 Command Execution Conditions**.

3.3 MultiBank Operation

Similar to SDR SDRAM, DDR SDRAM has multiple banks, each bank consisting of address decoders, memory cell arrays, and sense amplifiers. Each bank can be controlled independently. Such a configuration is referred to as multibank operation. By using the interleave operation of the bank, even while one bank is being precharged, other bank(s) can be accessed, to achieve better efficiency.

3.3.1 Four-bank configuration

DDR SDRAM has four banks A, B, C, and D, which are selected by bank addresses (BA0, BA1). For details, refer to **2.2.6 Bank Address input (BA0, BA1)**.

This four-bank configuration is outlined below using a comparison with EDO DRAM.

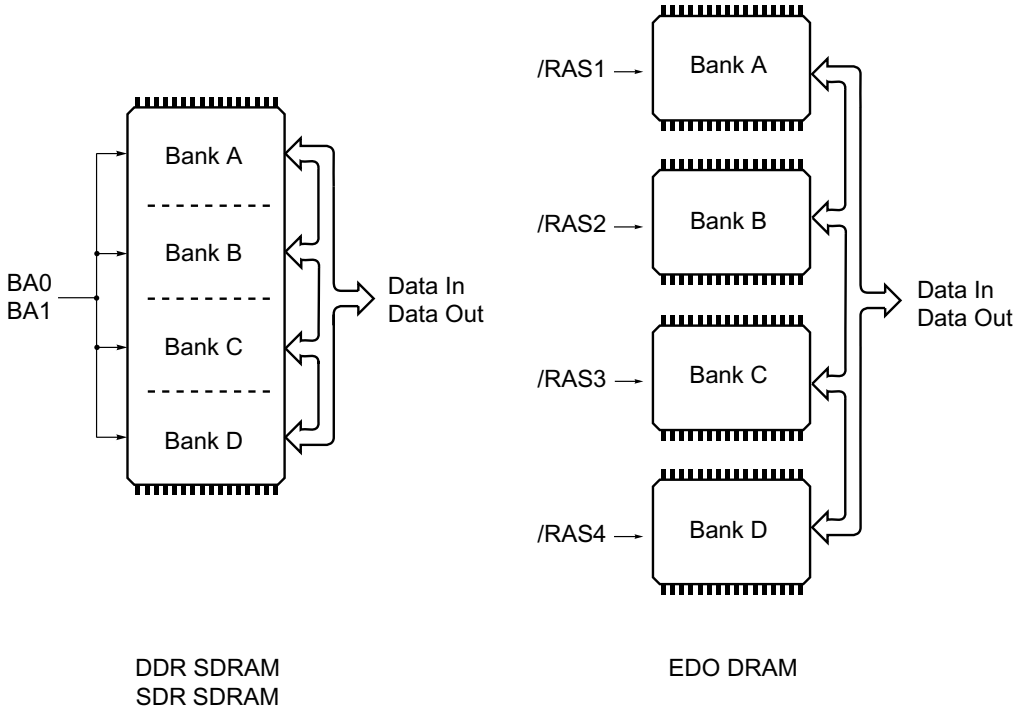
(1) EDO DRAM

To achieve four banks, four devices are necessary. These banks are selected by /RAS signals.

(2) DDR SDRAM/SDR SDRAM

Because DDR SDRAM/SDR SDRAM has four banks internally, four banks can be configured with one device.

Figure 3-4. Four-Bank Configuration



3.3.2 Multibank operations

There are various multibank operations depending on the current state and operations that follow.

(1) Burst read/burst write while burst read/burst write for different bank is in progress

Current State (Bank X)		Next Operation (Bank Y)
Burst read	Completed/Interrupted	Burst read
Burst read	Completed/Interrupted	Burst write
Burst write	Completed/Interrupted	Burst read
Burst write	Completed/Interrupted	Burst write

(2) Activate and burst read/burst write while burst read/burst write for different bank is in progress

Current State (Bank X)		Next Operation (Bank Y)
Burst read	Completed/Interrupted	Bank activate and burst read
Burst read	Completed/Interrupted	Bank activate and burst write
Burst write	Completed/Interrupted	Bank activate and burst read
Burst write	Completed/Interrupted	Bank activate and burst write

(3) Burst read/burst write while burst read/burst write with auto precharge for different bank is in progress

Current State (Bank X)		Next Operation (Bank Y)
Burst read with auto precharge	Completed/Interrupted	Burst read
Burst read with auto precharge	Completed/Interrupted	Burst write
Burst write with auto precharge	Completed/Interrupted	Burst read
Burst write with auto precharge	Completed/Interrupted	Burst write

Caution For the detailed timing charts of the operations described above (sections (1), (2), and (3)), refer to SDR SDRAM User's Manual. All the examples for SDR SDRAM are same as for DDR SDRAM, except /CAS latency and write latency.

3.4 Burst Operation

Since DDR SDRAM performs pipelined processing internally like SDR SDRAM, it can successively input/output a fixed number of data in synchronization with an external clock.

In pipelined architecture, operations from column address input to data input/output are divided into several processing blocks, each block operating in parallel to boost the transfer capability.

Burst transfer in EDO DRAM, SDR SDRAM, and DDR SDRAM is explained below using the read cycle as an example.

(1) EDO DRAM

The next read operation has to wait until a series of operations, from address input to data output, is completed.

(2) SDR SDRAM

A column operation is divided into three processing blocks (Y-decoder, Data amplifier and Output buffer). As each processing block can operate in parallel, each block can start the next process as soon as the current process is finished and handed over to the next processing block. When a column address is input, the internal address counter automatically increments the internal column address in synchronization with the clock (CK). The number of times the column address is incremented is determined by the burst length.

This internal structure enables reading or writing of successive address. Data is continuously output in synchronization with the rising edge of CK.

(3) DDR SDRAM

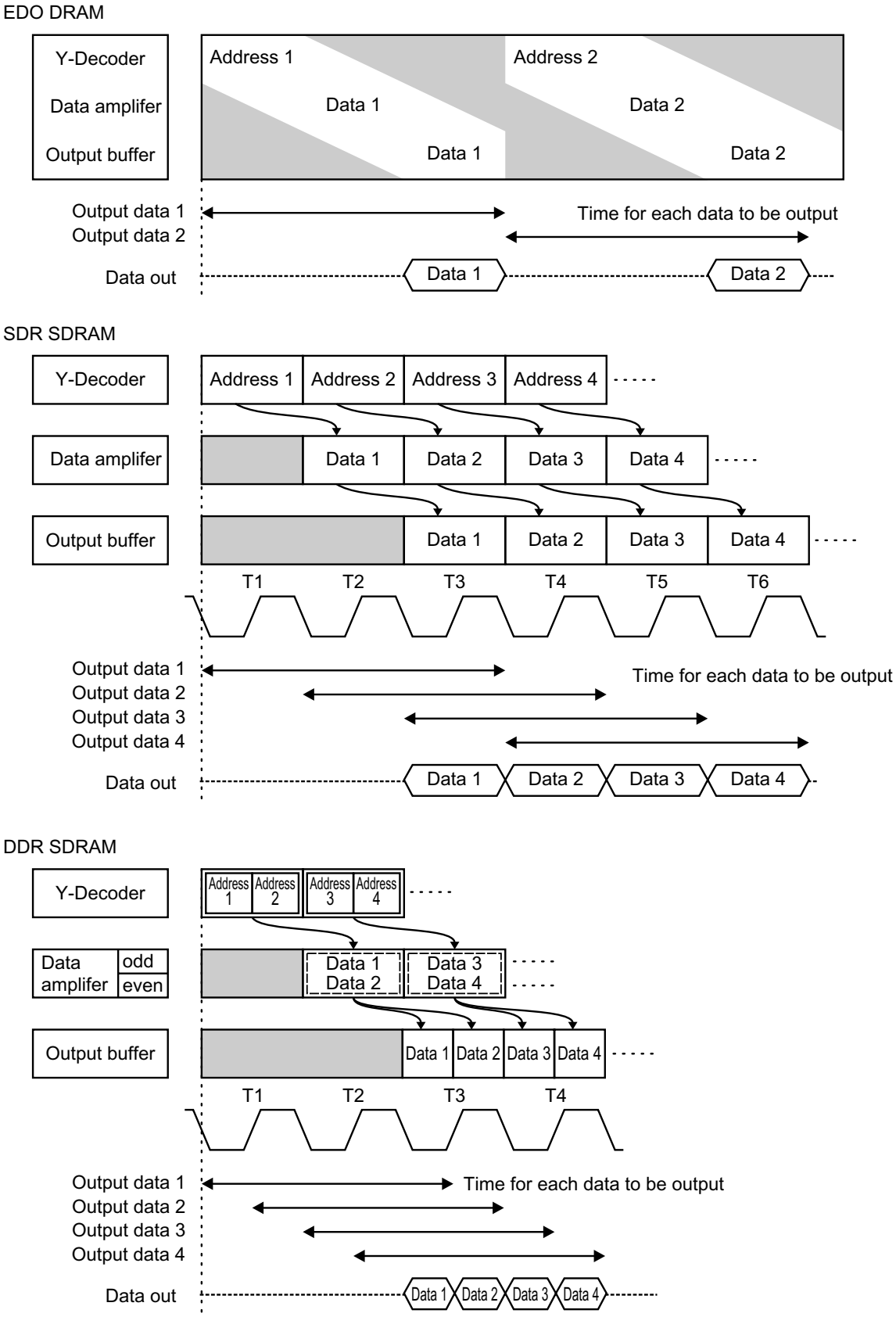
The basic transfer scheme is the same as SDR SDRAM, except that a 2-bit prefetch architecture is employed by DDR SDRAM.

In this architecture, 2n bits of data are transferred from the memory cell array to the I/O buffer every clock cycle. Data transferred to the I/O buffer is output n bits at a time (even and odd addresses) every half-clock cycle. As a result, data is output continuously in synchronization with the rising and falling edges of the clock. For further details about 2-bit prefetch architecture, refer to **1.1.1 Data transfer frequency, data rate**.

(4) Comparison between EDO DRAM, SDR SDRAM and DDR SDRAM

The time required for first data output is almost the same for all these DRAMs. But when it's a successive data access, SDR SDRAM and DDR SDRAM can achieve a faster data transfer rate than EDO DRAM due to the pipelined operation. DDR SDRAM, which uses 2-bit prefetch architecture, achieves an even faster data transfer rate than SDR SDRAM.

Figure 3-5. Burst Operation



3.5 Access Time

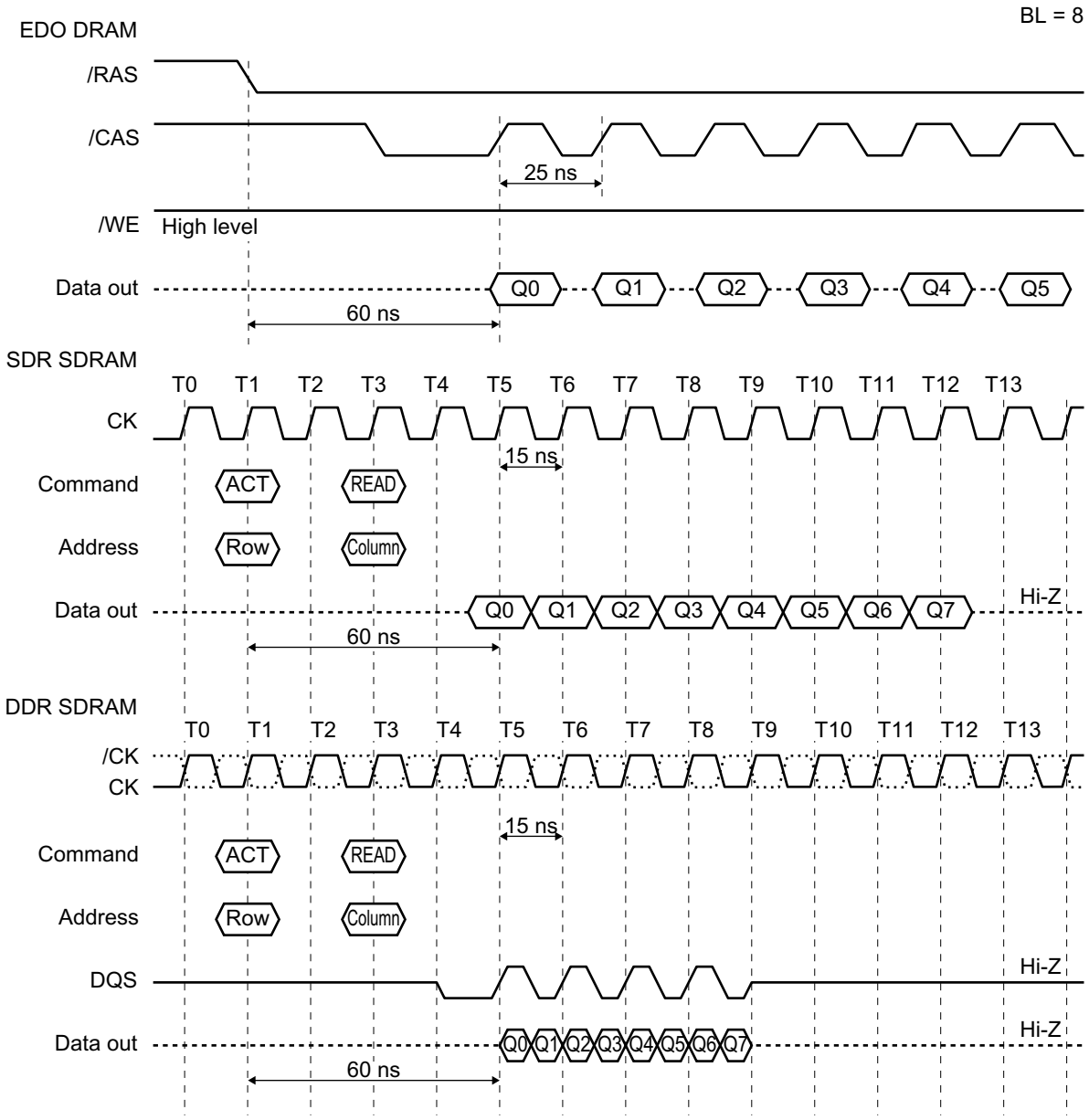
This section compares the access time of EDO DRAM, SDR SDRAM, and DDR SDRAM using the read cycle as an example.

Figure 3-6 shows the burst read cycle of EDO DRAM, SDR SDRAM, and DDR SDRAM, with a burst length of 8 and a clock frequency of 66MHz for SDR SDRAM and DDR SDRAM, and a /RAS access time of 60ns for EDO DRAM.

The first data access (/RAS access time) is approximately 60ns for all the devices, with little difference in time. This is because the internal memory structure is almost the same.

By contrast, as the burst length becomes longer, i.e., the second, third, and fourth data, the data output time difference becomes bigger, for the reason described in section **3.4 Burst Operation**.

Figure 3-6. Burst Read Cycle



Caution EDO DRAM is asynchronous.

Remark BL: Burst length

Figure 3-7. Access Time of DDR SDRAM, SDR SDRAM and EDO DRAM

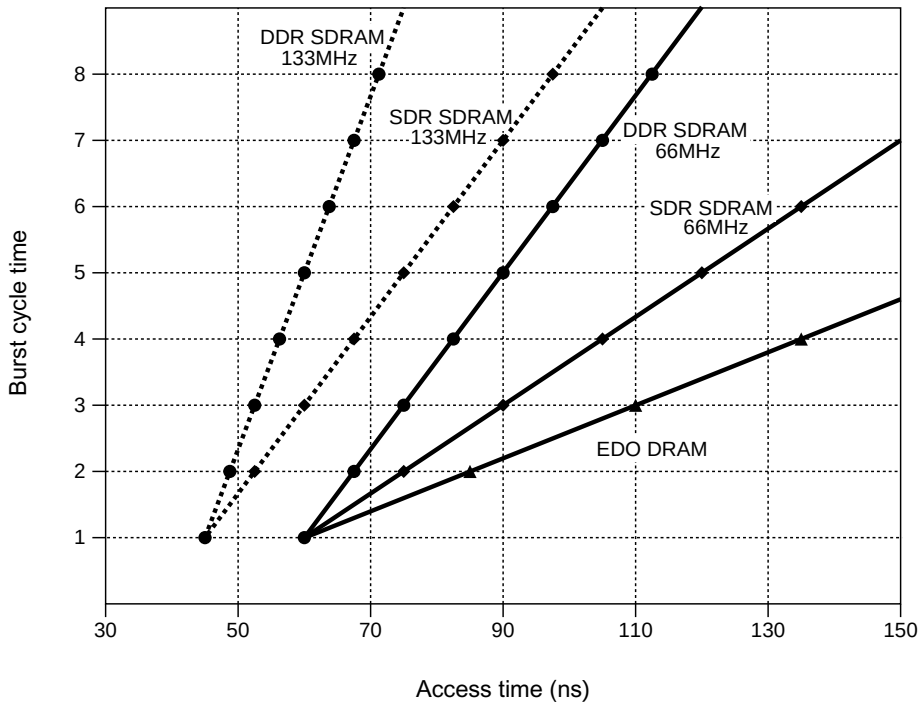


Table 3-2. Access Time of DDR SDRAM, SDR SDRAM and EDO DRAM

Access time	EDO DRAM –60	SDR SDRAM 66 MHz (15 ns)	DDR SDRAM 66 MHz (15 ns)	EDO DRAM –50	SDR SDRAM 100 MHz (10 ns)	DDR SDRAM 100 MHz (10 ns)	SDR SDRAM 133 MHz (7.5 ns)	DDR SDRAM 133 MHz (7.5 ns)
1st access	60 ns			50 ns			45 ns	
2nd access	85 ns	75 ns	67.5 ns	70 ns	60 ns	55 ns	52.5 ns	48.75 ns
3rd access	110 ns	90 ns	75 ns	90 ns	70 ns	60 ns	60 ns	52.5 ns
4th access	135 ns	105 ns	82.5 ns	110 ns	80 ns	65 ns	67.5 ns	56.25 ns
5th access	160 ns	120 ns	90 ns	130 ns	90 ns	70 ns	75 ns	60 ns
6th access	185 ns	135 ns	97.5 ns	150 ns	100 ns	75 ns	82.5 ns	63.75 ns
7th access	210 ns	150 ns	105 ns	170 ns	110 ns	80 ns	90 ns	67.5 ns
8th access	235 ns	165 ns	112.5 ns	190 ns	120 ns	85 ns	97.5 ns	71.25 ns

CHAPTER 4 INITIALIZATION

This chapter explains initialization after power on.

4.1 Initialization after Power On

The logical state of the internal circuit of DDR SDRAM is undefined right after power on. DDR SDRAMs must be powered up and initialized in a predefined manner to ensure correct operation. DDR SDRAM power-on and initialization sequence is as follows.

(1) Apply power first to V_{DD}, then to $V_{DD}Q$, and finally to V_{REF} and V_{TT}.

(2) Keep the clock enable signal (CKE) low in order to guarantee that DQ and DQS pins will be in the high impedance state.

(3) After all power supply and reference voltages are stable, and the clock is stable, wait 200μs before applying an executable command. Once the 200μs delay has been satisfied, a device deselect command (DESL) or no operation command (NOP) must be applied and CKE must be made high.

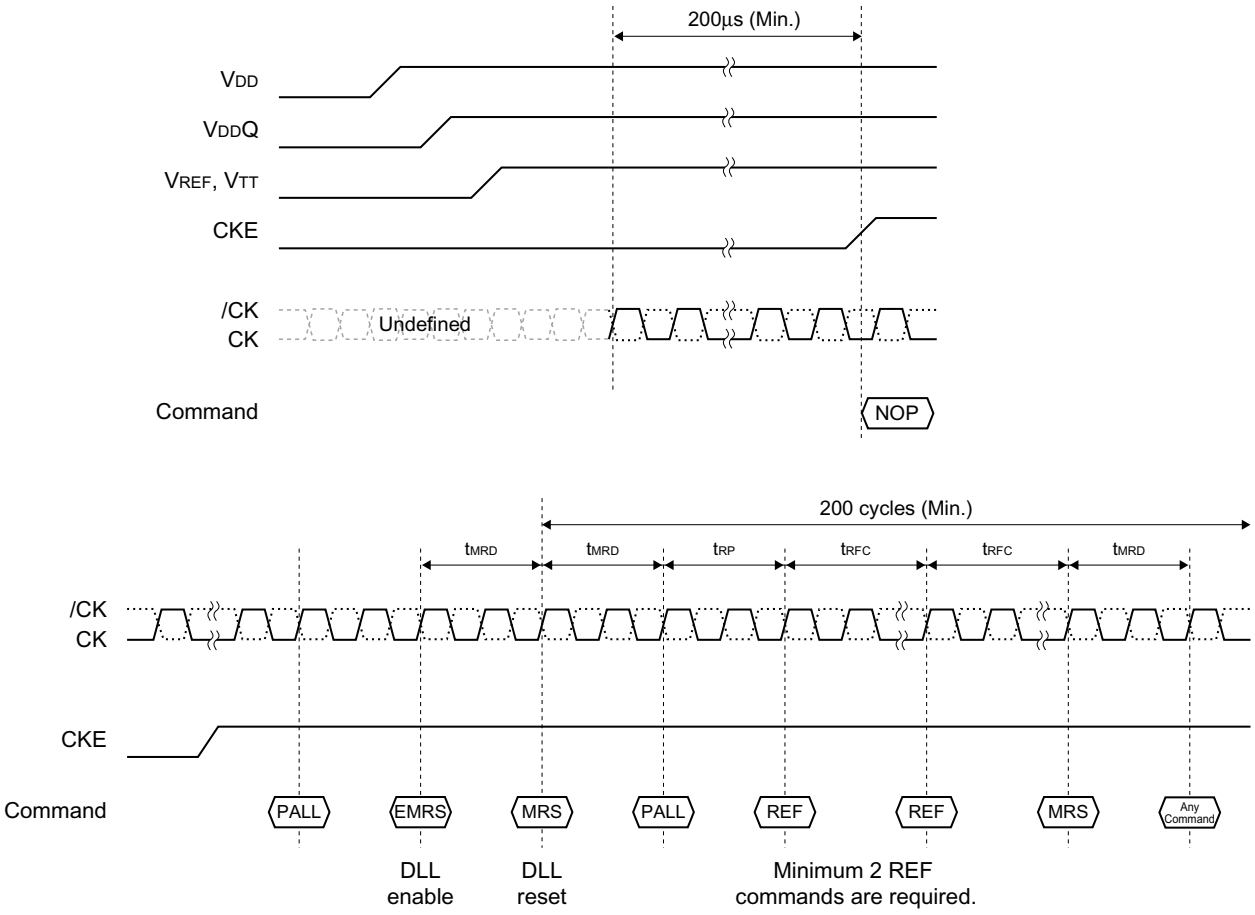
(4) Precharge all banks (the precharge all banks command (PALL) is recommended).

(5) Enable DLL by the extended mode register set command (EMRS). Then reset DLL by the mode register set command (MRS) with A8 high. 200 cycles are required between DLL reset and any read command.

(6) After precharging all the banks again, input two or more CBR (auto) refresh commands (REF).

(7) Input the mode register set command (MRS) to program the operating parameters.

Figure 4-1. Initializing DDR SDRAM



CHAPTER 5 MODE REGISTER SET

5.1 Programming the Mode Register

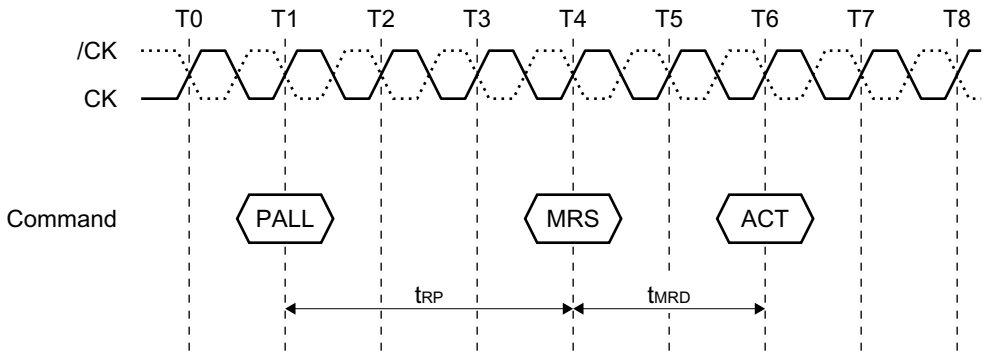
The mode register is used to define various operating parameters of DDR SDRAM, such as the latency mode, burst sequence (wrap type (WT)) and burst length. The extended mode register is used to enable/disable DLL.

The addresses (A0 through Ax) and the bank addresses (BA0, BA1) are used as input data to set the mode register and the extended mode register. Once the parameters are set, these registers retain the stored information until they are reprogrammed or the power is turned off.

(1) Execute the precharge all banks command (PALL) to precharge all banks. After t_{RP}, all banks become idle.

(2) Execute the mode register set command (MRS) and extended mode register set command (EMRS) to program the register.

Figure 5-1. Mode Register/Extended Mode Register Set Cycle



5.2 Parameters

The mode register has the following 5 functions:

(1) A0 through A2 : Burst length
(2) A3 : Burst sequence
(3) A4 to A6 : /CAS latency
(4) A7and A9 through Ax : Option
(5) A8 : DLL reset

The extended mode register has the following 2 functions:

(6) A0 : DLL enable/disable
(7) A1 through A11 : Option

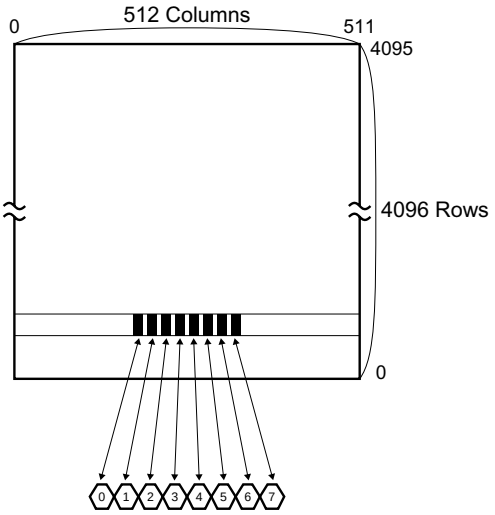
(1) Burst length

The burst length is the number of data that can be successively input or output. DDR SDRAM supports burst lengths of 2, 4 and 8.

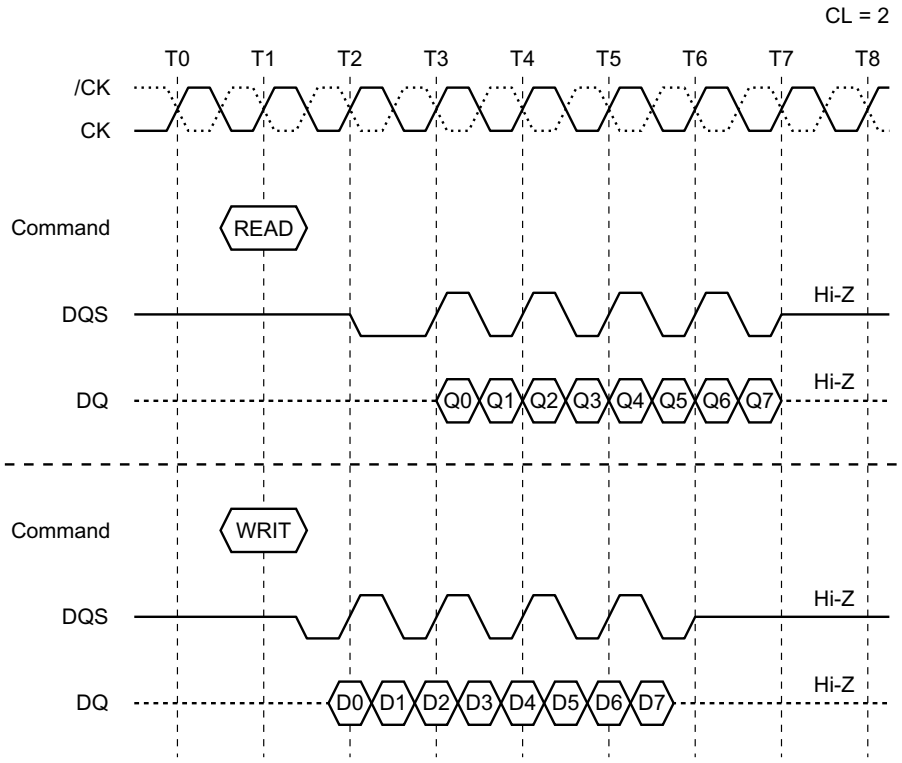
Example 1) Burst length of 8

Data of eight columns can be successively input or output by a single read command (READ) or write command (WRIT). When the burst operation has been completed, the data bus becomes high-impedance.

Figure 5-2. Read/Write Cycle with Burst Length of 8



Eight successive data synchronized with CK are input/output



Remark CL: /CAS latency

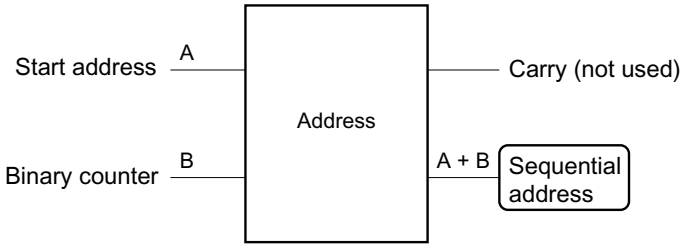
(2) Burst sequence

The burst sequence specifies the order in which the burst data address is incremented.

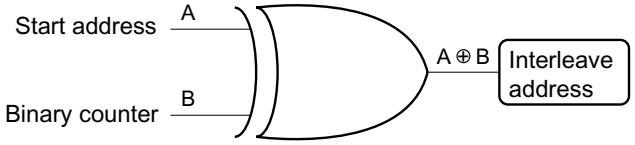
Similarly to SDR SDRAM, DDR SDRAM supports the sequential type and interleave type. When address A3 = 0, the sequential type is selected, when address A3 = 1, the interleave type is selected. Which type is to be selected depends on the type of CPU used in each system.

Figure 5-3. Burst Sequence

Sequential



Interleave



Burst length and burst sequence

The following tables show the start column address and addressing sequence of each burst length.

[Burst length = 2]

Start Address (column address A0, binary)	Sequential Burst Sequence (decimal)	Interleave Burst Sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst length = 4]

Start Address (column address A1 through A0, binary)	Sequential Burst Sequence (decimal)	Interleave Burst Sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

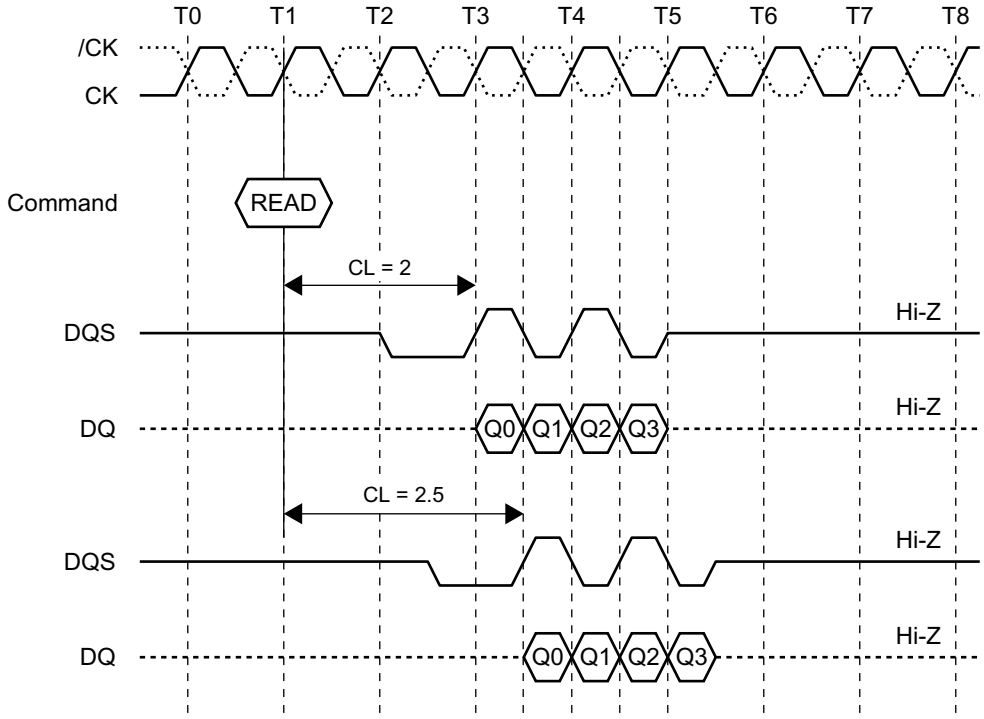
[Burst length = 8]

Start Address (column address A2 through A0, binary)	Sequential Burst Sequence (decimal)	Interleave Burst Sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

(3) /CAS latency

The /CAS latency is the number of clocks required between a read command (READ) and the first data output. The value of /CAS latency is limited by the operating frequency and speed grade of DDR SDRAM. A /CAS latency of 2 or 2.5 is available for DDR SDRAM.

Figure 5-4. Timing Differences between /CAS Latency = 2 and 2.5



Remark CL: /CAS latency

(4) Option

Addresses A7 and A9 through A11 are used for the option fields of the mode register set command.

(5) DLL reset

Address A8 is used to reset DLL when the mode register set command is input.

(6) Extended mode register set

If the bank addresses are BA0, BA1 = 1, 0 when the mode register is set, the device enters the extended mode register set cycle. DLL is enabled/disabled according to the information of address A0 during the cycle.

Although DLL is usually enabled, disabling DLL in the power down mode reduces the power consumption of the device.

(7) Option

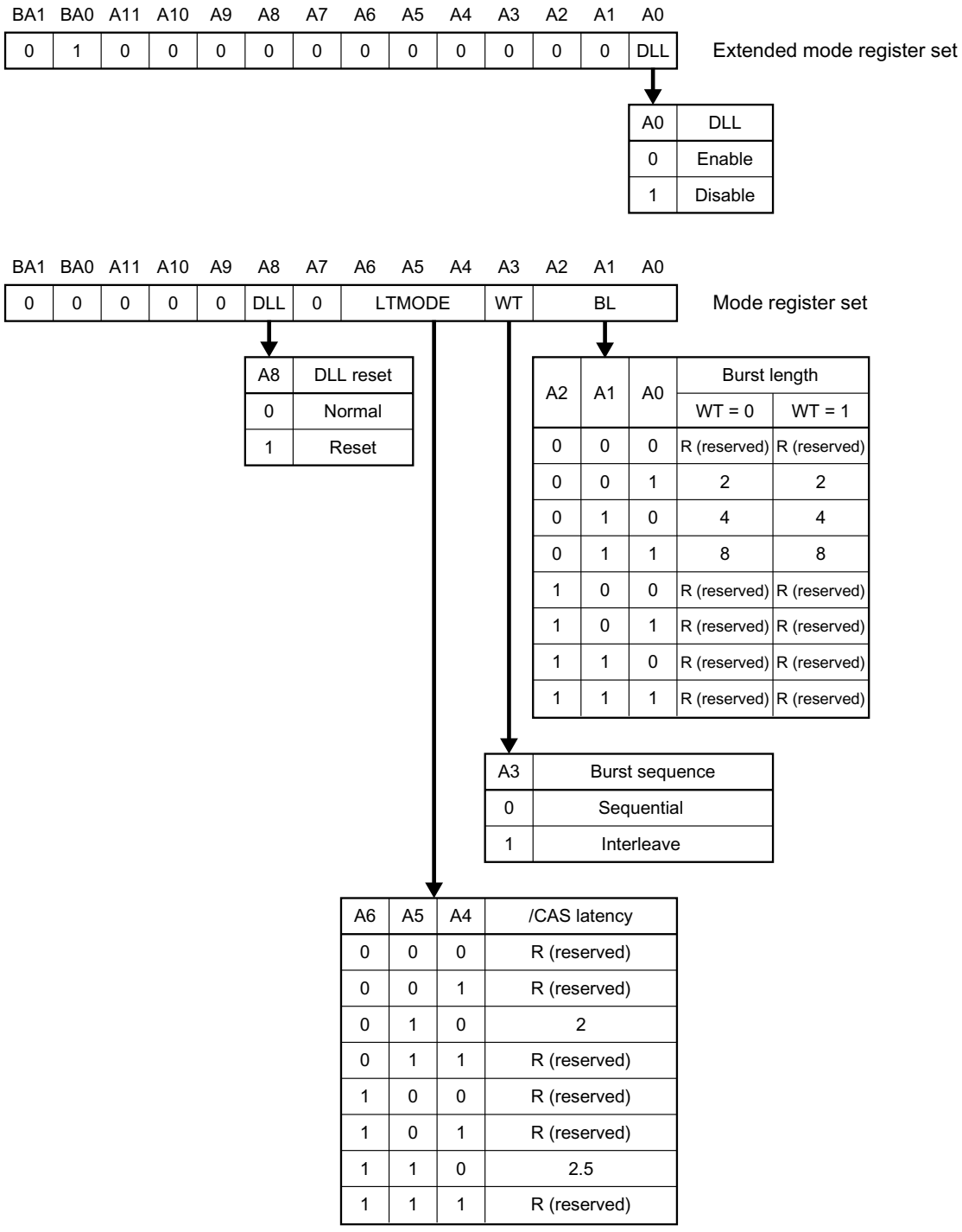
Addresses A1 through A11 are used for the option fields of the extended mode register set command.

5.3 Mode Register and Extended Mode Register Fields (with 128M bit DDR SDRAM)

To set the burst length, burst sequence, and /CAS latency using the mode register set command (MRS), set the option field addresses A7 and A9 through A1 = 0 and bank addresses BA0, BA1 = 0, 0.

To set DLL operation mode using the extended mode register set command (EMRS), set bank addresses BA0, BA1 = 1, 0.

Figure 5-5. Mode Register and Extended Mode Register fields (with 128M bit DDR SDRAM)

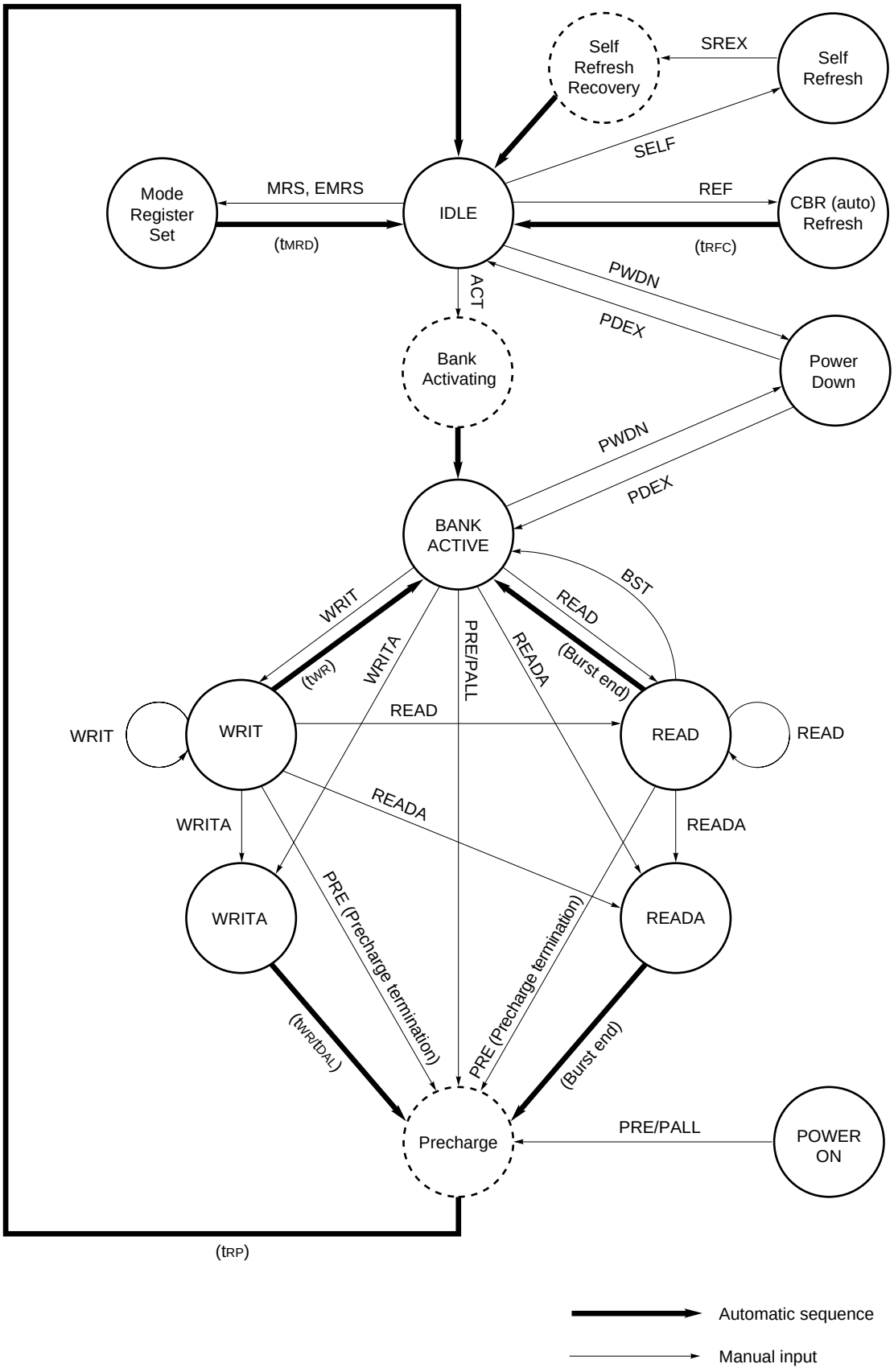


CHAPTER 6 SIMPLIFIED STATE DIAGRAM

6.1 Simplified State Diagram of DDR SDRAM

Figure 6-1 shows a simplified state diagram of DDR SDRAM. Circles in the figure indicate the current state, and arrows indicate the allowable transition.

Figure 6-1. Simplified State Diagram of 128M bit DDR SDRAM (EDD1216ALTA)



6.2 Current State Definition

6.2.1 Idle (IDLE)

The state in which the bank has been precharged and t_{RP} has been satisfied. The bank active command (ACT), mode register set command (MRS, EMRS) and refresh command (REF, SELF) may only be issued when the device or the bank to be selected is in the idle state.

6.2.2 Bank activating (Row activating)

For an operation (read or write) for a particular row in a particular bank, the bank has to be activated first to receive an operation request (read or write command).

Bank activating is the state in which the bank active command (ACT) has been issued but t_{RCD} has not been satisfied. The device automatically changes states from bank activating to bank active when t_{RCD} is satisfied.

6.2.3 Bank active (BANK ACTIVE) (Row active)

When t_{RCD} is satisfied (bank active), the device is ready to receive an operation request (read or write command).

6.2.4 Precharge

When current operation (read or write) is finished, the bank has to be idle state at first to activate a different row in the bank. To return to the idle state, the precharge command (PRE, PALL) has to be issued.

Precharge is the state in which the precharge command has been issued but t_{RP} has not been satisfied. As mentioned in **6.2.1 Idle (IDLE)**, the bank will return to idle state when t_{RP} is satisfied.

6.2.5 Read and write (READ, WRIT)

The state in which a read or write operation is in progress. By issuing the read or write command (READ, WRIT) along with a column address for the active bank, the read or write operation will start.

When the operation is completed, the bank automatically returns to the bank active state.

6.2.6 Read and write with auto precharge (READA, WRITA)

When the read or write with auto precharge command (READA, WRITA) is issued, the device automatically starts precharging and the bank returns to the idle state after the read or write operation is completed.

6.2.7 Mode register set

The mode register set or extended mode register set command (MRS, EMRS) can only be issued when all banks of the device are in the idle state. When data has been written to the mode register, the device automatically returns to the idle state after t_{MRD}.

6.2.8 CBR (Auto) refresh

The CBR (auto) refresh command (REF) can only be issued when all banks of the device are in the idle state. When the REF command is issued, a certain row address of every bank is selected, and refresh is executed. When CBR (auto) refresh is completed, the device automatically returns to the idle state after t_{RFC}.

6.2.9 Self refresh

The self refresh command (SELF) can only be issued when all banks of the device are in the idle state. In the self refresh state, the device automatically performs refresh. It is not necessary to execute the refresh command externally.

6.2.10 Self refresh recovery

The state in which the self refresh exit command (SREX) has been issued but t_{XSNR} has not been satisfied. The device automatically returns to the idle state after t_{XSNR}.

6.2.11 Power down

When the clock enable signal (CKE) is made low in the idle state or bank active state, power down mode is set. In this mode, all input buffers except clock (CK, /CK) and CKE are turned off to reduce the power consumption of the device.

To return to the original state (idle or active), CKE must return to high.

CHAPTER 7 COMMAND OPERATIONS

7.1 DDR SDRAM Command Truth Table

The command truth table of DDR SDRAM is shown below.

Table 7-1. 128M bit DDR SDRAM (×4/×8/×16-bit Organization) Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Address			
		n – 1	n					BA0	BA1	A10	A0 - A9, A11
Device deselect	DESL	H	X	H	X	X	X	X		X	X
No operation	NOP	H	X	L	H	H	H	X		X	X
Burst stop	BST	H	X	L	H	H	L	X		X	X
Read	READ	H	X	L	H	L	H	V		L	V
Read with auto precharge	READA									H	
Write	WRIT	H	X	L	H	L	L	V		L	V
Write with auto precharge	WRITEA									H	
Bank active	ACT	H	X	L	L	H	H	V		V	V
Precharge selected bank	PRE	H	X	L	L	H	L	V		L	X
Precharge all banks	PALL							X		H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	L	V
Extended mode register set	EMRS							H	L	L	V
CBR (auto) refresh	REF	H	H	L	L	L	H	X		X	X
Self refresh entry	SELF	H	L								
Self refresh exit	SREX	L	H	H	X	X	X	X		X	X
				L	H	H	X	X		X	X
Power down entry	PWDN	H	L	H	X	X	X	X		X	X
				L	H	H	X	X		X	X
Power down exit	PDEX	L	H	H	X	X	X	X		X	X
				L	H	H	X	X		X	X

Remark H: High level, L: Low level, ×: High or low level (Don't care), V: Valid data

7.2 Command Execution Conditions

The state in which each command can be executed is shown below. Also refer to **6.1 Simplified State Diagram of DDR SDRAM** and **6.2 Current State Definition**.

Table 7-2. Command Executable Condition

Command	Symbol	Command Executable Condition (current state)
Device deselect	DESL	All state.
No operation	NOP	All state.
Burst stop	BST	During read or write operation.
Read	READ	Selected bank is active (t_{RCD} after active command).
Read with auto precharge	READA	Selected bank is active (t_{RCD} after active command).
Write	WRIT	Selected bank is active (t_{RCD} after active command).
Write with auto precharge	WRITA	Selected bank is active (t_{RCD} after active command).
Bank active	ACT	Selected bank is idle.
Precharge selected bank	PRE	Selected bank is active (t_{RAS} after active command).
Precharge all banks	PALL	All banks are active (t_{RAS} after active command).
Mode register set	MRS	All banks are idle.
Extended mode register set	EMRS	All banks are idle.
CBR (auto) refresh	REF	All banks are idle.
Self refresh entry	SELF	All banks are idle.
Self refresh exit	SREX	Self refresh.
Power down entry	PWDN	Idle or bank active.
Power down exit	PDEX	Power down.

7.3 Command Operation of 128M bit DDR SDRAM (EDD1216ALTA)

This section describes the command operations in 128M bit DDR SDRAM.

Current state: Idle

Input Command	Action	Note
DESL	No operation or power down	
NOP	No operation or power down	
BST	Illegal	**Note 1**
READ/READA	Illegal	**Note 1**
WRIT/WRITA	Illegal	**Note 1**
ACT	Bank activating	
PRE/PALL	No operation	**Note 2**
REF/SELF	CBR (auto) refresh or self refresh	**Note 3**
MRS	Mode register set	**Note 3**
EMRS	Extended mode register set	**Note 3**

Notes 1. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

2. Precharge may be enabled depending on the state of the bank specified by the bank addresses (BA0, BA1).

3. Illegal if there is a bank that is not idle.

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Bank active

Input Command	Action	Note
DESL	No operation	
NOP	No operation	
BST	Illegal	**Note 1**
READ/READA	Begin read/read with auto precharge	
WRIT/WRITA	Begin write/write with auto precharge	
ACT	Illegal	**Note 1**
PRE/PALL	Precharge (selected bank/all banks)	**Note 2**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Notes 1. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

2. Illegal if t_{RAS} is not satisfied.

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Read

Input Command	Action	Note
DESL	No operation (Bank active after burst end)	
NOP	No operation (Bank active after burst end)	
BST	Burst stop → Bank active	**Note 1**
READ/READA	Burst stop → Start new read/read with auto precharge	**Note 1**
WRIT/WRITA	Illegal	
ACT	Illegal	**Note 2**
PRE/PALL	Burst stop → Precharge (selected bank/all banks)	**Note 1**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Notes 1. Must satisfy command interval and/or burst interrupt condition.

2. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Write

Input Command	Action	Note
DESL	No operation (Bank active after t_{WR})	
NOP	No operation (Bank active after t_{WR})	
BST	Illegal	
READ/READA	Burst stop → Start read/read with auto precharge	**Note 1**
WRIT/WRITA	Burst stop → Start new write/write with auto precharge	**Note 1**
ACT	Illegal	**Note 2**
PRE/PALL	Burst stop → Precharge (selected bank/all banks)	**Note 1**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Notes 1. Must satisfy command interval and/or burst interrupt condition.

2. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Read with auto precharge

Input Command	Action	Note
DESL	No operation (Precharge after burst end)	
NOP	No operation (Precharge after burst end)	
BST	Illegal	
READ/READA	Illegal	
WRIT/WRITA	Illegal	
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Write with auto precharge

Input Command	Action	Note
DESL	No operation (Idle after t_{DAL})	
NOP	No operation (Idle after t_{DAL})	
BST	Illegal	
READ/READA	Illegal	
WRIT/WRITA	Illegal	
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Precharge

Input Command	Action	Note
DESL	No operation (Idle after t_{RP})	
NOP	No operation (Idle after t_{RP})	
BST	Illegal	**Note 1**
READ/READA	Illegal	**Note 1**
WRIT/WRITA	Illegal	**Note 1**
ACT	Illegal	**Note 1**
PRE/PALL	No operation (Idle after t_{RP})	**Note 2**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Notes 1. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

2. Precharge may be enabled depending on the state of the bank specified by the bank addresses (BA0, BA1).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Bank activating

Input Command	Action	Note
DESL	No operation (Bank active after t_{RCD})	
NOP	No operation (Bank active after t_{RCD})	
BST	Illegal	**Note**
READ/READA	Illegal	**Note**
WRIT/WRITA	Illegal	**Note**
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Write recovery

Input Command	Action	Note
DESL	No operation (Bank active after t_{WR})	
NOP	No operation (Bank active after t_{WR})	
BST	No operation (Bank active after t_{WR})	
READ/READA	Start read/read with auto precharge	
WRIT/WRITA	Start write/write with auto precharge	
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remarks 1. Write recovery: In order to write all burst data to the memory cell correctly, the asynchronous parameter t_{WR} must be satisfied. t_{WR} defines the earliest time that a precharge command can be issued after the last input data.

2. Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Write recovery with auto precharge

Input Command	Action	Note
DESL	No operation (Idle after t_{DAL})	
NOP	No operation (Idle after t_{DAL})	
BST	Illegal	
READ/READA	Illegal	
WRIT/WRITA	Illegal	
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Refresh

Input Command	Action	Note
DESL	No operation (Idle after t_{RFC})	
NOP	No operation (Idle after t_{RFC})	
BST	No operation (Idle after t_{RFC})	**Note 1**
READ/WRIT	Illegal	**Note 1**
ACT	Illegal	**Note 2**
PRE/PALL	Illegal	**Note 2**
REF/SELF	Illegal	
MRS	Illegal	
EMRS	Illegal	

Notes 1. Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

2. Precharge may be enabled depending on the state of the bank specified by the bank addresses (BA0, BA1).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Mode register set

Input Command	Action	Note
DESL	No operation (Idle after t_{MRD})	
NOP	No operation (Idle after t_{MRD})	
BST	Illegal	**Note**
READ/WRIT	Illegal	**Note**
ACT	Illegal	**Note**
PRE/PALL	Illegal	**Note**
REF/SELF	Illegal	**Note**
MRS	Illegal	**Note**
EMRS	Illegal	**Note**

Note Illegal for the same bank (these commands may be valid depending on the state of the bank specified by the bank addresses (BA0, BA1)).

Remark Illegal: Device operation and/or data integrity are not guaranteed.

CHAPTER 8 BASIC OPERATION MODES

This chapter describes the three basic operation modes of DDR SDRAM:

Read mode
Write mode
Refresh mode

8.1 Read Mode

A read operation is executed by issuing the read command (READ) for an active bank. The read operation sequence is as follows.

(1) To activate a particular row in a particular bank, the bank active command (ACT) is issued along with a row address and bank address.

(2) After the lapse of t_{RCD} from the ACT command, the starting column and bank addresses are provided with the READ command.

(3) After the lapse of the /CAS latency from the READ command, the read burst data is available, starting from the column address specified in (2). The number of successive burst data is determined by the burst length (BL).

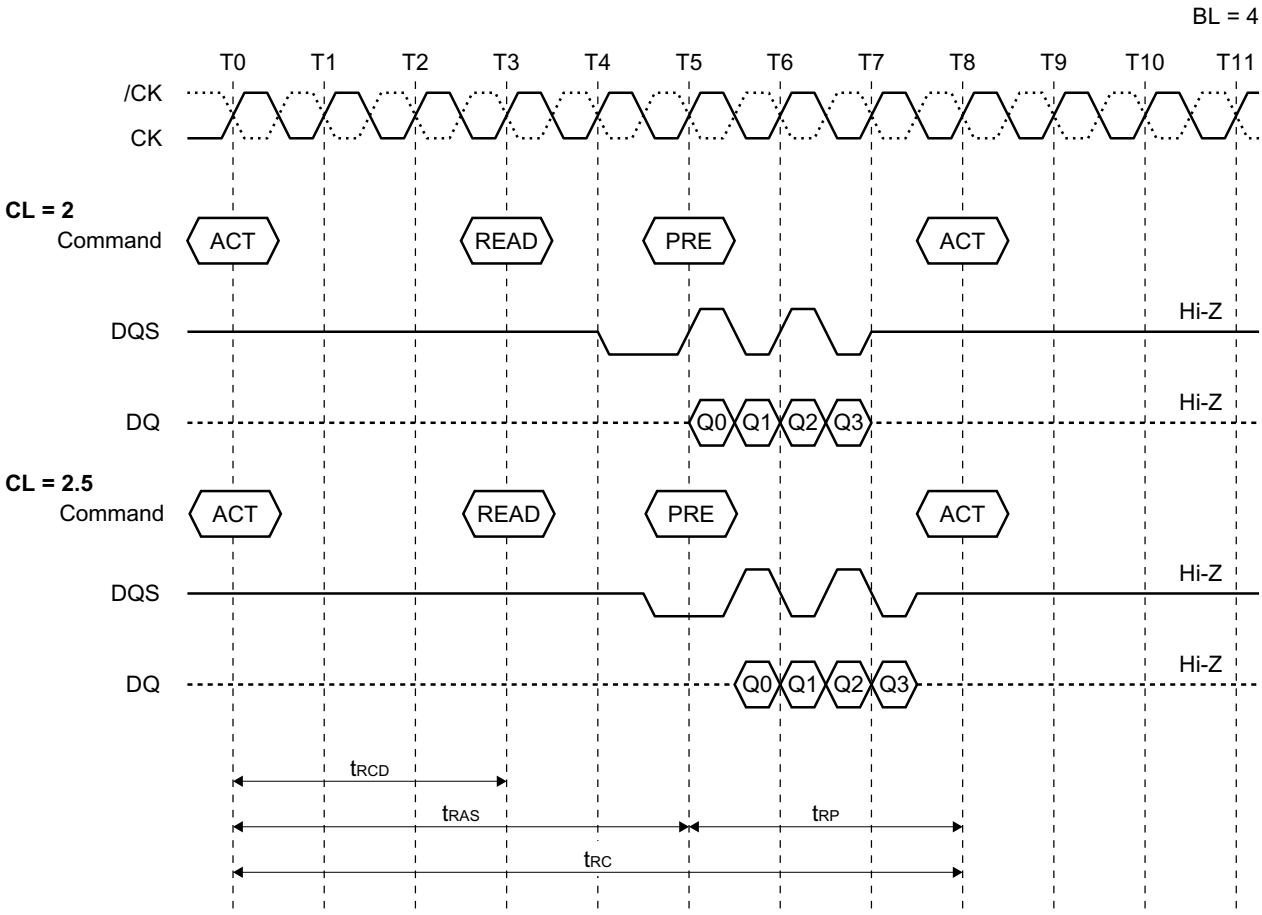
(4) After the lapse of t_{RAS} from the ACT command, the precharge command (PRE) is input. To output all the burst data, the earliest timing for PRE command is (burst length/2) clocks after the READ command.

Caution The precharge command input timing (t_{RAS}) may differ depending on the DDR SDRAM product. For details, refer to the data sheet of each product.

(5) After the lapse of t_{RP}, the corresponding bank becomes idle.

Figure 8-1 shows the basic operation timing chart for the read cycle when the burst length = 4.

Figure 8-1. Read Cycle



Remark CL: /CAS latency, BL: Burst length

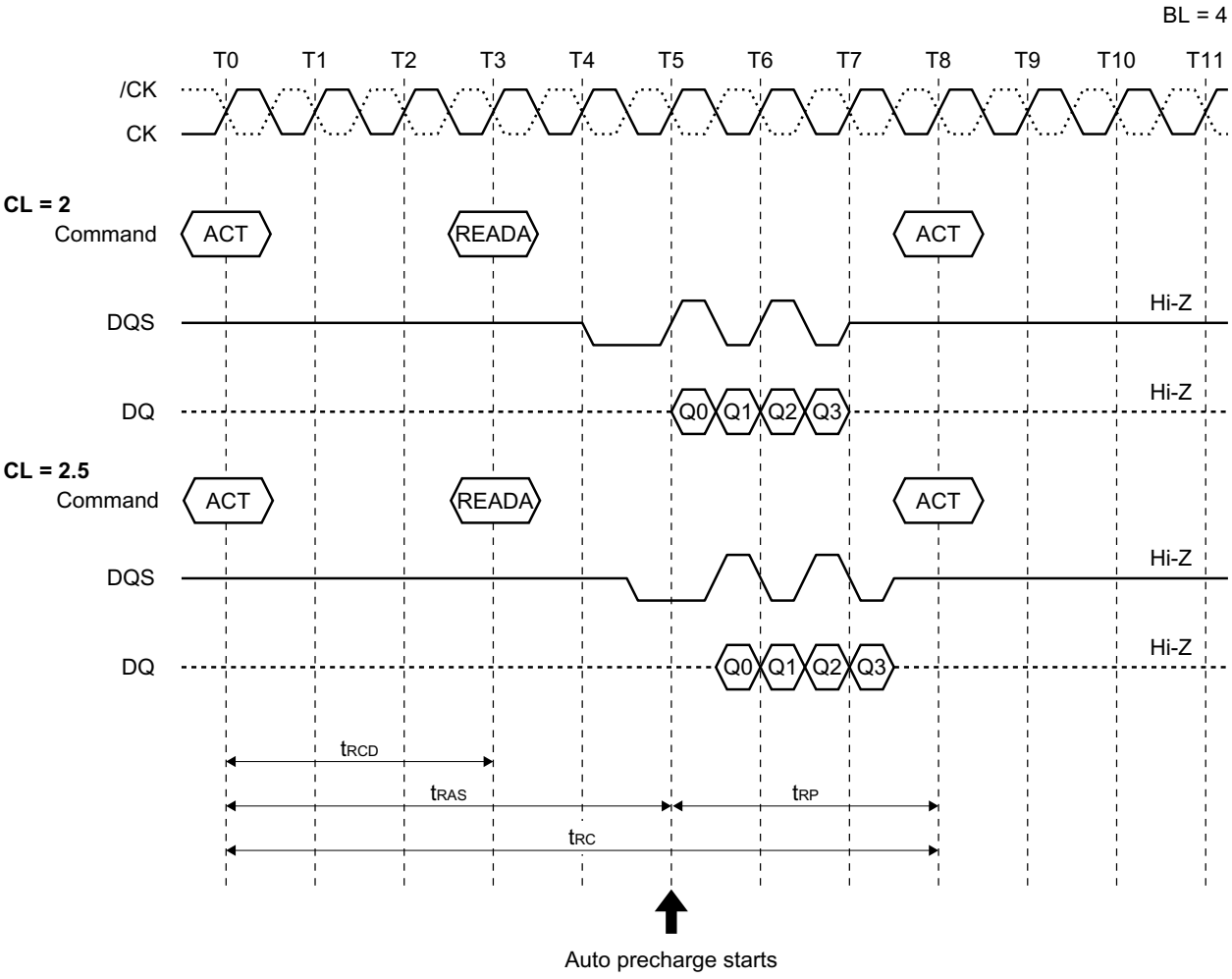
Figure 8-2 shows the read cycle with auto precharge (READA). In this cycle, it is not necessary to input the precharge command (PRE) because precharge starts automatically.

When using auto precharge in the read cycle, it is necessary to know when the precharge operation starts in order to satisfy t_{RAS} and t_{RP}. The next bank active command (ACT) for the bank cannot be issued until the auto precharge cycle is completed (until t_{RP} is satisfied).

Auto precharge will start after the lapse of (burst length/2) clocks from the READA command.

Caution The auto precharge start timing may differ depending on the DDR SDRAM product. For details, refer to the data sheet of each product.

Figure 8-2. Read Cycle with Auto Precharge



Remark CL: /CAS latency, BL: Burst length

8.2 Write Mode

A write operation is executed by issuing the write command (WRIT) for an active bank. The write operation sequence is as follows.

(1) To activate a particular row in a particular bank, the bank active command (ACT) is issued along with a row address and bank address.

(2) After the lapse of t_{RCD} from the ACT command, the starting column and bank addresses are provided with the WRIT command.

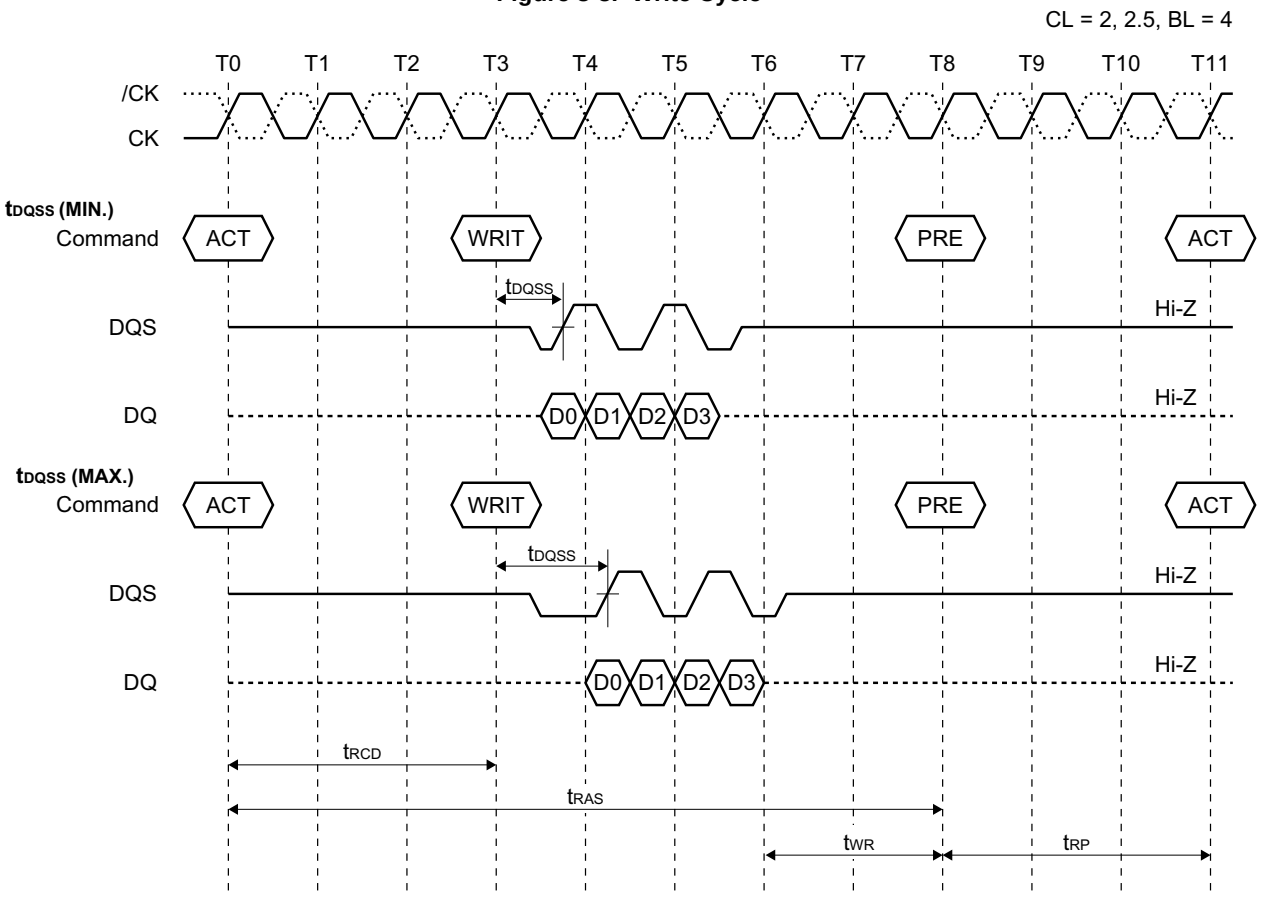
(3) During write bursts, the first valid data-in element will be registered on the first rising edge of the data strobe signal (DQS) and subsequent data elements will be registered on successive edges of DQS.

(4) After the lapse of t_{RAS} from the ACT command, the precharge command (PRE) is input.

(5) After the lapse of t_{RP}, the corresponding bank becomes idle.

Figure 8-3 shows the basic operation timing chart for the write cycle when the burst length = 4.

Figure 8-3. Write Cycle



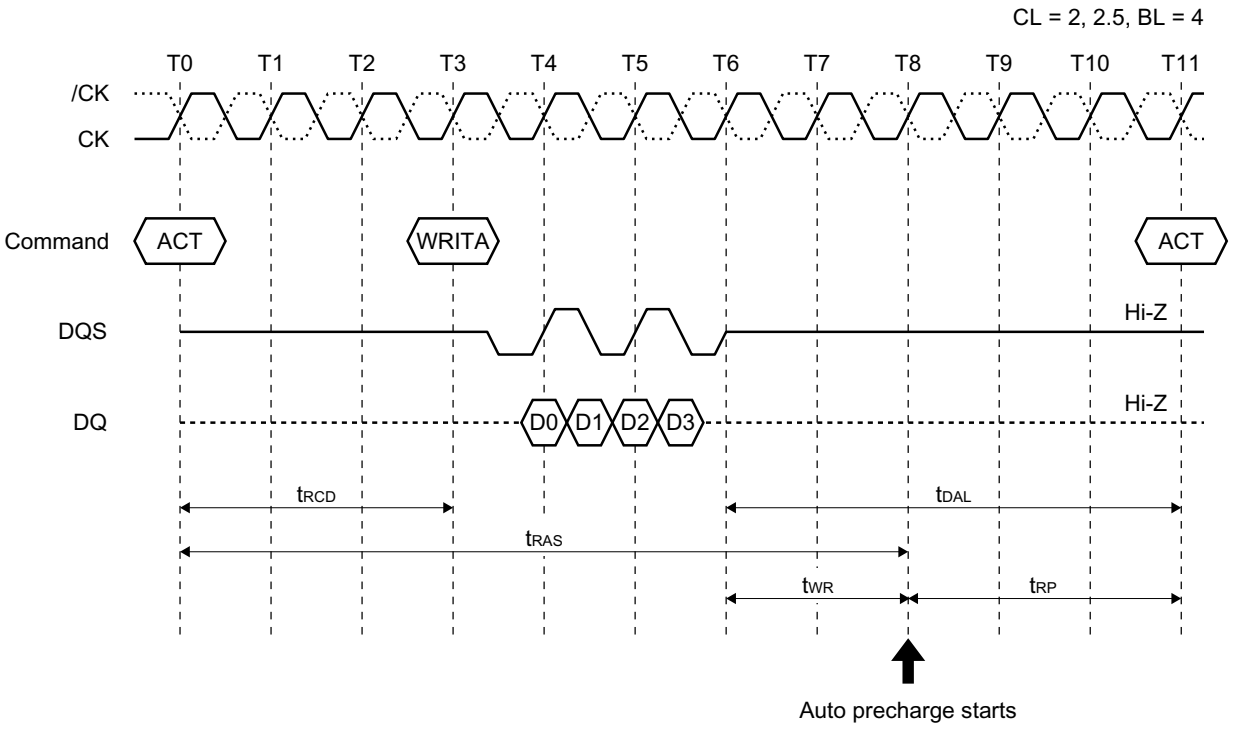
Remark CL: /CAS latency, BL: Burst length

Figure 8-4 shows the write cycle with auto precharge (WRITA). In this cycle, it is not necessary to input the precharge command (PRE) because precharge starts automatically.

When using auto precharge in the write cycle, it is not necessary to know when the precharge operation starts. As long as t_{DAL} is satisfied, the next bank active command (ACT) for the same bank can be issued.

Caution The auto precharge start timing may differ depending on the DDR SDRAM product. For details, refer to the data sheet of each product.

Figure 8-4. Write Cycle with Auto Precharge



Remark CL: /CAS latency, BL: Burst length

8.3 Refresh Mode

Similar to SDR SDRAM, a refresh operation is necessary for DDR SDRAM. There are two refresh modes:

CBR (auto) refresh

Self refresh

The CBR (auto) refresh sequence is as follows.

(1) The CBR (auto) refresh command (REF) can only be issued in the idle state. If the device is not idle, the precharge all banks command (PALL) has to be issued first.

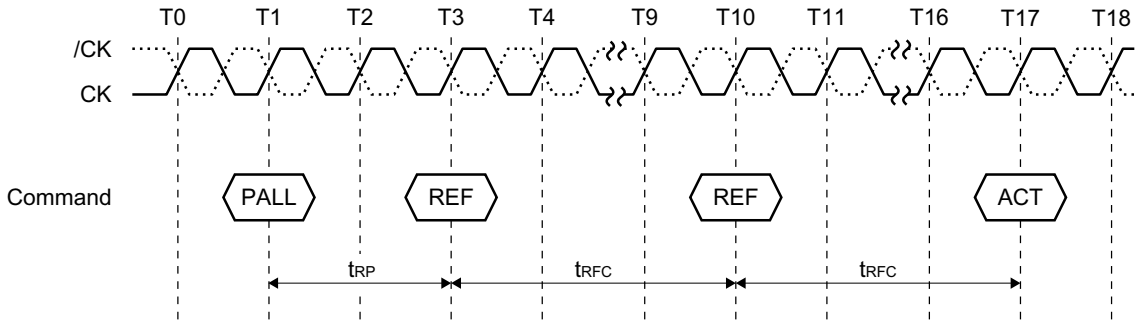
(2) Input the REF command. Since the refresh address is generated internally, it is not necessary to specify refresh address.

(3) The device becomes idle after t_{RFC}.

For the self refresh mode operation, refer to **11.2.2 Self refresh mode**.

Figure 8-5 shows the basic operation timing chart for the CBR (auto) refresh cycle.

Figure 8-5. CBR (Auto) Refresh Cycle



CHAPTER 9 DATA STROBE SIGNAL (DQS) CONTROL OPERATION

This chapter describes the data strobe signal (DQS) newly introduced in DDR SDRAM. This signal is used to control the I/O buffer.

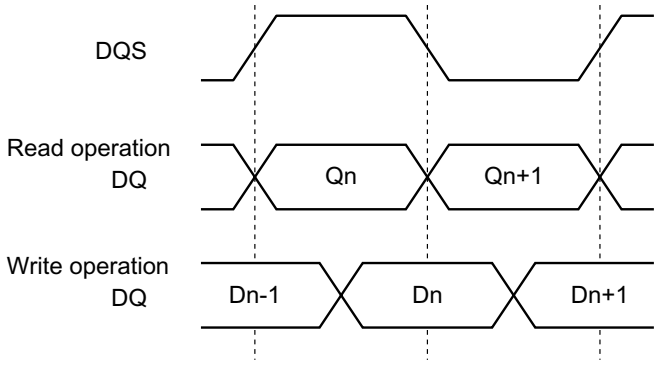
9.1 Data Strobe Signal (DQS)

Since DDR SDRAM performs data input/output at twice the frequency of the external clock, the valid data window is narrower than for SDR SDRAM. If the wiring length between the memory and the controller is different, the time required for data to reach the receiver (flight time) is different. This makes it difficult for the receiver to determine the data acceptance timing.

DDR SDRAM employs a data strobe signal (DQS) to notify the receiver of the data transfer timing. DQS is a bi-directional strobe signal and functions as the basic operating clock for DQ during read/write operations.

Note Data is edge-aligned to DQS for read data and center-aligned for write data. This means that when controller receives read data from DDR SDRAM, it will internally delay the received strobe to the center of the received data window.

Figure 9-1. Relationship between Data Strobe Signal and Data Input/Output



9.1.1 Data strobe signal (DQS) in read cycle

In the read cycle, DDR SDRAM drives the data strobe signal (DQS), which is in synchronization with the clock (CK). The receiver captures the data (DQ) using DQS as a timing reference.

The operation of DQS in the read cycle is as follows.

(1) High impedance while data is not output (<1> in figure).

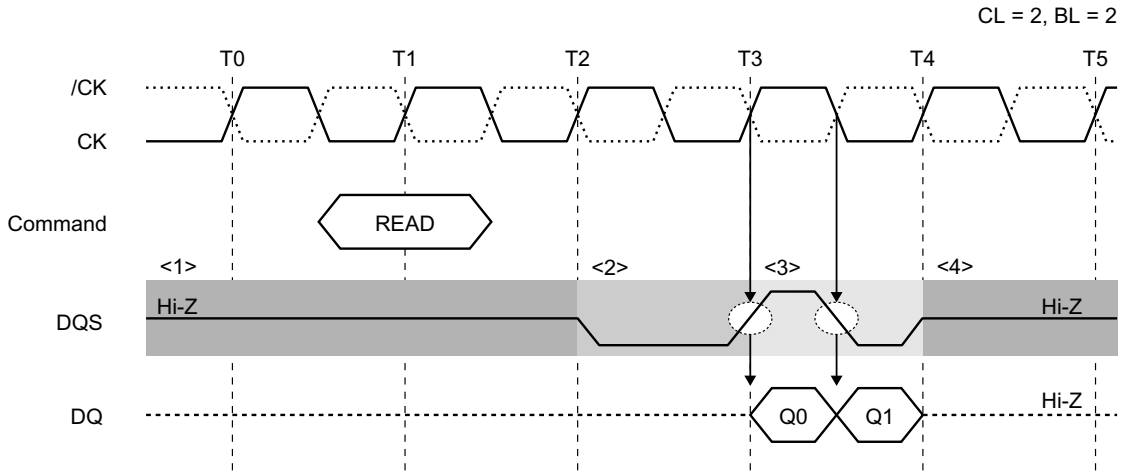
(2) After read command (READ) input, DQS changes to low level approximately 1 clock prior to data output (<2> in figure).

(3) DQS starts toggling at the same frequency as the clock (CK) (<3> in figure).

(4) DQS toggling continues until the burst read operation is completed. When the burst read operation is completed, DQS changes back to high impedance (<4> in figure).

Figure 9-2 shows the operation timing of DQS for the read cycle.

Figure 9-2. Data Strobe Signal in Read Cycle



Remark CL: /CAS latency, BL: Burst length

9.1.2 Data strobe signal (DQS) in write cycle

In the write cycle, the controller drives the data strobe signal (DQS), which is in synchronization with the clock (CK). DDR SDRAM captures the data (DQ) using DQS as a timing reference.

The operation of DQS in the write cycle is as follows.

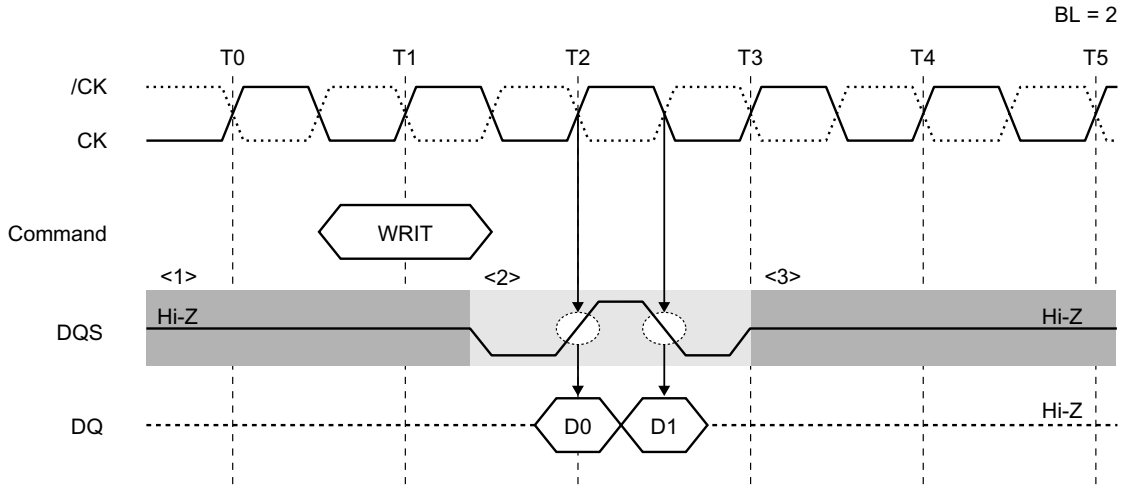
(1) High impedance while data is not input (<1> in figure).

(2) Approximately 1/2 clock after the write command (WRIT), DQS starts toggling at same frequency as the clock (CK) (<2> in figure).

(3) DQS toggling continues until the burst write operation is completed. 1/2 clock after the last burst data, DQS changes back to high impedance (<4> in figure).

Figure 9-3 shows the operation timing of DQS for the write cycle.

Figure 9-3. Data Strobe Signal in Write Cycle



Remark BL: Burst length

9.2 Relationship between Data Strobe Signal (DQS) / Output Data (DQ) and Clock (CK, /CK) during Read Cycle

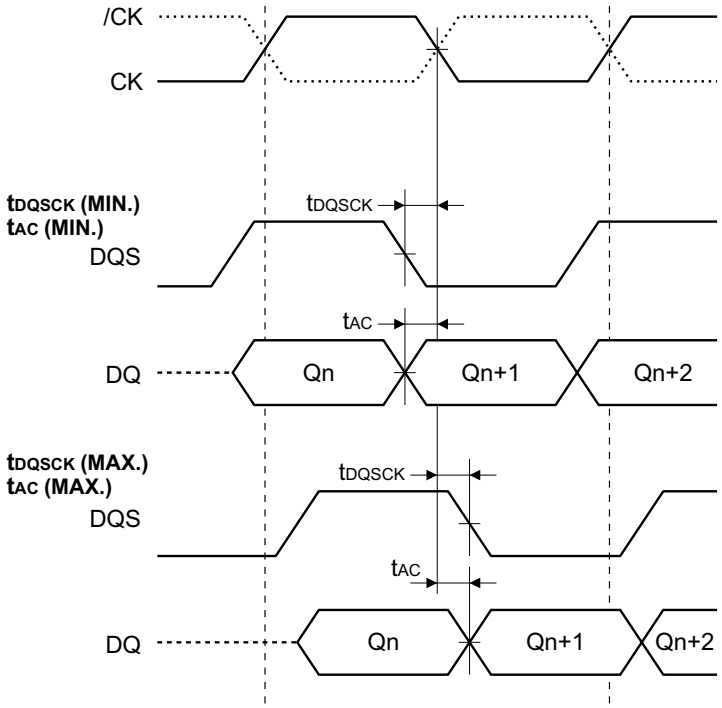
During the read cycle, the rising and falling edges of the data strobe signal (DQS) and the valid data window edges of DQ almost coincide with the rising and falling edges of the clock (CK, /CK) through the use of the DLL circuit or similar internal control.

Timing specifications and examples for DQ and DQS as related to CK are shown below.

Table 9-1. AC Characteristics of Data Strobe Signal and Output Data in Read Cycle

Parameter		Symbol	MIN.	MAX.	Unit
DQS output access time from CK, /CK	DDR266A/DDR266B	t_{DQSCK}	–0.75	+0.75	ns
	DDR200		–0.8	+0.8	
DQ output access time from CK, /CK	DDR266A/DDR266B	t_{AC}	–0.75	+0.75	ns
	DDR200		–0.8	+0.8	

Figure 9-4. Data Strobe Signal and Output Data Timing as Related to Clock in Read Cycle



9.3 Relationship between Data Strobe Signal (DQS) and Output Data (DQ) in Read Cycle

In the read cycle, the valid data window edge nearly coincides with the rising and falling edges of the data strobe signal (DQS). The valid data window is affected by DQS - DQ skew.

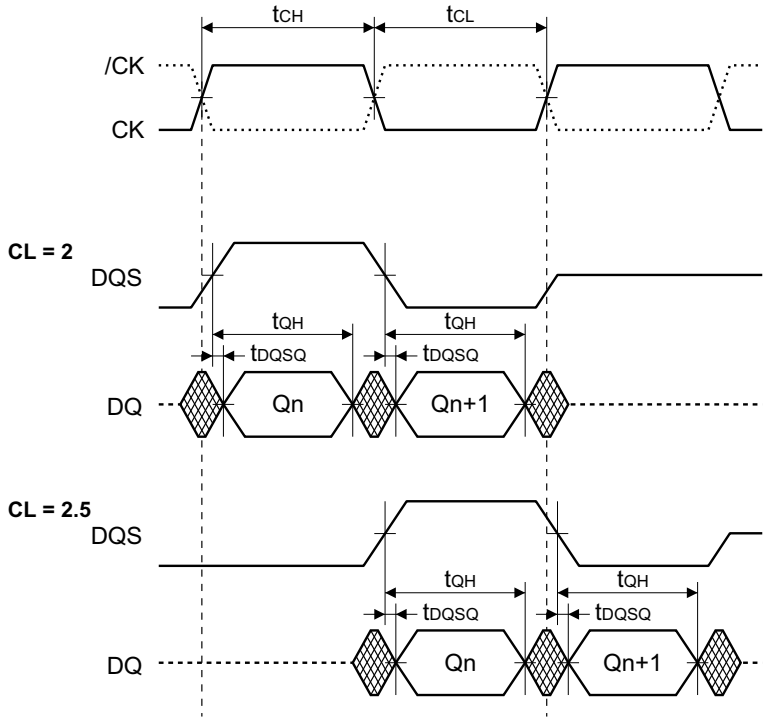
Timing specifications and examples for DQ vs. DQS are shown below.

Table 9-2. AC Characteristics of Data Strobe Signal and Output Data in Read Cycle

Parameter	Symbol	MIN.	MAX.	Unit
DQ output hold time from DQS	t_{QH}	t_{HP} – 0.75	—	ns
DQS - DQ skew	t_{DQSQ}	—	0.5	ns
Valid data window	t_{QH} – t_{DQSQ}	—	—	ns

Remark $t_{HP} = t_{CH}, t_{CL}$ (MIN.)

Figure 9-5. Data Strobe Signal and Output Data in Read Cycle



Remark CL: /CAS latency

9.4 Data Strobe Signal (DQS) Read Preamble and Read Postamble

The data strobe pattern for a read operation consists of preamble, toggling, and postamble portions.

When DDR SDRAM receives the read command (READ) in the bank active state, the data strobe signal (DQS) changes from the high-impedance state to low level. This is the read preamble portion. The read preamble occurs approximately 1 clock prior to the first data output.

Following the read preamble, the strobes will toggle at the same frequency as the clock signal while data is present on the data input/output pin (DQ).

The low time following the last data transition is known as the read postamble. The read postamble occurs approximately 1/2 clock from the last data edge.

When a burst read is completed and another new burst read is expected to follow (read-to-read data bus transition), a read postamble and preamble are not required between the two burst read operations.

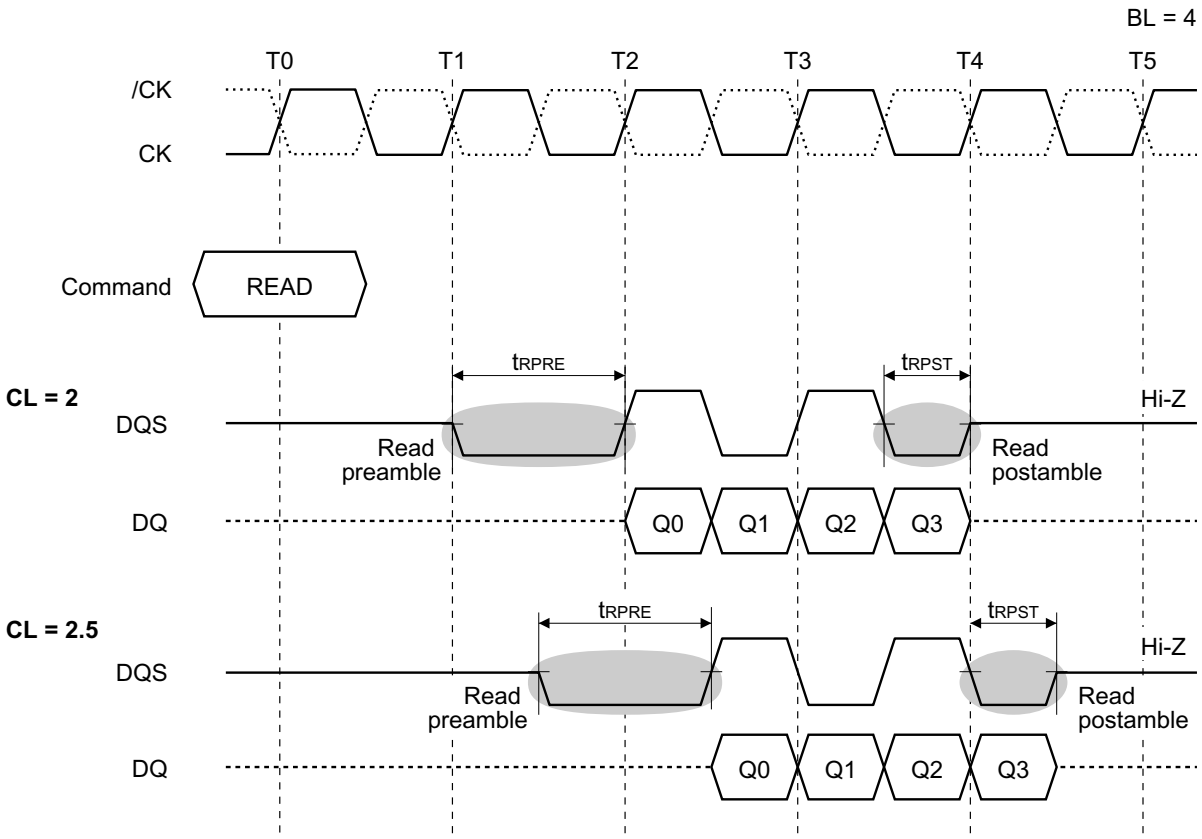
Timing parameters for the DQS read preamble and read postamble are shown below.

Table 9-3. AC Characteristics of Data Strobe Signal Read Preamble and Read Postamble

Parameter	Symbol	MIN.	MAX.	Unit
Read preamble	t_{RPRE}	0.9 t_{CK}	1.1 t_{CK}	ns
Read postamble	t_{RPST}	0.4 t_{CK}	0.6 t_{CK}	ns

Remark t_{CK}: Clock cycle time

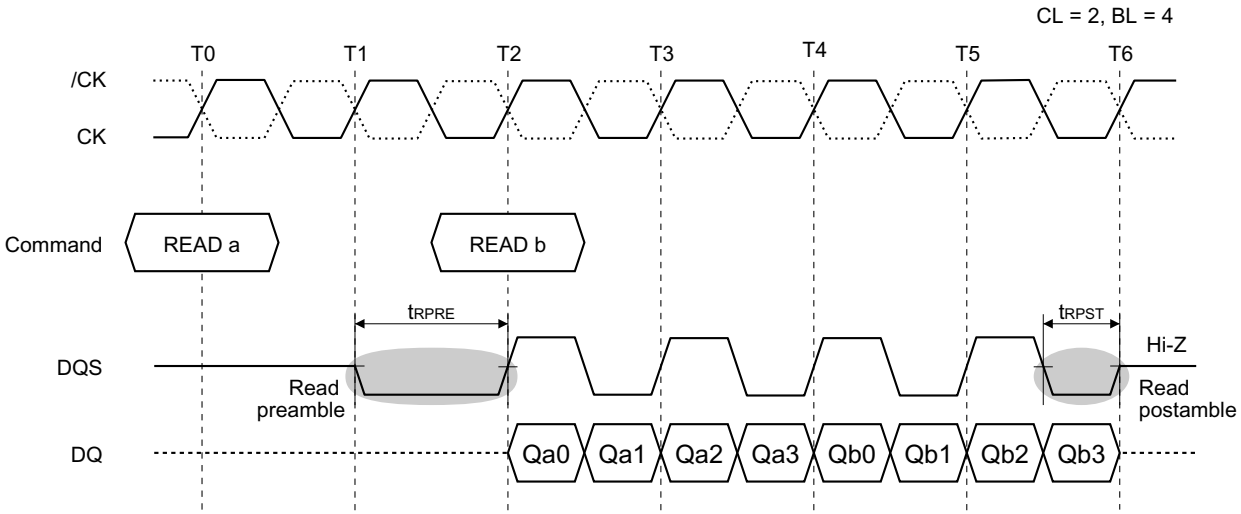
Figure 9-6. Timing of Data Strobe Signal Read Preamble and Read Postamble 1



Remark CL: /CAS latency, BL: Burst length

Figure 9-7. Timing of Data Strobe Signal Read Preamble and Read Postamble 2

(Read-to-Read Data Bus transition)



Remark CL: /CAS latency, BL: Burst length

9.5 Relationship between Data Strobe Signal (DQS) and Input Data (DQ) / DQ Write Mask Enable Signal (DM) during Write Cycle

Input data (DQ) and the DQ write mask enable signal (DM) are center-aligned to the data strobe signal (DQS) during write cycle.

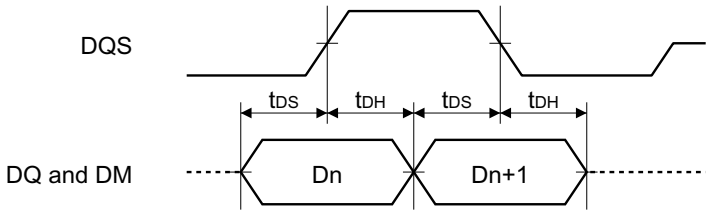
Timing parameters of DQ/DM for DQS are shown below.

Table 9-4. AC Characteristics of DQ/DM in Write Cycle

Parameter	Symbol	MIN.	MAX.	Unit
DQ and DM input setup time	t_{DS}	0.075 t_{CK}	—	ns
DQ and DM input hold time	t_{DH}	0.075 t_{CK}	—	ns

Remark t_{CK}: Clock cycle time

Figure 9-8. Timing Parameters of DQ/DM during Write Cycle



9.6 Data Strobe Signal (DQS) Write Preamble and Write Postamble

The data strobe pattern for a write operation also consists of preamble, toggling, and postamble portions.

When DDR SDRAM receives the write command (WRIT) in the bank active state, the data strobe signal (DQS) input changes from the high-impedance to low level. This is the write preamble portion. The write preamble occurs at the falling edge of the clock at which the WRIT command is input.

Following the write preamble, the strobes will toggle at the same frequency as the clock signal while data is present on the data input/output pin (DQ).

The low time following the last data transition is known as the write postamble. The write postamble occurs approximately 1/2 clock from the last data edge.

When a burst write is completed and another new burst write is expected to follow, a write postamble and preamble are not required between the two burst write operations.

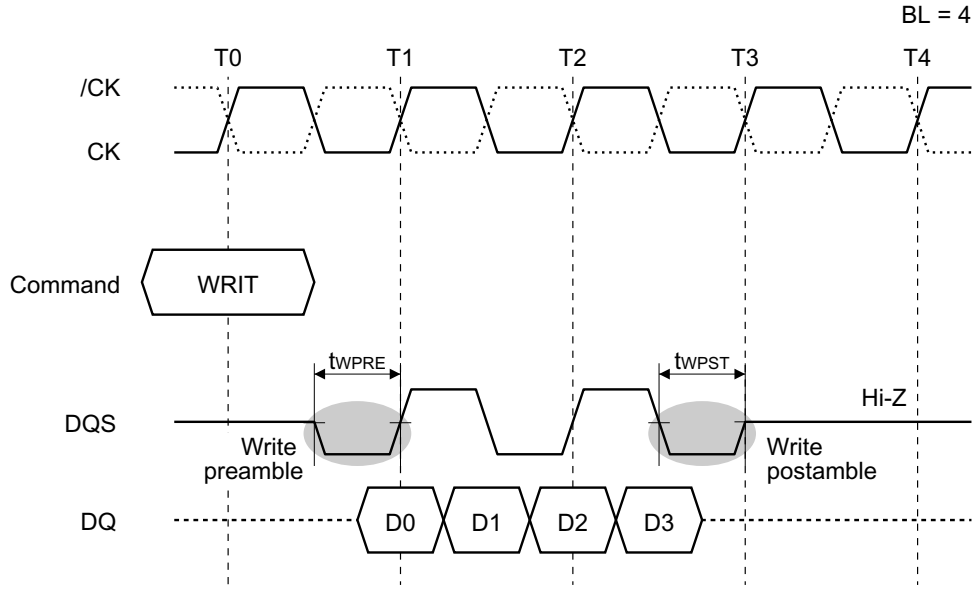
Timing parameters for the DQS write preamble and write postamble are shown below.

Table 9-5. AC Characteristics of Data Strobe Signal Write Preamble and Write Postamble

Parameter	Symbol	MIN.	MAX.	Unit
Write preamble	t_{WPRE}	0.25 t_{CK}	—	ns
Write postamble	t_{WPST}	0.4 t_{CK}	0.6 t_{CK}	ns

Remark t_{CK}: Clock cycle time

Figure 9-9. Timing of Data Strobe Signal Write Preamble and Write Postamble



Remark CL: /CAS latency, BL: Burst length

CHAPTER 10 DQ WRITE MASK ENABLE SIGNAL (DM) CONTROL OPERATION

This chapter describes DQ write mask enable signal (DM) control. DM masks input data.

Unlike SDR SDRAM, data masking is only available in the write cycle for DDR SDRAM. The burst stop command (BST) is available during burst read, but burst stop during write is illegal. Data masking is available during write, but data masking during read is not available.

10.1 DQ Write Mask Enable Signal (DM)

DQ pins controlled by the DQ write mask enable signal (DM) differ depending on the bit organization.

(1) ×4-bit organization

DM controls DQ0 through DQ3.

(2) ×8-bit organization

DM controls DQ0 through DQ7.

(3) ×16-bit organization

LDM controls DQ0 through DQ7 (lower bit control).

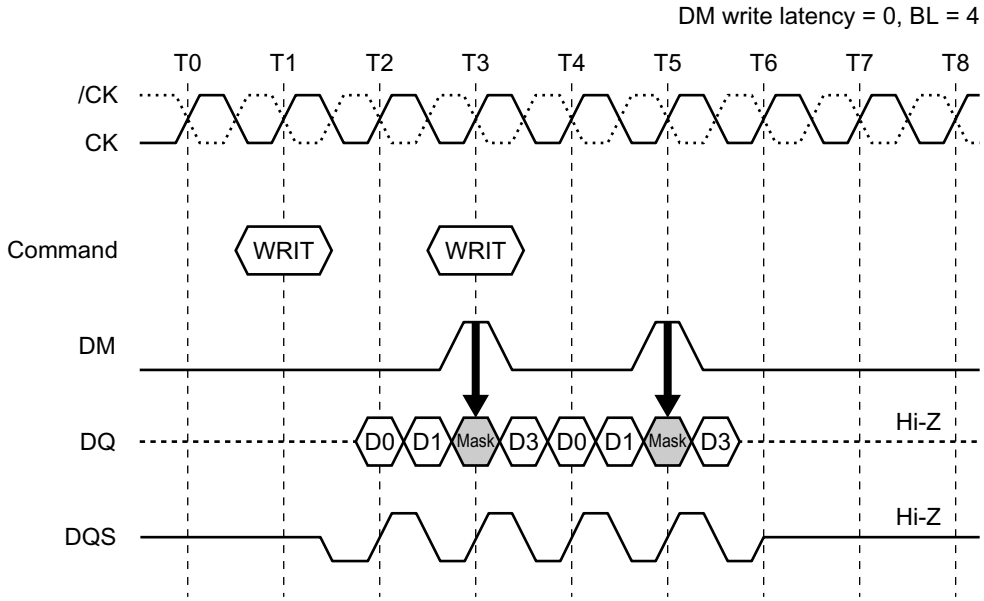
UDM controls DQ8 through DQ15 (upper bit control).

10.2 DQ Write Mask Enable Signal (DM) Control in Write Cycle

The DM latency in the write cycle is 0 regardless of the /CAS latency.

As shown in Figure 10-2, write data is masked when the corresponding DQ write mask enable signal (DM) is high.

Figure 10-1. DQ Write Mask Enable Signal Control during Write Cycle



Remark BL: Burst length

10.3 DQ Write Mask Enable Signal (DM) Truth Table

Table 10-1 shows the command truth table of the DQ write mask enable signal (DM).

Table 10-1. DQ Write Mask Enable Signal Truth Table

Function	Symbol	CKE		DM	
		n – 1	n	UDM	LDM
Data write enable	ENB	H	×	L	
Data mask	MASK	H	×	H	
Upper byte write enable	ENBU	H	×	L	×
Lower byte write enable	ENBL	H	×	×	L
Upper byte write inhibit	MASKU	H	×	H	×
Lower byte write inhibit	MASKL	H	×	×	H

Remark H = High level, L = Low level, × = High or Low level (Don't care)

CHAPTER 11 CLOCK ENABLE SIGNAL (CKE) CONTROL OPERATION

This chapter explains the basic control method using the clock enable signal (CKE). CKE is a signal that controls clock (CK, /CK) enable/disable.

(1) When CKE is high at the rising edge of the preceding CK

The rising edge of CK is valid and signals are input.

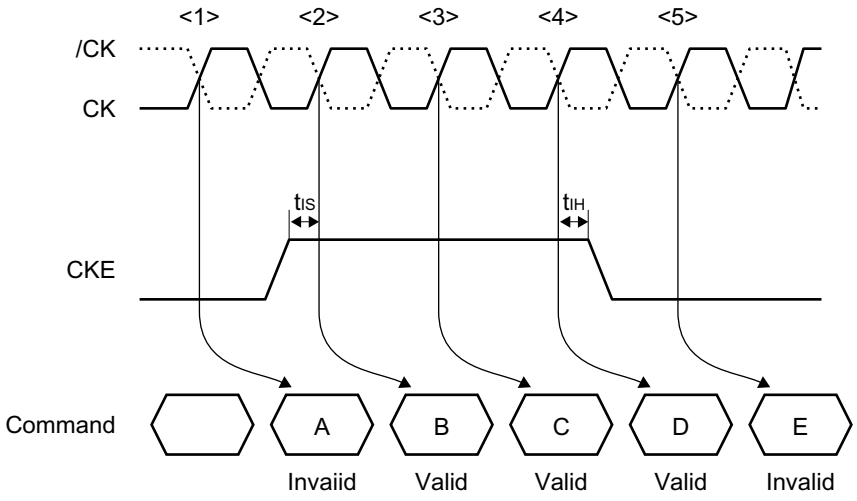
(2) When CKE is low at the rising edge of the preceding CK

The rising edge of CK is invalid and signals are ignored.

11.1 Basic Control

Figure 11-1 shows the signal input timing controlled by the clock enable signal (CKE).

Figure 11-1. Signal Input Timing Controlled by Clock Enable Signal



When CKE is high at the rising edge of the clock (CK) as in <2>, <3>, and <4> above (where setup time t_{IS} and hold time t_{IH} are satisfied), commands B, C, and D at the rising edge of the next CK can be loaded.

When CKE is low at the rising edge of CK as in <1> and <5>, the command at the rising edge of the next CK is ignored.

11.2 Example of Clock Enable Signal (CKE) Control

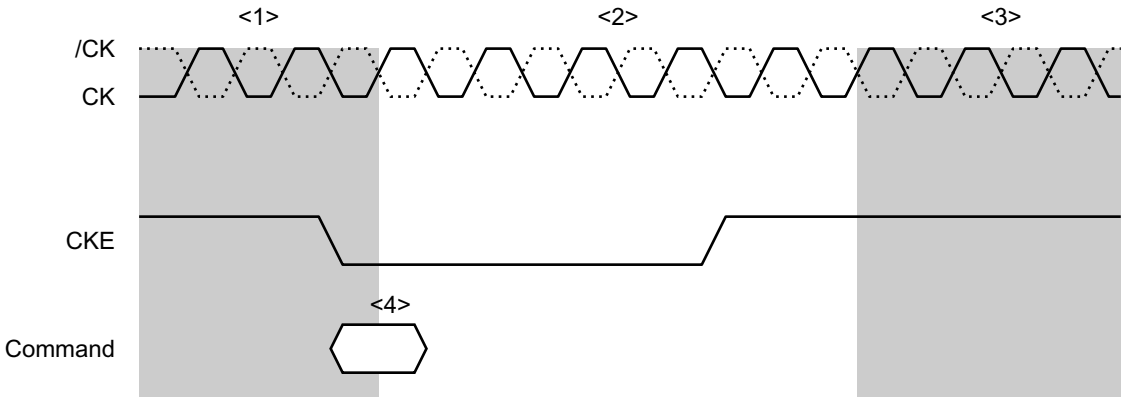
There are two operation modes controlled by the clock enable signal (CKE):

Power down mode

Self refresh mode

Figure 11-2 shows command input controlled by CKE. In the figure, the command is loaded only during the period <1> and <3>, and the command is ignored during <2>.

Figure 11-2. Example of Clock Enable Signal Control



11.2.1 Power down mode

In the power down mode, the internal clock of the device is deactivated to reduce the power consumption of the device. Figure 11-3 shows the timing in the power down mode.

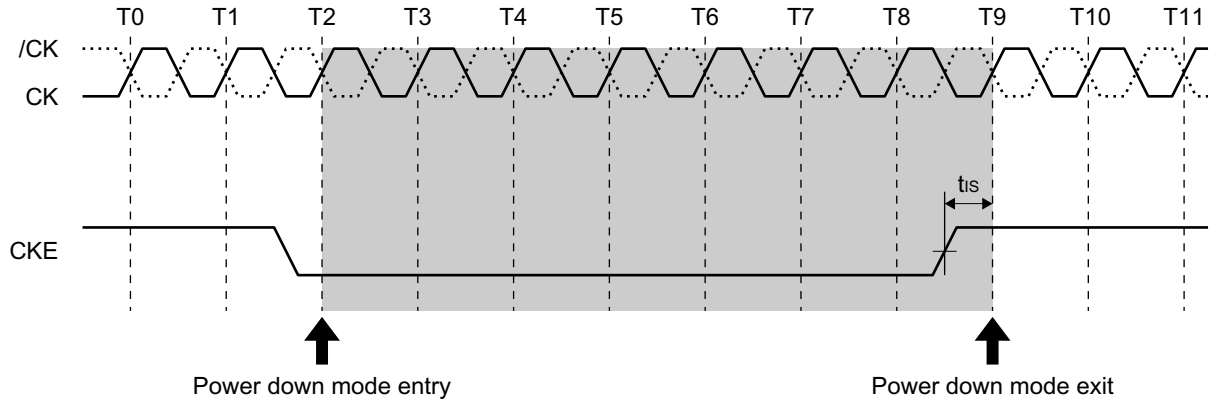
(1) Starting power down mode

The power down mode is started at T2 when the clock enable signal (CKE) is changed from high to low (T1 - T2) in the all banks idle or bank active state. When power down mode is started, all the input signals other than CKE are ignored (don't care state (high or low level)), and the data bus becomes high-impedance. CKE must be kept low in power down mode.

(2) Exiting power down mode

The power down mode is exited at T9 when CKE is changed from low to high (T8 - T9), and the next command can be input starting from T10. The clock must toggle at least one cycle before CKE goes high.

Figure 11-3. Power Down Mode



Remarks **1.** Commands cannot be input in the power down mode.

2. Make sure that t_{REF} is satisfied.

11.2.2 Self refresh mode

Self refresh is the operation mode used to reduce power consumption of the device by deactivating the internal clock, while at the same time executing refresh operations automatically.

This mode is useful when it's necessary to keep memory cell data but a write/read operation is not necessary.

Figure 11-4 shows the timing of self refresh mode.

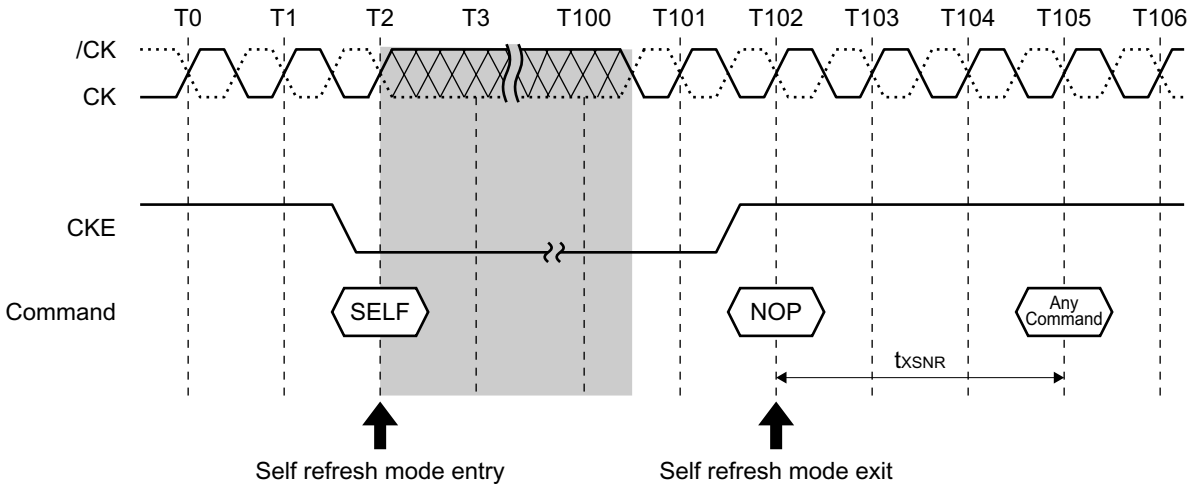
(1) Starting self refresh mode

The self refresh mode is started at T2 by changing the clock enable signal (CKE) from high to low (T1 - T2) when the self refresh entry command (SELF) is input. In self refresh mode, all the input signals except CKE are in the don't care state (high or low level), and the data bus becomes high-impedance. CKE must be kept low in self refresh mode.

(2) Exiting self refresh mode

The self refresh mode is exited by changing CKE from low to high (T101 - T102). The clock must toggle at least one cycle before CKE goes high. In addition, t_{XSNR} must be satisfied before the next command is input.

Figure 11-4. Self Refresh Mode



Caution For customers using concentrated CBR (auto) refresh (non average periodic refresh), to make sure memory cell data is not lost, concentrated CBR (auto) refresh for all the row is required just before and after a self refresh operation.

11.2.3 Clock enable signal (CKE) command truth table (128M bit DDR SDRAM (EDD1216ALTA))

The clock enable signal (CKE) command truth table is shown below.

Current state: Self refresh

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	×	×	×	×	×	×		Illegal (Impossible)	
L	H	H	×	×	×	×	SREX	Exit self refresh → Self refresh recovery	**Note**
		L	H	H	×	×			
L	L	×	×	×	×	×		Maintain self refresh	

Note CKE low to high transition will re-enable the clock (CK) and other inputs asynchronously. A minimum setup time must be satisfied before any command other than exit is input.

Remark H: High level, L: Low level, ×: High or low level (Don't care)
Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Self refresh recovery

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	H	H	×	×	×	×	DESL	No operation (Idle after t_{RC})	
H	H	L	H	H	H	×	NOP	No operation (Idle after t_{RC})	
H	L	×	×	×	×	×		Illegal	
L	×	×	×	×	×	×		Illegal (Impossible)	

Remark H: High level, L: Low level, ×: High or low level (Don't care)
Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Power down

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	×	×	×	×	×	×		Illegal (Impossible)	
L	H	H	×	×	×	×	PDEX	Exit power down → Idle state	
		L	H	H	×	×			
L	L	×	×	×	×	×		Maintain power down	

Remark H: High level, L: Low level, ×: High or low level (Don't care)
Illegal: Device operation and/or data integrity are not guaranteed.

Current state: All banks idle

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	H	V	V	V	V	×		Refer to **CHAPTER 7 COMMAND OPERATIONS**	
H	L	H	×	×	×	×	PWDN	Power down entry	**Note**
H	L	L	H	H	H	×	PWDN	Power down entry	**Note**
H	L	L	×	×	L	×		Illegal	
H	L	L	H	L	×	×		Illegal	
H	L	L	L	H	×	×		Illegal	
H	L	L	L	L	H	×	SELF	Self refresh entry	**Note**
L	×	×	×	×	×	×		Power down	

Note Self refresh can be entered only from the all banks idle state. Power down can be entered only from the all banks idle or row active state.

Remark H: High level, L: Low level, ×: High or low level (Don't care), V: Valid data
Illegal: Device operation and/or data integrity are not guaranteed.

Current state: Row active

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	×	×	×	×	×	×		Refer to **CHAPTER 7 COMMAND OPERATIONS**	
L	×	×	×	×	×	×		Power down	

Remark H: High level, L: Low level, ×: High or low level (Don't care), V: Valid data

Current state: Other than above

CKE		/CS	/RAS	/CAS	/WE	Address	Command	Action	Note
(n – 1)	(n)								
H	H	V	V	V	V	V		Refer to **CHAPTER 7 COMMAND OPERATIONS**	
H	L	×	×	×	×	×		Illegal	
L	×	×	×	×	×	×		Illegal (Impossible)	

Remark H: High level, L: Low level, ×: High or low level (Don't care), V: Valid data
Illegal: Device operation and/or data integrity are not guaranteed.

CHAPTER 12 BURST OPERATION

This chapter explains the burst operation.

12.1 Terminating Burst Operation

The burst operation can be terminated in the following ways:

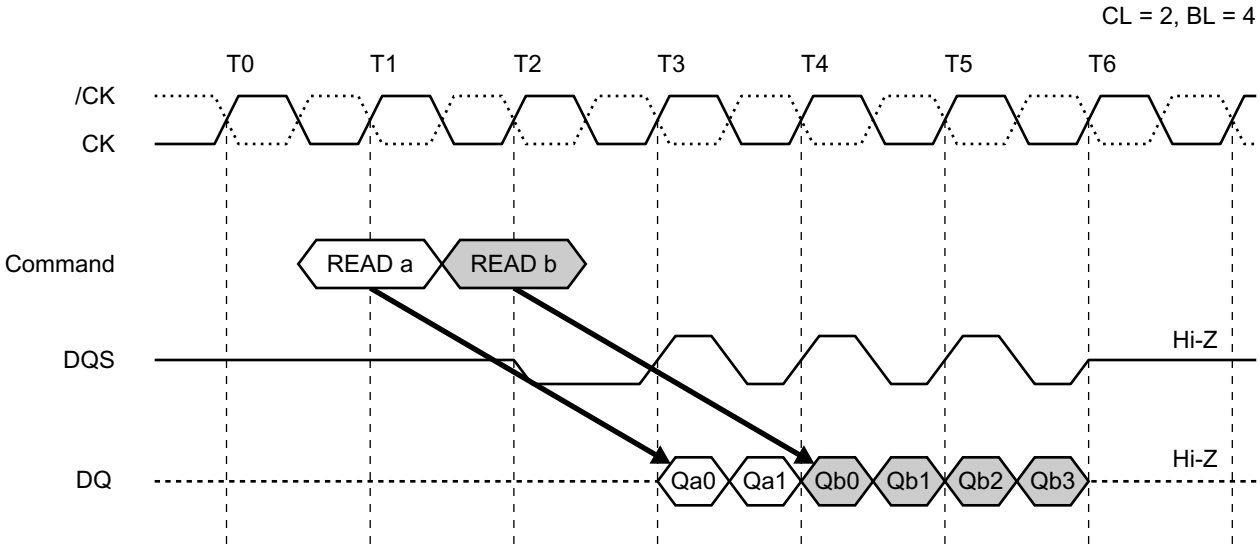
(1) By using read command (READ)
(2) By using write command (WRIT)
(3) By using burst stop command (BST)
(4) By using precharge command (PRE)

12.1.1 Data interrupt by read command

(1) Read cycle

The preceding burst read operation can be aborted by inputting a new read command (READ b).
The data for the new read command is output after the lapse of the /CAS latency.

Figure 12-1. Read/Read Command



Remark CL: /CAS latency, BL: Burst length

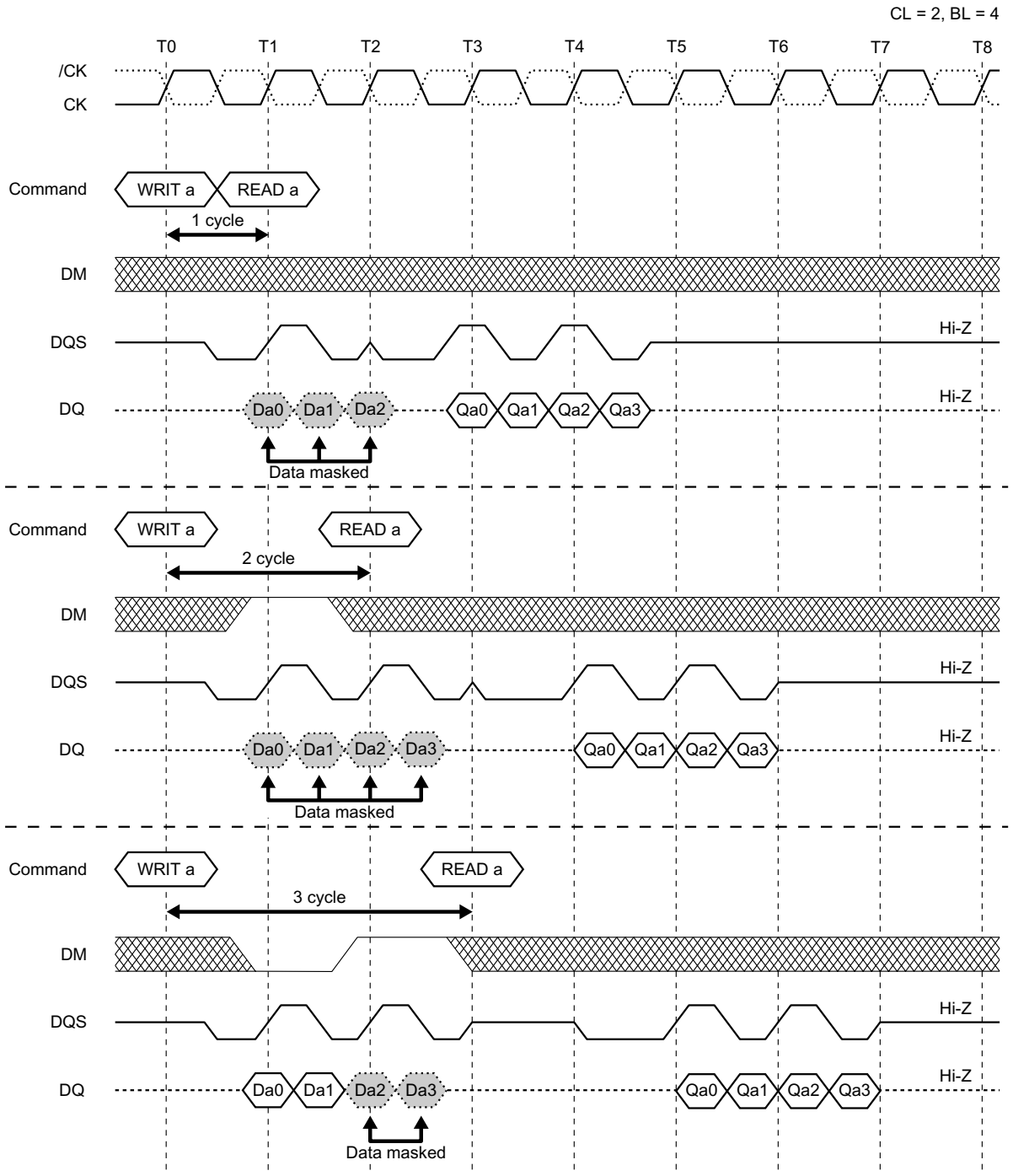
(2) Write cycle

The preceding burst write operation can be aborted by inputting a read command (READ a).

In the case where the write to read command interval is 1 clock cycle, all the write data is masked by the read command. In the case where the write to read command interval is greater than 1 clock cycle, DQ write mask enable (DM) must be used to mask the last two input data which precede the read command.

The data of the read command is output after the lapse of the /CAS latency.

Figure 12-2. Write/Read Command



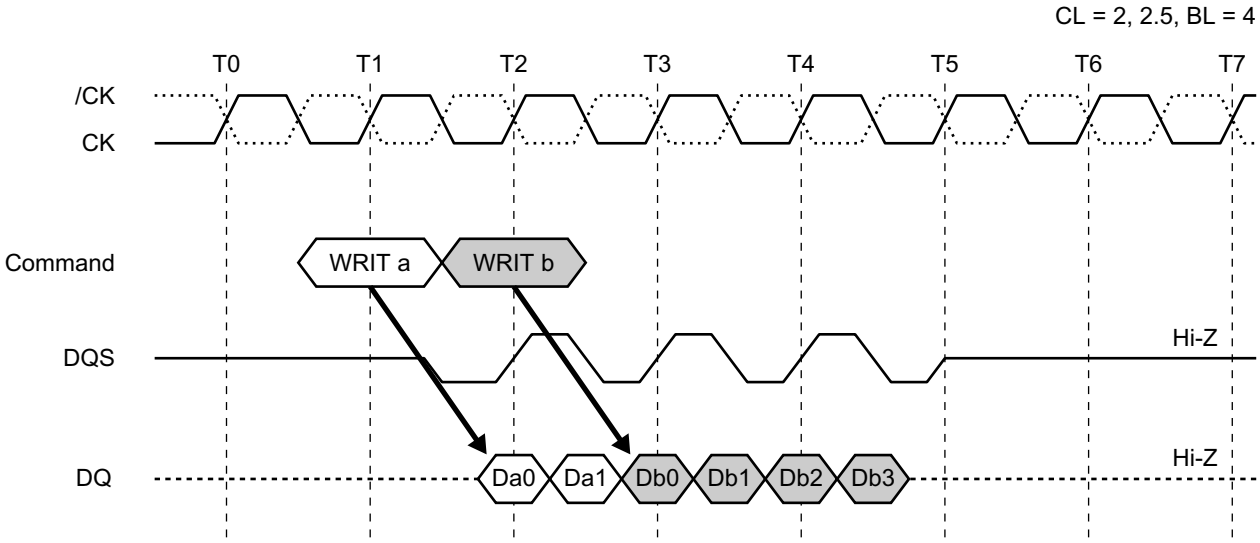
Remark CL: /CAS latency, BL: Burst length

12.1.2 Data interrupt by write command

(1) Write cycle

The preceding burst write operation can be aborted by inputting a new write command (WRIT b).

Figure 12-3. Write/Write Command

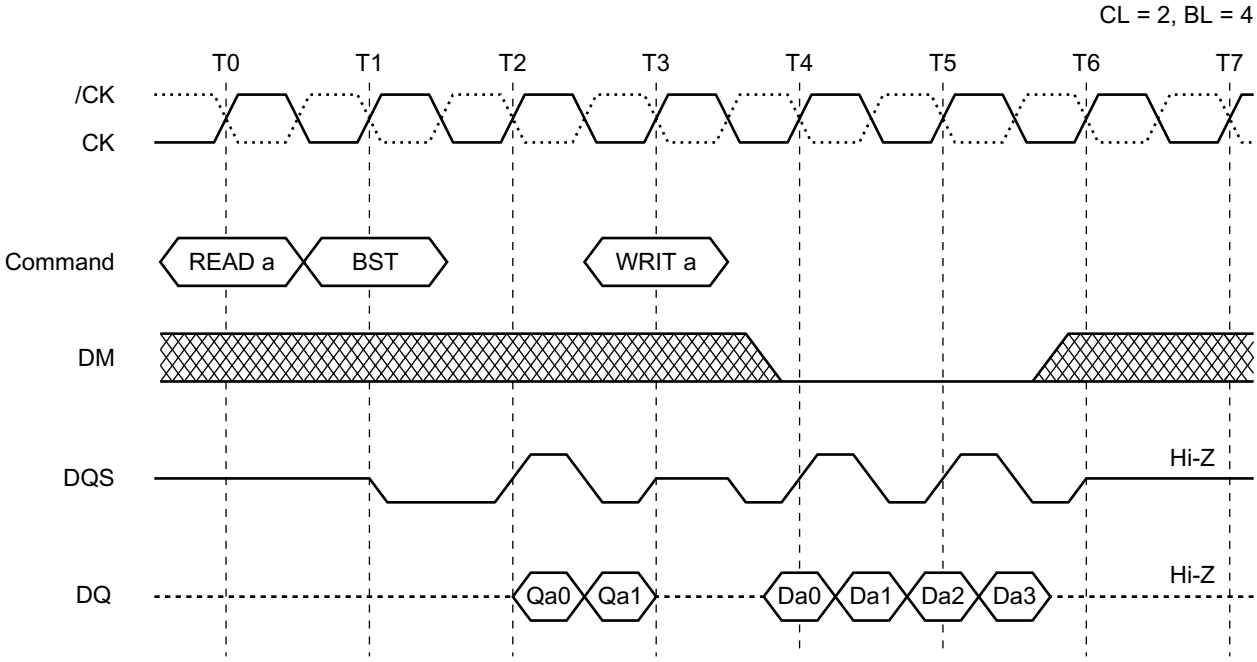


Remark CL: /CAS latency, BL: Burst length

(2) Read cycle

To abort the preceding burst read operation and start a burst write operation, the burst stop command (BST) is required before the write command (WRIT a).

Figure 12-4. Read/Burst Stop/Write Command

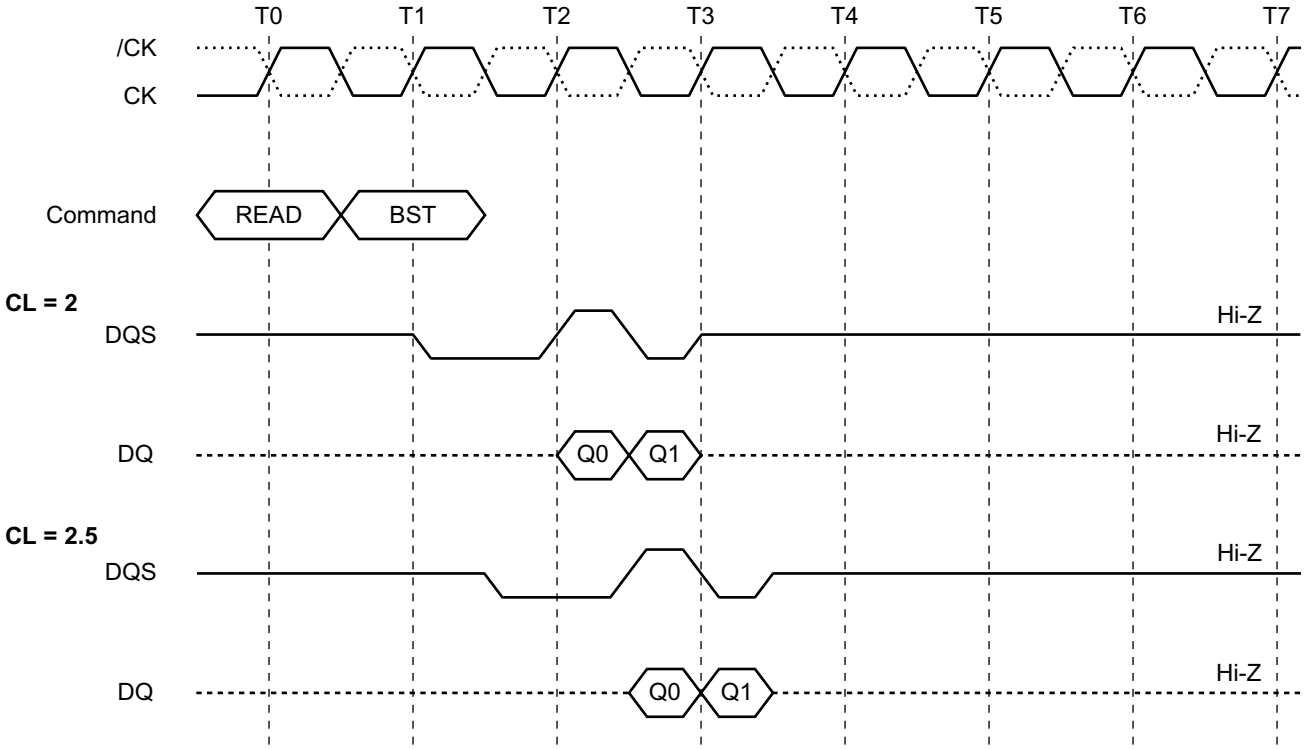


Remark CL: /CAS latency, BL: Burst length

12.1.3 Ending burst operation by burst stop command

The burst read operation can be aborted by inputting the burst stop command (BST) in the read cycle. The data bus becomes high impedance after the lapse of the /CAS latency from the burst stop command. The burst stop command is only available in read cycles for DDR SDRAM.

Figure 12-5. Read/Burst Stop Command



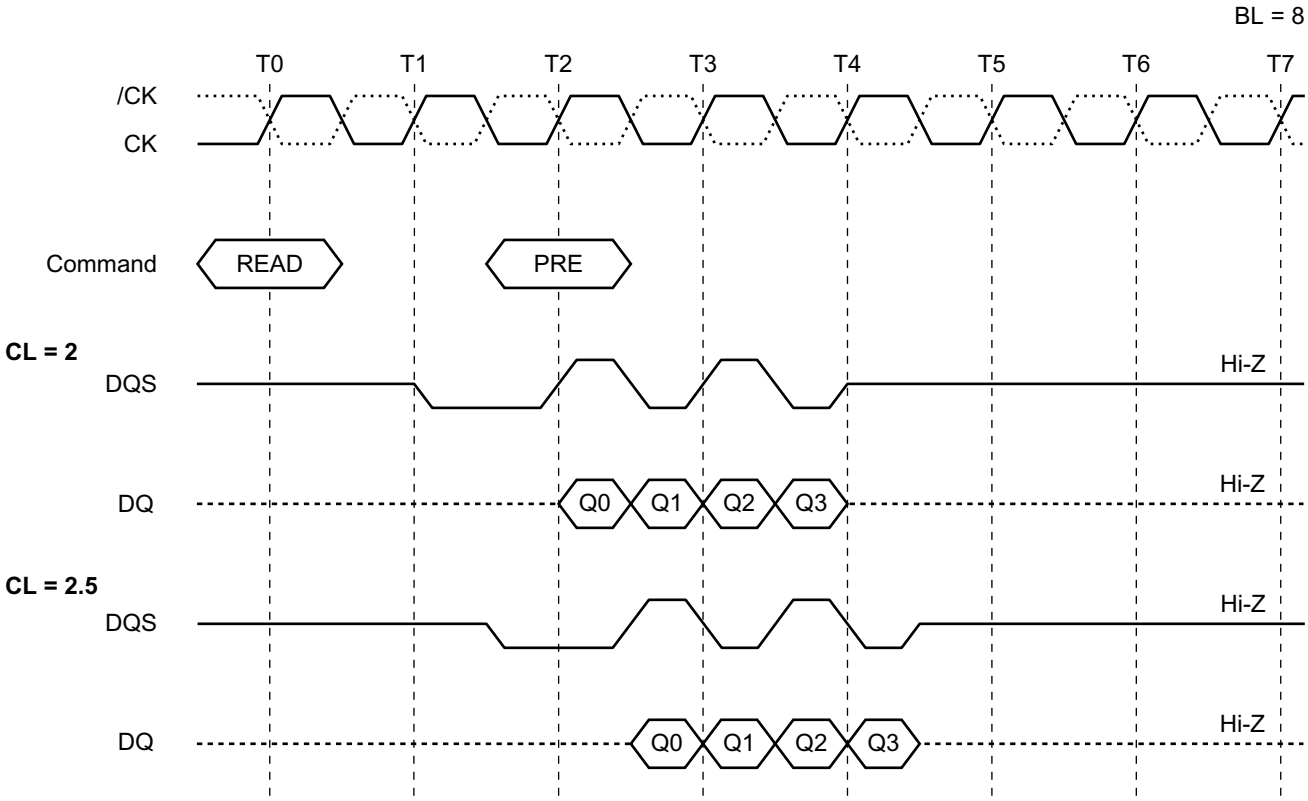
Remark CL: /CAS latency

12.1.4 Terminating burst operation by precharge command

(1) Read cycle

The burst read operation is terminated by inputting the precharge command (PRE). To input the precharge command, t_{RAS} must be satisfied. To activate the same bank again, t_{RP} must be satisfied.

Figure 12-6. Read/Precharge Command

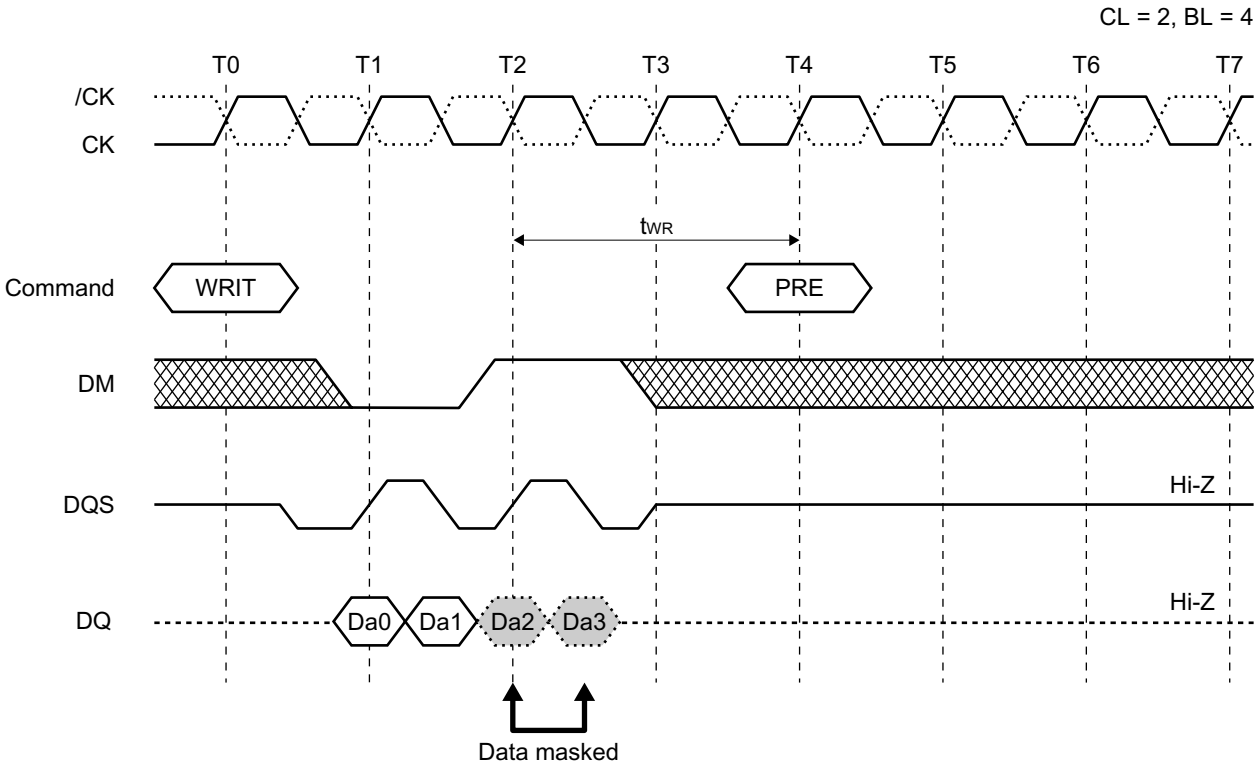


Remark CL: /CAS latency, BL: Burst length

(2) Write cycle

The burst write operation can be terminated by inputting the precharge command (PRE). To input the precharge command, t_{RAS} must be satisfied. To activate the same bank again, t_{RP} must be satisfied. Data prepared t_{WR} before the precharge command will be correctly written to the memory cell.

Figure 12-7. Write/Precharge Command



Remark CL: /CAS latency, BL: Burst length

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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