United Electronic Industries

The High-Performance Alternative

DNx-AI-222

—

User Manual

12-Channel, fully isolated RTD / resistance input board
for the PowerDNA Cube and PowerDNR RACKtangle

Release 4.6

January 2015

PN Man-DNx-AI-222-115

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Contacting United Electronic Industries

Mailing Address:

27 Renmar Avenue
Walpole, MA 02081
U.S.A.

For a list of our distributors and partners in the US and around the world, please see http://www.ueidaq.com/partners/

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Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-222 board. The DNx-AI-222 is a 12-channel analog input module for the PowerDNA I/O Cube (DNA-AI-222) and the DNR-1G HalfRACK / RACKtangle / FLATRACK chassis (DNR-AI-222).

1.1 Organization of Manual

This AI-222 User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-AI-222 Analog Input Board features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  This chapter is an overview of low-level API commands for configuring and using the AI-222 series board.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-222 board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

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Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbadim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle^{TM} rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

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1.2 The AI-222 Interface Board

The DNA/DNR-AI-222 are 12-channel fully isolated, simultaneously sampling RTD input boards compatible with UEI's popular Cube and RACKtangle chassis respectively. The DNA/DNR versions are electronically identical. The DNx-AI-222 features 24-bit A/D converters with 50 µA excitation current for resistances up to 40kΩ. The AI-222 provides an input resolution of better than 0.005 °C or 0.002 Ohm when measuring 100Ω RTDs using a range of 0-312Ω.

An A/D per channel configuration allows simultaneous sampling at rates up to 150 S/s each (1800 S/s aggregate). The A/D per channel configuration virtually eliminates input cross talk and channel settling time issues.

The DNx-AI-222 is an ideal, high accuracy RTD measurement device, offering total errors of less than 0.2 °C on all standard 100 Ohm RTDs. This accuracy combined with the 350 VDC/Vrms channel-to-channel and channel-to-chassis isolation makes the board a perfect solution for industrial temperature measurement, even when using non-isolated RTDs in high voltage environments.

The software included will perform all required RTD linearization and compensation and returns data in °C, °K, °F or °R when desired. The software also allows the temperature conversion to be disabled and the inputs can measure resistance in Ohms up to 40 kOhms.

Software included with the DNx-AI-222 provides a comprehensive yet easy to use API that supports all popular Windows programming languages as well as supporting programmers using Linux and most real-time operating systems including QNX, RTX, InTime, VXworks and more. The UEIDAQ Framework supplies complete support for those creating applications in data acquisition software packages such as LabVIEW, MATLAB/Simulink, DASYLab or any application which supports ActiveX or OPC servers.

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1.3 Features

The AI-222 layer has the following features:

- 12 fully differential analog input channels
- 2, 3, and 4 wire RTD connections (per channel selectable)
- 100 Ohm DIN and US measurements
- Channel-to-channel and channel-to-chassis isolation
- 0.005°C resolution, 0.2°C accuracy
- 0 to 40000 Ohm resistance range
- Built-in 50, 60Hz rejection at <20S/s and 400 Hz at <160S/s
- Weight of 120 g or 4.24 oz for DNA-AI-222; 630 g or 22.2 oz with PPC5

1.4 Specification

The technical specification for the DNx-AI-222 board are listed in **Table 1-1**.

Table 1-1. DNx-AI-222 Technical Specifications

Number of channels:	12 fully differential
ADC resolution	24 bits, < 0.005 °C with 100 Ω PT RTDs < 0.002 Ω in resistance measurement mode
Sampling rate	up to 150 samples/sec per channel 1800 S/S board aggregate
Measurement error RTDs (100 Ω PT) 0 to 312 Ω range 0 to 1250 Ω range 0 to 5000 Ω range 0 to 40,000 Ω range	(@ 25 ±5°C / over -40°C to +85°C) ±0.2 °C / ±0.4 °C ±0.05 Ω / ±0.1 Ω ±0.1 Ω / ±0.2 Ω ±0.2 Ω / ±0.4 Ω ±0.2 Ω ±0.02% / ±1% of reading
Excitation current	50 µA typical (all ranges)
Resistance range	0 - 40,000 Ω
General A/D specifications	
Gain error	±0.005 % (typical)
Input INL error	6 ppm typical, 15 ppm max
Input impedance	>5000 MΩ
Anti-Aliasing filtering	@47.6% of sample rate, ~100 dB/decade
50/60/400 Hz notch filtering	>70 dB at sample rate = 20 Hz or less
Isolation	350 Vrms, chan-to-chan & chan-to-chassis
Overvoltage protection	-15 V to +15 V (power on or off, current must be limited to ±20 mA)
Power consumption	4 W max
Operating temp. (tested)	-40°C to +85°C
Operating humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500Hz, broadband random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	230,000 hours

* mode can be used for burnout / open detection
* recommended for RTDs

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1.5 Device Architecture

Figure 1-1 is a block diagram of the architecture of the AI-222 layer.

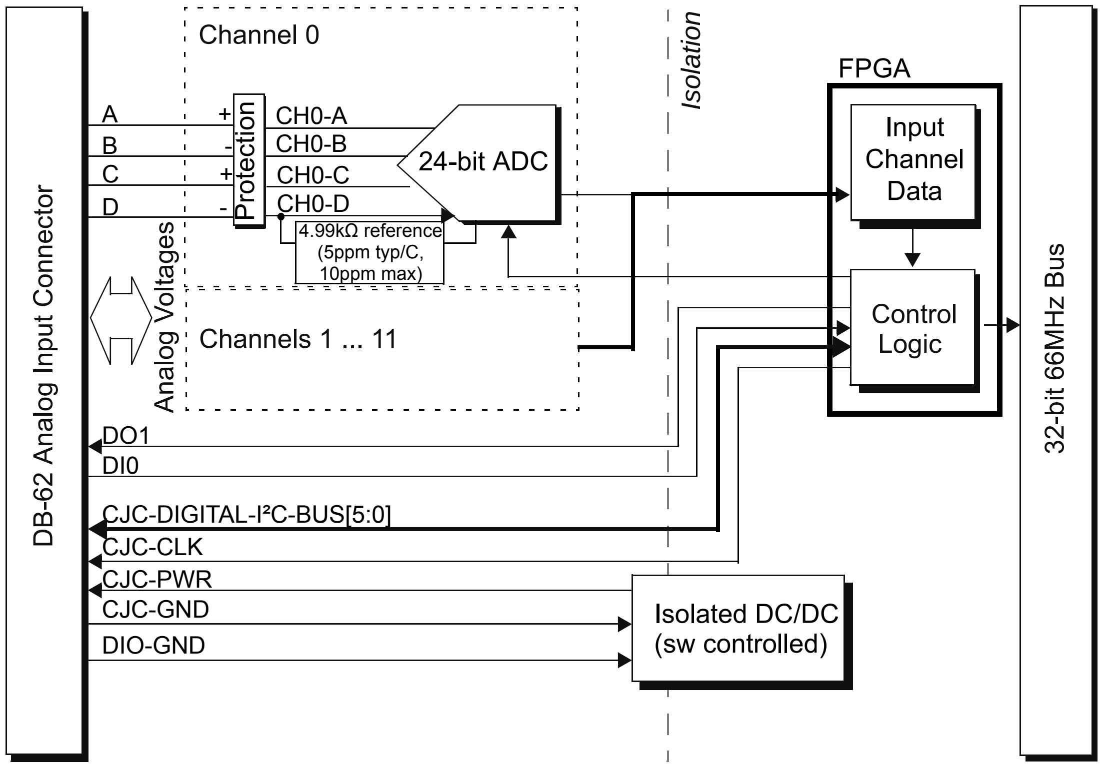

Figure 1-1. Block Diagram of the AI-222 Layer

Each AI-222 has twelve differential input channels designed for high-resolution analog voltage signal measurement. Each channel has 24-bit sampling resolution and maximum sampling rate of 150 samples per second (one sample every $6.\overline{6}$ msec), up to 1800 max samples per second per board. Each channel is individually isolated and uses dedicated components to avoid crosstalk/noise between channels and also ensures that one channel's failure (e.g. due to accidental over-voltage) does not affect other channels or the board.

Each channel's input consists of four analog input and excitation lines. The analog lines carry your input voltages to be compared differentially against one other before being sampled digitally. Design was intended for RTDs, but any resistance from 0 to 40kΩ may be measured. The analog input lines (A/B/C/D in **Figure 1-1**) enter through the DB-62 connector pins into a SP724 protection circuit designed to redirect ESD / transients to the channel's isolated power supply before entering the A/D converter.

There is one 24-bit A/D converter per differential input channel. The converter is a highly-integrated, precision delta-sigma (ΔΣ) ADC with 24-bit resolution. It has a low-noise programmable-gain-amplifier (PGA) with selectable gains that are selected by the firmware to best match the resistance range you choose. The ADC has hardware support for sensor burnout detect, matched current sources for RTDs to cancel errors caused by sensor lead resistance, and a digital filter that settles in one cycle. Dedicating one single ADC for each input channel virtually eliminates input cross talk and channel settling time issues even when connected to high impedance signal sources.

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The converter control & data lines are wired (through an isolation barrier) to the board's main controller. The 350V isolation barrier ensures that disturbances or damage to one channel does not affect other channels, allowing the AI-222 to be an ideal solution for precise temperature measurement that must happen over long periods of time.

The main controller, in addition to containing the standard logic to provide DNx functionality, also contains AI-222 specific logic blocks with the role to send commands to all 12 channels, provide clocking & synchronization, receive & process data from channels, and provide sampled data and configuration access to the Cube & RACKtangle applications.

To perform data acquisition, the main controller sends a command to sample up to all 12 analog inputs simultaneously, receive 24-bit values from the conversion chip and provide them in output buffer. The output buffer is made accessible to standard DNx function calls and is read using software calls in either the UEIDAQ Framework (see Chapter 2) or the low-level API (see Chapter 3).

In addition to each channel's analog inputs *AIn*+ and *AIn*-, described above, each layer also has a digital input, digital output line, and digital ground line. The digital lines are wired through a protection circuit directly into the main controller.

1.6 Indicators

A photo of the DNx-AI-222 unit is illustrated below.

The front panel has two LED indicators:

- RDY: indicates that the layer is receiving power and operational.
- STS: can be set by the user using the low-level framework.

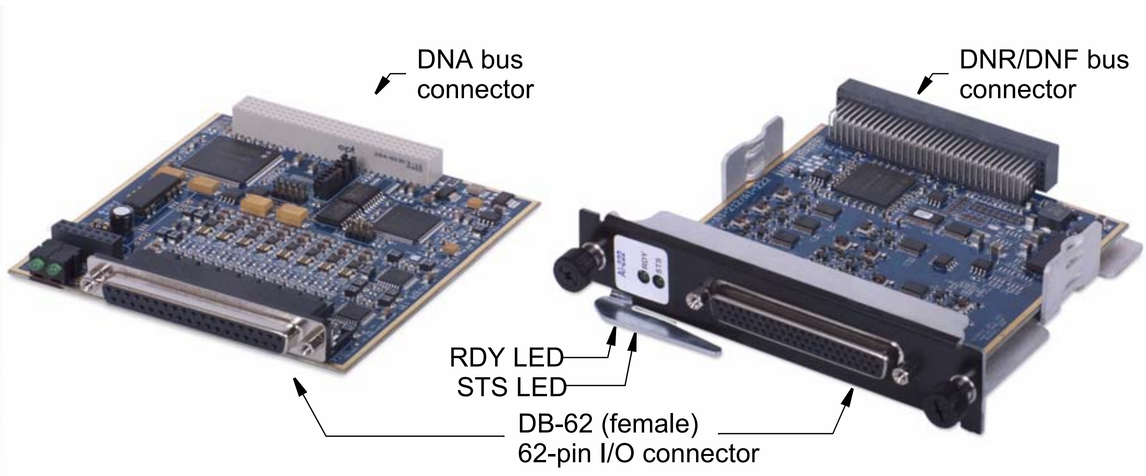
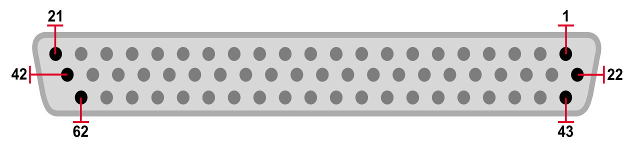


Figure 1-2. The DNR-AI-222 Analog-Input Layer

1.7 Layer Connectors and Wiring

Figure 1-3 below illustrates the pinout of the AI-222. The AI-222 layer uses a B-size 62-pin D-sub connector. The following signals are located at the connector:

- AI0 to 11 — analog input channel. Wiring setups provided on next page.
- +5VDC (100mA max) - provides power for external accessories; Gnd for 5VDC provides a reference ground for this power supply.
- DIO — digital I/O lines:
  - DI0: digital input line
  - DO1: digital output line
  - DGND digital ground line
- DNC - do not connect to these pins.



Pin	Signal	Pin	Signal	Pin	Signal
1	Rsvd	22	Rsvd	43	Rsvd
2	Rsvd	23	Rsvd	44	Rsvd
3	5 VDC (100 mA Max)	24	Gnd for 5VDC	45	Gnd for 5VDC
4	Rsvd	25	Rsvd	46	CH 11.A
5	CH 11.C	26	CH 11.B	47	CH 11.D
6	CH 10.B	27	CH 10.A	48	CH 10.C
7	CH 9.A	28	CH 10.D	49	CH 9.B
8	CH 9.D	29	CH 9.C	50	CH 8.A
9	CH 8.C	30	CH 8.B	51	CH 8.D
10	CH 7.B	31	CH 7.A	52	CH 7.C
11	CH 6.A	32	CH 7.D	53	CH 6.B
12	CH 6.D	33	CH 6.C	54	CH 5.A
13	CH 5.C	34	CH 5.B	55	CH 5.D
14	CH 4.B	35	CH 4.A	56	CH 4.C
15	CH 3.A	36	CH 4.D	57	CH 3.B
16	CH 3.D	37	CH 3.C	58	CH 2.A
17	CH 2.C	38	CH 2.B	59	CH 2.D
18	CH 1.B	39	CH 1.A	60	CH 1.C
19	CH 0.A	40	CH 1.D	61	CH 0.B
20	CH 0.D	41	CH 0.C	62	DO 1
21	DI 0	42	DIO Gnd		

Figure 1-3. Pinout Diagram of the AI-222 Layer

NOTE: If you are using a accessory panel with the AI-222, please refer to the Appendix for a description of the panel.

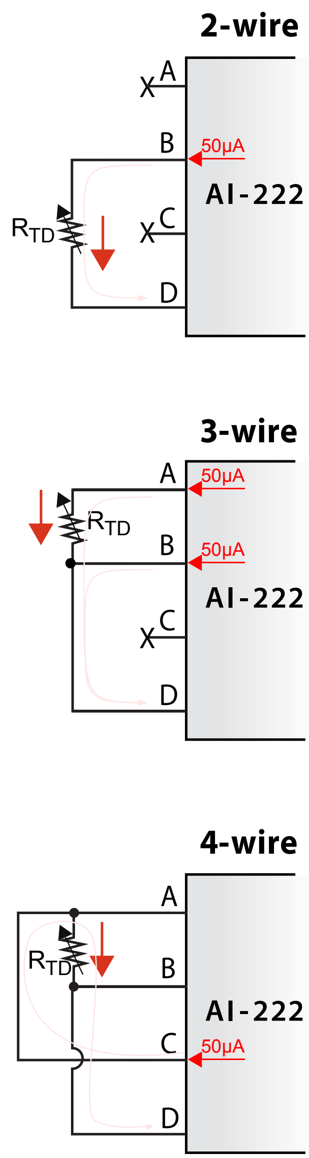


Figure 1-4. Wiring for 2/3/4-wire RTD for the AI-222 Layer

Chapter 2 Programming with the High Level API

This section describes how to control the DNx-AI-222 using the UeiDaq Framework High Level API.

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input

CUeiSession aiSession;
```

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

2.3 Configuring the Input

This section will show you how to configure your input for voltage measurement or thermocouple measurement.

2.3.1 Resistance Measurement

Resisstance measurements are configured using the Session object method “`CreateResistanceChannel`”.

```
// add three channels (0, 2 and 4) to the channel list and configure
// the channels to measure a resistance between 0 and 5000 Ohms.
// The resistance is connected to the DAQ device using four wires.

aiSession.CreateResistanceChannel("pdna://192.168.100.2/dev0/Ai0,2,4",
                                   0, 5000.0, UeiFourWires, 0.0,
                                   UeiAIChannelInputModeDifferential);
```

Note that reading a resistance beyond this range (e.g. a 6k resistance when configured for 0-5k) will appear as overrange or the maximum value.

2.3.2 RTD Measurement

RTD measurements are configured using the Session object method "`CreateRTDChannel`".

RTD sensors are resistive sensors whose resistance varies with temperature. Knowing the resistance of an RTD, we can calculate the temperature using the "Callendar Van-Dusen" equations. RTD sensors are specified using the "alpha" (α) constant. It is also known as the temperature coefficient of resistance, which defines the resistance change factor per degree of temperature change. The RTD type is used to select the proper coefficients A, B and C for the Callendar Van-Dusen equation, which is used to convert resistance measurements to temperature.

You must configure the RTD type and its nominal resistance at 0° Celsius, as shown in the following example:

```
// Add 4 channels (0 to 3) to the channel list and configure them to
// measure a temperature between 0.0 and 200.0 °C.
// The RTD sensor is connected to the DAQ device using two wires
// The RTD alpha coefficient is 0.00385, the nominal resistance at 0° C
// is 100 Ohms, and the measured temperature will be returned in °C.

aiSession.CreateRTDChannel("pdna://192.168.100.2/dev0/Ai0:3",
                            0, 1000.0, UeiTwoWires, 0.0,
                            UeiRTDType3850, 100.0,
                            UeiTemperatureScaleCelsius,
                            UeiAIChannelInputModeDifferential);
```

2.4 Configuring the Timing

You can configure the AI-222 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode. In simple mode, the delay between samples is determined by software on the host computer. In buffered mode, the delay between samples is determined by the AI-222 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the "UeiDaq Framework User's Manual" to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)

aiSession.ConfigureTimingForSimpleIO();
```

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2.5 Read Data

Reading data is done using *reader* object(s). There is a reader object to read raw data coming straight from the A/D converter. There is also a reader object to read data already scaled to resistance or temperature.

The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session’s stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan, where the buffer will contain one value per channel
aiReader.ReadSingleScan(data);
```

2.6 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

Chapter 3 Programming with the Low-level API

The PowerDNA cube and PowerDNR RACKtangle and HalfRACK can be programmed using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to access device registers directly.

However, we recommend that, when possible, you use the UeiDaq Framework High-Level API (see **Chapter 2**), because it is easier to use. You should need to use the low-level API only if you are using an operating system other than Windows.

For additional information about low-level programming of the AI-222, please refer to the PowerDNA API Reference Manual document under:

Start » Programs » UEI » PowerDNA » Documentation

Refer to the PowerDNA API Reference Manual on how to use low-level functions of AI-222, as well as others related to cube operation.

Appendix A

A. Accessories

The following cables and STP boards are available for the AI-222 layer.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

DB-62 (female)
62-pin connector:

62	to J2	42	to J2	21	to J2
61	to JT1	41	to JT1	20	to JT1
60	to JT1	40	to JT1	19	to JT1
59	to JT1	39	to JT1	18	to JT1
58	to JT1	38	to JT1	17	to JT1
57	to JT1	37	to JT1	16	to JT1
56	to JT1	36	to JT1	15	to JT1
55	to JT2	35	to JT1	14	to JT1
54	to JT2	34	to JT2	13	to JT2
53	to JT2	33	to JT2	12	to JT2
52	to JT2	32	to JT2	11	to JT2
51	to JT2	31	to JT2	10	to JT2
50	to JT2	30	to JT2	9	to JT2
49	to JT2	29	to JT2	8	to JT2
48	to JT3	28	to JT3	7	to JT2
47	to JT3	27	to JT3	6	to JT3
46	to JT3	26	to JT3	5	to JT3
45	to JT3	25	to JT3	4	to JT3
44	to JT3	24	to JT3	3	to JT3
43	to JT3	23	to JT3	2	to JT3
		22	to JT3	1	to JT3

JT3 — 20-position terminal block:	JT2 — 20-position terminal block:	JT1 — 20-position terminal block:	J2 — 5-position terminal block:	
22	55	20	5	SHIELD
1	13	41	4	GND
43	34	61	3	62
23	54	19	2	42
2	12	40	1	21
44	33	60		
24	53	18		
3	11	39		
45	32	59		
25	52	17		
4	10	38		
46	31	58		
26	51	16		
5	9	37		
47	30	57		
27	50	15		
6	8	36		
48	29	56		
28	49	14		
GND	7	35		

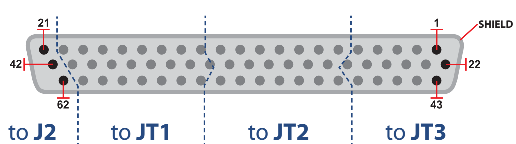

Figure A-1. Pinout and photo of DNA-STP-62 screw terminal panel

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