Modicon TSX Quantum

140 ERT 854 10

Smart Digital Input Module

User Manual

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GROUPE SCHNEIDER

■ Merlin Gerin ■ Modicon ■ Square D ■ Telemecanique

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Note This symbol emphasizes important facts.

Caution This symbol refers to a frequent source of error.

Warning This symbol points to a source of danger that may cause financial or health damage or have other aggravating consequences.

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An example of this is the space following the thousands and the decimal point in the number 12 345.67.

Application Note

Caution The relevant regulations must be observed for control applicatons involving safety requirements.
For reasons of safety and to ensure compliance with documented system data, repairs to components should be performed only by the manufacturer.

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IV Preface

Contents

Chapter 1
Functionality

1.1 Module Overview

The 140 ERT 854 10 is an intelligent 32–point input module for TSX Quantum, featuring fully configurable input processing enhancements, and able to register input signal states of 1 millisecond. Up to 9 ERT's can be mounted in local or remote backplanes for PLC applications, as well as RTU, with Concept V 2.2 upwards.

The 32 inputs are designed for input voltages from 24 – 125 VDC and divided into 2 isolated groups. Each group is provided a separate external reference voltage to influence operating threshold (typically 24, 48, 60, or 125 VDC) and minimum current drain. The module stati Ready, Active, and Fault, as well as the true input (pin) states are clearly displayed through the module's status LEDs.

The 140 ERT 854 10 firmware always processes inputs in four separately–configurable functionality blocks of 8 inputs, each supporting the following user–selectable functionality:

- □ Discrete inputs
  Processed input values, transferred cyclically to the PLC.
- □ Event inputs
  Time–tagged event logging for 1, 2, or 8 processed points, featuring 5–byte time tag, on–board FIFO buffering for 4096 events, and user–acknowledged PLC transfers.
- □ Counter inputs
  32–bit summation of processed events at up to 500 Hz, transferred cyclically to the PLC.

Processing of individual inputs can be fully parameterized: (disabled, inversion, edges monitored, and debounce filter). Event & counter inputs can also apply a configurable chatter filter.

The module clock requires a time synchronization signal and provides a 24 VDC potential input for the following DCF77– formatted time standard receiver modules:

- □ DCF 77E (long wave reception only available in Europe)
- □ 470 GPS 001 (global satellite reception)

The ERT's internal SW clock can alternatively also be set directly from within the user program, or left to run freely.

A validity reserve can be configured, limiting the time during which the module clock may be without external synchronization.

Acquired ERT data can be protected from power failures with a typical drain of 0.07 mA from the XCP 900 00 battery module.

The current internal SW clock time is transferred at relatively large intervals into state RAM, allowing the CPU clock to be set by the user program. For details refer to page 50.

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1.2 User Functions and Services

1.2.1 Input Processing – Registration and Filtration

All input processing is performed as parameterized.

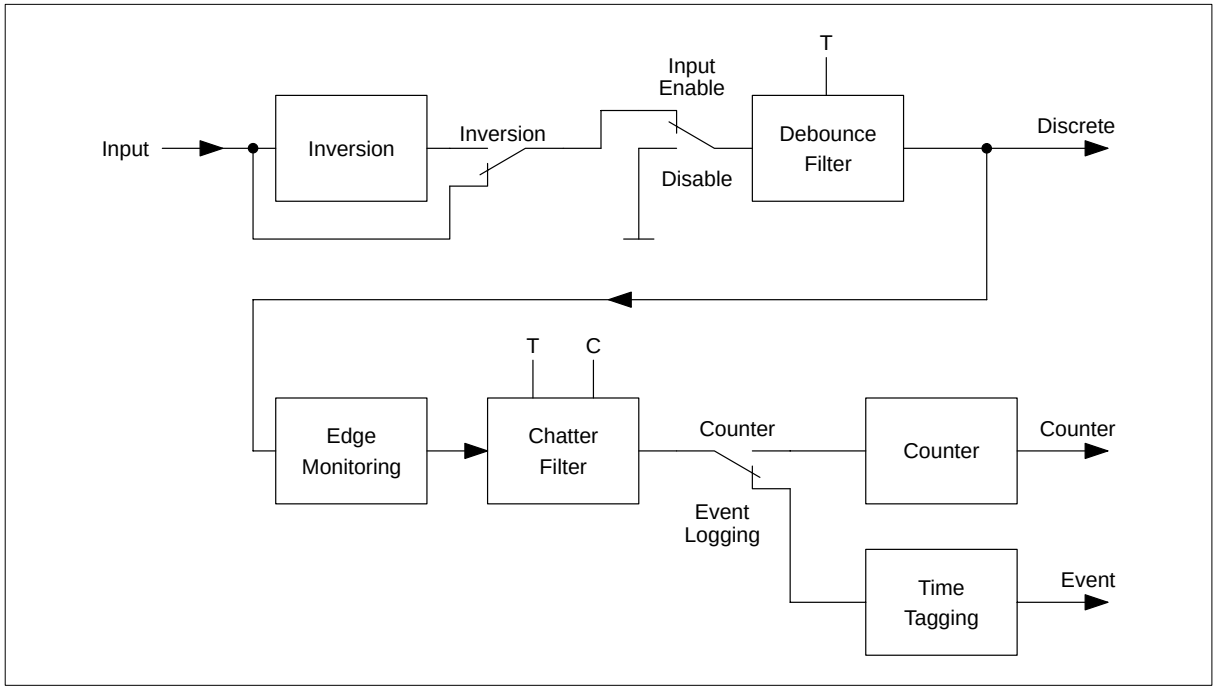

Figure 1 Signal processing order

1.2.1.1 Registration

Input processing can be fully parameterized for individual inputs: (disabled, inversion, edges monitored, and debounce filter time). Event inputs can also apply a configurable chatter filter.

□ Disabled
A disabled input always provides ’0’ regardless of the input state.

□ Inversion
Input polarity is inverted before further input processing. When active, input processing
will use the state opposite that displayed upon the input’s status LED.

□ Edges monitored
Determines the edge transitions to be monitored for active event and counter inputs. ”Both edges” processes rising and falling edges. Otherwise only a single edge is processed: falling/rising for respectively with/without active inversion.

1.2.1.2 Filtration

The configurable filtration is executed in 2 stages: debouncing and dechattering.

Warning The purpose of filtration is to falsify input recognition in a desired fashion. Filtration must be used judiciously however, to prevent an excessive, and unwanted suppression of input data.

Debouncing

Debouncing can be applied for all input functions and prevents the processing of fast input state changes, like those caused by contact bouncing. Signal changes are ignored according to the filter type and time applied. The filter time values range from 0 ... 255 milliseconds; a 0 value deactivates debounce filtering.

The selection of debounce filter type ”steady state” or ”integrating” applies to all 8 functionality block inputs.

□ ”Steady state” filtering
A signal change is only registered when the changed polarity has remained fully stable over the given filter time (every new change resets the filter timer).

□ ”Integrating” filtering
A signal change is only registered after the polarity has remained in the opposite state over a total time span which equals the programmed filter time, inspite of any polarity changes.

Note Debounce time values >=1 millisecond are recommended to provide sufficient immunity to EM disturbances. As a result, input signal states >= 2 milliseconds and events at up to 250 Hz can be processed. In uncritical EM environments the debounce time value can be set to 0, avoiding additional filtration delays. Acquisition of input state changes >= 1 millisecond is then reliable and events up to 500 Hz can be processed.

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Dechattering
Dechattering only applies to event & counter inputs. It limits the number of registered events to a configurable count during a configurable time. The goal is to prevent multiple event registrations for the same input, e.g. a disturbance interfering with a slow changing input (perhaps the comparator hysteresis was chosen to be too small).

The chatter counter is configurable for individual inputs, chatter time for each input pair. The selection of ”dechattering” in the parameter screen enables chatter filtering for all 8 functionality block inputs. Chatter filtering for individual inputs can still be disabled by 0 chatter count values. A ”dechattering active” bit within the ”Status” output word (bit 7 – DC) passed back from the ”ERT_854_10” transfer EFB (refer to the EFB description, Section 3.3) signals that a ”chattering” input is being filtered. The bit is reset as soon as the chatter time of the last actively filtered input has expired.

□ Chatter time
The time period within which the chatter counter limit is effective. Values range from 1 ... 255 * 100 milliseconds = 0.1 ... 25.5 seconds.

□ Chatter count
The maximum number of registered events allowed to pass within the chatter time period. Values range from 1 ... 255, a 0 value deactivates chatter filtering.

Warning Dechattering is a mighty processing tool which may cause undesirable side effects. Its application to counter inputs is especially questionable. In particular for event monitoring of ”both edges”, an odd chatter counter value would only allow an unsymmetrical stream of events to pass for PLC processing (i.e. an ”unmatched” falling or rising edge).

1.2.2 Discrete Inputs

All inputs of the functionality block are passed to the PLC after the third input processing stage (i.e. disabling, inversion, and debounce filtering), but before chatter filtering and edge monitoring. These processed values of **all 32 inputs** are cyclically transferred direct into the first and second input register words of the ERT's seven word 3x–register block every second scan. The mapping sequence of the module inputs is in line with standard discrete input modules, i.e. inputs 1 ... 16 map correspondingly to bits 15 ... 0. User acknowledgment is not required.

It should be stressed that these processed values are available for all 32 inputs, **regardless of the functions selected** for the associated functionality blocks (i.e. counter or event inputs). The input processing is still performed as configured, but the ERT copies processed values from a point immediately after the third input processing stage!

☞ **Note** If the BoolArr32 output array "Input" of the "ERT_854_10" transfer EFB (refer to the EFB description, Section 2.2) is configured, the processed values will also be directly available as Bool values.

1.2.3 Counted Values

All inputs of the functionality block are passed through all five input processing stages (i.e. disabling, inversion, debounce and chatter filtering, as well as edge monitoring). Counting takes place when an edge successfully passes through edge monitoring (one or both edges). For event monitoring which is not for "both edges", the configured inversion decides whether a rising or falling edge is counted.

☞ **Note** Inversion is probably not meaningful for monitoring of "both edges".

Counted values are 32–bit sums. The PLC cyclically receives a complete sequence (as–configured: 8, 16, 24, or 32) of time–consistent counted values in a multiplex procedure from the "ERT_854_10" transfer EFB (refer to the EFB description, Section 2.2. The EFB places the values into the configured UDIntArr32 output array "Cnt_Data" without user acknowledgment. After the

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transfer of new counted values is complete, the EFB sets a 'new data' signal, Bool variable "ND_Count", for one scan.

☞ **Note** Counted value transfer always begins with functionality block 1, and ends with the last functionality block configured as counter inputs. Thus transfer resources are saved when a closed series of functionality blocks is configured for counter inputs, starting with the first. Since counted value transfer also competes with the transfer of logged events, faster reaction times are possible for both types when an ERT module is configured with either counter **or** event inputs. Discrete and status inputs have no influence.

1.2.4 Event Logging

This function binds the high time–resolution registration of functionality block input state changes with correct ordering. The time–tagged logging of events can be configured to respond for a pool of either 1, 2, or 8 processed points.

All inputs of the functionality block are passed through all five input processing stages (i.e. disabling, inversion, debounce and chatter filtering, and edge monitoring). Logging (including time tag fixation) takes place when an edge successfully passes through edge monitoring (one or both edges). For event monitoring which is not for "both edges", the configured inversion decides whether a rising or falling edge is to be logged.

☞ **Note** Inversion is probably not meaningful for monitoring of "both edges".

A pool is registered as an event when at least one point within the pool has successfully passed through edge monitoring, i.e.:

- □ any single input (1, 2 ... 7, 8),
- □ any input of a pair (1–2, 3–4, 5–6, 7–8),
- □ or any input of the block.

Events contain a host of information within an 8 byte block, including the processed values of **all** pool points with their common time tag:

- □ Module number
- □ Type of point pool and number of it’s first bit
- □ The actual pool values
- □ Time tag: milliseconds
- □ Time tag: minute
- □ Time tag: hour
- □ Time tag: day of the week/day of the month

The pool values are stored right–aligned in an event structure byte. The ERT stores events in it’s battery buffered 4096–entry FIFO buffer. The ERT also provides error bits within the ”Status” output word (bits 5/6 – PF/PH) passed back from the ”ERT_854_10” transfer EFB (refer to the EFB description, Section 3.3) for respectively, buffer overflow/buffer half full.

Single events are transferred conditionally to the PLC through the ”ERT_854_10” transfer EFB into a ”ERT_10_TTag” structure. After processing the event the user must actively signal readiness to receive a new event. Refer to the EFB description, Section 3.3.

If desired, the ”Complete time report” parameter can be selected to provide the time values month and year. To this end a special pseudo event without pool values is prepared, containing complete time information with month and year. This event is marked as ”complete time” and must always precede a ”true” event. See the ”complete time” details accompanying(refer to Table 1 on page 17).

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1.2.5 Status Inputs

The ”Status” output word passed back cyclically from the ”ERT_854_10” transfer EFB (refer to the EFB description, Section 3.3) contains the following ERT/EFB error bits:

D8 ... D0 ERT error bits:

D0 =	FW =	firmware error, selftest failure within EPROM, RAM or DPM (fatal module error)
D1 =	FP =	parameterization error (fatal internal error)
D2 =	TE =	external time reference error (time base signal disturbed or missing)
D3 =	TU =	time has become invalid
D4 =	TA =	time not synchronized (free–running clock w/o synchronization)
D5 =	PF =	FIFO buffer overflow (results in loss of newest events)
D6 =	PH =	FIFO buffer half full
D7 =	DC=	dechattering active (results in loss of several events)
D8 =	CE =	ERT communications error (procedural error or time–out)

A subset of these errors can be additionally configured to signalize a composite error with the ”F” LED, and in the module’s error byte within the status table. All others are then defined as warnings.

D11 ... D9 reserved

D15 ... D12 EFB error bits:

1000	= 8 HEX	EFB communication time–out
0101	= 5 HEX	wrong slot
0110	= 6 HEX	health status bit not set (ERT appears to be absent)
other values		internal error

See ”EFB/ERT status word” details in the EFB description , Section 3.3).

After transfer of new status inputs is complete, the EFB sets a ’new data’ signal, Bool variable ”ND_Stat”, for one scan.

☞ **Note** ERT/EFB error messages are displayed in the Concept ”ONLINE EVENT” screen with error number and explanation (see details in the EFB description , at the end of Section 3.3).

1.3 Time Synchronization with Standard Time

Time–tagged event logging requires an accurate internal clock. The ERT module makes use of a software clock to count time in millisecond intervals. This SW clock normally needs to be synchronized through an external time base signal (time standard receiver) in one minute intervals, but can also remain free running.

The incoming time signal is examined for plausibility; any SW clock runtime discrepancies are corrected. The module requires 2 to 3 minutes after start–up before times are provided. This should allow the SW clock to fully synchronize within 3 minutes after initial transmitter reception. This takes longer should the incoming time messages be invalid or absent during this period. Thereafter the module determines the standard deviation of the SW clock with regard to the external time base over a defined period, and compensates the clock accordingly. This takes place continuously during the entire running time. After several hours runtime (as a rule within 2 hours), the SW clock will have reached its maximum precision.

During periods of non–plausible, or failing time messages the SW clock will continue to run without synchronization and thus larger deviation, up to period specified by a configurable ”validity reserve”, before being resynchronized by the next valid incoming time message. Should this period expire before the module receives a valid message, the ERT will set a ”time invalid” bit within the ”Status” output word (bit 3 – TU) passed back from the ”ERT_854_10” transfer EFB (refer to the EFB description, Section 3.3) and invalidate any time tag data made thereafter. The bit is reset as soon as the next valid time message is received.

Should the module not receive a valid time message within 10 minutes, the ERT sets a ”time reference error” bit within the ”Status” output word (bit 2 – TE) passed back from the ”ERT_854_10” transfer EFB (refer to the EFB description, Section 3.3). The bit is reset as soon as the next valid time message is received.

Three synchronization possibilities are provided:

- □ DCF 77E receiver module
  (German standard – long wave reception only in Europe)
- □ 470 GPS 001 satellite receiver providing DCF77–formatted output
  (global satellite reception)
- □ Synchronization from the PLC through the ”ERT_854_10” EFB
  (much lower accuracy).

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DCF time base

The DCF 77E receiver delivers a DCF77–formatted signal at 24 VDC and can supply up to 16 ERT modules in parallel. The BCD coded time signal is transmitted every minute and synchronizes the ERT minute changes. At a new ERT start the internal SW clock is fully synchronized within 3 minutes after initial transmitter reception. Thereafter the accuracy of the ERT's SW clock is fully aligned with the standard time transmitter. If the transmitter signal is unavailable, the synchronized SW clock is still usable with a lower accuracy. The DCF transmitter also delivers daylight savings time; even leap seconds and years are all taken into consideration.

GPS time base

Applications requiring a GPS satellite receiver interface must use a special module with demodulator like the 470 GPS 001. This module demodulates the GPS signal and delivers a DCF77–formatted output signal at 24 VDC. The ERT decodes the signal frames and synchronizes the internal SW clock minute changes. The GPS satellites broadcast UTC time (Universal Time Coordinated) which is essentially GMT (Greenwich Mean Time). Leap seconds and years are taken into consideration, but no account is made for the local time zone. The 470 GPS 001 must be informed of the local time zone to actually perform the adjustment to daylight savings time.

The recommended validity reserve value for DCF/GPS time base signals is1 hour (the setting for DCF/GPS–sync ranges from 1 ... 5 hours).

EFB–synchronized internal clock

If a clock with low accuracy is sufficient, the ERT's internal SW clock can be used alone. Synchronization is performed by a time set transfer from the master. The SW clock is never realigned. Accuracy is typically lower than 100 milliseconds per hour and the SW clock must be synchronized often. The "ERT_854_10" transfer EFB provides the necessary time synchronization. It can supply multiple ERT modules with nearly the same time, using the ESI 062 00 module's "DPM_Time" derived data structure as time source.

The validity reserve value setting for the EFB–synchronized internal SW clock ranges from 1 ... 254 hours. Should this period expire before the next time set transfer takes place, the ERT will set a "time invalid" bit within the "Status" output word (bit 3 – TU) passed back from the "ERT_854_10" transfer EFB , Section 3.3) and invalidate any time tag data made thereafter. The bit is reset as soon as the next time set transfer takes place.

Free–running internal clock

A validity reserve value setting of 0 with the internal SW clock marks the **free running** modus which is designated by a set ”time not synchronized” bit within the ”Status” output word (bit 4 – TA) passed back from the ”ERT_854_10” transfer EFB , Section 3.3. There is no validity reserve to ”expire” and thus no time tag invalidation. The ”external reference error” and ”time invalid” bits within the ”Status” output word (bits 2/3 – TE/TU) are never set. The default initial internal clock setting is 0 hours, 1/1/1990. The time can be set using the ESI 062 00 module’s ”DPM_Time” derived data structure as time source.

☞ **Note** Use of the free–running internal SW clock still allows meaningful event sequence processing to be made within the scope of a single ERT.

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1.4 Typical Application Areas

The following areas of applicability result for the 140 ERT 854 10:

- □ Discrete input processing
  Use as a standard I/O module (with filtering) and an input range of 24 – 125 VDC.

- □ Event logging
  The occurrence of particular process states can be recorded with the corresponding time of day (time tagging). This allows a later reconstruction of when, and in which sequence, particular process signals ”came” or ”dropped”.

- □ Counted values
  Use as a standard I/O module (with filtering, 32–bit sums, and max. 500 Hz) having an input range of 24 – 125 VDC.

- □ Periodic time–tagging of process values
  Logging of counted values in defined time intervals. The combined use of both functionality groups can be used here to advantage.

- □ Time–dependent switching actions
  Outputs can be time–dependently set for control of lighting, heating, ventilation, temperatures (building electrification) or for enabling/disabling doors, machines, ... (security measures). These output states can be logged with the ERT.

Chapter 2
140 ERT 854 10 Configuration

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2.1 Parameter Screen

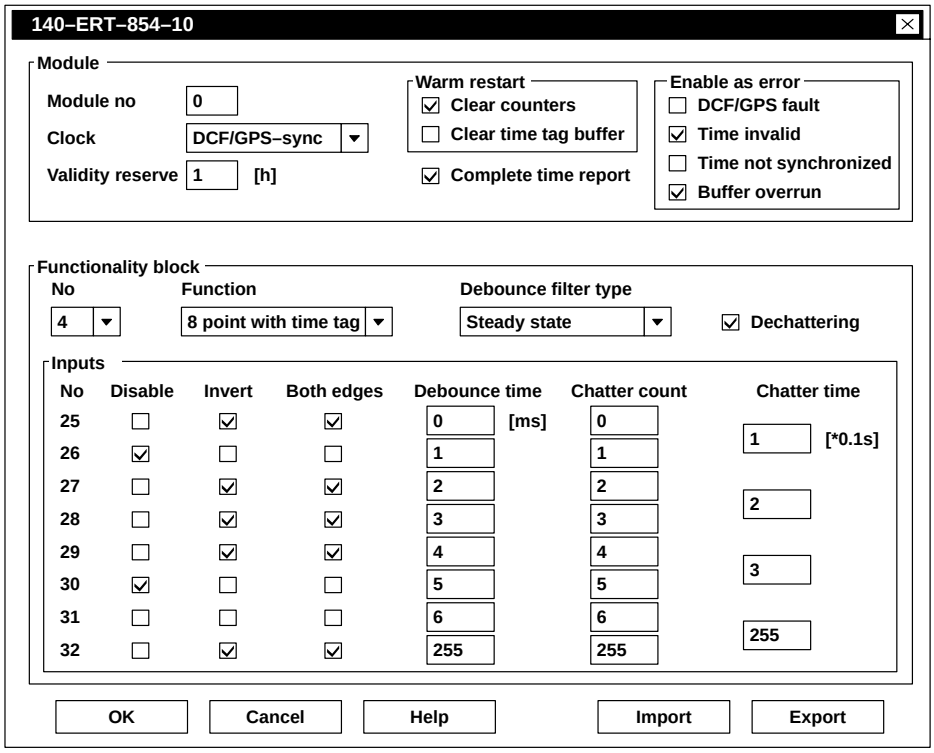

Figure 2 Parameter Screen Layout

The parameter screen consists of 4 pages, each with common parameters for the module and separate parameters for each functionality block. Parameters are preset in the ”I/O map” with a default set of values and can be edited by the user. The export function saves the module’s parameter set into a (*.ert) file, from which import can then reload the parameters. (These files are also usable as an interface to an off–line parameter tool). Editing of parameter data is only possible while the user program is halted.

Table 1 List of parameter items and default values

Name	Default value	Range	Function
Module			
Module no	0	1... 127	User defined, will be inserted in events. Uniqueness of the value will be not checked. 0 = default, i.e. no selection chosen
Clock	DCF/GPS–sync	DCF/GPS–sync	External synchronization with DCF77–formatted time base signal from a DCF or GPS receiver.
		Internal clock	Synchronized by time structure input to EFB: The clock is either free running or monitored within a configured validity reserve.
		No	Internal clock is disabled
Validity reserve	1 hour	1 ... 5 hours	DCF/GPS–sync: 1 hour is recommended
		1 ... 254 hours	Internal clock: time since last synchronization until TU bit set in Status and time tags are invalid
		0	Internal clock: 0 = free running modus without expiration (TE/TU bits are never set)
Complete time report	y	n/y	Provides a complete time (with month and year) for internal clock synchronization purposes. Transfer is made: after module new start, change of month, at each PLC user program start/stop, on event FIFO buffer clearing, or internal clock start/set, but must ALWAYS have a true event to ”precede” and may thus remain ”stuck” in the ERT.
Warm restart: Clear counters	n	n/y	Counters are initialized to 0 at warm restart
Warm restart: Clear time tag buffer	n	n/y	Contents of the event FIFO buffer are purged at warm restart
Enable as error: DCF/GPS fault Time invalid Time not synchronized Buffer overrun	 n y n y	n/y	Error conditions which should light error ”F” LED: Enabled items are handled as errors. Any disabled items are still treated as warnings. (The module selftest is always an error).
Functionality block			The following items are all applicable to specific functionality blocks (i.e. 4 separate masks)
No	1	1....4	Number of the selected functionality block
Function	1 point with time tag	Discrete Counter 1 point with time tag 2 point with time tag 8 point with time tag	Only discrete inputs Discrete + counted values Discrete + 1 point event logging Discrete + 2 point event logging Discrete + 8 point event logging
Debounce filter type	Steady state	Steady state Integrating	Debounce filter type
Dechattering	n	n/y	Disable/enable chatter filter

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Table 1 List of parameter items and default values

Name	Default value	Range	Function
Inputs			The following items all apply to a single input **(Caution: chatter time affects an input pair)**
No	1 – 8	1 – 8, 9 – 16, 17 – 24, 25 – 32	Input number sequences for the selected functionality block
Disable	n	n/y	Disables input processing for the input (input value then remains fixed as 0)
Invert	n	n/y	Input polarity inversion
Both edges	y	n/y	Edge monitoring for both edges
Debounce time	1	0 .. 255	Debounce time 0 ... 255 milliseconds 0 = without any internal SW delay
Chatter count	0	0 .. 255	Chatter count 0 ... 255 (for event/counter inputs) 0 = chatter filtering deactivated
Chatter time	1	1 .. 255	Chatter filter time period 1 ... 255*0.1 seconds (**Caution:** applies to an adjacent pair of inputs!)

Warning In regard to a running ERT whose backplane is equipped with the XCP 900 00 battery module: transfer of parameter sets (i.e. parameterization) will always initiate an ERT warm restart as usual. Any changes to the active ERT process data acquisition characteristics will cause all of the acquired events and counted value states to be purged and re–initialized to defined states, since their registration was based upon factors contradictory to the new parameter set. Details can be found in Section 3.3.

Chapter 3
Commissioning the ERT 854 10

3.1 140 ERT 854 10 Module Limitations and Resource Constraints

All of the following items should be accepted as being tolerable before beginning the actual configuration:

- ☐ Concept V 2.2 upwards
- ☐ Usable in local or remote backplanes (RIO) with RIO drop firmware newer than V 1.20
- ☐ Not usable in DIO drops
- ☐ Up to 9 ERT's can be mounted in local or remote backplanes
- ☐ Able to process signal states > 1 millisecond + filtration time
- ☐ Counter inputs at up to 500 Hz with 32–bit summation
- ☐ Each ERT requires an "ERT_854_10" transfer EFB
- ☐ 7 IN words, 5 OUT words per ERT
- ☐ Several ERT modules may be connected to a single time standard receiver. The 140 ERT 854 10 draws 5 mA from the receiver
- ☐ Maximal drain of 0.07 mA from the XCP 900 00 battery module for counters, event FIFO buffer, and parameter set data retention.

3.2 Time Standard Receivers

Time standard receivers must provide a DCF77–formatted output signal at 24 VDC.

Use may be made of the following time standard receivers:

□ A DCF long wave receiver for Europe
□ A GPS satellite receiver

3.2.1 The DCF Receiver

The DCF 77E module serves as receiver with integrated antenna.

The module receives and converts the received time base signals into the German DCF77 format, amplifying it before passing it on to the 140 ERT 854 10 module.

DCF Signal
The DCF signal available in central Europe is called DCF77 and provides MET (Middle European Time). It is derived from an atomic clock standard at the Physikalisch–Technischen Bundesanstalt in Braunschweig, Germany and transmitted over a station in Mainflingen at a long wave frequency of 77.5 kHz, (and thus the name). It can be received in all of middle Europe (roughly 1000 km around Frankfurt).

When selecting an antenna mounting site, take the following sources of disturbance into account which can significantly impair, or even block, the reception of your DCF receiver:

□ EMC–ridden sites
Avoid the vicinity of potential sources of interference such as strong transmitters, switching stations, and airports. Strong interference can also be caused by large construction machinery and cranes.

□ Steel reinforcement in buildings, rooms and housing
Bad reception can be found in e.g. basements, underground parking, and closed service cabinets.

□ ”Shadows” & ”dead spots” of mountains, large buildings, ...

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3.2.2 The GPS Receiver

The 470 GPS 001 00 module functions as GPS receiver. Other conventional GPS time standard receivers are also usable. The only requirement being that the supplied GPS signal be in DCF77 format with 24 VDC potential.

GPS Signal
A host of dedicated, low polar–orbiting GPS (Global Positioning System) satellites broadcast GPS signals. Their orbits are distributed evenly in space, so that virtually every point of the earth's surface is within the transmission range of at least three different satellites at any given time. The GPS signal is thus available world–wide. The absolute time accuracy derivable from GPS signals is somewhat better than that provided by DCF receivers.

The satellites broadcast UTC time (Universal Time Coordinated) which is essentially GMT (Greenwich Mean Time). Leap seconds and years are taken into consideration. The 470 GPS 001 must be informed of the local time zone to actually perform the adjustment to daylight savings time.

Calendar, and time of day data are evaluated from the GPS signal and passed on to the 140 ERT 854 10 module.

As a rule, the antenna must be procured separately from the GPS receiver. Read the particulars in your receiver's data sheet.

When selecting an antenna mounting site, take the following sources of disturbance into account which can significantly impair, or even block, the reception of your GPS receiver:

- □ EMC–ridden sites
  Avoid the vicinity of potential sources of interference such as strong transmitters, switching stations, and airports.

- □ Unrestricted view to the heavens and horizon
  The antenna must be mounted outdoors to guarantee noise–free operation. Closed rooms or service cabinets block satellite reception.

- □ Antenna cable length
  Don't exceed the permissible length of the antenna cable.

- □ Atmospheric conditions
  Heavy snow–fall and strong rain can impair, or even block, the reception of your GPS receiver.

3.3 Start/Restart Behavior and Data Retention

Cold start This is the default ERT behavior upon the return or initial availability of a stable supply voltage.

- □ All acquired events, counted value states, and the ERT's current parameter set are are initialized to defined states.
- □ Acquisition of process data is delayed until the PLC has started and provided the ERT with a valid parameter set.
- □ Since the ERT has no hardware clock, the internal SW clock is invalid until some form of synchronization has taken place:
  - □ Depending upon the configured clock synchronization source, time tags of registered events will contain invalid times up until: either the internal clock has been set from the DPM_Time fed to the EFB, or 2 ... 3 minutes after synchronization was successful from an external time base signal.
  - □ A special case exists, should the ERT's "Clock" parameter have been configured as an "Internal clock" in **free running** modus (with a validity reserve value of zero), the internal clock is set initially to 0 hours, 1/1/1990.
- □ When a "Complete time report" is configured, a complete time transfer is performed immediately preceding the next registered event after successful clock synchronization.

ERT 854 10 resident data can be protected from power failures when the backplane is equipped with the XCP 900 00 battery module. As a defined–response to a supply voltage below a given level recognized by the backplane, acquired events, counted value states, and the ERT's current parameter set are all transferred under firmware control into on–board, non–volatile RAM for use at the next **warm restart** (see below). Situations preventing backplane reaction to such changes from reaching the ERT (5 VDC short–circuit, or hotswap of the ERT module), will always result in a subsequent **cold start** for the ERT.

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Warm restart The return of a stable supply voltage initiates an ERT module **warm restart** when the module was able to consistently secure it's resident data.

- □ All acquired events, counted value states, and the ERT's current parameter set are restored under firmware control from on–board, non–volatile RAM.
- □ If required by the parameter set's configured "Warm restart" parameters ("Clear counters"/"Clear time tag buffer"), the acquired events or counted value states will be purged.
- □ The acquisition of process data by the ERT continues immediately with the same parameter set, even when the PLC or remote connection has not yet recovered.
- □ Since the ERT has no hardware clock, the internal SW clock is invalid until some form of synchronization has taken place:
  - □ Depending upon the configured clock synchronization source, time tags of newly–registered events will contain invalid times up until: either the internal clock has been set from the DPM_Time fed to the EFB, or 2 ... 3 minutes after synchronization was successful from an external time base signal.
  - □ A special case exists, should the ERT's "Clock" parameter have been configured as an "Internal clock" in **free running** modus (with a validity reserve value of zero), the internal clock is set initially to 0 hours, 1/1/1990.
- □ When a "Complete time report" is configured, a complete time transfer is performed immediately preceding the next registered event after successful clock synchronization.
- □ When the appropriate "ERT_854_10" transfer EFB becomes active again in the PLC, the transfer of FIFO–buffered events and counted value states retained by the ERT will resume. Current discrete input values and Status words will also be transferred.
- □ Should the PLC however, later provide a new, valid parameter set reflecting changes to process data acquisition characteristics, then all of the acquired events and counted value states would be purged and re–initialized to defined states, since their registration was based upon factors contradictory to the new parameter set.

3.4 Check List

The following steps should be carried out to successfully put the 140 ERT 854 10 into service:

Step 1 Mount the 140 ERT 854 10 module within the local or remote backplane.

Step 2 Connect the foreseen process peripherals and time standard receiver to the module (refer to the 140 ERT 854 10 Module Description). Don't forget to provide suitable reference input voltages to the ERT input groups.

Pay special attention that the time standard receiver antenna installation tips are respected.

Step 3 Enter the 140 ERT 854 10 in the I/O map.

Be sure to take into account that the module requires seven 3x–registers and five 4x–registers in state RAM.

Step 4 Configure the 140 ERT 854 10 through the appropriate parameterization screens to provide the required functionality.

Step 5 Make use of the proper ANA_IO library EFB to supply the "Slot" input parameter for the "ERT_854_10" transfer EFB: either "QUANTUM" for local, or "DROP" for remote backplanes.

Step 6 Apply the "ERT_854_10" transfer EFB from the EXPERTS library to transfer data from the ERT.

Define the EFB user data structures of the required types. Events can be "consumed" for example, by being protocolled to printer or stored in a centralized data base.

☞ **Note** The transfer of a new event by the "ERT_854_10" EFB overwrites the previous event information. The user acknowledgment should thus only be given after the data has been fully evaluated and no longer required.

Step 7 Remember to take the ERT's start/restart behavior into account, based upon whether the backplane is equipped with the XCP 900 00 battery module.

Breite: 185 mm
Höhe: 230 mm

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Chapter 4
Operating the ERT 140 854 10

The chapter deals with the following topics:

- ☐ General information
- ☐ Configuration EFBs
- ☐ Section Examples

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4.1 General Information

This section will present handling guidelines for those EFBs necessary to ERT 854 10 module operation. The EFBs are designed to enable configuration of the FBD program, which is largely independent of the hardware module used. Hardware–dependent configuration EFBs (Group: Quantum IO Config) are used to evaluate project–specific information on the PLC and provide access to configuration data. This means that changes in direct addresses or changes in input/output parameters can be detected automatically by the EFBs. The ERT_854_10 data transfer EFB operates with these data structures to read the ERT–processed values from the input words (3x), and write ERT handshake and clock synchronization data to the output words (4x). As the detection of configuration data only occurs once after loading, it is highly advisable to separate the hardware–dependent configuration EFBs into a special section.

The separation of execution into at least two sections is advisable:

- Configuration section
- Processing section

This division into a configuration section and processing section can lead to a significant CPU load reduction, as the configuration–related part (configuration section) is only executed once, eg. after loading. As a rule, the processing section must be executed continuously. The configuration section is controlled by the EN inputs of this section's individual EFBs. The EFBs are enabled by an unlocated variable which is set to 1 at the first cycle.

4.2 Configuration EFBs

Configuration data from analog input/output, and ERT 854 10 modules is accessed using EFBs from the ”Quantum IO Config” block library group within the ANA_IO library.

To do this, place a single QUANTUM EFB in the configuration section (CfgErt).

The configuration data from remote I/O (RIO) is accessed via an DROP EFB. Connect the DROP EFB to the slot on the RIO communication module. Each I/O station has its own number. Specify this number at the NUMBER input of the DROP EFB.

Each ERT 854 10 module has its own ERT_854_10 data transfer EFB. Connect the EFB to the corresponding slot on the QUANTUM or DROP EFB.

Note Do not specify literals at the slot inputs of the configuration EFBs. SLOT inputs must be connected to SLOT outputs.

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4.3 Section Examples

Configuration Section
Processing Section

4.3.1 Configuration Section

The configuration section is used to configure the ERT modules and controls the data exchange between the ERT_854_10 EFB, the state RAM and the configuration data.

The configuration section should be called ”CfgErt” and the unlocated variable for enable control should be called ”CfgErtDone” in order to ensure compatibility with future ConCept versions. Control of the configuration section can be achieved in 2 fashions:

- Control of the configuration section can be achieved through the EN inputs of the individual EFBs within this section. EFBs are then enabled through the SYSSTATE EFB, whose COLD or WARM outputs are set to 1 for a single scan after a coldstart, resp. warm restart.

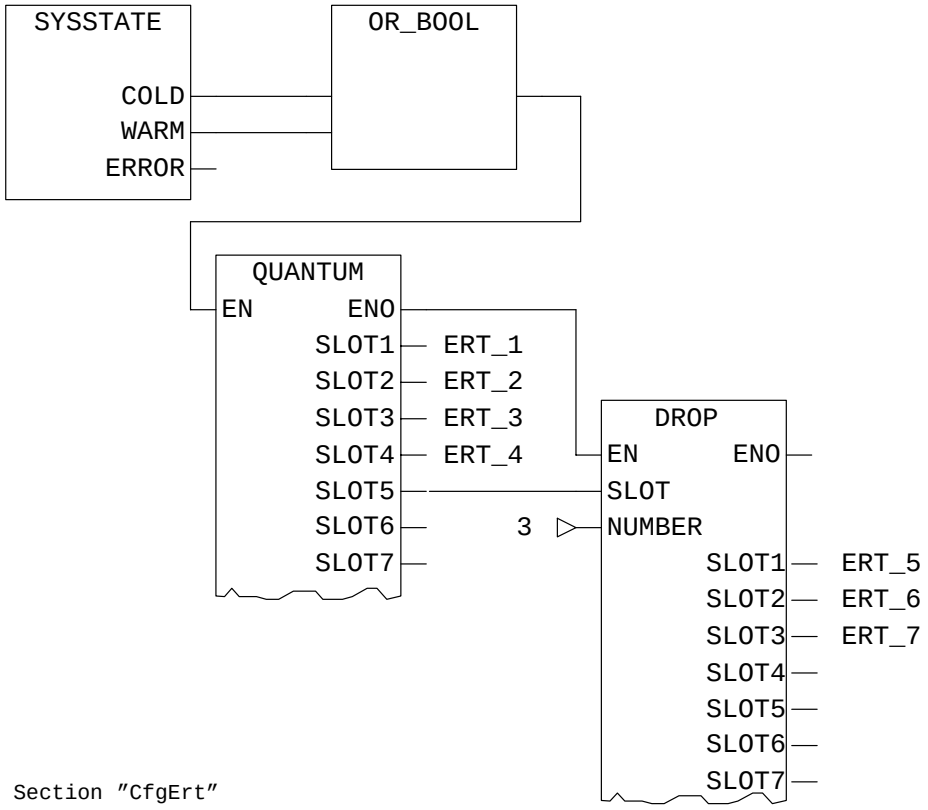

Figure 3 Example of a ”CfgErt” configuration section

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□ Control of the configuration section can also be achieved through the section enable and disable (also refer to the ”Section” chapter in the Concept User Manual, Volume 1). The configuration section enable is derived in a separate section from the SYSSTATE EFB, whose COLD or WARM outputs are set to 1 for a single scan after a coldstart, resp. warm restart. This 1–signal can be applied to enable and disable the configuration section. Daisy–chaining of EFB EN and ENO signals is not necessary for this approach.

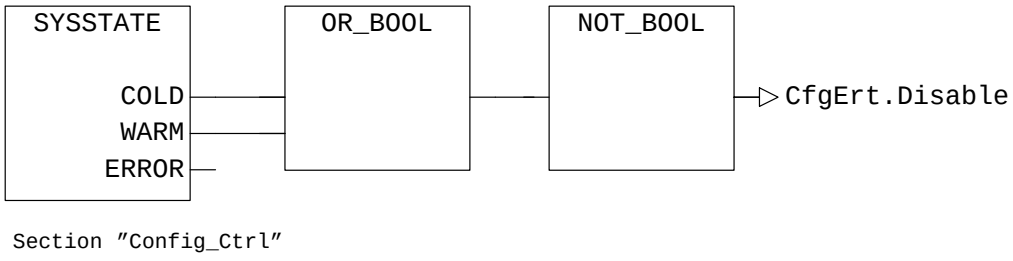

Figure 4 Example of a ”Config_Ctrl” control section

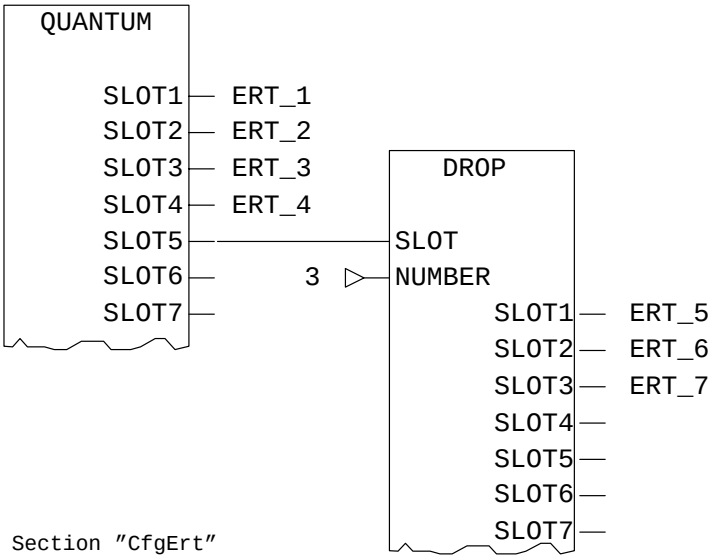

Figure 5 Example of a ”CfgErt” configuration section

4.3.2 Processing Section

The processing section is used for the actual processing of ERT–generated values. The following processing section example makes use of a ”SLOT” parameter value for its single ERT_854_10 EFB which could have been derived from either Figure 3 or Figure 5. Refer to the ERT_854_10 data transfer EFB section in Appendix A (starting at page 40).

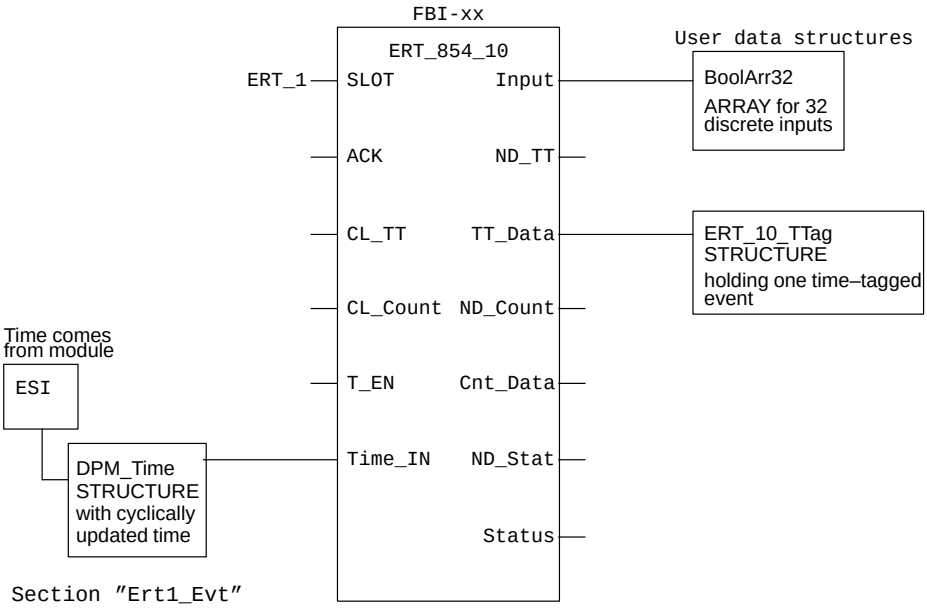

Figure 6 Typical processing section implementation of an ERT_854_10 EFB for a local backplane

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Appendix

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Appendix A
EFBs for 140 ERT 854 10

In this appendix the EFB's relevant to 140 ERT 854 10 operation are presented alphabetically:

- ☐ DROP: Configuring an I/O station subrack
- ☐ ERT_854_10: ERT854 10 data transfer EFB
- ☐ QUANTUM: Configuring a local backplane

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DROP: Configuring an I/O station subrack

1 Brief Description

The function block is used to edit the configuration data of a remote or distributed I/O station for subsequent processing by module configuration EFBs.

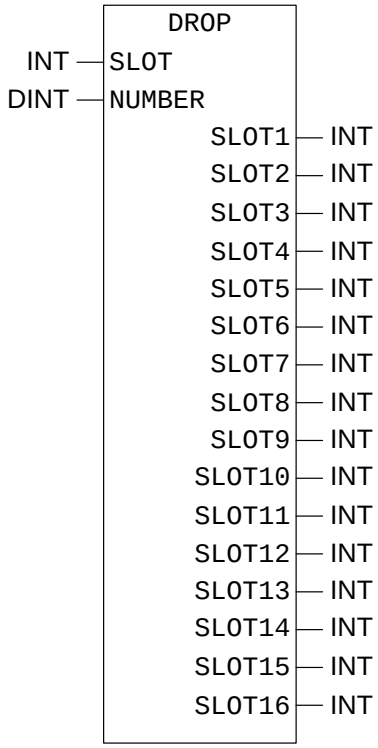
For configuration of an I/O station subrack, the DROP function block in the configuration section is connected to the corresponding SLOT output of the QUANTUM function block. The number of the I/O station defined in the I/O map has to be entered at the NUMBER input of the DROP function block. The function blocks for configuration of the analog modules of the I/O stations are connected to the SLOT outputs.

Additional parameters EN and ENO may be configured.

This EFB can be found in the ANA_IO library.

2 Representation

2.1 Symbol



2.2 Parameter Description

Parameters	Data type	Meaning
SLOT	INT	Slot for RIO, DIO, NOM
NUMBER	DINT	Number of RIO, DIO, NOM
SLOT1	INT	Slot 1
:	:	:
SLOT16	INT	Slot 16

3 Runtime Errors

If no ”Head” has been configured for the I/O station subrack, an error message appears.

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Höhe: 230 mm

ERT_854_10: ERT 854 10 data transfer EFB

1 Brief Description

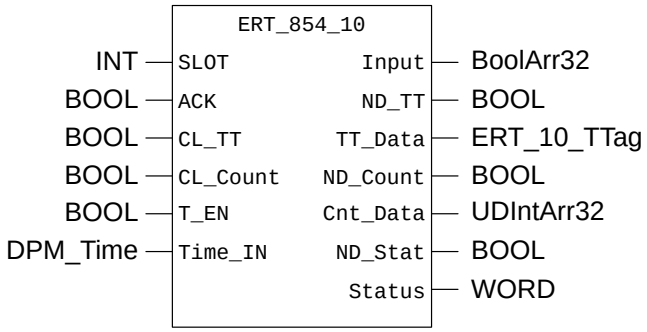
The mandatory ERT_854_10 EFB is able to autonomously coordinate the flow of multiplexed data from the ERT to the PLC through the IN and OUT reference registers. It also temporarily stores the intermediate counter data in an internally allocated memory region until the data is complete, so that the instruction list is presented a consistent set of counter values. A type–specific new data flag is always set after an input data type has been copied into the appropriate EFB output structure.

Additional parameters EN and ENO may be configured.

This EFB can be found in the EXPERTS library.

2 Representation

2.1 Symbol



2.2 Parameter Description

Parameter	Data Type	Meaning
SLOT	INT	Slot index as supplied by either the QUANTUM or DROP EFB to the ERT data, containing the configured IN and OUT references (3x– and 4x–registers)
ACK	BOOL	Event acknowledgment: setting ACK signals user readiness to receive the next event, releasing TT_Data. If ACK remains set, ”continuous operation” results.
CL_TT	BOOL	Clear the ERT’s event FIFO buffer by setting CL_TT. Event registration is blocked until CL_TT returns to 0.
CL_Count	BOOL	Clear all ERT counters by setting CL_Count. Counting is halted until CL_Count returns to 0.
T_EN	BOOL	Enables time transfers from ESI over Time_IN when set
Time_IN	DPM_Time	Input time structure from ESI for ERT time synchronization (carrying edge–triggered time synchronization in element ”Sync”)
Input	BOOLArr32	Output array for all 32 discrete inputs as BOOL (Also available as word references in 3x–registers 1+2)
ND_TT	BOOL	New time tag data in TT_Data flag: remains set until acknowledged by user through ACK
TT_Data	ERT_10_TTag	Time tag data output structure holding an event when ND_TT is set (user–released when ACK is set)
ND_Count	BOOL	New counter data in Cnt_Data flag: only on for 1 scan
Cnt_Data	UDIntArr32	Output array for 32 counter values (overwritten en–bloc after the EFB has received a complete sequence of (as–configured: 8, 16, 24, or 32) time–consistent counted values
ND_Stat	BOOL	New status data in Status flag: only on for 1 scan
Status	WORD	Output word for EFB/ERT status

DPM_Time structure for ERT internal clock synchronization through an ESI:

Element	Element Type	Meaning
Sync	BOOL	Clock synchronization on pos. edge (on hour or by command)
Ms	WORD	Fine time in milliseconds
Min	BYTE	Time invalid / Minutes
Hour	BYTE	Daylight savings time / Hours
Day	BYTE	Day of the week / Day of the month
Mon	BYTE	Month
Year	BYTE	Year

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ERT_10_TTag event structure with 5–byte time tags:

Element	Element Type	Meaning
User	BYTE	Complete time / User number [module number]
Input	BYTE	Event pool type / No. of first input point
In	BYTE	Event data: 1, 2, or 8 processed points
Ms	WORD	Fine time in milliseconds
Min	BYTE	Time invalid / Minutes
Hour	BYTE	Daylight savings time / Hours
Day	BYTE	Day of the week / Day of the month

3 Detailed Description

Mode of Functioning
EFB Configuration
Data Flow
Simple Example
Other Services
Using the DPM_Time Structure for ERT Internal Clock Synchronization
Application Examples: Making use of the ERT –>EFB Time Data Stream

3.1 Mode of Functioning

The number of I/O words available in local and remote backplanes is limited to 64 IN and 64 OUT. This limits the usable number of ERT modules per local/remote backplane to 9 with the currently chosen minimal requirements of 7 IN and 5 OUT words per module.

The size of the required ERT data transfers is substantially larger:

- 32 counters = 64 words,
- an event with 5–byte time tag = 4 words,
- 32 discrete values and the ERT status = 3 words.

This size conflict dictates the use of a specialized transfer EFB named ERT_854_10 to perform the necessary handling on the PLC side to accommodate the ERT's presentation of data in a multiplexed fashion. One such EFB is required for each ERT module.

As a convenience, only those EFB parameters need be configured which will be actually used. This can save considerable configuration effort, especially when counter and event inputs are not mixed. Unfortunately memory is not saved, as Concept links open outputs to invisible dummy variables.

Basic ERT_854_10 IN register block structure, consisting of seven 3x–registers for ERT to PLC transfers

Containing	Function
Discrete inputs 1 16	Discrete processed input data, cyclically updated (module input mapping sequence is in line with standard discrete input modules, i.e. inputs 1 ... 16 map correspondingly to bits 15 ... 0)
Discrete inputs 17 32	
Transfer status	IN transfer status (TS_IN)
MUX 1	Multiplex–data block for array transfers, either:
MUX 2	1 Event with 5–byte time tag or
MUX 3	2 Counter values of the configured max. of 32 or
MUX 4	1 Status word

Simplified ERT_854_10 OUT register block structure, consisting of five 4x–registers for PLC to ERT transfers

Containing	Function
Transfer status	OUT transfer status (TS_OUT)
MUX 1	Time data block to ERT for clock synchronization
MUX 2	
MUX 3	
MUX 4	

3.2 EFB Configuration

The EFB attachment to the IN and OUT references (3x– and 4x–registers) is made through a graphical link to the ERT slot no. in the same manner as for analog modules. The presently available QUANTUM and DROP EFBs from the ANA_IO library are used: QUANTUM for local, and DROP for remote backplanes. These EFBs are able to supply integer indexes to the ERT data structures holding the configured values for a specific slot. The module parameters and id can be found there, in addition to addresses and lengths of the allocated IN and OUT references (3x– and 4x–registers).

A significant runtime savings can be realized by disabling the QUANTUM or DROP EFB after a first execution.

3.3 Data Flow

Discrete inputs
Counter inputs
Event inputs
Status inputs

Discrete inputs

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There is **no** new data flag provided for this input type. The discrete inputs in the first and second input register words are directly updated by the ERT, typically in each second scan – the EFB is however still involved. The EFB makes the processed values available as Bool if the BoolArr32 output array has been correspondingly configured.

Counter inputs
The cyclic update of counted values takes significantly longer than other types. Counted values are stored en–bloc in ”Cnt_Data” after a complete sequence (as–configured: 8, 16, 24, or 32) of time–consistent counted values have been transferred in a multiplex–fashion from the ERT. The ”ND_Count” new data flag is set for one scan.

Event inputs
Since the user must actively acknowledge readiness to receive a new event, flag handling is somewhat complexer (requiring a handshake mechanism). Event data remains in the ERT_10_TTag structure and the ”ND_TT” new data flag set, until the user sets the ”ACK” input requesting a new event. The EFB then responds by resetting ”ND_TT” for at least one scan. After transferring the new event into the ERT_10_TTag structure, ”ND_TT” is set again by the EFB. To prevent the new event data from being overwritten, the user must be sure to always reset the ”ACK” input after the EFB has reset the ”ND_TT” new data flag. This state can then remain stable to provide the user program time for event processing as required. Any subsequent events logged by the ERT will be buffered internally in it’s event FIFO buffer.

New events will be transferred in intervals of at least 2 scans directly from the EFB’s internal event buffer as long as the **”ACK” input remains set** (for the specialized **continuous operation** mode), which in turn causes ”ND_TT” to only remain set for one scan. In this special mode however, it still remains the responsibility of the user program to complete event processing before ”ND_TT” signals transfer of another new event into the ERT_10_TTag structure, since no handshake–protection is offered by ”ACK” in this case.

ERT_10_TTag event structure with 5–byte time tags

Byte	Type	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Byte	CT	Module no. 0 ... 127							Complete time: CT = 1 indicates that this time tag is a ”complete time” having month and year values in bytes 2 & 3 / Module no. can be arbitrarily chosen in the parameterization screen
2	Byte	P2	P1	Input no.						Event pool type (P2, P1): 1 ... 3 / No. of event pool’s first input point: 1 ... 32 ***)** [Month value when CT = 1]
3	Byte	Event pool data (D7... D0, right aligned)								Either 1, 2, or 8 processed points [Year value when CT = 1]
4	Byte	Fine time (L)								0 ...
5	Byte	Fine time (H)								59999 milliseconds (max. 61100) ****)**
6	Byte	TI	R	Minutes						Time invalid: TI = 1 for an invalid time / Reserved = 0 / Minutes: 0 ... 59 *****)**
7	Byte	DS	R	R	Hours					Daylight savings time: DS = 1 indicates a time adjusted for daylight savings / Hours: 0 ... 23
8	Byte	DOW			DOM					Weekday: Mo–So = 1 ... 7 / Day of month: 1 ... 31

***)** D7, D6 = Event pool type: 01 = 1 point; 10 = 2 points; 11 = 8 points
D5 ... D0 = Number of the event pool’s first input point: 1 ... 32 = Actual input pin number; 1, 3, 5, ... 31 = First input point in the pool; 1, 9, 17, 25 = First input point in the pool

****)** The fine time value for leap–seconds can approach 61100 milliseconds (respecting a tolerance of 100 milliseconds)

*****)** In time tags containing an invalid time (TI = 1), fine time is set to FFFF HEX. Minutes, Hours, and DOW/DOM values are invalid (i.e. undefined).

When ”Complete time report” has been enabled during ERT configuration, a transfer of complete time (with month/year) is made under the following circumstances: after change of month, module new start, at each PLC user program start/stop, on clearing the ERT’s event FIFO buffer, or clock start/set. The transfer of this special pseudo event without pool values must ALWAYS have a true event to ”precede” and may thus remain ”stuck” in the ERT when no events are outstanding. Within the time tag of a ”complete time” the CT bit is always set, byte 2 holds month, byte 3 the year, and bytes 4 ... 8 mirror the time tag values from the true event which it must precede.

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Status inputs
The ”ND_Stat” new data flag is set for one scan. Status inputs can be overwritten again after 2 scan cycles.

EFB/ERT status word internal structure:

EFB error bits					**ERT error bits**										
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CE	DC	PH	PF	TA	TU	TE	FP	FW

D8 ... D0 ERT error bits:

D0 =	FW =	firmware error, selftest failure within EPROM, RAM or DPM (fatal module error)
D1 =	FP =	parameterization error (fatal internal error)
D2 =	TE =	external time reference error (time base signal disturbed or missing)
D3 =	TU =	time has become invalid
D4 =	TA =	time not synchronized (free–running clock w/o synchronization)
D5 =	PF =	FIFO buffer overflow (results in loss of newest events)
D6 =	PH =	FIFO buffer half full
D7 =	DC=	dechattering active (results in loss of several events)
D8 =	CE =	ERT communications error (procedural error or time–out)

A subset of these errors can be additionally configured to signalize a composite error with the ”F” LED, and in the module’s error byte within the status table. All others are then defined as warnings.

D11 ... D9 reserved

D15 ... D12 EFB error bits:

1000	= 8 HEX	EFB communication time–out
0101	= 5 HEX	wrong slot
0110	= 6 HEX	health status bit not set (ERT appears to be absent)
other values		internal error

The following ERT/EFB error messages are displayed in the Concept ”ONLINE EVENT” screen with error number and explanation:

EFB error messages:

–2710	[User Error 11] =	EFB communication time–out
–2711	[User Error 12] =	EFB internal error
–2712	[User Error 13] =	EFB internal error
–2713	[User Error 14] =	EFB internal error
–2714	[User Error 15] =	EFB internal error
–2715	[User Error 16] =	wrong slot
–2716	[User Error 17] =	health status bit not set (ERT appears to be absent)
–2717	[User Error 18] =	EFB internal error

ERT error messages:

–2700	[User Error 1] =	ERT internal error
...	...	...
–2707	[User Error 8] =	ERT internal error

3.4 Simple Example

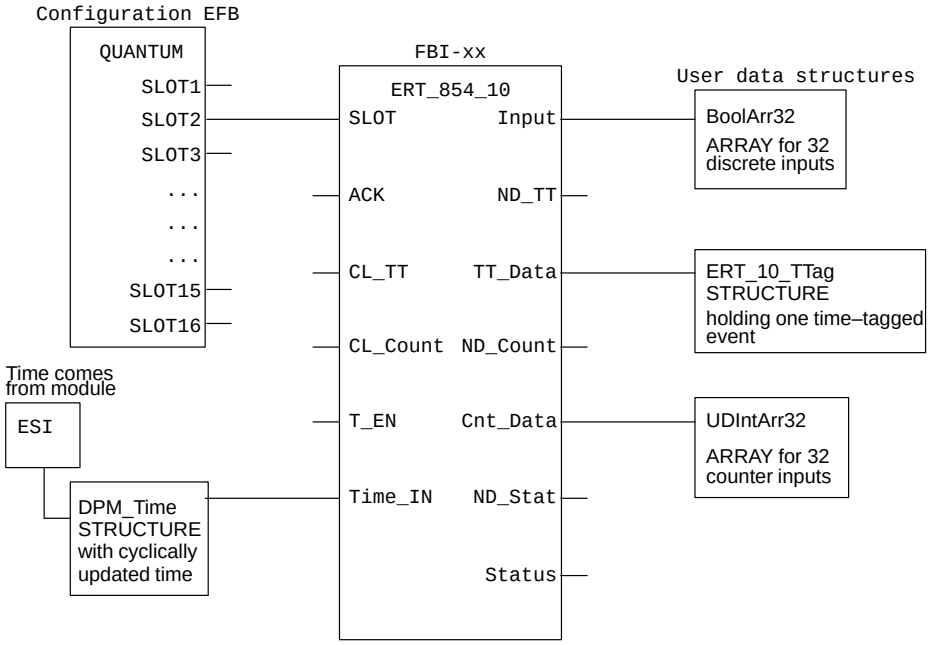

Figure 7 ERT_854_10 EFB connections

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3.5 Other Services

Setting the ”CL_TT” input flag requests that the ERT’s event FIFO buffer be cleared by the EFB. Setting the flag for one scan is sufficient.

Setting the ”CL_Count” input flag requests that the ERT counters be cleared by the EFB. Setting the flag for one scan is sufficient.

3.6 Using the DPM_Time Structure for ERT Internal Clock Synchronization

Should time synchronization not be obtainable from a time standard receiver, time information can alternatively be taken from the ESI 062 00 communications module. The ESI makes updated time in a DPM_Time structure directly available to the EFB through the ”Time_IN” parameter.

With Validity Reserve

When the ERT’s ”Clock” parameter has been configured as an ”Internal clock” with a non–zero validity reserve value (i.e. not free running), the EFB must make use of ESI–provided time for synchronization of the ERT internal clock. Until an initial synchronization takes place, the ERT will continue to return a set ”time invalid” bit within the ”Status” output word (bit 3 – TU).

The conditions to initiate active ERT internal clock synchronization through the DPM_Time structure are:

- The EFB set time enable parameter ”T_EN” must change values from 0–>1.
- ESI–provided time data in ”Time_IN” must be:
  - valid (i.e. the time invalid bit within the ”Min” value may not be set),
  - and the ”Ms” values must be ”ticking”.

Should the time data become invalid later, TU will only go to 1 after expiration of the configured validity reserve.

Synchronization/setting of the ERT internal clock through the DPM_Time structure then takes place when:

- The EFB set time enable parameter ”T_EN” is 1.
- ESI–provided time data in ”Time_IN” is valid (i.e. the time invalid bit within the ”Min” value may not be set).
- The state of the DPM_Time element ”Sync” changes from 0–>1.
  This change is always generated by the ESI 062 00 on every full hour, but may also be triggered as the result of an appropriate telecontrol command.

Accuracy of the ESI–provided time is influenced directly by the semi–fixed retardation attributable to the PLC’s scan cycle time, and a cumulative component reflecting the ERT’s software clock drift (< 360 milliseconds/hour).

Without Validity Reserve

When however, the ERT's ”Clock” parameter has been configured as an ”Internal clock” in **free running** modus (with a validity reserve value of zero), the default initial internal clock setting is 0 hours, 1/1/1990. The time can also be set in this case using the ESI 062 00 module's DPM_Time derived data structure as time source, as described above. Since there is no validity reserve to ”expire” and thus no time tag invalidation in this modus, the ”time not synchronized” bit within the ”Status” output word (bit 4 – TA) passed back from the EFB is always set.

Breite: 185 mm
Höhe: 230 mm

3.7 Application Examples: Making use of the ERT –>EFB Time Data Stream

Expert This section details an internal ”service” provided by the ERT for basic diagnosis & development, involves the cyclic–transport of the ERT’s own clock time at semi–regular intervals (up to roughly 200 user program scans) to the corresponding EFB. The application of this time, either originating from the free running internal clock, or synchronized through an external time base signal, can be of real practical value (for display, setting the PLC clock, etc.). An ERT time derived from the ESI will not likely be of any use. The time appears as a DPM_Time structure beginning at word 4 of the ERT’s IN register block. The following figure demonstrates the basic logic involved.

Commissioning details: An ERT_854_10 has been placed at the IN references 30001 ... 30007 in the I/O map. The IN transfer status (TS_IN) in the register block 3rd word is fed to an OR_WORD block. A DPM_Time structure is defined as variable Mux_IN within the variable editor at the 4th IN register block word, and thus mapped from 30004 ... 30007. This variable is given to the MOVE block as input. The output for the MOVE block is a further DPM_Time structure defined by the variable editor as variable ERT_Time.

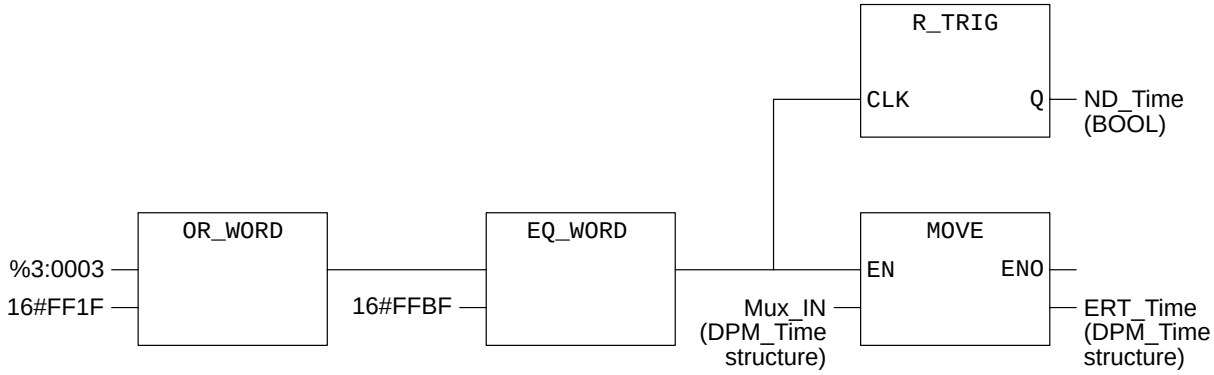


Figure 8 Basic ERT time data capture mechanism

Note The ERT_854_10 EFB must be active and error free.

Explanation: The MOVE block transports time data resident in the MUX section of the IN register block to the user’s DPM_Time structure ERT_Time whenever the OR_WORD and EQ_WORD blocks signal a time data transfer. R_TRIG provides a pulse in ”ND_Time” for further processing of the time data. The BOOL ”Sync” element value of ERT_Time should appear to ”tick” with each new transfer from the ERT.

Example 1: Extracting time values for display (or use with the SET_TOD EFB)

A number of simple logic operations are necessary to usefully display DPM_Time structure time information. The same actions are, in general, applicable to the ERT_10_TTag structure values too. Since Example 2 will be dealing with setting the PLC clock using the SET_TOD EFB, individual values will be transformed directly into the required formats.

☞ **Note** The reference data editor (RDE) can display the WORD ”Ms” value directly in **UnsDec**, the BYTE ”Min” value in **Dec** format.

SET_TOD requires that the WORD milliseconds value ”Ms” be transformed to a BYTE seconds value. The BYTE minute value ”Min” contains an invalid bit which must be removed (values > 128 are invalid).

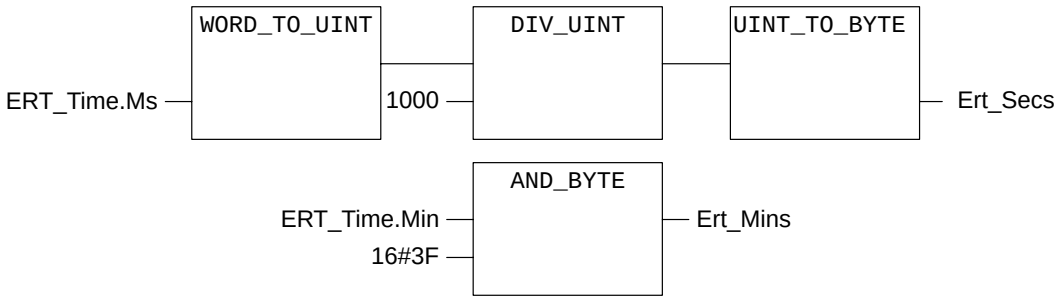


Figure 9 Transform the milliseconds WORD value directly to a seconds BYTE for SET_TOD and clean–up minutes

Breite: 185 mm
Höhe: 230 mm

The BYTE hour value ”Hour” contains the daylight savings time bit, which must be removed. The bit can also be directly recovered with the BYTE_TO_BIT block.

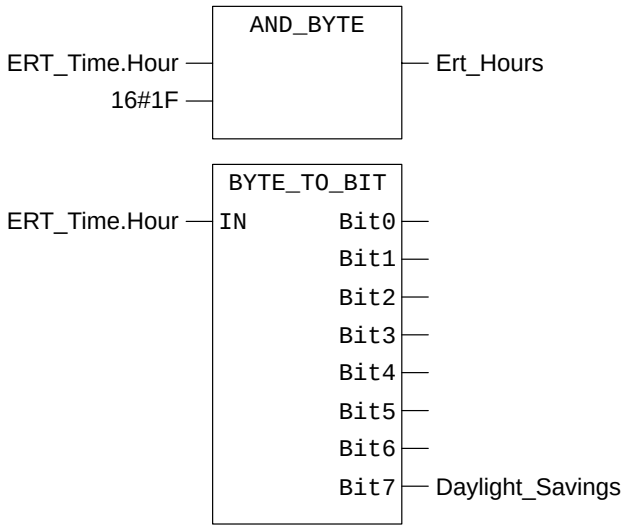


Figure 10 Remove/recover the daylight savings bit from Hour

The BYTE value ”Day” contains both the week and calendar day values. The day of the week as presented by the DPM_Time structure gives the 1 value to Monday. SET_TOD needs a week day parameter with the 1 value as Sunday.

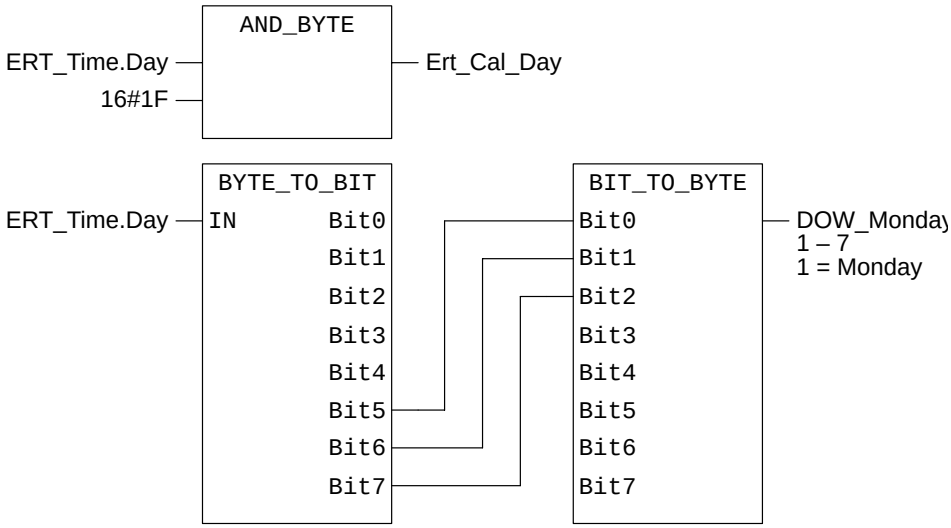


Figure 11 Extract calendar day, and day of the week based on Monday

More work needs to be done to transform the day of the week based on 1 value as Monday to 1 value as Sunday.

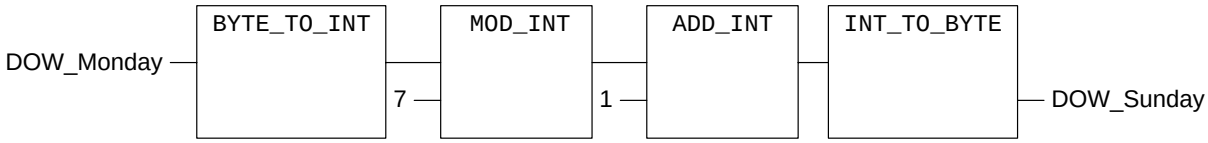


Figure 12 Perform modulo and add to shift the day of the week value sequence

Breite: 185 mm
Höhe: 230 mm

Example 2: Set the PLC clock with the SET_TOD EFB using ERT time data

All of the parameter values as required by the SET_TOD EFB have now been derived. The ”ND_Time” pulse used to signify the DPM_Time structure MOVE is combined here with a user enable (given perhaps only on the hour), to set the PLC clock only after new, error–free, and externally–synchronized time data has been transferred by the ERT. The negated ERT error bits should not be applied for ERT time data derived from the internal clock in free running mode.

The SET_TOD EFB is within the HSBY group of the SYSTEM library. It’s use requires the entry of the TIME OF DAY register under SPECIALS during configuration.

Caution The ”Status” parameter value is not synchronized in any way with the time data stream, and thus can only be a ”reflection of tendency”.

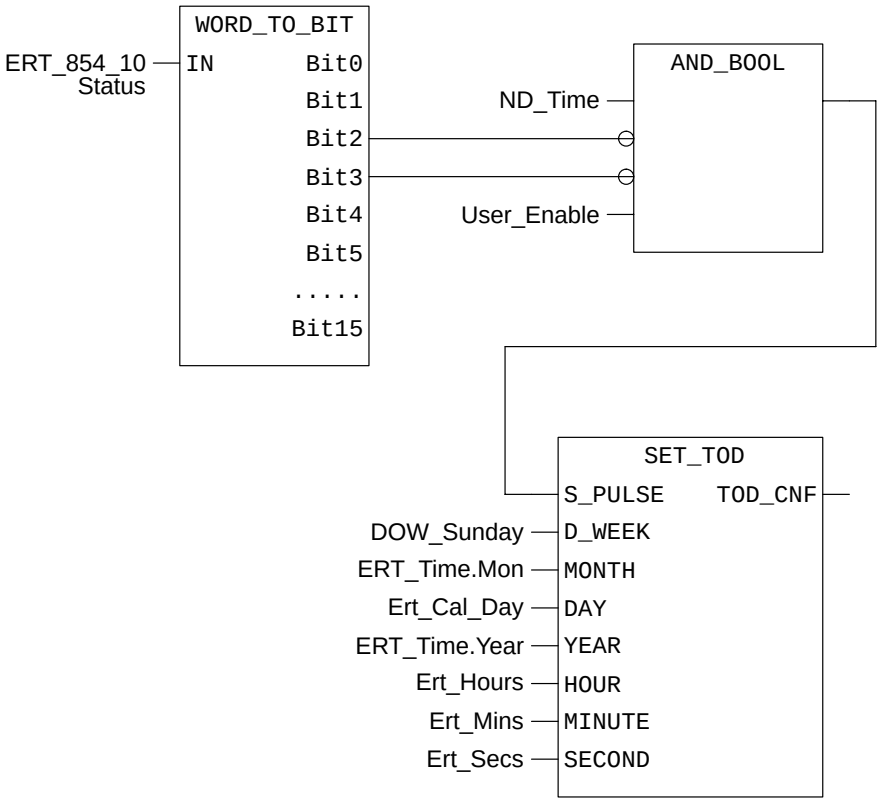


Figure 13 User–enabled PLC clock setting–scheme using the SET_TOD EFB

QUANTUM: Configuring a local backplane

1 Brief Description

The function block is used to edit the configuration data of a QUANTUM local backplane for subsequent use by the scaling EFBs.

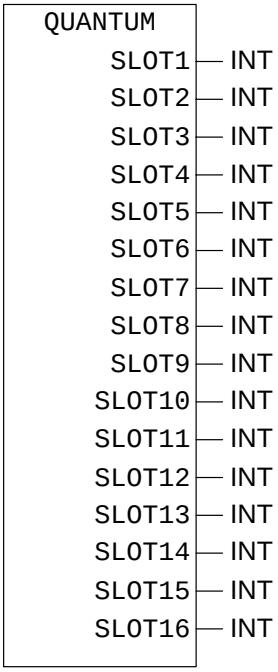
To configure a QUANTUM local backplane, the QUANTUM function block is inserted into the configuration section. The function blocks for the configuration of analog modules or the DROP function block for the I/O station are connected at its SLOT outputs.

EN and ENO can be configured as additional parameters.

This EFB can be found in the ANA_IO library.

2 Representation

2.1 Symbol



Width: 185 mm
Height: 230 mm

2.2 Parameter Description

Parameters	Data Type	Meaning
SLOT1	INT	Slot 1
:	:	:
SLOT16	INT	Slot 16

3 Runtime Errors

Internal I/O map errors will cause an error message.

Appendix B
Module Description

Breite: 185 mm
Höhe: 230 mm

140 ERT 854 10
Smart Digital Input Module
Module Description

140 ERT 854 10 is a TSX Quantum expert module with 32 isolated inputs (24 ... 125 VDC). The module is suitable for the acquisition of discrete, counter, and event inputs.

The following module specific information is presented:

- ☐ Features and Function
- ☐ Configuration
- ☐ Diagnosis
- ☐ Technical Specifications

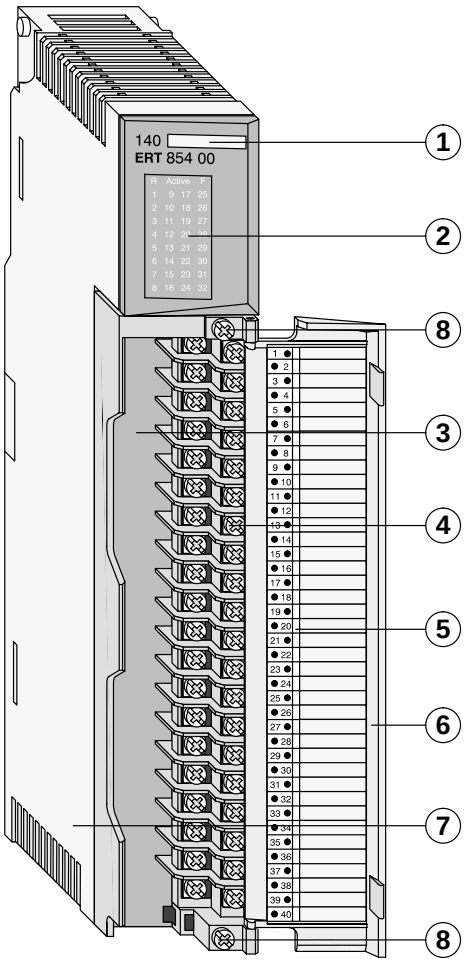


Figure 14 ERT 854 10 Front View

Positions of the User Accessable Parts

1 Color Code
2 LED Status Display
3 I/O Block
4 Terminal block
5 Label Inlay (Inner Side)
6 I/O Block Cover
7 Standard–Size Module (Housing)
8 I/O Block Mounting Screws

Breite: 185 mm
Höhe: 230 mm

1 Features and Function

1.1 Features

The ERT 854 10 is an expert module featuring two groups of 16 discrete inputs suitable for 24 ...125 VDC, isolated by group and from internal logic. In addition to counted values, discrete inputs can be registered with or without event logging. A digital time standard (DTS) receiver can be connected for time synchronization.

1.2 Functional Details

The ERT 854 10 registers counting pulses of up to 500 Hz with a pause/impulse duration ≥1 ms, making 32–bit sums available to the PLC. The module is logically divided into 4 blocks of 8 inputs, each able to process inputs discretely, as events, or as counted values through parameter assignment.

Input processing (debounce time, edge, and inversion) is configurable for each individual input.

The module supports a DCF77–formatted DTS receiver.

2 Configuration

You must configure:

- ☐ A Quantum backplane slot (local or RIO drop).
- ☐ ERT Parameters
  All four ERT 854 10 input blocks may be configured with differing functionality (i.e. counted values, or inputs with/without event logging).
- ☐ Connection to a reference voltage for each input group.
- ☐ Connection of the process peripherals.
- ☐ Connection of the DTS receiver

2.1 Backplane Mounting Slot

Install the module into any free I/O slot within the backplane (local or remote drop). The mounting screw must be tight to to guarantee EMC functionality.

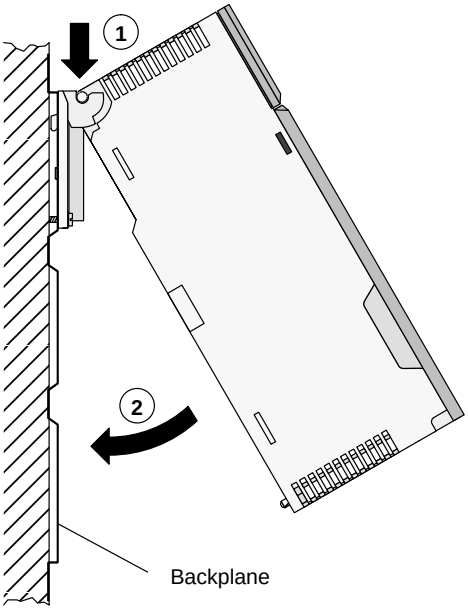


Figure 15 Mounting the ERT 854 10

Breite: 185 mm
Höhe: 230 mm

2.2 Module Wiring

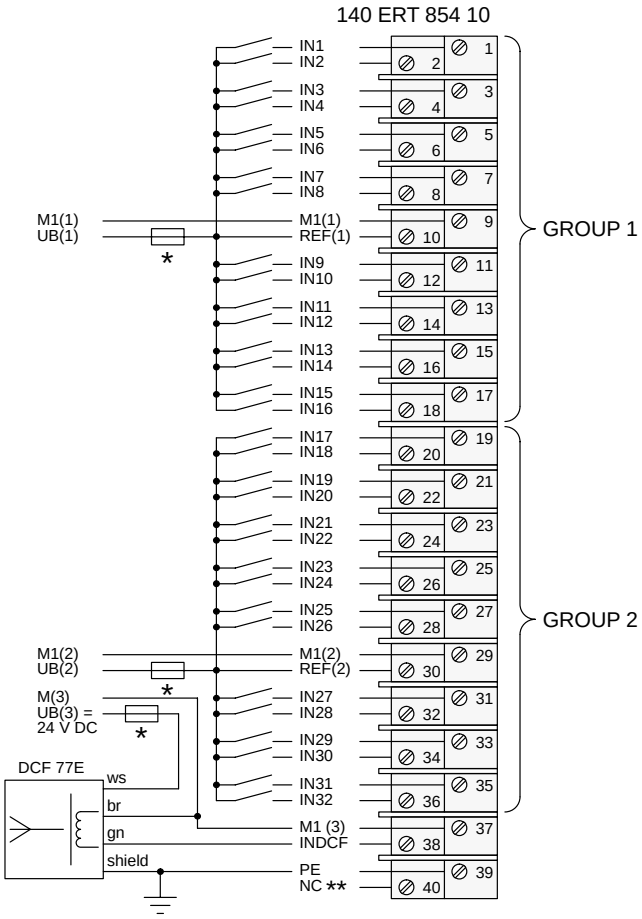


Figure 16 Connection example for a DCF 77E time receiver

Legend

* Separate fusing recommended: UB(1), UB(2): 24 ... 125 VDC, UB(3): 24 VDC

** not connected, suitable as UB(3) terminal point

Note: Several ERT modules may be connected to a single time standard receiver. The 140 ERT 854 10 draws 5 mA from the receiver.

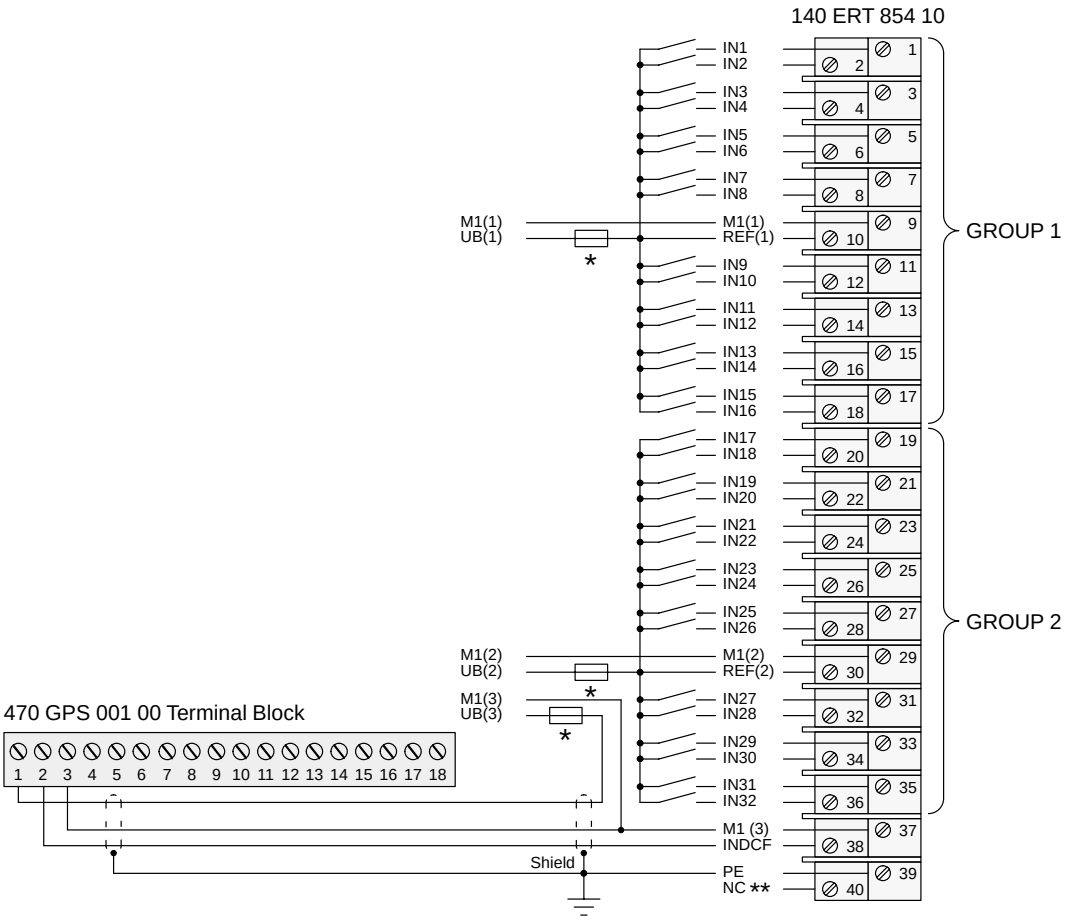


Figure 17 Connection example for a GPS 001 time receiver

Legend

* Separate fusing recommended, UB(1), UB(2): 24 ... 125 VDC, UB(3): 24 VDC

** not connected, suitable as UB(3) terminal point

Breite: 185 mm
Höhe: 230 mm

3 Diagnosis

The module contains the following LED status display:

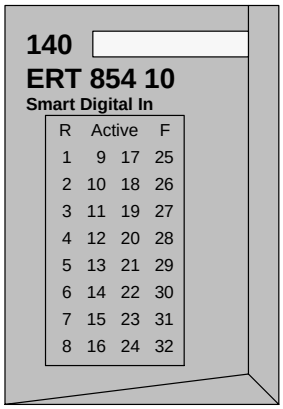


Figure 18 ERT 854 10 Status LEDs

Table 2 Meaning of the LEDs

LEDs	Color	Function
R	Green	Ready. The power on selftest (POS) was successful. The firmware is running correctly and the module is ready for service.
Active	Green	Communication with the TSX Quantum CPU is active.
F	Red	Composite Fault. Lights for all occurances of the configured faults.
1 ... 32	Green	Input signals. Lights for process input ”1” signal.

4 Technical Specifications

Supply Voltage	
Reference input voltage for each process input group	24 ... 125 VDC, (max. 18 ... 156 VDC) current drain per group: max. 3 mA
Internal via backplane	5 VDC, max. 300 mA
Data retention current drain	Typically 0.07 mA from the XCP 900 00
Process Inputs	
Number	32 in 2 groups
Input voltage	24 ... 125 VDC
Potential isolation	Inputs to the Quantum–Bus, group 1 to group 2 (optical coupler)
Debounce time	Configurable 0 ... 255 milliseconds
Inversion	Configurable
Max. wiring length	400 m unshielded, 600 m shielded
Switching level: Rated signal input voltage Min. current for 1 signal Signal level for 0 signal Signal level for 1 signal	 24 V 48 V 60 V 125 V 6 mA 2.5 mA 2.5 mA 1 mA nominal 0 % from the group's reference input min. –5 %, max. +15 % nominal 100% from the group's reference input min. 75 %, max. 125 %
Internal power consumption over process inputs	Max. 7.5 W
Digital Time Standard (DTS) Input	
Number	1, DCF77 data format from DCF or GPS receiver
Input voltage	24 VDC
Potential isolation	Optical coupler
Time tag resolution	1 ms
Mechanical Design	
Dimensions	Width = 40.34 mm (Standard–Size Module)
Weight	0.45 kg
Connection Styles	
Process inputs, DTS receiver	40 pin I/O block
Environmental Conditions	
System data	Refer to the Quantum User Manual
Power dissipation	Max. 9 W, typically 5 W

Breite: 185 mm
Höhe: 230 mm