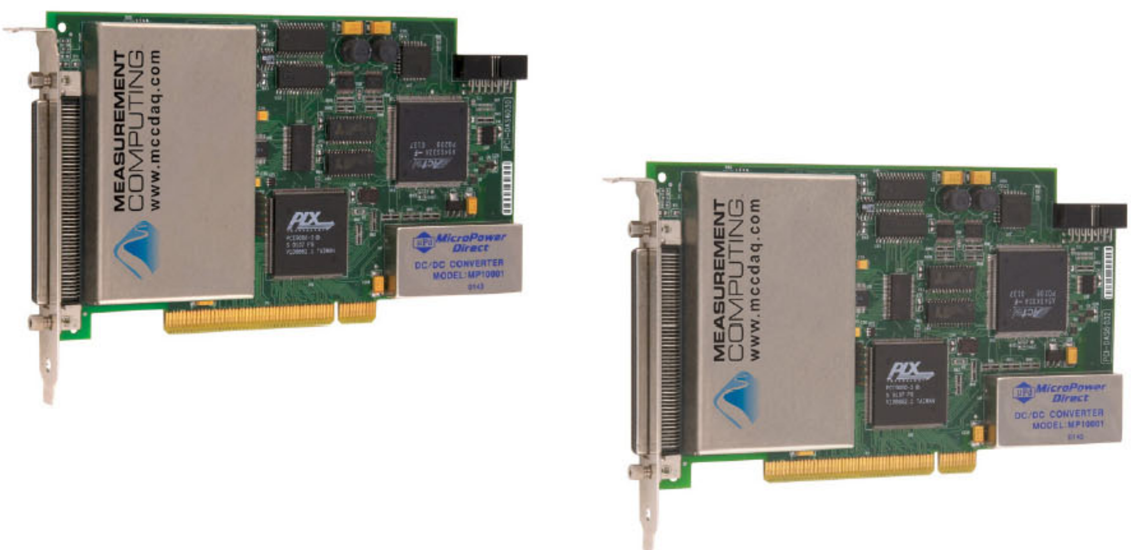
PCI-DAS6030 & PCI-DAS6032

Analog and Digital I/O Boards

User's Guide



MEASUREMENT COMPUTING.

PCI-DAS6030
and
PCI-DAS6032

Analog and Digital I/O Boards

User's Guide

MEASUREMENT COMPUTING™

Document Revision 6, May, 2006

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Table of Contents

About this User's Guide

What you will learn from this user's guide

This user's guide explains how to install, configure, and use the PCI-DAS6030 and PCI-DAS6032 so that you get the most out of the analog, digital, and timing I/O features.

This user's guide also refers you to related documents available on our web site, and to technical support resources that can also help you get the most out of these boards.

Conventions in this user's guide

For more information on …
Text presented in a box signifies additional information and helpful hints related to the subject matter you are reading.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

<#:#>	Angle brackets that enclose numbers separated by a colon signify a range of numbers, such as those assigned to registers, bit settings, etc.
bold text	**Bold** text is used for the names of objects on the screen, such as buttons, text boxes, and check boxes. For example: **1.** Insert the disk or CD and click the **OK** button.
italic text	*Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase. For example: The *Insta*Cal installation procedure is explained in the *Quick Start Guide*. *Never* touch the exposed pins or circuit connections on the board.

Where to find more information

The following electronic documents provide information that can help you get the most out of your PCI-DAS6030 and PCI-DAS6032 boards.

The following electronic documents provide helpful information relevant to the operation of the PCI-DAS6030 and PCI-DAS6032.

- MCC's *Specifications: PCI-DAS6030 and PCI-DAS6032* (the PDF version of the Electrical Specification Chapter in this guide) is available on our web site at www.mccdaq.com/pdfs/PCI-DAS6030-32.pdf.
- MCC's *Quick Start Guide* is available on our web site at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.
- MCC's *Guide to Signal Connections* is available on our web site at www.mccdaq.com/signals/signals.pdf.
- MCC's *Universal Library User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-user-guide.pdf.
- MCC's *Universal Library Function Reference* is available on our web site at www.mccdaq.com/PDFmanuals/sm-ul-functions.pdf.
- MCC's *Universal Library for LabVIEW™ User's Guide* is available on our web site at www.mccdaq.com/PDFmanuals/SM-UL-LabVIEW.pdf.

PCI-DAS6030 & PCI-DAS6032 User's Guide (this document) is also available on our web site at www.mccdaq.com/PDFmanuals/PCI-DAS6030-32.pdf.

Introducing the PCI-DAS6030 and PCI-DAS6032

Overview: PCI-DAS6030 and PCI-DAS6032 features

This manual explains how to install and use the PCI-DAS6030 and PCI-DAS6032 boards.

The PCI-DAS6030 and PCI-DAS6032 boards provide either eight differential or 16 single-ended analog inputs with 16 bit resolution. Input ranges are either Bipolar or Unipolar. Bipolar input ranges are ±10V, ±5V, ±2.0V, ±1V, ±0.5V, ±0.2V, and ±0.1V. Unipolar input ranges are 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V and 0 to 0.1V. The input ranges are software-selectable.

The PCI-DAS6030 and PCI-DAS6032 have eight lines of digital I/O. The PCI-DAS6030 also provides two digital-to-analog outputs.

Each board has nine user-configurable trigger/clock/gate pins that are available at a 100-pin I/O connector. Six pins are configurable as inputs and three are configurable as outputs. Refer to Chapter 4 ("Functional Details") and Chapter 6 ("Specifications") for more information.

The PCI-DAS6030 and PCI-DAS6032 provide triggering and synchronization capability. There are five trigger/strobes and a synchronizing clock provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction can be set. Refer to Chapter 2 ("Installing the Board") and Chapter 6 ("Specifications") for more information on these signals.

Interrupts can be generated by up to seven ADC sources and four DAC sources. Interrupt sources are listed in Chapter 6 ("Specifications").

The PCI-DAS6030 and PCI-DAS6032 boards contain an 82C54 counter chip, which consists of three 16-bit counters. Clock, gate, and output signals from two of the three counters are available on the 100-pin I/O connector. The third counter is used internally.

Software features

For information on the features of *Insta*Cal and the other software included with your PCI-DAS6040, refer to the *Quick Start Guide* that shipped with your device. The *Quick Start Guide* is also available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Check www.mccdaq.com/download.htm for the latest software version or versions of the software supported under less commonly used operating systems.

Installing the PCI-DAS6030 and PCI-DAS6032

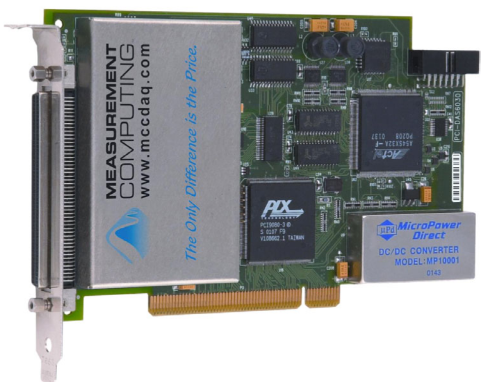
What comes with your PCI-DAS6030 and PCI-DAS6032 shipment?

The following items are shipped with the PCI-DAS6030 and PCI-DAS6032.

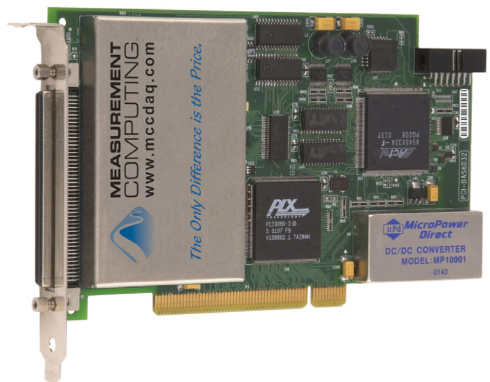
Hardware

The following items should be included with your shipment.

- PCI-DAS6030 board or PCI-DAS6032 board



PCI-DAS6030



PCI-DAS6032

Additional documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide* (available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf). This booklet supplies a brief description of the software you received with your USB-3110 and information regarding installation of that software. Please read this booklet completely before installing any software or hardware.

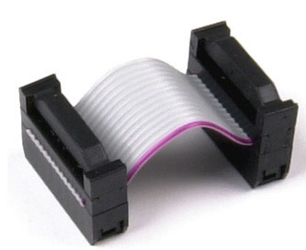
Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

- Cables

C100HD50-x

C100MMS-x



CDS-14-*x*

- Signal termination and conditioning accessories

  MCC provides signal termination products for use with the PCI-DAS6030 and PCI-DAS6032. Refer to the "Field wiring, signal termination and conditioning" section on page 2-8 for a complete list of compatible accessory products.

Unpacking the PCI-DAS6030 and PCI-DAS6032

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS6030 and PCI-DAS6032 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Installing the software

Refer to the *Quick Start Guide* for instructions on installing the software on the *Measurement Computing Data Acquisition Software CD*. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the hardware

The PCI-DAS6030 and PCI-DAS6032 boards are completely plug-and-play. There are no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into any available PCI slot.

2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play (such as Windows 2000 or Windows XP), a dialog box pops up as the system loads indicating that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the *Measurement Computing Data Acquisition Software* CD and click **OK**.

3. To test your installation and configure your board, run the *Insta*Cal utility installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load *Insta*Cal.

Allow your computer to warm up for at least 15 minutes before acquiring data with these boards board. The high speed components used on these boards generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Configuring the hardware

All hardware configuration options on the PCI-DAS6030 and PCI-DAS6032 are software controlled. You can select some of the configuration options using *Insta*Cal, such as the analog input configuration (16 single-ended or eight differential channels), the edge used for triggering when using an external pacer, and the source for the two independent counters. Once selected, any program that uses the Universal Library will initialize the hardware according to these selections.

Following is an overview of the available hardware configuration options for these boards. There is additional general information regarding analog signal connection and configuration in the *Guide to Signal Connections* (available on our web site at http://www.measurementcomputing.com/signals/signals.pdf).

Differential input mode

When all channels are configured for differential input mode, eight analog input channels are available. In this mode, the input signal is measured with respect to the low input. The input signal is delivered through three wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The wire carrying the reference signal connects to CH# IN LO.
- The third wire is connected to LLGND.

Differential input mode is the preferred configuration for applications in noisy environments, or when the signal source is referenced to a potential other than PC ground.

Single-ended input mode

When all channels are configured for single-ended input mode, 16 analog input channels are available. In this mode, the input signal is referenced to the board's signal ground (LLGND). The input signal is delivered through two wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The other wire is connected to LLGND.

Non-referenced single-ended input mode

This mode is a compromise between differential and single-ended modes. It offers some of the advantages of each mode. Using non-referenced single-ended mode, you can still get noise rejection, but not the limitation in the number of channels resulting from a fully differential configuration. The possible downside is that the external reference input must be the same for every channel. It is equivalent to configuring the inputs for differential mode and then tying all of the low inputs together and using that node as the reference input.

When configured for non-referenced single-ended input mode, 16 analog input channels are available. In this mode, each input signal is not referenced to the board's ground, but to a common reference signal (AISENSE). The input signal is delivered through three wires:

- The wire carrying the signal to measure connects to CH# IN HI.
- The wire carrying the reference signal connects to AISENSE.
- The third wire is connected to LLGND.

This mode is useful when the application calls for differential input mode but the limitation on channel count prevents it.

DAQ-Sync configuration

You can interconnect multiple boards in the PCI-DAS6000 series to synchronize data acquisition or data output. To do this, order and install a CDS-14-*x* cable at the DAQ-Sync connectors (P2) between the boards to be synchronized.

The "x" in the CDS-14-*x* part number specifies the number of connectors available on the cable, and therefore, the number of boards you can interconnect. Using a CDS-14-*2*, you can connect two PCI-DAS6000 series boards together for I/O synchronization. Using a CDS-14-*3*, you can synchronize three boards, and so on. You can connect up to five PCI-DAS6000 series boards. A CDS-14-3 cable is shown in Figure 2-3 on page 2-8.

By default, all DAQ-Sync connectors are configured as inputs (slave mode). In order to be useful, one board must be set through software to serve as the master, and the signal sources of the slave boards must be defined.

Connecting the board for I/O operations

Connectors, cables – main I/O connector

Table 2-1 lists the board connectors, applicable cables and compatible accessory boards.

Table 2-1. Board connectors, cables, accessory equipment

Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet (Figure 2-1)
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters (Figure 2-2)
Compatible accessory products (with the C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with the C100MMS-x cable)	SCB-100

Pinout – main I/O connector

Table 2-2.
8-channel differential mode

Signal Name	Pin	Pin	Signal Name
GND	100	50	GND
CTR2 OUT	99	49	AUXIN5 / A/D PACER GATE
CTR2 GATE	98	48	AUXIN4 / D/A START TRIGGER
CTR2 CLK	97	47	AUXIN3 / D/A UPDATE
GND	96	46	AUXIN2 / A/D STOP TRIGGER
CTR1 OUT	95	45	AUXIN1 / A/D START TRIGGER
CTR1 GATE	94	44	n/c
CTR1 CLK	93	43	AUXIN0 / A/D CONVERT / ATRIG
DIO7	92	42	AUXOUT2 / SCANCLK
DIO6	91	41	AUXOUT1 / A/D PACER OUT
DIO5	90	40	AUXOUT0 / D/A PACER OUT
DIO4	89	39	PC +5 V
DIO3	88	38	D/A OUT1 *
DIO2	87	37	D/A GND
DIO1	86	36	D/A OUT 0 *
DIO0	85	35	AISENSE
n/c	84	34	n/c
n/c	83	33	n/c
n/c	82	32	n/c
n/c	81	31	n/c
n/c	80	30	n/c
n/c	79	29	n/c
n/c	78	28	n/c
n/c	77	27	n/c
n/c	76	26	n/c
n/c	75	25	n/c
n/c	74	24	n/c
n/c	73	23	n/c
n/c	72	22	n/c
n/c	71	21	n/c
n/c	70	20	n/c
n/c	69	19	n/c
n/c	68	18	LLGND
n/c	67	17	CH7 IN LO
n/c	66	16	CH7 IN HI
n/c	65	15	CH6 IN LO
n/c	64	14	CH6 IN HI
n/c	63	13	CH5 IN LO
n/c	62	12	CH5 IN HI
n/c	61	11	CH4 IN LO
n/c	60	10	CH4 IN HI
n/c	59	9	CH3 IN LO
n/c	58	8	CH3 IN HI
n/c	57	7	CH2 IN LO
n/c	56	6	CH2 IN HI
n/c	55	5	CH1 IN LO
n/c	54	4	CH1 IN HI
n/c	53	3	CH0 IN LO
n/c	52	2	CH0 IN HI
n/c	51	1	LLGND

PCI slot ↓

* = N/C on the PCI-DAS6032

Table 2-3.
16-channel single-ended mode

Signal Name	Pin		Pin	Signal Name
GND	100	• •	50	GND
CTR2 OUT	99	• •	49	AUXIN5 / A/D PACER GATE
CTR2 GATE	98	• •	48	AUXIN4 / D/A START TRIGGER
CTR2 CLK	97	• •	47	AUXIN3 / D/A UPDATE
GND	96	• •	46	AUXIN2 / A/D STOP TRIGGER
CTR1 OUT	95	• •	45	AUXIN1 / A/D START TRIGGER
CTR1 GATE	94	• •	44	n/c
CTR1 CLK	93	• •	43	AUXIN0 / A/D CONVERT / ATRIG
DIO7	92	• •	42	AUXOUT2 / SCANCLK
DIO6	91	• •	41	AUXOUT1 / A/D PACER OUT
DIO5	90	• •	40	AUXOUT0 / D/A PACER OUT
DIO4	89	• •	39	PC +5 V
DIO3	88	• •	38	D/A OUT1 *
DIO2	87	• •	37	D/A GND
DIO1	86	• •	36	D/A OUT 0 *
DIO0	85	• •	35	AISENSE
n/c	84	• •	34	n/c
n/c	83	• •	33	n/c
n/c	82	• •	32	n/c
n/c	81	• •	31	n/c
n/c	80	• •	30	n/c
n/c	79	• •	29	n/c
n/c	78	• •	28	n/c
n/c	77	• •	27	n/c
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n/c	75	• •	25	n/c
n/c	74	• •	24	n/c
n/c	73	• •	23	n/c
n/c	72	• •	22	n/c
n/c	71	• •	21	n/c
n/c	70	• •	20	n/c
n/c	69	• •	19	n/c
n/c	68	• •	18	LLGND
n/c	67	• •	17	CH15 IN
n/c	66	• •	16	CH7 IN
n/c	65	• •	15	CH14 IN
n/c	64	• •	14	CH6 IN
n/c	63	• •	13	CH13 IN
n/c	62	• •	12	CH5 IN
n/c	61	• •	11	CH12 IN
n/c	60	• •	10	CH4 IN
n/c	59	• •	9	CH11 IN
n/c	58	• •	8	CH3 IN
n/c	57	• •	7	CH10 IN
n/c	56	• •	6	CH2 IN
n/c	55	• •	5	CH9 IN
n/c	54	• •	4	CH1 IN
n/c	53	• •	3	CH8 IN
n/c	52	• •	2	CH0 IN
n/c	51	• •	1	LLGND

* = N/C on the PCI-DAS6032

PCI slot ↓

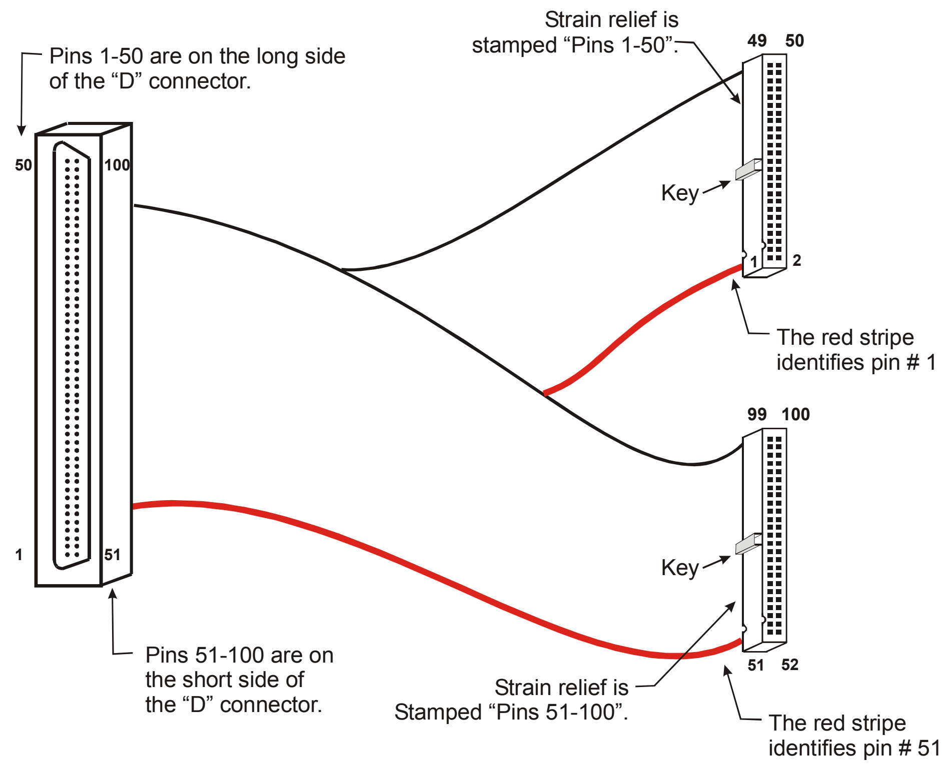

Figure 2-1. C100HD50-x cable

Details on the C100HD50-x cable are available on our web site at
www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=104&pf_id=1203.

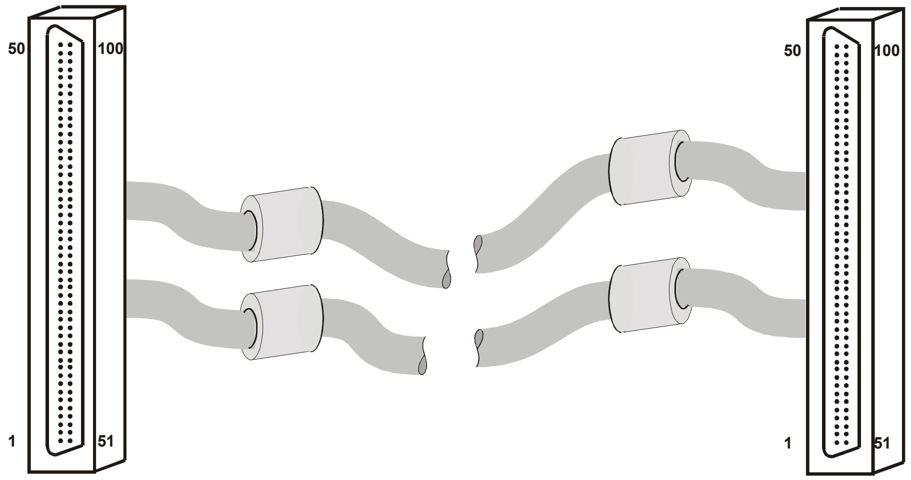

Figure 2-2. C100 MMS-x cable

Details on the C100MMS-x cable are available on our web site at
www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=104&pf_id=1514.

DAQ-Sync connector and pin out

Table 2-4. DAQ-Sync connector & cable types

Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n: CDS-14-*x*, 14 pin ribbon cable for board-to board DAQ-Sync connection; x = number of boards (Figure 2-3)

Table 2-5. DAQ-Sync connector pin out (view from top)

Signal Name	Pin	Pin	Signal Name
DS A/D START TRIGGER	1	2	GND
DS A/D STOP TRIGGER	3	4	GND
DS A/D CONVERT	5	6	GND
DS D/A UPDATE	7	8	GND
DS D/A START TRIGGER	9	10	GND
RESERVED	11	12	GND
SYNC CLK	13	14	GND

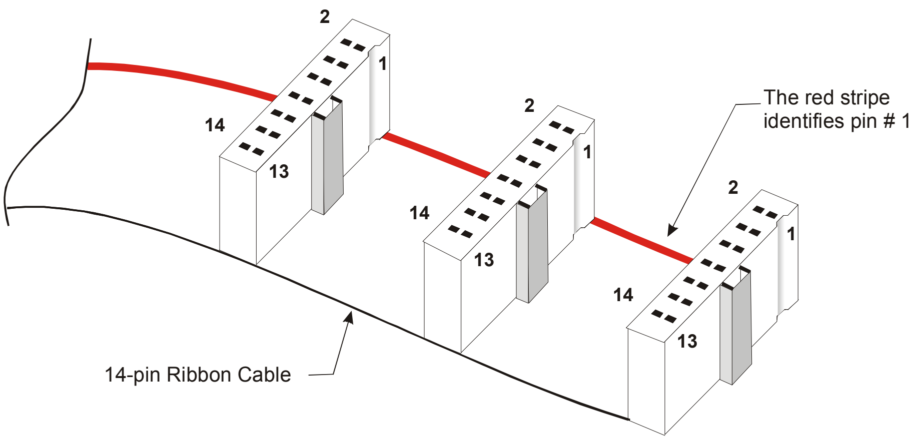

Figure 2-3. CDS-14-3 cable

Details on the CDS-14-x cable are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=104&pf_id=1528.

Field wiring, signal termination and conditioning

You can use the following BNC and screw terminal boards to terminate field signals and route them into the PCI-DAS6030 and PCI-DAS6032 using the C100HD50-x cable:

- BNC-16SE – Brings analog signals to standard BNC connectors. Designed for boards operating in single-ended mode. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=101&pf_id=713.
- BNC-16DI – Brings analog signals to standard BNC connectors. Designed for boards operating in differential mode. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=101&pf_id=714.
- CIO-MINI50 – 50-pin screw terminal board. Two boards are required. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=258.
- CIO-TERM100 – 100-pin screw terminal board (daisy-chained 50-pin IDC connectors). Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=102&pf_id=281.
- SCB-50 – 50 conductor, shielded signal connection/screw terminal box provides two independent 50-pin connections. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1168.

You can use the following screw terminal box to terminate field signals and route them into the PCI-DAS6030 and PCI-DAS6032 board using the C100MMS-x cable:

- SCB-100 – 100 conductor, shielded signal connection/screw terminal box provides two independent 50-pin connections. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=196&pf_id=1169

For analog signal conditioning and expansion, you can use the following signal conditioning accessory products with the C100HD50-x cable:

- ISO-RACK-16/P – 16-channel ISO-5B module rack for connecting an ISO-5B module to an analog input. Details on this product are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=127&pf_id=1111.
- ISO-RACK-DA02/P – 2-channel, 5B module rack for 50-pin DA02 & 100-pin series, detachable terminals are available. Details are available on our web site at www.mccdaq.com/cbicatalog/cbiproduct.asp?dept_id=128&pf_id=711.

Programming and Developing Applications

After following the installation instructions in Chapter 2, your board should now be installed and ready for use. Although the board is part of the larger DAS family, in general there may be no correspondence among registers for different boards[1]. Software written at the register level for other DAS models will not function correctly with your board.

Programming languages

Measurement Computing's Universal Library™ provides access to board functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic® or any other language, please refer to the *Universal Library User's Guide* (available on our web site at www.measurementcomputing.com/PDFmanuals/sm-ul-user-guide.pdf).

Packaged applications programs

Many packaged application programs, such as SoftWIRE®, Labtech Notebook™, and HP-VEE™, now have drivers for your board. If the package you own does not have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain drivers.

Some application drivers are included with the Universal Library package, but not with the application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us by phone, fax or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

Register-level programming

You should use the Universal Library or one of the packaged application programs mentioned above to control your board. Only experienced programmers should try register-level programming. If you need to program at the register level in your application, you can find more information in the *STC Register Map for the PCI-DAS6000 Series* (available at www.mccdaq.com/registermaps/RegMapSTC6000.pdf).

[1] An exception to this is the DAQ Sync capability of these boards that permit synchronized data acquisition by multiple boards in this series.

Functional Details

Basic architecture

Figure 4-1 shows a simplified block diagram of the PCI-DAS6030 and PCI-DAS6032. This board provides all of the functional elements shown in the figure.

The System Timing and Control (STC) is the logical center for all DAQ, DIO, and DAC (if applicable) operations. It communicates over two major busses: a local bus and a memory bus.

The local bus carries digital I/O data and software commands from the PCI Bus Master. There are two Direct Memory Access (DMA) channels provided for data transfers to the PC.

Primarily, the memory bus carries A/D and D/A related data and commands. There are three buffer memories provided on the memory bus:

- The *queue buffer* (8K configuration memory) stores programmed channel numbers, gains, and offsets.
- The *ADC buffer* (8K FIFO [First In, First Out]) temporarily stores scanned and converted analog inputs.
- The *DAC 16K buffer* stores data to be output as analog waveforms.

Auxiliary input & output interface

The board's 100-pin I/O connector provides six software-selectable inputs, and three software-selectable outputs. The signals are user-configurable clocks, triggers and gates.

Refer to "DAQ signal timing" for information about these signals and their timing requirements.

Table 4-1 lists all of the possible signals and the default signals you use on the nine pins.

Table 4-1. Auxiliary I/O Signals

I/O Type	**Signal Name**	**Function**
AUXIN<5:0> sources (software selectable)	A/D CONVERT	External ADC Convert Strobe (default)
	A/D TIMEBASE IN	External ADC Pacer Time Base
	A/D START TRIGGER	ADC Start Trigger (default)
	A/D STOP TRIGGER	ADC Stop Trigger (default)
	A/D PACER GATE	External ADC Gate (default)
	D/A START TRIGGER	DAC Trigger/Gate (default)
	D/A UPDATE	DAC Update Strobe (default)
	D/A TIMEBASE IN	External DAC Pacer Time Base
AUXOUT<2:0> sources (software selectable)	STARTSCAN	A pulse indicating the start of conversion.
	SSH	An active signal that terminates at the start of the last conversion in a scan.
	A/D STOP	Indicates the end of a scan
	A/D CONVERT	ADC convert pulse (default)
	SCANCLK	Delayed version of ADC convert (default)
	CTR1 CLK	CTR1 clock source
	D/A UPDATE	D/A update pulse (default)
	CTR2 CLK	CTR2 clock source
	A/D START TRIGGER	ADC Start Trigger Out
	A/D STOP TRIGGER	ADC Stop Trigger Out
	A/D PACER GATE	External ADC gate
	D/A START TRIGGER	DAC Start Trigger Out
Default selections summary	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D PACER GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK

DAQ-Sync signals

The DAQ-Sync hardware provides the capability of triggering or clocking up to four slave boards from a master board to synchronize data input and/or output.

The PCI-DAS6030 and PCI-DAS6032 boards provide the capability of inter-board synchronization between boards in the PCI-DAS6000 family. There are five trigger/strobes and a synchronizing clock provided on a 14-pin header. Table 4-2 lists the available signals.

Table 4-2. DAQ-Sync signals

DS A/D START TRIGGER
DS A/D STOP TRIGGER
DS A/D CONVERT
DS D/A UPDATE
DS D/A START TRIGGER
SYNC CLK

Except for the SYNC CLK signal, the DAQ-Sync timing and control signals are a subset of the AUXIO signals available at the 100-pin I/O connector. These versions of the signals are used for board-to-board synchronization and have the same timing specifications as their I/O connector counterparts. Refer to "DAQ signal timing" for explanations of signals and timing.

Use the SYNC CLCK signal to determine the master/slave configuration of a DAQ-Sync-enabled system. Each system can have one master and up to three slaves. SYNC CLK is the 40 MHz time-base used to derive all board timing and control. The master provides this clock to the slave boards so that all boards in the DAQ-sync-enabled system are timed from the same clock.

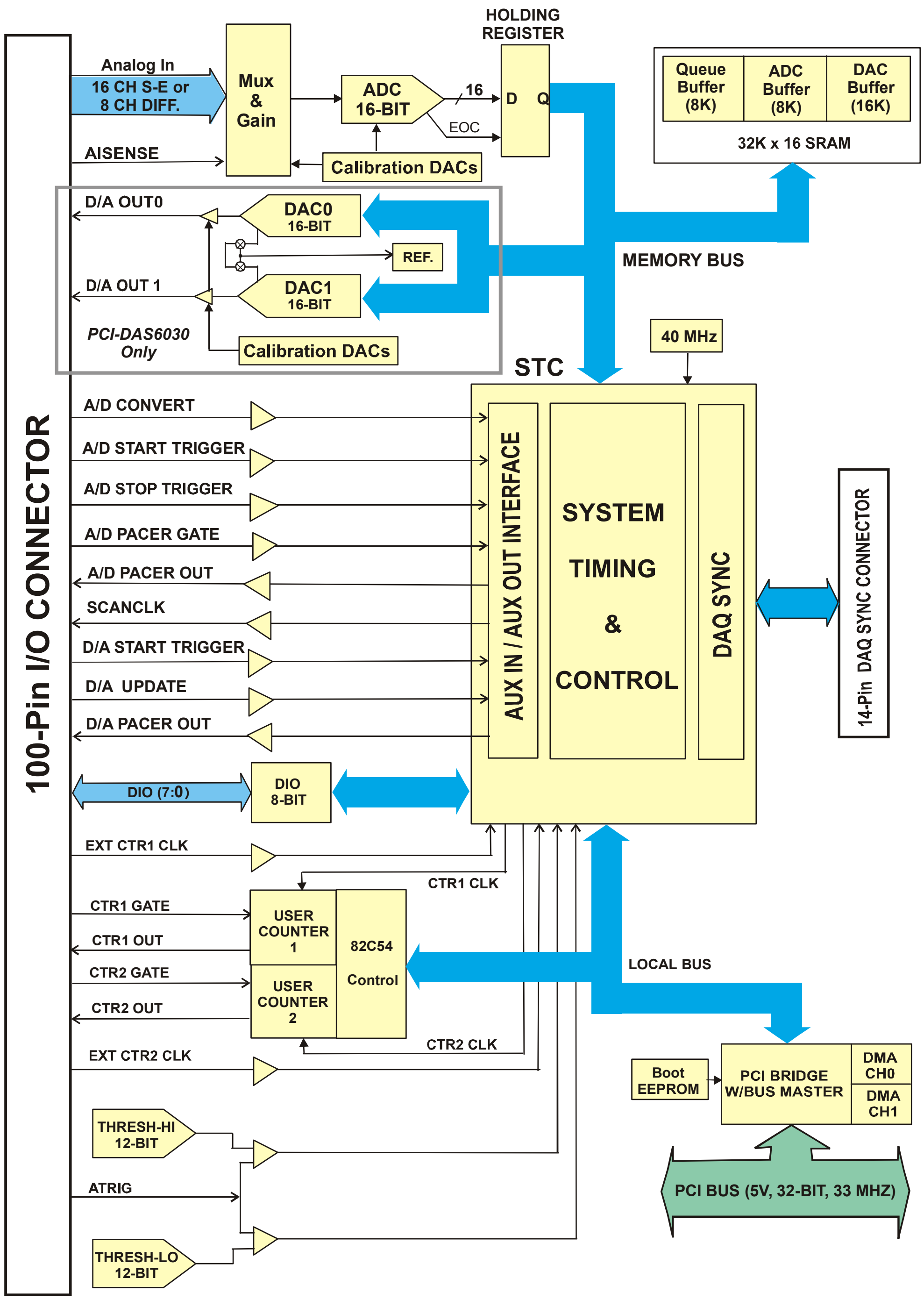

Figure 4-1. Block diagram – PCI-DAS6030/32

DAQ signal timing

The DAQ timing signals are:

- SCANCLK
- A/D START TRIGGER
- A/D STOP TRIGGER
- STARTSCAN
- SSH
- A/D CONVERT
- A/D PACER GATE
- A/D EXTERNAL TIME BASE
- A/D STOP
- ATRIG

SCANCLK signal

SCANCLK is an output signal that may be used for switching external multiplexers. It is a 400 ns wide pulse that follows the CONVERT signal after a 50 ns delay. This is adequate time for the analog input signal to be acquired so that the next signal may be switched in. The polarity of the SCANCLK signal is programmable. The default output pin for the SCANCLK signal is AUXOUT2, but any of the AUXOUT pins may be programmed as a SCANCLK output.

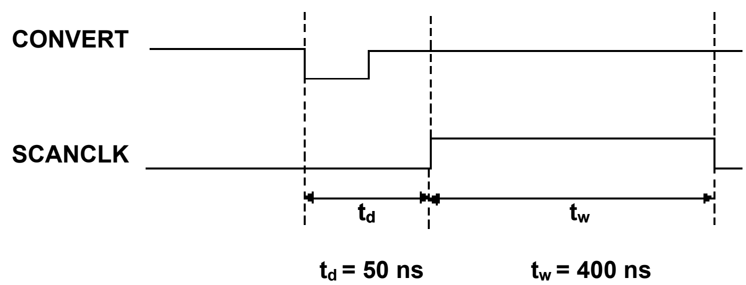

Figure 4-2. SCANCLK signal timing

A/D START TRIGGER signal

Use the A/D START TRIGGER signal for conventional triggering (when you only need to acquire data after a trigger event). Figure 4-3 shows the A/D START TRIGGER signal timing for a conventionally triggered acquisition.

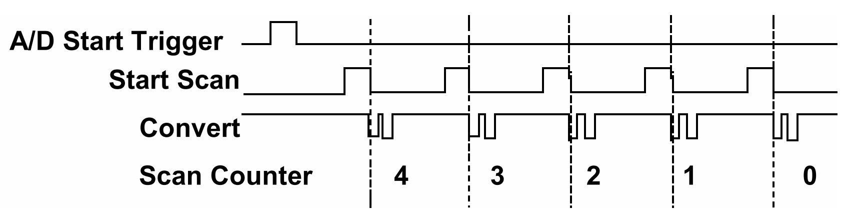

Figure 4-3. Data acquisition example for conventional triggering

The A/D START TRIGGER source is programmable and may be set to any of the AUXIN inputs or to the DAQ-Sync DS A/D START TRIGGER input. The polarity of this signal is also programmable to trigger acquisitions on either the positive or negative edge.

The A/D START TRIGGER signal is also available as an output and can be programmed to appear at any of the AUXOUT outputs. Refer to Figure 4-4 and Figure 4-5 for A/D START TRIGGER input and output timing requirements.

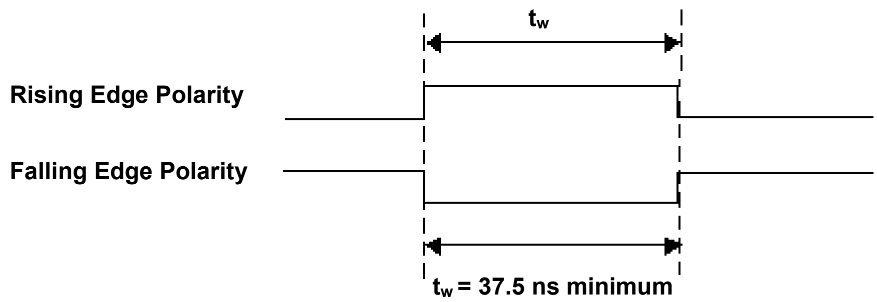

Figure 4-4. A/D START TRIGGER input signal timing

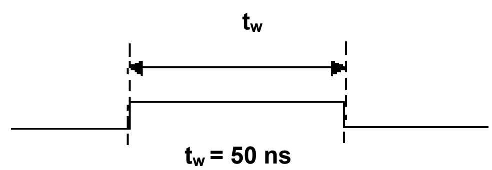

Figure 4-5. A/D START TRIGGER output signal timing

The A/D START TRIGGER signal is also used to initiate pre-triggered DAQ operations (when you need to acquire data just before a trigger event). In most pre-triggered applications, the A/D START TRIGGER signal is generated by a software trigger. The use of A/D START TRIGGER and A/D STOP TRIGGER in pre-triggered DAQ applications is explained next.

A/D STOP TRIGGER signal

Pre-triggered data acquisition continually acquires data into a circular buffer until a specified number of samples have been collected after the trigger event. Figure 4-6 illustrates a typical pre-triggered DAQ sequence.

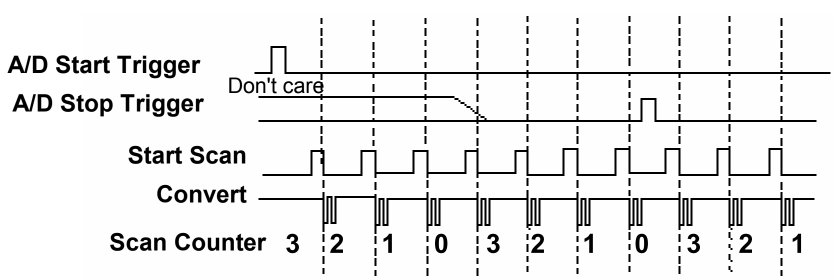

Figure 4-6. Pre-triggered data acquisition example

The A/D STOP TRIGGER signal signifies when the circular buffer should stop and when the specified number of post trigger samples should be acquired. It is available as an output and an input. By default, it is available at AUXIN2 as an input but may be programmed for access at any of the AUXIN pins or the DAQ-Sync "DS A/D STOP TRIGGER" input. It may be programmed for access at any of the AUXOUT pins as an output.

When using the A/D STOP TRIGGER signal as an input, the polarity may be configured for either rising or falling edge. The selected edge of the A/D STOP TRIGGER signal initiates the post-triggered phase of a pre-triggered acquisition sequence.

As an output, the A/D STOP TRIGGER signal indicates the event separating the pre-trigger data from the post-trigger data. The output is an active high pulse with a pulse width of 50 ns. Figure 4-7 and Figure 4-8 show the input and output timing requirements for the A/D STOP TRIGGER signal.

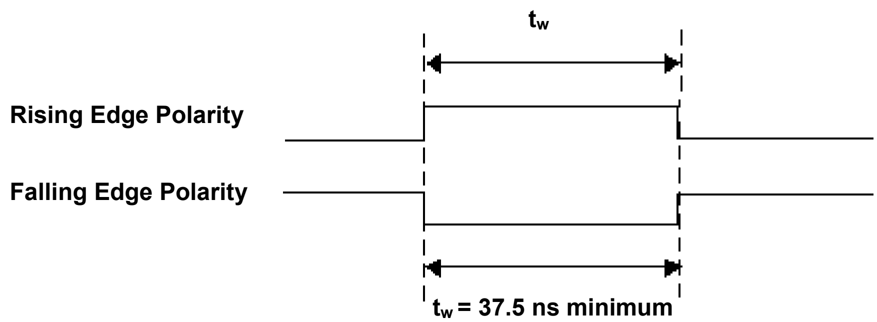

Figure 4-7. A/D STOP TRIGGER input signal timing

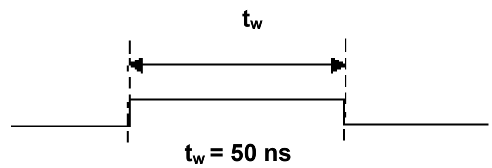

Figure 4-8. A/D STOP TRIGGER output signal timing

STARTSCAN signal

The STARTSCAN output signal indicates when a scan of channels has been initiated. You can program this signal to be available at any of the AUXOUT pins. The STARTSCAN output signal is a 50 ns wide pulse the leading edge of which indicates the start of a channel scan. Figure 4-9 shows the timing for the STARTSCAN signal.

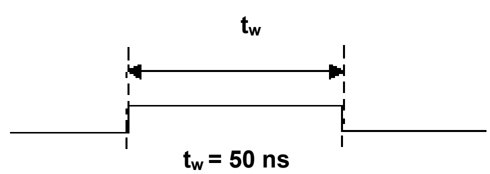

Figure 4-9. STARTSCAN start of scan timing

SSH signal

The SSH signal can be used as a control signal for external sample/hold circuits. The SSH signal is a programmable polarity pulse that is asserted throughout a channel scan. The state of this signal changes after the start of the last conversion in the scan. The SSH signal may be routed via software selection to any of the AUXOUT pins. Figure 4-10 shows the timing for the SSH signal.

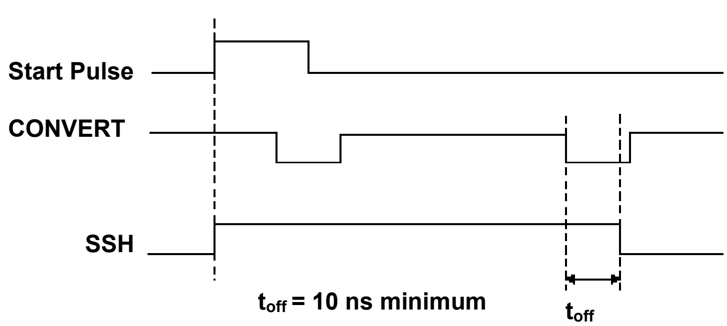

Figure 4-10. SSH signal timing

A/D CONVERT signal

The A/D CONVERT signal indicates the start of an A/D conversion. It is available through software selection as an input to any of the AUXIN pins (defaulting to AUXIN0) or the DAQ-Sync DS A/D CONVERT input and as an output to any of the AUXOUT pins.

When used as an input, the polarity is software selectable. The A/D CONVERT signal starts an acquisition on the selected edge. The selected edge (either rising of falling) of the convert pulses must be separated by a minimum of 10 µs to remain within the 100 kS/s conversion rate specification.

Refer to Figure 4-3 and Figure 4-6 for the relationship of A/D CONVERT to the DAQ sequence. Figure 4-11 and Figure 4-12 show the input and output pulse width requirements for the A/D CONVERT signal.

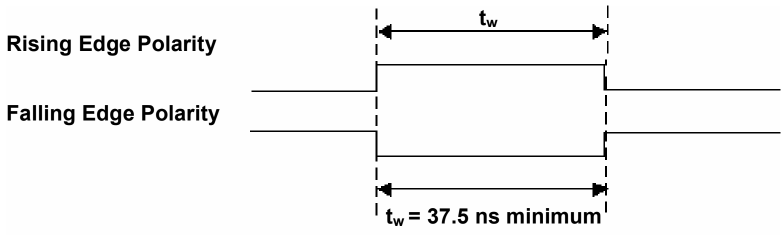

Figure 4-11. A/D CONVERT signal input timing requirement

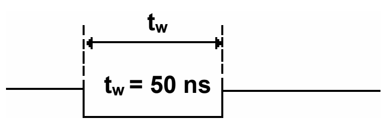

Figure 4-12. A/D CONVERT Signal Output Timing Requirement

The A/D CONVERT signal is generated by the on-board pacer circuit unless the external clock option is in use. This signal may be gated by hardware (A/D PACER GATE) or software.

A/D PACER GATE signal

The A/D PACER GATE signal is used to disable scans temporarily. This signal may be programmed for input at any of the AUXIN pins.

If the A/D PACER GATE signal is active, no scans can occur. If the A/D PACER GATE signal becomes active during a scan in progress, the current scan is completed and scans are then held off until the gate is de-asserted.

A/D EXTERNAL TIME BASE signal

The A/D EXTERNAL TIME BASE signal can serve as the source for the on-board pacer circuit rather than using the 40 MHz internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the A/D EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 4-13 shows the timing specifications for the A/D EXTERNAL TIME BASE signal.

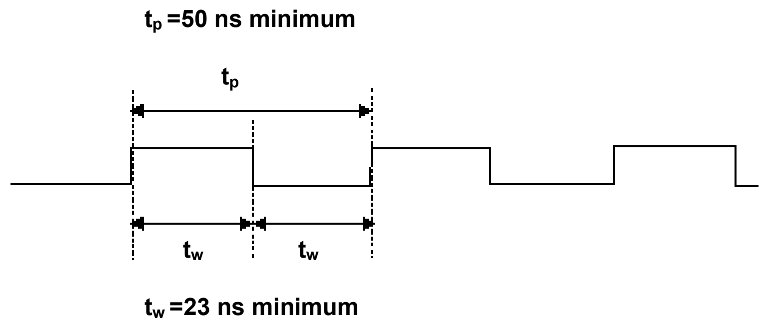

Figure 4-13. A/D EXTERNAL TIME BASE signal timing

A/D STOP signal

The A/D STOP signal indicates a completed acquisition sequence. You can program this signal to be available at any of the AUXOUT pins. The A/D STOP output signal is a 50 ns wide pulse whose leading edge indicates a DAQ done condition. Figure 4-14 shows the timing for the A/D STOP signal.

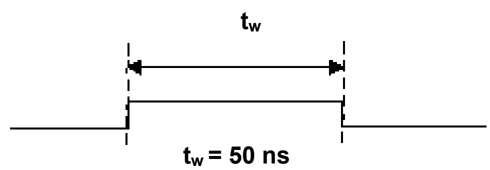

Figure 4-14. A/D STOP signal timing

ATRIG signal

In addition to standard digital trigger features, the PCI-DAS6030 and PCI-DAS6032 also provide analog triggering capability. When using the analog trigger, acquisitions may be started and controlled via an analog signal. There are four trigger/gate modes available using the analog trigger feature:

- Trigger – positive or negative slope.
- Gate – above reference or below reference.
- Hysteresis – positive or negative hysteresis.
- Window – inside or outside window.

The Trigger mode is used to start an acquisition sequence. The remaining modes provide gating functions during an acquisition sequence which start and stop the acquisition based on the gate condition.

There are two possible inputs for the analog trigger source (see Figure 4-15). The first is the AUXIN0/ATRIG pin on the 100-pin I/O connector. This is a software selectable dual-purpose pin that supports either digital or analog trigger inputs. The source selection defaults to analog trigger on power-up and may be modified at any time using *Insta*Cal. The input range on the ATRIG pin is always ±10V. 12-bit DACs are used to set the HI and LO levels for the threshold(s). The threshold resolution in this mode is 4.88mV per step.

Caution! Remove all analog inputs before configuring this pin as a digital input. Any voltage levels above ±15V in this configuration may cause damage to the product!

The second possible analog trigger source is the post-gain version of any one of the 16 analog inputs. In this mode, the voltage present on the first channel in the scan may be used to initiate the acquisition sequence.

Since the input to the analog trigger circuit has been scaled by the selected range, the effective resolution of the thresholds is equal to the A/D's full-scale-range (±2.5V) divided by 4096. For example, the ±2.5V range allows for 5V/4096, or 1.2 mV of threshold resolution.

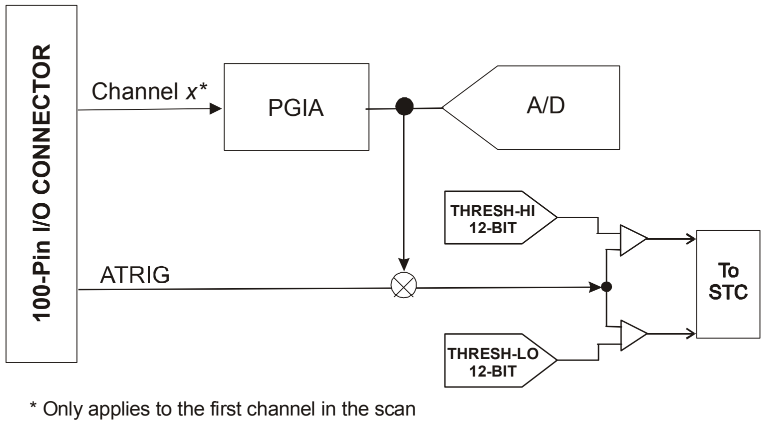

Figure 4-15. ATRIG Circuit

The next section includes a detailed description of each mode of operation. In each case, a ±2V triangle waveform is used as the ATRIG input source. The THRESH_HI is set to 1.0V and the THRESH_LO signal is set to -1.0V.

In the following analog trigger signal diagrams, the bold portion of the waveform indicates the data acquired for the given ATRIG mode.

Trigger Above

The acquisition will begin when the ATRIG signal first goes above the THRESH_HI. This mode is non-retriggerable.

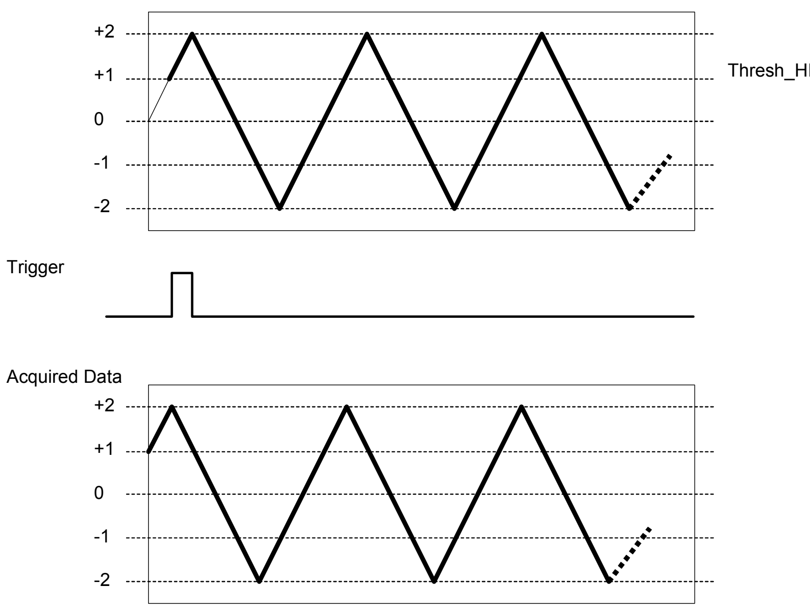

Figure 4-16. Trigger Positive Slope

Trigger Below

The acquisition will begin when ATRIG signal fist goes below the THRESH_LO level. This mode is non-retriggerable.

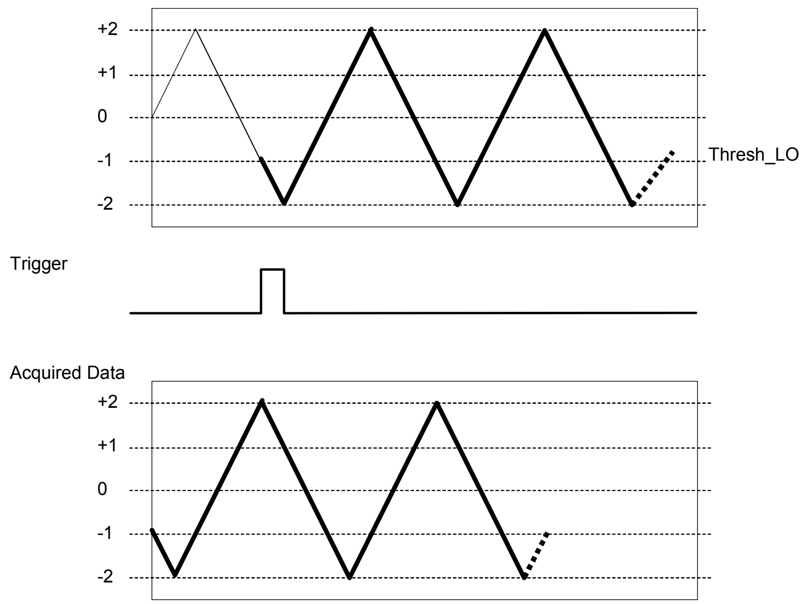

Figure 4-17. Trigger Negative Slope

Gate Above

Data acquisition is enabled whenever ATRIG goes above the THRESH_HI level. Acquisition is suspended whenever the ATRIG signal goes below the THRESH_HI level. This is a level-sensitive gating mode.

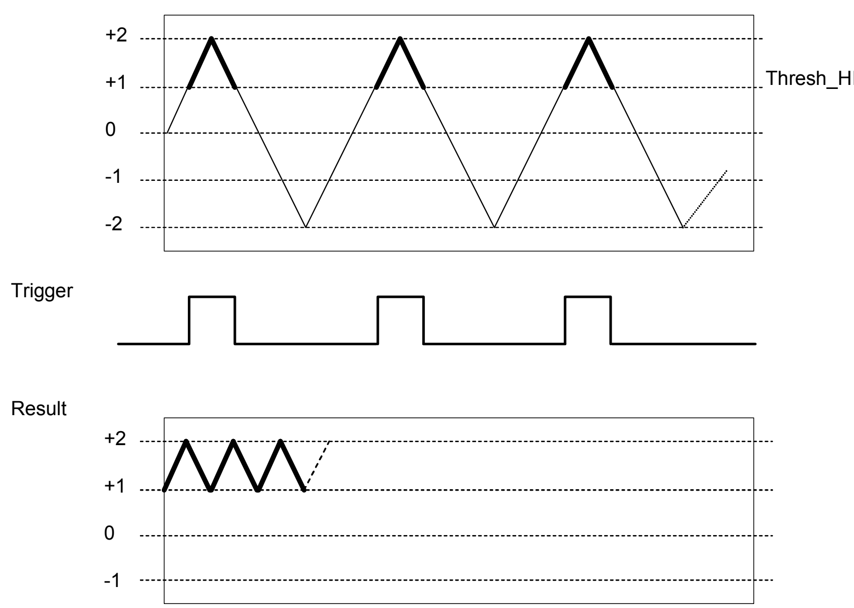

Figure 4-18. Gate Above

Gate Below

Data acquisition is enabled whenever ATRIG goes below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal goes above the THRESH_LO level. This is a level-sensitive gating mode.

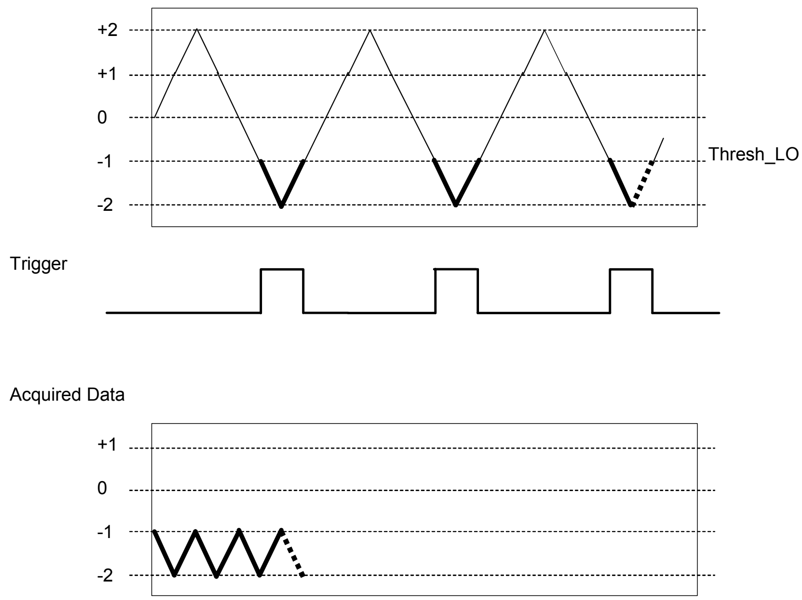

Figure 4-19. Gate Below

Gate Negative Hysteresis

Data acquisition is enabled whenever ATRIG goes above the THRESH_HI level. Acquisition is suspended whenever the ATRIG signal goes below the THRESH_LO level. The hysteresis level is set by THRESH_LO. This is a level-sensitive gating mode.

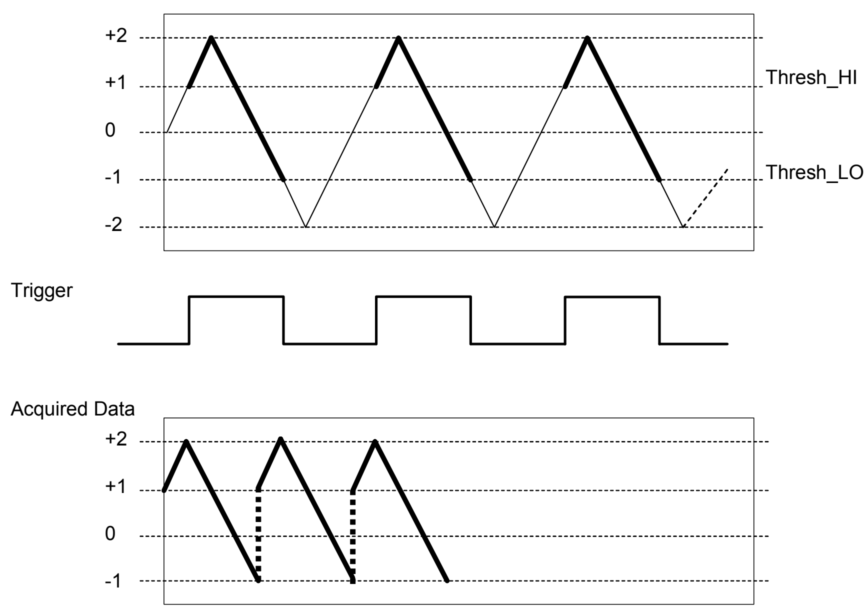

Figure 4-20. Gate Negative Hysteresis

Gate Positive Hysteresis

Data acquisition is enabled whenever ATRIG goes below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal goes above the THRESH_HI level. The hysteresis level is set by THRESH_HI. This is a level-sensitive gating mode.

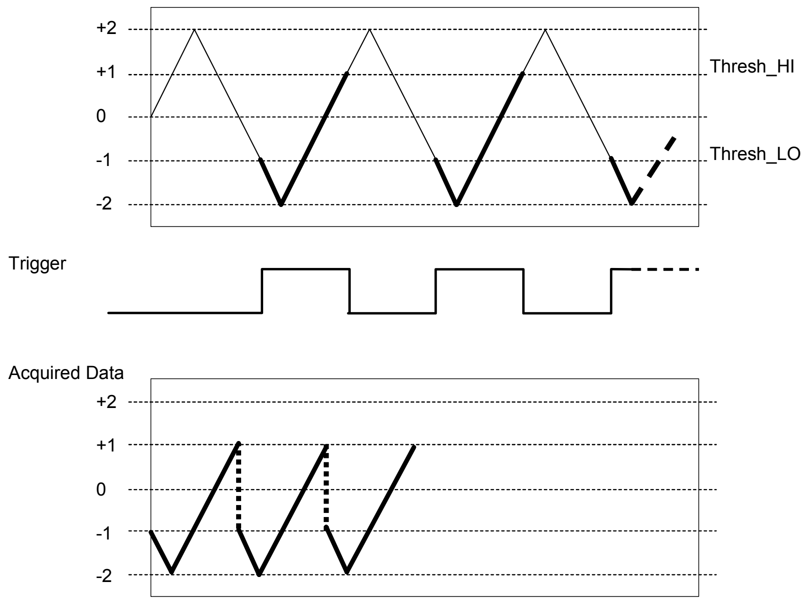

Figure 4-21. Gate Positive Hysteresis

Gate Inside Window

Data acquisition is enabled whenever ATRIG is below the THRESH_HI level and above the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal is outside of this region. This is a level-sensitive gating mode

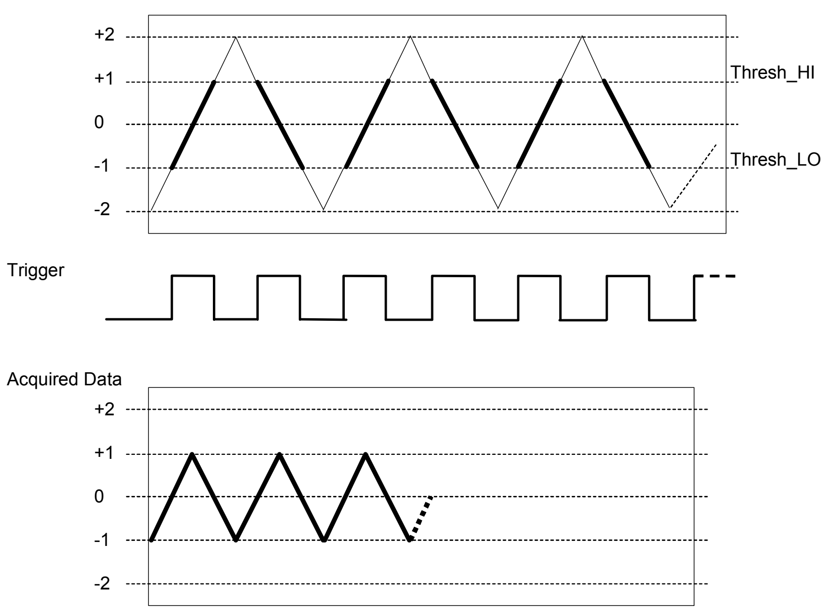

Figure 4-22. Gate Inside Window

Gate Outside Window

Data acquisition is enabled whenever ATRIG is above the THRESH_HI level or below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal is between the THRESH_HI and THRESH_LO levels. This is a level-sensitive gating mode

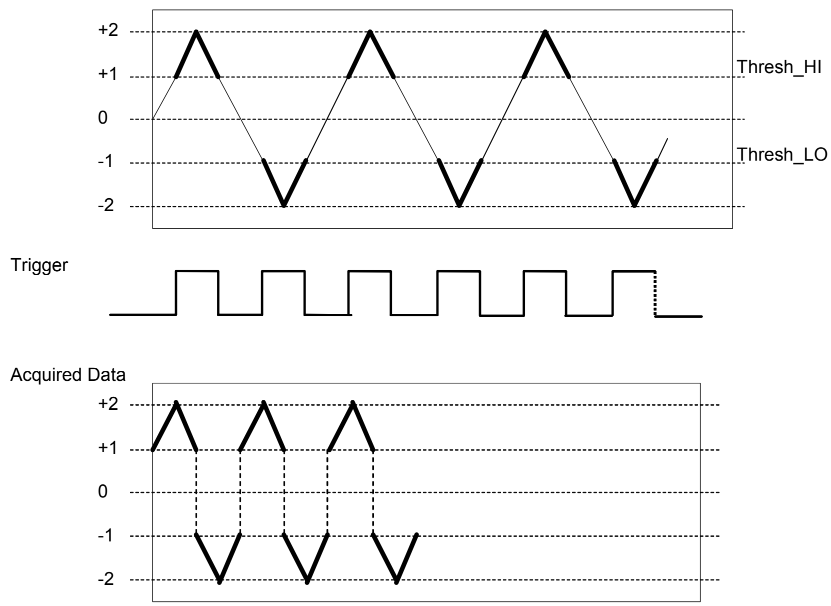

Figure 4-23. Gate Outside Window

Waveform generation timing signals

The signals that control the timing for the analog output functions on the PCI-DAS6030 are:

- D/A START TRIGGER
- D/A UPDATE
- D/A EXTERNAL TIME BASE

D/A START TRIGGER signal

The D/A START TRIGGER signal is used to hold off output scans until after a trigger event. The DAQ-Sync "DS D/A START TRIGGER" input or any AUXIN pin can be programmed to serve as the D/A START TRIGGER signal. It is also available as an output on any AUXOUT pin.

When used as an input, the D/A START TRIGGER signal may be software selected as either a positive or negative edge trigger. The selected edge of the D/A START TRIGGER signal causes the DACs to start generating the output waveform.

The D/A START TRIGGER signal can be used as an output to monitor the trigger that initiates waveform generation. The output is an active-high pulse having a width of 50 ns.

Figure 4-24 and Figure 4-25 show the input and output timing requirements for the D/A START TRIGGER signal.

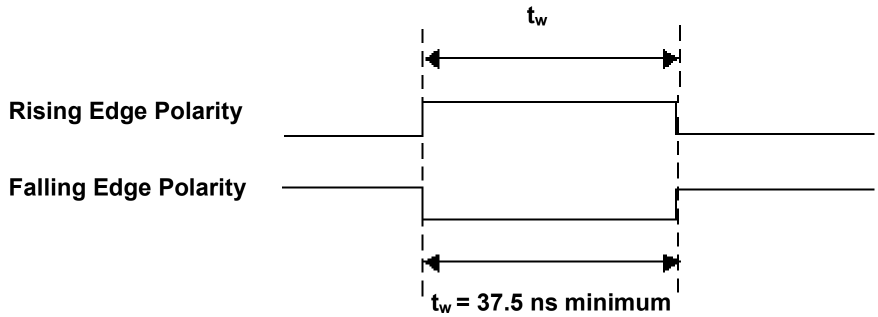

Figure 4-24. D/A START TRIGGER input signal timing

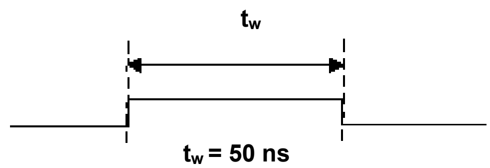

Figure 4-25. D/A START TRIGGER output signal timing

D/A CONVERT signal

The D/A CONVERT signal causes a single output update on the D/A converters. You can program the DAQ-Sync DS D/A UPDATE input or any AUXIN pin to accept the D/A CONVERT signal. It is also available as an output on any AUXOUT pin.

The D/A CONVERT input signal polarity is software selectable. DAC outputs update within 100ns of the selected edge. The D/A CONVERT pulses should be no less than 100 µs apart.

When used as an output, the D/A CONVERT signal may be used to monitor the pacing of the output updates. The output has a pulse width of 225 ns with selectable polarity.

Figure 4-26 and Figure 4-27 show the input and output timing requirements for the D/A CONVERT signal.

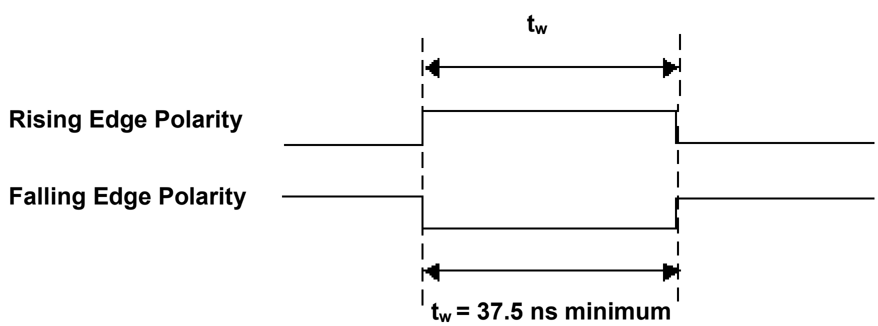

Figure 4-26. D/A CONVERT input signal timing

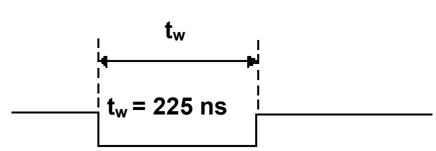

Figure 4-27. D/A CONVERT output signal timing

D/A EXTERNAL TIME BASE signal

The D/A EXTERNAL TIME BASE signal can serve as the source for the on-board DAC pacer circuit rather than using the internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the D/A EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 4-28 shows the timing requirements for the D/A EXTERNAL TIME BASE signal.

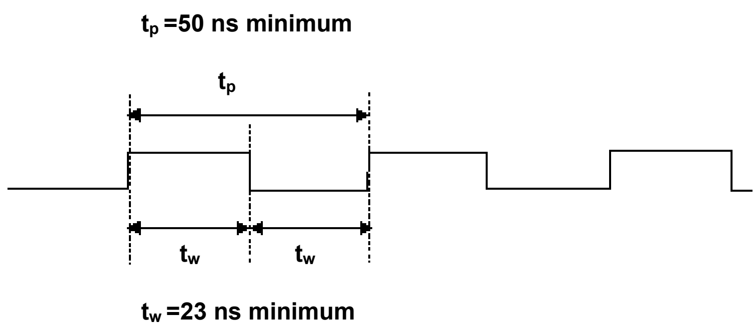

Figure 4-28. D/A EXTERNAL TIME BASE signal timing

General-purpose counter signal timing

The general-purpose counter signals are:

- CTR1 CLK
- CTR1 GATE
- CTR1 OUT
- CTR2 CLK
- CTR2 GATE
- CTR2 OUT

CTR1 CLK signal

The CTR1 CLK signal can serve as the clock source for independent user counter 1. It can be selected through software at the CTR1 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified.

Figure 4-29 shows the timing requirements for the CTR1 CLK signal.

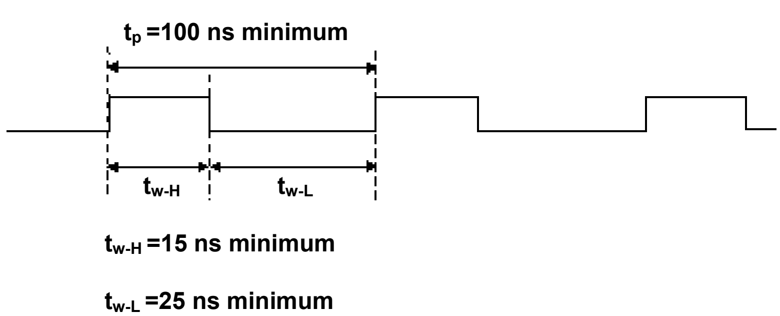

Figure 4-29. CTR1 CLK signal timing

CTR1 GATE signal

You can use the CTR1 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR1 GATE pin.

Figure 4-30 shows the minimum timing requirements for the CTR1 GATE signal.

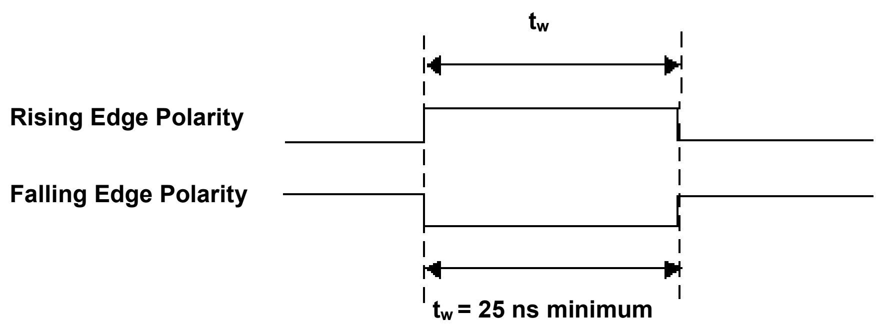

Figure 4-30. CTR1 GATE signal timing

CTR1 OUT signal

This signal is present on the CTR1 OUT pin. The CTR1 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip.

For detailed information on counter operations, please refer to the data sheet on our WEB page at http://www.measurementcomputing.com/PDFmanuals/82C54.pdf.

Figure 4-31 shows the timing requirements for the CTR1 OUT signal for counter mode 0 and mode 2.

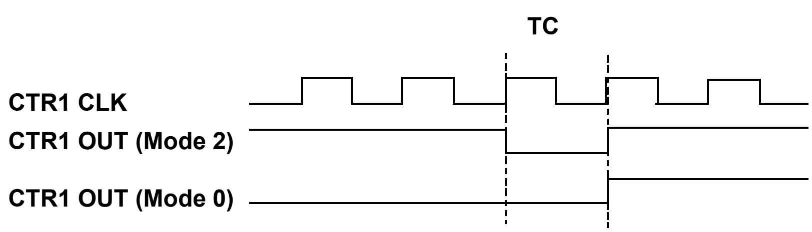

Figure 4-31. CTR1 OUT signal timing

CTR2 CLK signal

The CTR2 CLK signal can serve as the clock source for independent user counter 2. It can be selected through software at the CTR2 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified.

Figure 4-32 shows the timing requirements for the CTR2 CLK signal.

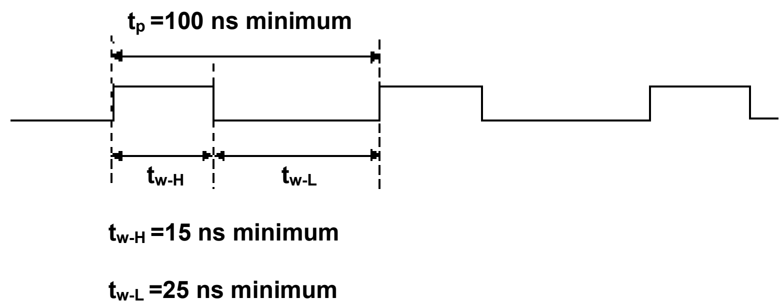

Figure 4-32. CTR2 CLK signal timing

CTR2 GATE signal

You can use the CTR2 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR2 GATE pin.

Figure 4-33 shows the timing requirements for the CTR2 GATE signal.

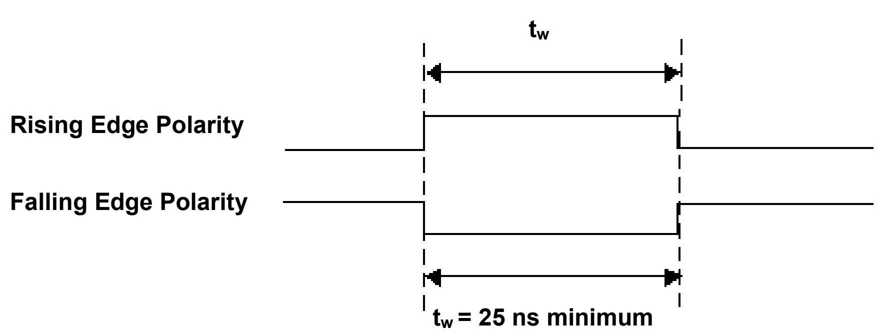

Figure 4-33. CTR2 GATE signal timing

CTR2 OUT signal

This signal is present on the CTR2 OUT pin. The CTR2 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip.

For detailed information on counter operations, please refer to the data sheet on our web site at http://www.measurementcomputing.com/PDFmanuals/82C54.pdf.

Figure 4-34 shows the timing of the CTR1 OUT signal for mode 0 and for mode 2.

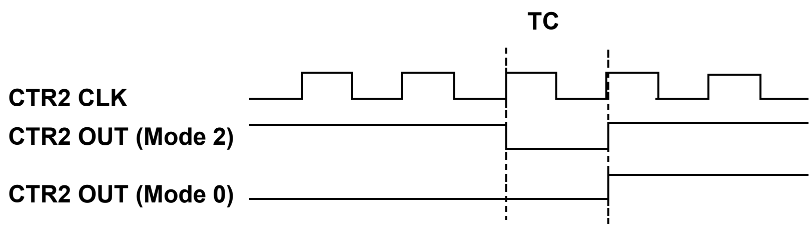

Figure 4-34. CTR2 OUT signal timing

Calibrating the Board

Introduction

You should calibrate the board (using the *Insta*Cal utility) after the board has fully warmed up. The recommended warm-up time is 15 minutes. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. Pre-measurement calibration ensures that your board is operating at optimum calibration values.

Calibration theory

Analog inputs are calibrated for offset and gain. Offset calibration for the analog inputs is performed directly on the input amplifier (PGIA) with coarse and fine trim DACs acting on the amplifier.

For input gain calibration, a precision calibration reference is used with coarse and fine trim DACs acting on the ADC (see Figure 5-1).

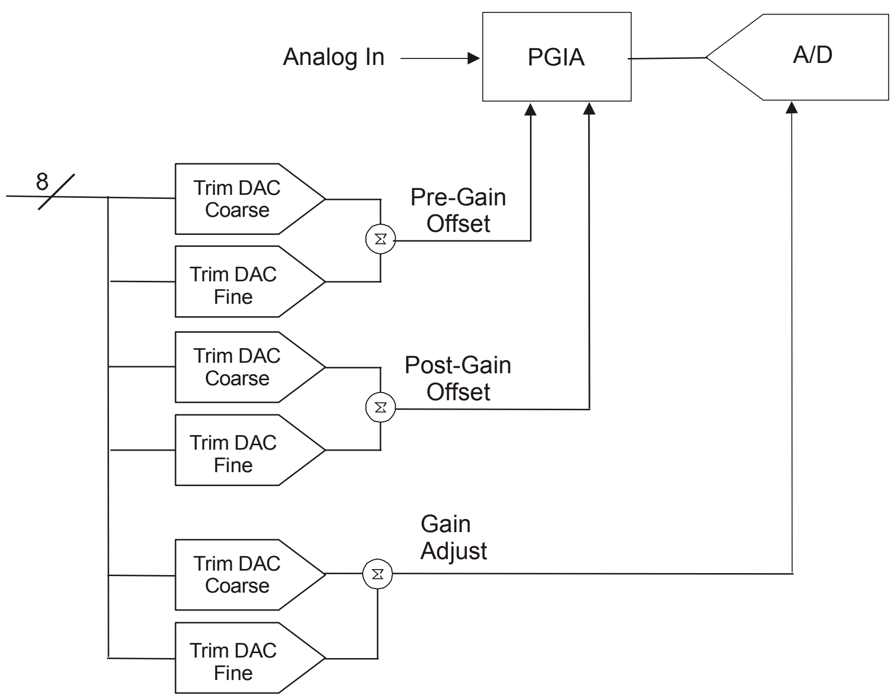

Figure 5-1. Analog input calibration - basic elements

A similar method is used to calibrate the analog output components. A trim DAC is used to adjust the gain of the DAC. A separate DAC is used to adjust offset on the final output amplifier. The calibration circuits are duplicated for both analog outputs (see Figure 5-2).

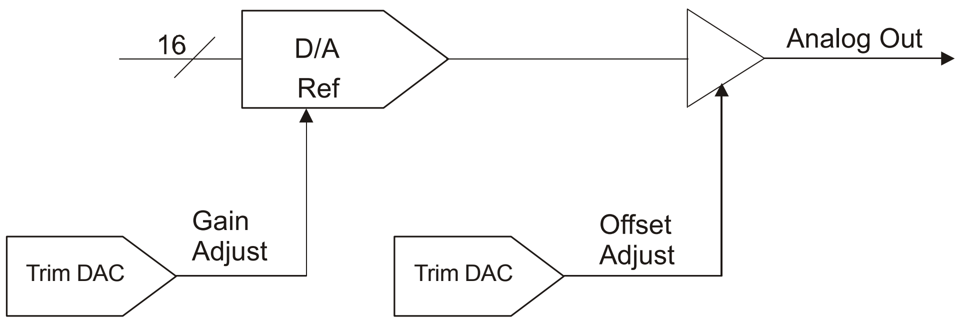

Figure 5-2. Analog output calibration – basic elements

Chapter 6

Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog Input

Table 1. Analog input specifications

A/D converter	Successive approximation type
Resolution	16 bits, 1 in 65536
Maximum sample rate	100 kS/s
Number of channels	16 single ended / 8 differential, software selectable
Input ranges	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, ±0.1 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2 V, 0 to 1 V, 0 to 0.5 V, 0 to 0.2 V, 0 to 0.1 V Software selectable
A/D pacing	Internal counter – ASIC. Software selectable time base: ▪ Internal 40 MHz, 50 ppm stability ▪ External source via AUXIN<5:0>, Software selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software selectable option, burst rate = 10 µS.
A/D gate sources	External digital: A/D GATE
	External analog: ATRIG input CH0 IN through CH15 IN
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to *Analog Trigger* on page 6.
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Refer to *Analog Trigger* on page 6.
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples.
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 K samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or Non-demand using scatter-gather.
Configuration memory	Up to 8 K elements. Programmable channel, gain, and offset.
Streaming-to-disk rate	100 kS/s, system dependent

Accuracy

100 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1 °C of internal calibration temperature and ±10 °C of factory calibration temperature. Calibrator test source high side tied to channel 0 high and low side tied to channel 0 low. Low-level ground is tied to channel 0 low at the user connector.

Table 2. Absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±3.81 LSB
±5 V	±13.61 LSB
±2 V	±13.69 LSB
±1 V	±13.83 LSB
±500 mV	±14.09 LSB
±200 mV	±16.71 LSB
±100 mV	±19.99 LSB
0 to 10 V	±6.40 LSB
0 to 5 V	±26.11 LSB
0 to 2 V	±26.28 LSB
0 to 1 V	±26.54 LSB
0 to 500 mV	±27.13 LSB
0 to 200 mV	±32.11 LSB
0 to 100 mV	±38.70 LSB

Table 3. Absolute accuracy components – all values are (±)

Range	% of Reading	Offset (µV)	Noise +Quantization (µV)		Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged[1]		
±10 V	0.0061	479.2	634.1	54.9	0.0001	1.147
±5 V	0.0361	243.6	317.1	27.5	0.0006	2.077
±2 V	0.0361	102.2	126.8	11.0	0.0006	0.836
±1 V	0.0361	55.1	63.4	5.5	0.0006	0.422
±500 mV	0.0361	31.6	36.8	3.2	0.0006	0.215
±200 mV	0.0411	17.4	22.5	2.0	0.0006	0.102
±100 mV	0.0461	12.7	19.6	1.8	0.0006	0.061
0 to 10 V	0.0061	326.6	417.8	36.6	0.0001	0.976
0 to 5 V	0.0361	167.3	208.9	18.3	0.0006	1.992
0 to 2 V	0.0361	71.7	83.6	7.3	0.0006	0.802
0 to 1 V	0.0361	39.9	41.8	3.7	0.0006	0.405
0 to 500 mV	0.0361	23.9	28.1	2.5	0.0006	0.207
0 to 200 mV	0.0411	14.4	19.6	1.8	0.0006	0.098
0 to 100 mV	0.0461	11.2	18.1	1.7	0.0006	0.059

1. Averaged measurements assume averaging of 100 single-channel readings.

Each PCI-DAS6030 and PCI-DAS6032 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

Table 4. Relative accuracy – all values are (±)

Range	Relative Accuracy (µV)	
	Single Point	Averaged [1]
±10 V	723.3	72.3
±5 V	361.6	36.2
±2 V	144.7	14.5
±1 V	72.3	7.2
±500 mV	42.2	4.2
±200 mV	26.5	2.7
±100 mV	24.1	2.4
0 to 10 V	482.2	48.2
0 to 5 V	241.1	24.1
0 to 2 V	96.4	9.6
0 to 1 V	48.2	4.8
0 to 500 mV	33.1	3.3
0 to 200 mV	24.1	2.4
0 to 100 mV	22.9	2.3

1. Averaged measurements assume averaging of 100 single-channel readings.

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 5. Differential non-linearity specifications

All ranges	±0.5 LSB typ	±1.0 LSB max

Settling time

Settling time is defined as the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to channel 1; a +FS DC signal is presented to channel 0.

Table 6. Settling time specifications

Condition	Range	±0.00076% (±0.5 LSB)	±0.0015% (±1 LSB)	±0.0061%(±4 LSB)	±0.012% (±8 LSB)
Same range to same range	±10 V	40 µS max	20 µS max	10 µS max	5 µS typ
	±5 V	40 µS max	20 µS max	10 µS max	5 µS typ
	±2 V	40 µS max	20 µS max	10 µS max	5 µS typ
	±1 V	40 µS max	20 µS max	10 µS max	5 µS typ
	±500 mV	40 µS max	20 µS max	10 µS max	5 µS typ
	±200 mV	40 µS max	20 µS max	10 µS max	5 µS typ
	±100 mV	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 10 V	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 5 V	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 2 V	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 1 V	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 500 mV	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 200 mV	40 µS max	20 µS max	10 µS max	5 µS typ
	0 to 100 mV	40 µS max	20 µS max	10 µS max	5 µS typ

Parametrics

Table 7. Parametrics specifications

Max working voltage (signal + common-mode)	±11 V
CMRR @ 60 Hz	±10 V range and 0 to 10 V: 92 dB
	±5 V range and 0 to 5 V: 97 dB
	±2 V range and 0 to 2 V: 101 dB
	±1 V range and 0 to 1 V: 104 dB
	±0.5 V range and 0 to 0.5 V: 105 dB
	±0.2 V range and 0 to 0.2 V: 105 dB
	±0.1 V range and 0 to 0.1 V: 105 dB
Small signal bandwidth, all ranges	*255 kHz*
Input coupling	*DC*
Input impedance	*100 GOhm in normal operation.*
	820 Ohm typ in powered off or overload condition.
Input bias current	*±200 pA*
Input offset current	*±100 pA*
Absolute maximum input voltage	*±25 V power on, ±15 V power off. Protected Inputs:* ▪ *CH<15:0> IN* ▪ *AISENSE*
Crosstalk	Adjacent Channels: -75 dB
	All other Channels: -90 dB

Noise performance

Table 8 summarizes the noise performance for the PCI-DAS6030 and PCI-DAS6032. Noise distribution is determined by gathering 50 K samples with inputs tied to ground at the user connector. Samples are gathered 100 kS/s sampling rate. The specification applies to both single-ended and differential modes of operation.

Table 8. Analog input noise performance specifications

Range	LSBrms	Typical counts
±10 V	0.6	8
±5 V	0.6	8
±2 V	0.6	8
±1 V	0.6	8
±500 mV	0.7	8
±200 mV	1.1	11
±100 mV	2.0	17
0 to 10 V	0.8	8
0 to 5 V	0.8	8
0 to 2 V	0.8	8
0 to 1 V	0.8	8
0 to 500 mV	1.1	11
0 to 200 mV	2.0	17
0 to 100 mV	3.8	25

Analog output (PCI-DAS6030 only)

Table 9. PCI-DAS6030 analog output specifications

D/A converter type	Double-buffered, multiplying
Resolution	16-bits, 1 in 65536
Number of channels	2 voltage output
Voltage range	±10 V, 0 to 10 V, software selectable
Monotonicity	*16-bits, guaranteed*
Update rate	100 kS/s per channel
Slew rate	5 V/µs typ.
Settling time (full scale step)	10 µs max to ±1 LSB
Noise	60 µVrms, DC to 1 MHz BW
Current drive	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms max.
Power up and reset	DACs cleared to 0 volts ±20 mV max.

Table 10. Analog output absolute accuracy specifications

Range	**Absolute Accuracy**
±10 V	±4.7 LSB
0 to 10 V	±7.9 LSB

Table 11. Absolute accuracy components - all values are (±)

Range	**% of Reading**	**Offset (µV)**	**Temp Drift (%/ºC)**	**Absolute Accuracy at FS (mV)**
±10 V	0.0062	813	0.0001	1.430
0 to 10 V	0.0062	584	0.0001	1.201

Each PCI-DAS6030 is tested at the factory to assure that the board's overall error does not exceed the values specified in Table 10.

Table 12. Relative accuracy specifications

Range	**Relative Accuracy**	
All ranges	±0.5 LSB, typical	±1.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog output pacing and triggering

Table 13. Analog output pacing and triggering specifications

DAC pacing (software programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz, 50 ppm stability. External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate sources (software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input; CH0 IN through CH15 IN
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to *Analog Trigger* below
DAC trigger sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH15 IN
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for Positive or Negative slope.
DAC pacer out	Available at user connector D/A PACER OUT
RAM buffer size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously, software selectable.
DMA modes	Demand or non-demand using scatter gather.
Waveform generation throughput	100 kS/s max per channel, 2 channels simultaneous

Analog trigger

Table 14. Analog trigger specifications

Analog trigger sources software selectable	External: ATRIG input CH0 IN through CH15 IN, first channel in scan	
Analog trigger levels	ATRIG input: ±10 V	
	CH0 IN through CH15 IN: ± Full-scale, range dependent	
Analog trigger modes	External analog: Software-configurable for: ▪ Positive or negative slope	
Analog gate modes	External analog: software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window	
Resolution	12-bits, 1-in-4096	
Accuracy	±1% full-scale range max	
Bandwidth (-3 dB)	ATRIG input	4 MHz
	CH0 IN through CH15 IN	255 kHz

Analog input / output calibration

Table 15. Analog I/O calibration specifications

Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 5.000 V ± 1 mV. Actual measured values stored in EEPROM.*
	Tempco: 0.6 ppm/°C max
	Long-term stability: ±6 ppm/sqrt (1000 hrs)
Calibration interval	1 year

Digital input / output

Table 16. Digital I/O specifications

Digital type	Discrete, 5V/TTL compatible
Number of I/O	8
Configuration	8 bits, independently programmable for input or output. All pins pulled up to +5 V via 47 K resistors (default). Positions available for pull down to ground. Hardware selectable via solder gap.
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20 V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupt Section

Table 17. Interrupt specifications

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9080
ADC interrupt sources (software programmable)	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE: Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL: Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE: Interrupt is generated after each conversion completes.
	DAQ_EOSCAN: Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ: Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (software programmable)	DAC_ACTIVE: Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE: Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY: Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL: Interrupt is generated when the DAC high channel output is updated.

Counters

Table 18. Counter specifications

User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5 V/TTL
CTRn base clock source (software selectable)	Internal 10 MHz, internal 100 kHz or external connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE).
Counter n output	Available at connector (CTRn OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15 ns min*
Low pulse width (clock input)	*25 ns min*
Gate width high	*25 ns min*
Gate width low	*25 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6030 and PCI-DAS6032 provide nine user-configurable trigger/clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs while three are configurable as outputs.

Table 19. Configurable triggers/clocks specifications

AUXIN<5:0> sources (SW selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> sources (SW selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections:	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5 V/TTL	
Minimum pulse width	37.5 ns	

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 20. DAQ-Sync signal specifications

DAQ-Sync signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power Consumption

Table 21. Power consumption specifications

+5 V	PCI-DAS6030/32: 1.3 A typical, 1.5 A max. Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1 A max, protected with a resettable fuse

Environmental

Table 22. Environmental specifications

Operating temperature range	0 to 55 °C
Storage temperature range	-20 to 70 °C
Humidity	0 to 90% non-condensing

Mechanical

Table 23. Mechanical specifications

Card dimensions	PCI half card: 174.4 mm (L) x 106.9 mm (W) x 11.65mm (H)

DAQ-Sync connector and pin out

Table 24. DAQ-Sync connector specifications

Connector type	14-pin right-angle 100mil box header
Compatible cables	MCC p/n: CDS-14-x, 14 pin ribbon cable. x = number of boards (2 - 5)

Table 25. DAQ-Sync connector pin out

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

Main connector and pin out

Table 26. Main connector specifications

Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100

Table 27. 8-channel differential mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN HI	52	n/c
3	CH0 IN LO	53	n/c
4	CH1 IN HI	54	n/c
5	CH1 IN LO	55	n/c
6	CH2 IN HI	56	n/c
7	CH2 IN LO	57	n/c
8	CH3 IN HI	58	n/c
9	CH3 IN LO	59	n/c
10	CH4 IN HI	60	n/c
11	CH4 IN LO	61	n/c
12	CH5 IN HI	62	n/c
13	CH5 IN LO	63	n/c
14	CH6 IN HI	64	n/c
15	CH6 IN LO	65	n/c
16	CH7 IN HI	66	n/c
17	CH7 IN LO	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6032

Table 28. 16-channel single-ended mode pin out

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	n/c
2	CH0 IN	52	n/c
3	CH8 IN	53	n/c
4	CH1 IN	54	n/c
5	CH9 IN	55	n/c
6	CH2 IN	56	n/c
7	CH10 IN	57	n/c
8	CH3 IN	58	n/c
9	CH11 IN	59	n/c
10	CH4 IN	60	n/c
11	CH12 IN	61	n/c
12	CH5 IN	62	n/c
13	CH13 IN	63	n/c
14	CH6 IN	64	n/c
15	CH14 IN	65	n/c
16	CH7 IN	66	n/c
17	CH15 IN	67	n/c
18	LLGND	68	n/c
19	n/c	69	n/c
20	n/c	70	n/c
21	n/c	71	n/c
22	n/c	72	n/c
23	n/c	73	n/c
24	n/c	74	n/c
25	n/c	75	n/c
26	n/c	76	n/c
27	n/c	77	n/c
28	n/c	78	n/c
29	n/c	79	n/c
30	n/c	80	n/c
31	n/c	81	n/c
32	n/c	82	n/c
33	n/c	83	n/c
34	n/c	84	n/c
35	AISENSE	85	DIO0
36	D/A OUT 0*	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1*	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	n/c	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6032

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6030

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN 61326 (1997) Amendment 1 (1998)

Emissions: Group 1, Class A

- EN 55011 (1990)/CISPR 11: Radiated and Conducted emissions.

Immunity: EN61326, Annex A

- IEC 1000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- IEC 1000-4-3 (1995): Radiated Electromagnetic Field immunity Criteria B.
- IEC 1000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- IEC 1000-4-5 (1995): Surge immunity Criteria A.
- IEC 1000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- IEC 1000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

Tests to IEC 1000-4-8 were not required. The PCI boards do not contain components that would be susceptible to magnetic fields.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in June, 2004. Test records are outlined in Chomerics Test Report #EMI3889.04.

We hereby declare that the equipment specified conforms to the above Directives and Standards.

Carl Haapaoja, Director of Quality Assurance

CE Declaration of Conformity

Manufacturer: Measurement Computing Corporation
Address: 10 Commerce Way
Suite 1008
Norton, MA 02766
USA

Category: Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6032

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EU EMC Directive 89/336/EEC: Electromagnetic Compatibility, EN 61326 (1997) Amendment 1 (1998)

Emissions: Group 1, Class A

- EN 55011 (1990)/CISPR 11: Radiated and Conducted emissions.

Immunity: EN61326, Annex A

- IEC 1000-4-2 (1995): Electrostatic Discharge immunity, Criteria A.
- IEC 1000-4-3 (1995): Radiated Electromagnetic Field immunity Criteria B.
- IEC 1000-4-4 (1995): Electric Fast Transient Burst immunity Criteria A.
- IEC 1000-4-5 (1995): Surge immunity Criteria A.
- IEC 1000-4-6 (1996): Radio Frequency Common Mode immunity Criteria A.
- IEC 1000-4-11 (1994): Voltage Dip and Interrupt immunity Criteria A.

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Carl Haapaoja, Director of Quality Assurance

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