FuturePlus Systems Corporation

FS4430 DP State Analysis Preprocessor

User Manual

For use with Agilent Logic Analyzers

Revision – 1.4

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Product Warranty

This FuturePlus Systems product has a warranty against defects in material and workmanship for a period of 1 year from the date of shipment. During the warranty period, FuturePlus Systems will, at its option, either replace or repair products proven to be defective. For warranty service or repair, this product must be returned to the factory.

Due to the complex nature of the FS4430 and the wide variety of customer target implementations, the FS4430 has a 30 day acceptance period by the customer from the date of receipt. If the customer does not contact FuturePlus Systems within 30 days of the receipt of the product it will be said that the product has been accepted by the customer. If the customer is not satisfied with the FS4430 they may return the FS4430 within 30 days for a refund.

For products returned to FuturePlus Systems for warranty service, the Buyer shall prepay shipping charges to FuturePlus Systems and FuturePlus Systems shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to FuturePlus Systems from another country.

FuturePlus Systems warrants that its software and hardware designated by FuturePlus Systems for use with an instrument will execute its programming instructions when properly installed on that instrument. FuturePlus Systems does not warrant that the operation of the hardware or software will be uninterrupted or error-free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. FUTUREPLUS SYSTEMS SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

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Assistance

Product maintenance agreements and other customer assistance agreements are available for FuturePlus Systems products. For assistance, contact Technical Support.

Introduction

How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the DP Bus** chapter introduces you to the FS4430 and lists the minimum equipment required and accessories supplied for DP bus analysis.
- The **State Analysis** chapter explains how to configure the FS4430 to perform state analysis on your bus.
- The **General Information** chapter provides information on the operating characteristics, and cable header pinout for the FS4430 probe.

Definitions

The following terms are used to describe aspects of the DP bus:

- Channel - One differential signal (2 wires).
- Link - One direction of a DP link. The FS4430 handles 1 DP and 1 Aux link.

Analyzing the DP Bus

This chapter introduces you to the FuturePlus Systems FS4430 preprocessor and lists the minimum equipment required for analysis.

The FS4430 is a DP State Analysis preprocessor. The preprocessor can connect to the target by either a half-size midbus probe, or flying leads. The “sideband” signals, such as AUX and HPD connect to the probe using separate cables. The preprocessor itself is controlled by the Probe Manager software, which runs under Windows and communicates with the preprocessor via a USB cable.

The FS4430 “snoops” a link without significantly degrading its signal integrity. The high speed serial signal is deserialized and processed for packet identification by the FS4430 before being sent to the logic analyzer connections. Additionally, the preprocessor provides trigger and filtering functions. The dis-assembler software running on the logic analyzer provides information regarding the transactions within the captured traffic.

Accessories Supplied

The FS4430 product consists of the following accessories:

- The FS4430 preprocessor, power supply and cable, Protocol Disassemblers (FS4430 and Aux Port for DP), FS44xx Probe Manager application and USB drivers on a CD. A USB cable is provided for connecting the FS4430 preprocessor to the Windows 2000 or XP based machine that the Probe Manager is loaded on.
- This User Manual and Quick Start sheet.

Minimum Equipment Required

The minimum equipment required for analysis of a DP consists of the following equipment:

- Agilent 169xx analysis frame with the 169xx modules. One is required for each DP and AUX link.
- A DPI target bus. It is **STRONGLY recommended** that the user review and apply the probing guidelines described in the FuturePlus Systems application note “Logic Analyzer Probing Design Guide for the FS440x” when planning for use of the preprocessor on any target system.

Probing System Overview

The architecture of the FS4430 preprocessor and the design of the DP link to be probed should both be thoroughly understood before attempting to use the probe.

The following is a general outline of the steps to be taken when probing a new link. Read the following pages for more specific information.

The FS4430 preprocessor requires the understanding and correct set-up of 4 different systems before a trace should be taken.

1. Probe Manager software. This software is identified as FS44xx Probe Mgr.exe and is on the CD that comes with the FS4430. Additionally, there is a folder within this CD that contains all the necessary USB drivers that your Windows system requires. When Windows searches for the USB drivers to load during the first connection of the FS4430, **Windows MUST be directed to load the drivers from this CD** in the system or the proper USB drivers will not load. In some cases it may necessary to temporarily disconnect the Windows system from the local network to insure that Windows does not automatically default to getting the drivers from the Internet. If the correct USB drivers are not loaded the user will see a Windows error ("Unable to load DLL") as soon as the "Run" button is used.

NOTE: The Microsoft .NET Framework must be on the system for the Probe Manager application to load properly.

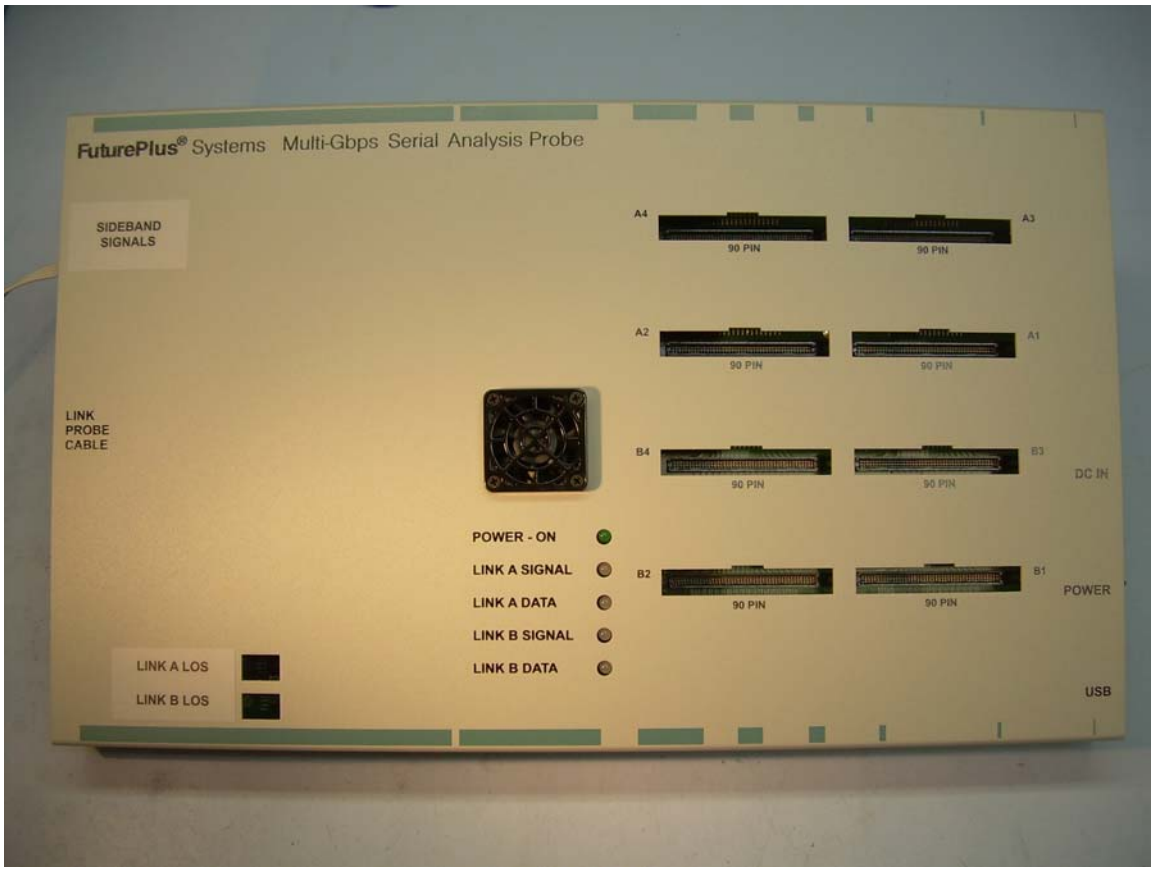
2. FS4430 probe. This preprocessor requires its own DC power supply which is provided. Additionally, this preprocessor is completely initialized, set-up and controlled by the Probe Manager software that resides on a Windows (2000 or XP) based system (either stand alone PC or logic analyzer). All communication to the FS4430 preprocessor is by means of the USB port on the PC (or logic analyzer). Improper or incomplete installation of either the correct USB driver or the Probe Manager software will prevent operation of the FS4430.
3. Agilent Logic Analyzer. The configuration files for the 169xx are on a CD (FS4430 and Aux). Install these files as required and follow the instructions for logic analyzer module (card) interconnections and logic analyzer connections to the FS4430 probe.
4. Target platform. There are two probing options, mid-bus probe or flying lead. There are also a variety of link implementations besides widths. There are protocol attributes such as lane inversion, data scrambling, and lane reversal, which need to be defined in the Probe Manager in order for the preprocessor to capture data properly.

It is strongly recommended that the user methodically proceed in the following manner when setting up the probe. There is more detail on each step in this manual.

1. Load the Probe Manager software and FS4430/AUX.exe files on the PC and/or logic analyzer. Leave the CD in the system for access to the USB drivers.
2. Configure (merge) the logic analyzer modules as required, and run the Agilent Logic analyzer's internal diagnostics. If the analyzer passes, then make the appropriate target probe connections to the FS4430 probe and from the probe to the Agilent logic analyzer. Use the Properties button on the probes shown in the Overview screen of the Agilent application for guidance on connecting the cables.
3. Connect the appropriate probing cable(s) to the target system, power up the probe. This may result in a Windows dialog searching for the "*FTDI FTD2XX*" USB drivers; direct it to the Probe Manager CD. Check the Windows Device Manager to make sure that it loaded properly.
4. Open up the Probe Manager application and select the appropriate settings for the probe cable being used and the target link. Check that the expected Pad assignments for the probed link show green. For the first capture turn off all the filters.
5. If the FS4430 preprocessor LEDs are all Green and the first trace file captured on the logic analyzer has no error messages then it is a good indication that all initial settings are correct.
6. A link showing Signal LED green and Data LED orange constantly, needs settings for link width, lane reverse or lane inversion adjusted in the Probe Config window.
7. A link showing Signal LED orange or red may have a problem with the r connection. More information on link signal status can be seen in the Log File window.

Depending on the DP target system's Reference Clock and data lane signal characteristics, such as jitter tolerance and jitter spectrum, the user may always see some level of orange LED activity and see the corresponding errors recorded on the analyzer and in the Probe Error Log.

Front Panel



The connections and features of the FS4430 preprocessor include:

- DC input for provided external AC to DC power supply (please note that the use of any other power supply voids the warranty on the FS4430), On/Off switch and USB connections to the Windows PC/169xx analyzer where the Probe Manager software will be loaded.
- Link Probe cable connection for 1 of the probing cables (mid-bus or FL)
- Logic Analyzer 90 and 40 pin pod connections. A1 – A4 are connections for A Link Processor (DP Link), and B1 – B4 are for B Link Processor (AUX link).
- Cables for connection to AUX and HPD.
- LED indication of preprocessor power on and Link status. There is a pair of LEDs which have the following states:

Link A Signal LED color	Meaning	Link A Data LED color	Meaning
Green	Link OK	Green	Data clocking Into Analyzer
Dark	Loss of Signal	Dark	No Data clocking into Analyzer
Orange	Data Invalid (8b10b error)	Orange	Any Error: 8b10b, Align, Framing, Idle
Red	Receiver Fault or Int	Red	Preprocessor Clock Error

Note: DP Link Status WILL ONLY Show on LINK A LEDs

FS4430 Probing Cables

The FS4430 can be configured with different probing cables dependent on what the user requires:

FS1032	½ size midbus footprint probe cable for x1 to x4
FS1036	Flying lead probing cable for x1 to x4
FS1040	DisplayPort Interposer

The “PCI Express Probing Design Guide for the FS440X” provides specific information on the successful application of midbus probing and also details general requirements for the Reference Clock signal and other aspects of the link to be probed. The FS4430 manual assumes that the user is familiar with this information and has applied it.

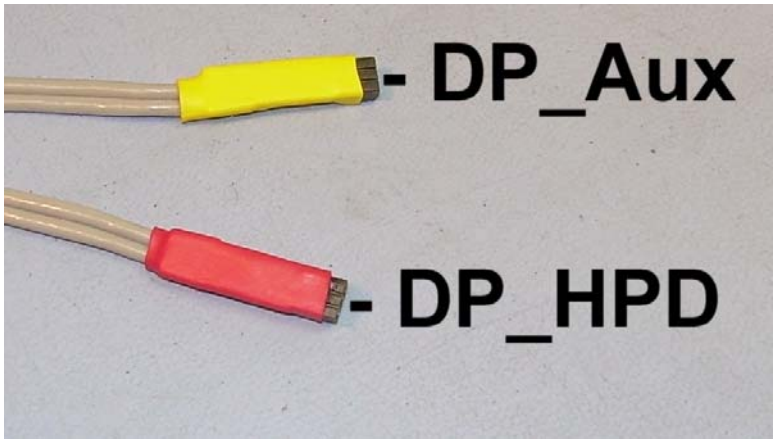
The cable should be attached to the FS4430 and carefully secured with the 2 captive fasteners on the cable. The probing end should be attached to the target by screwing into the retention module (midbus probe) Use of the flying lead probe requires careful installation and mechanical support of special flex circuit tips

The “sideband” signals for DP need to be connected to the FS4430 preprocessor separately from the data link probing cables. There are uniquely identified and labeled cables for doing this. **These must be properly oriented for polarity.**

The DP AUX channel requires a high speed differential connection using a Samtec .050 header where pins 1 and 3 are AUXp and AUXn. The HP_INT signal has its own cable that also connects to a .050 header, pin 1 is the signal and pin 2 is the ground connection.

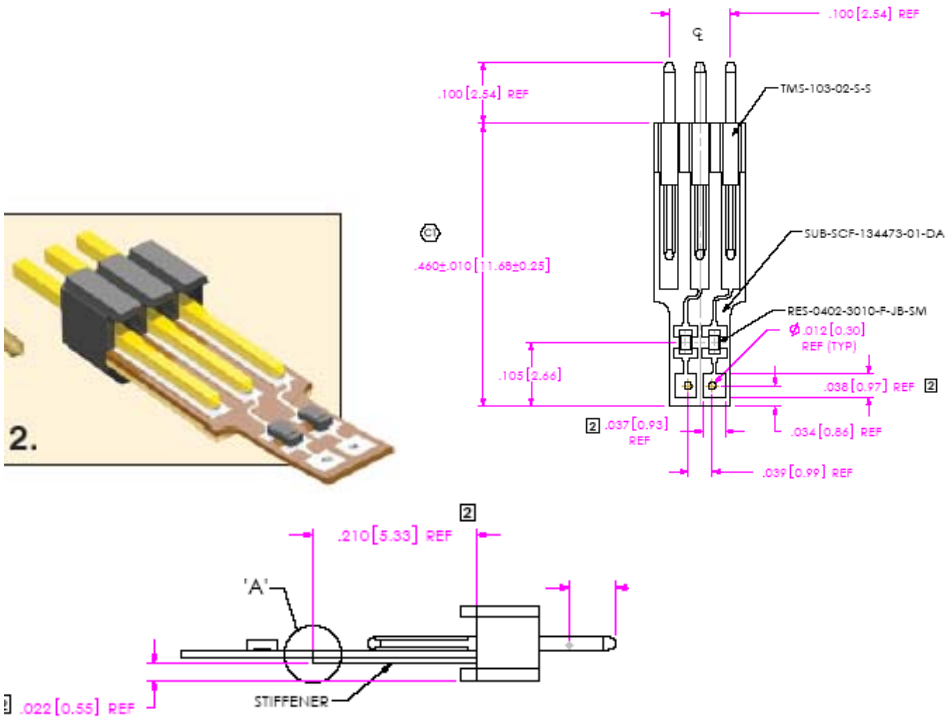
“sideband” cables

NOTE: These signals cannot see voltages higher than 4 VDC or there is a risk of damaging the preprocessor.



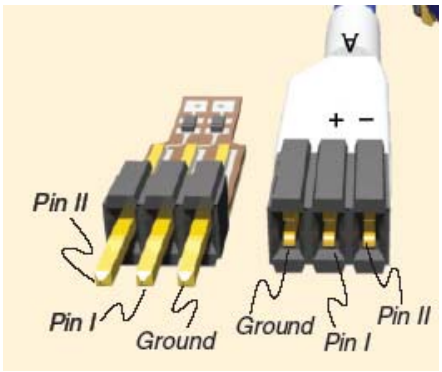
Flying Lead Probing (FS1036 cable assembly)

The FS1036 flying lead cable assembly allows the FS4430 preprocessor to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb.



A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036 cable that provides detail on how to solder the flex pcb to your board. Refer to this document.
2. Polarity matters. Makes sure you know how the + and – sides of the signal are connected. Adjustment to polarity can be made in the Probe manager.



FS1036 Flying Lead flex tips only.

Not the “sideband signals

The FS1036 flying lead cable has 8 pairs of channel connectors which are labeled A-G for up to 4 channels of a link and B-H which can be used for another link.

Make the appropriate cable and channel selections in the Probe Manager before taking any measurements.

Installing your Software for the First Time

The following outlines the software installation procedure when using the preprocessor for the first time. Please do not attach the preprocessor to the analyzer or computer that will be controlling the preprocessor until told to do so.

1. Place the software CD that came with the product into the logic analyzer or computer that you will be installing the software on. In the case of a machine that does not have a CD drive, the machine will either have to be put on a network and the files loaded remotely or the CD files can be transferred from a USB drive.

2. Navigate to the installation CD using Windows explorer and click on the following files. Follow the instructions on the screen to install.*

   - FS4430 and AUX.exe Protocol Dis-assemblers

   - FS44xx Probe Mgr.exe

3. Once all the above files have been installed, connect the FS4430 to the analyzer/computer via the USB port. Power on the FS4430 probe.

4. The found new hardware wizard should appear the first time the preprocessor is attached and powered up. Select “No, not this time” when it asks if the computer can go to Windows update to search for the software. Then select Next.

5. On the next screen select the Advanced option (not the Recommended) to select from a specific list or location. Select Next.

6. Select the CD-ROM drive to load the driver from; you do not have to select a specific directory. Select Next.

7. There may be a warning that comes up about Windows XP compatibility, ignore this warning and continue with installation.

8. Click Finish to complete the installation.

Once all the previous steps have completed all necessary software as well as USB drivers will be installed. This procedure only needs to be done on initial install. You may now go to the desktop and click on the Probe manager icon to start the probe manager.

*If you are installing on a PC to only control the FS4430 then you can omit the installation of the FS4430/AUX.exe, but you must follow the rest of the steps.

For instructions on loading system files please refer to the section on loading system files later in this manual.

Connecting the Agilent logic analyzer to the FS4430

The FuturePlus Systems connectors on the FS4430 are designed to connect directly to the cables on either the 16910/1 (40 pin headers) or the 16950 (90 pin headers).

The FS4430 is designed to enable the user to connect the FS4430 to the widest possible range of Agilent logic analyzer modules (cards). This table describes the possible configurations:

Module PN	Pods per module	Conn Style	Module State speed norm/turbo	Module Qty for x1 - x4 1.6 Gb/sDP link" (LA state clock 160 MHz)	Module Qty for x1 - x4 2.7 Gb/sDP link" (LA state clock 270 MHz)	Module Qty for AUX" (state clock 67 KHz)
16950A	4	90 pin	300/600	1	1	1
16911	4	40 pin	250/500	1	2 (turbo)	1
16910	6	40 pin	250/500	1	1 (turbo)	1

Logic Analyzer		FS4430	Comment
DP LA outputs are fixed regardless of which input link is used			
Card 1 Pod	1	A1	Clock
	2	A2	
	3	A3	
	4	A4	
AUX LA outputs are fixed regardless of which input link is used			
Card 2 Pod	1	B1	Clock
	2	B2	
	3	B3	
	4	B4	
10b Link A and B (need 6 pods to include time tags)			
Master	1	A1 or B1	Clock
	2	A2 or B2	
	3	A3 or B3	
	4	A4 or B4	
	5 & 6 for time tags		

Based on the probing needs install the appropriate modules into the Agilent logic analyzer and remove any adapter cables that may be attached to the module cables. When probing a single direction of an x1, x2 or x4 link, the FS4430 drives 4 pods of signals to the logic analyzer.

It is important before you load a system file you initiate a self test on all your modules installed in your logic analyzer to insure all modules are working properly.

Loading configuration files

DP – x1, x2, x4 DP link analysis. Requires 68 logic analysis channels.

AUX – AUX analysis requires 68 logic analysis channels.

Setting up the 1690x or 1680x Analyzer

The 16900 Analyzer is a PC based application that requires a PC running Windows OS with the Agilent logic analyzer software installed or a 169xx frame.

Before installing the protocol decoder for the FS4400 on a PC you **must** install the Agilent logic analyzer software first. Once the Agilent logic analyzer software is installed, you can install the FS4400 protocol decoder by placing the CD-ROM disk into the CD-ROM drive of the target computer or Analyzer and executing the .exe setup program that is contained on the disk. The .exe setup file can be executed from within the File Explorer PC Utility. You must navigate to the FS4430.exe file on the CD-ROM disk and then double click the FS4430.exe file from within the File Explorer navigation panel.

The installation procedure does not need to be repeated. It only needs to be done the first time the Analysis Probe is used.

168/90x Licensing

The FS4430 Protocol Decoder is a licensed product that is locked to a single hard drive. The licensing process is performed by Agilent. There are instructions on this process on the SW Entitlement certificate provided with this product.

Loading configuration files

When the software has been licensed you should be ready to load a configuration file. You can access the configuration files by clicking on the folder that was placed on the desktop. When you click on the folder it should open up to display all the configuration files to choose from. If you put your mouse cursor on the name of the file a description will appear telling you what the setup consists of, once you choose the configuration file that is appropriate for your configuration the 16900 operating system should execute. The protocol decoder automatically loads when the configuration file is loaded. If the decoder does not load, you may load it by selecting tools from the menu bar at the top of the screen and select the decoder from the list.

Offline Analysis

Data that is saved on a 16900 analyzer data as an *.ala file, can be imported into the 1680/90/900 environment for analysis. You can do offline analysis on a PC if you have the 1680/90/900 operating system installed on the PC, if you need this software please contact Agilent.

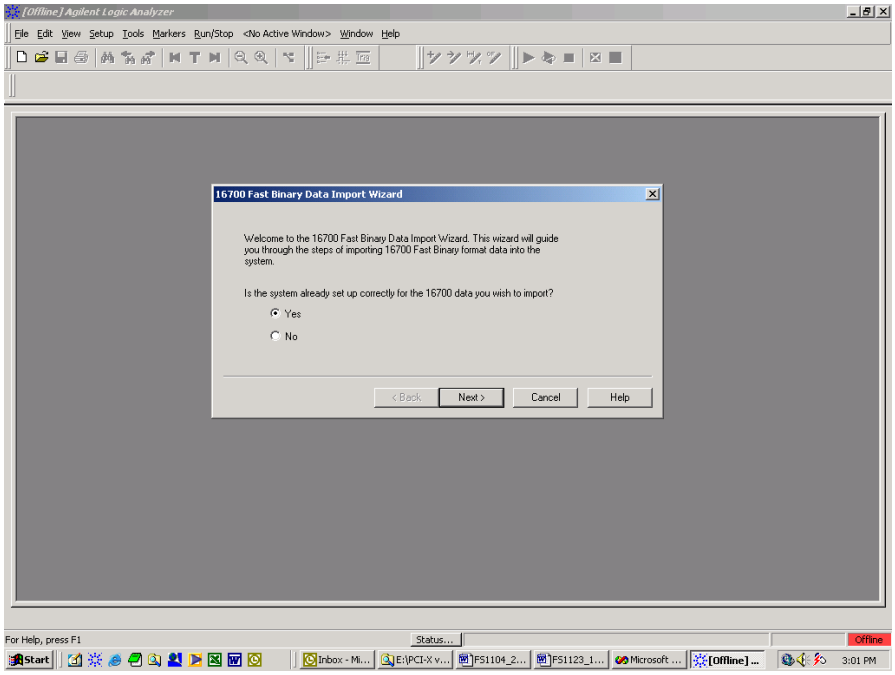
Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

If you have already used the license that was included with your package on a 1680/90/900 analyzer and would like to have the offline analysis feature on a PC you may get additional licenses at no charge, please contact FuturePlus.

In order to view decoded data offline, after installing the 1680/90/900 operating system on a PC, you must install the FuturePlus software. Please follow the installation instructions for “Setting up 1680/90/900 analyzer”. Once the FuturePlus software has been installed and licensed follow these steps to import the data and view it.

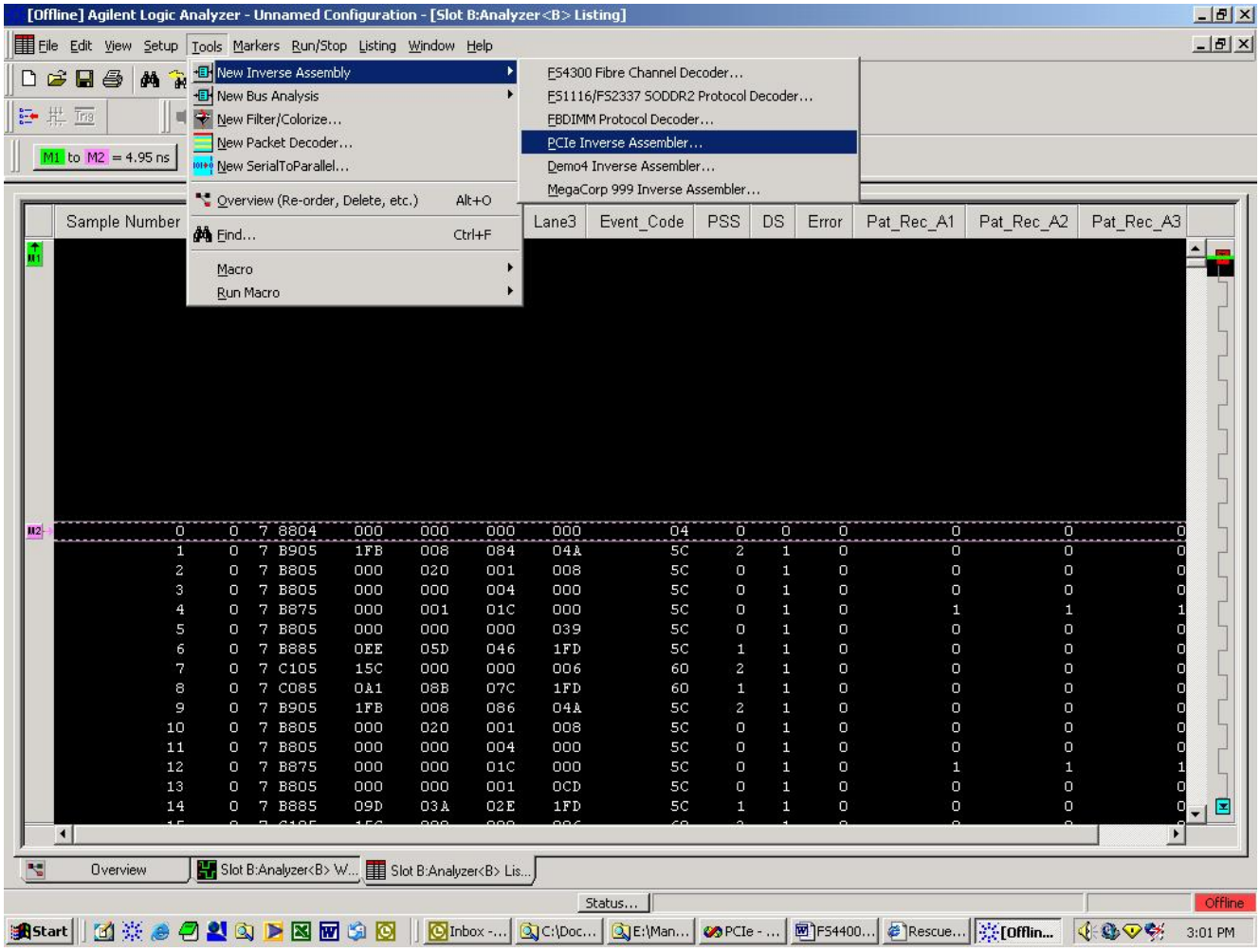
From the desktop, double click on the Agilent logic analyzer icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

For data from a 1680/90/900 analyzer, open the .ala file using the File, Open menu selections and browse to the desired .ala file.



After clicking “next” you must browse for the fast binary data file you want to import. Once you have located the file and clicked start import, the data should appear in the listing.

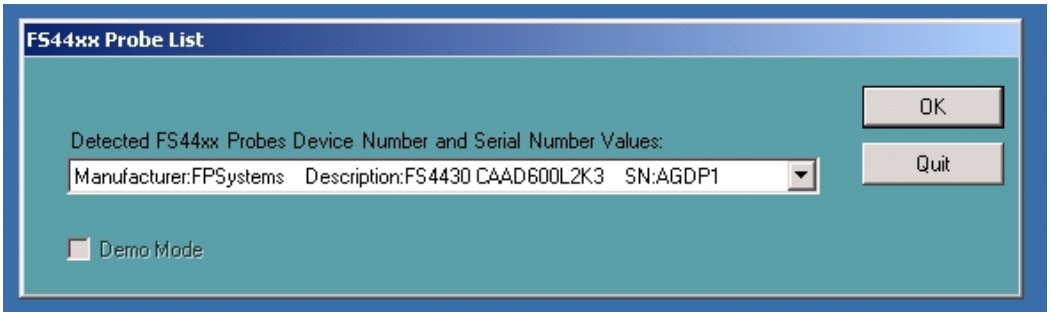
After the data has been imported you must load the protocol decoder before you will see any decoding. To load the decoder select Tools from the menu bar, when the drop down menu appears select Inverse Assembler, then choose the name of the decoder for your particular product. The figure below is a general picture; please choose the appropriate decoder for the trace you are working with.


[Offline] Agilent Logic Analyzer - Unnamed Configuration - [Slot B:Analyzer<B> Listing]
File Edit View Setup Tools Markers Run/Stop Listing Window Help
New Inverse Assembly
New Bus Analysis
New Filter/Colorize...
New Packet Decoder...
New SerialToParallel...
Overview (Re-order, Delete, etc.) Alt+O
Find... Ctrl+F
Macro
Run Macro
FS4300 Fibre Channel Decoder...
FS1116/FS2337 SODDR2 Protocol Decoder...
FBDIMM Protocol Decoder...
PCIe Inverse Assembler...
Demo4 Inverse Assembler...
MegaCorp 999 Inverse Assembler...
M1 to M2 = 4.95 ns
Sample Number
Lane3
Event_Code
PSS
DS
Error
Pat_Rec_A1
Pat_Rec_A2
Pat_Rec_A3
0 0 7 8804 000 000 000 000 04 0 0 0 0 0 0
1 0 7 B905 1FB 008 084 04A 5C 2 1 0 0 0 0
2 0 7 B805 000 020 001 008 5C 0 1 0 0 0 0
3 0 7 B805 000 000 004 000 5C 0 1 0 0 0 0
4 0 7 B875 000 001 01C 000 5C 0 1 0 1 1 1
5 0 7 B805 000 000 000 039 5C 0 1 0 0 0 0
6 0 7 B885 0EE 05D 046 1FD 5C 1 1 0 0 0 0
7 0 7 C105 15C 000 000 006 60 2 1 0 0 0 0
8 0 7 C085 0A1 08B 07C 1FD 60 1 1 0 0 0 0
9 0 7 B905 1FB 008 086 04A 5C 2 1 0 0 0 0
10 0 7 B805 000 020 001 008 5C 0 1 0 0 0 0
11 0 7 B805 000 000 004 000 5C 0 1 0 0 0 0
12 0 7 B875 000 000 01C 000 5C 0 1 0 1 1 1
13 0 7 B805 000 000 001 0CD 5C 0 1 0 0 0 0
14 0 7 B885 09D 03A 02E 1FD 5C 1 1 0 0 0 0
Overview
Slot B:Analyzer<B> W...
Slot B:Analyzer<B> Lis...
Status...
Offline
Start
Inbox -...
C:\Doc...
E:\Man...
PCIe - ...
FS4400...
Rescue...
[Offlin...
3:01 PM

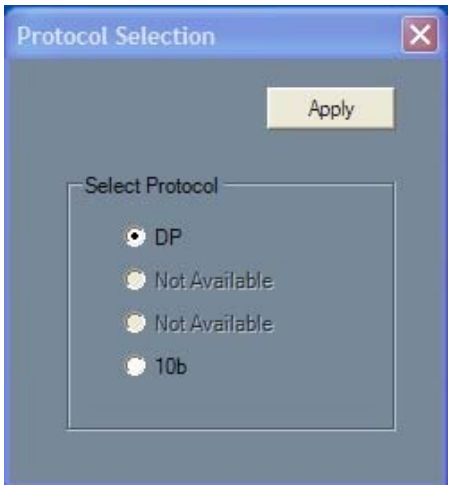
Probe Manager Application

The Probe Manager software can be found as the FS44xx Probe Mgr.exe file on the CD provided in the Documentation package. Insert the CD into the computer that will be used to control the FS4430 probe. This computer must have a USB connection. Using Windows File Manager, select the FS44xx Probe Mgr.exe file and double-click it, which initiates the installation software on the computer and places an icon on the desktop. Follow the directions that follow including agreeing to the license terms, once the software installation is complete click on finish. To start the program manager simply double click its desktop icon.

The Probe Manager application detects all FS44xx probes that are connected to the USB bus and allows the user to select which preprocessor will be controlled by the current instance of the Probe Manager application from the initial screen as seen below.



The initial screen is followed by the Protocol Selection screen, in which the user selects a protocol to configure the FS4430 Probe. The FS4430 has choices for DP and raw 10b decode.



Once the protocol has been selected, the application displays the Main dialog as seen below:

The user configures and controls the preprocessor from the main form. The form is composed of a menu bar, a tool bar and a status message bar. The menu bar provides options that allow the user to configure and run the probe. The tool bar provides options to configure the preprocessor and the status bar displays the probes current status and/or any errors that may have been encountered. Error messages displayed in the status bar are also logged in the Log Form if logging is enabled.

The menu bar contains the following options:

File

- Open Config File – Displays an open file dialog in which the user may navigate to and open the file contains a previous session's saved probed settings.
- Save As - Displays a save file dialog in which the user may specify where a preprocessor settings system file may be saved.
- Exit – Shut down the application.

Edit

- Modify Title String – Allows the user to specify the title string that appears in all sub-dialog's title bar. This is helpful when running multiple probes.

Run/Stop

- Run Probe Mgr – Running the preprocessor with the current settings. This is an alternative to clicking the tool bar Run button.
- Stop Probe Mgr - Stop the probe. This is an alternative to clicking the tool bar Stop button

Upgrade

- FPGA – Upgrade one of four protocol specific FPAG configurations.

Help

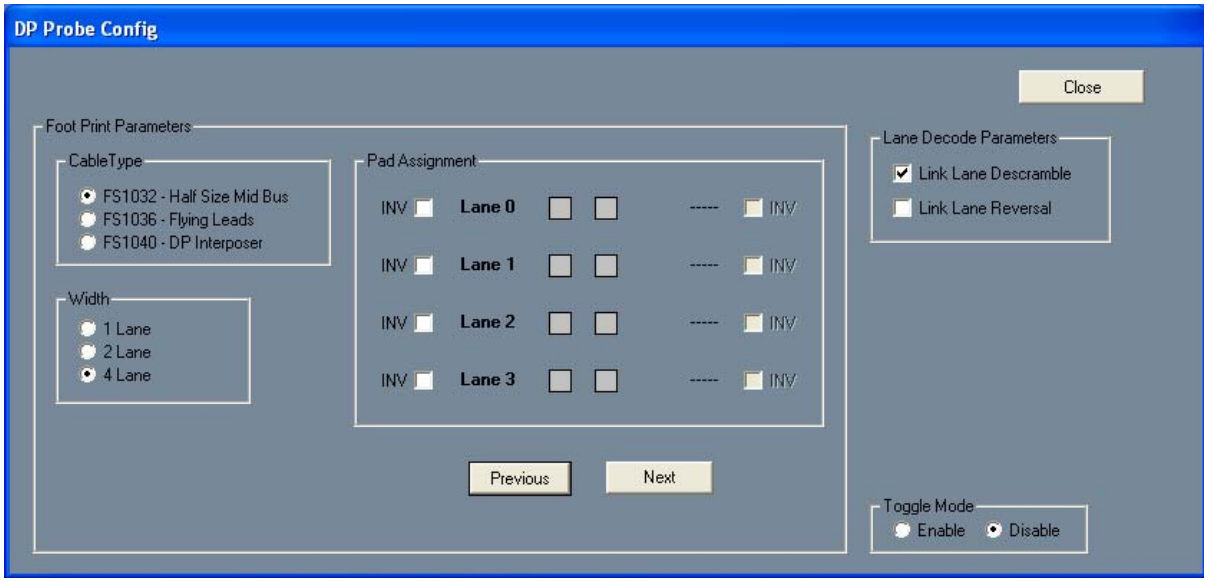
- About – Display version numbers for the Probe Manager application and FPGA configuration.

Preprocessor Configuration

The application displays up to five sub-dialogs. These are used to configure the FS4430 probe.

The four sub-forms are:

- Probe Configuration – Covers the type of cable used and basic aspects of the link being probed.
- Filters – Allows the user to specify the types of packets to be filtered
- Pixel Recognizers – Allows triggering on specific pixel values
- Log Entries – Run time preprocessor status.



DP Probe Config X1 X2 X4 Dialog

Note: there is no Config required for Aux signals

The functions provided on these forms include:

- Selection of the Probing Cable type, Link width, and pad arrangement (referring to the arrangement of lanes on the mid-bus probe pads; see the "PCI Express Probing Design Guide for the FS440X" for more specific information).
- The Pad Assignment graphic shows the assignment of logical lanes as a result of user selections, and also represents the physical layout of mid-bus pads. The FS4430 processes channels from the left column in link-processor A and from the right column in link-processor B.
- Next or Previous buttons scroll through the various types of currently supported pad assignments.
- Lane Inversion can be selected on an individual channel basis by clicking the INV button associated with each lane.
- While the preprocessor is stopped, signal activity indicators are provided on each channel. Signal presence is indicated by an up-down arrow symbol and a lack of signal presence is indicated by a flat horizontal line symbol.
- Selection of Lane Reversal on each link.
- Selection of Data Descrambling on each link.
- Selection of Toggle mode. When activated, the preprocessor output signals to the logic analyzer pods and the link status LEDs are toggled.

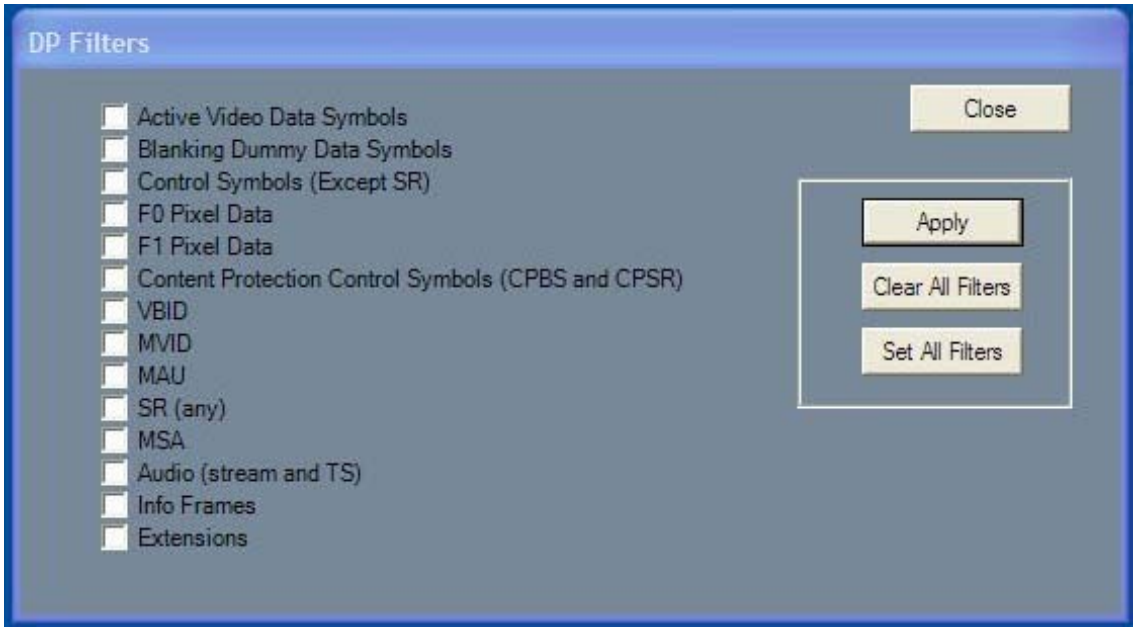
Dynamic Lane width tracking

The FS4430 can maintain lock and processing on a DP link as it changes lane width. Because a reset to the preprocessor's serdes would result in the loss of lane data, the serdes is not reset when lane width changes. For this reason we recommend that the FS4430 be set in the Probe Manager to the maximum lane width at the start. As the lane width decreases the user will notice that the Signal LED goes dark, but the Data LED stays green. This is acceptable as it is just an indication that the serdes has lost signal on the lanes no longer operating. Also, the error log will show errors on the lanes that are no longer in operation.

You can stop the probe, reconfigure the lane width, and then restart the probe. This will set-up the serdes properly for that new lane width and all the LEDs and Error Log should operate properly at that new lane width.

Filtering

The Filter dialogue page provides the user with a comprehensive suite of predefined filter functions to apply to either Link. These filters are state based, which means that the event has to occur on all active lanes for it to be filtered.



DP Filters Dialog

Filter types include all types of states. Many of the filters will operate on several types of states, e.g. “Content Protection Control Symbols” will filter all control symbols associated with any Content Protection sequence of states.

Filters can be enabled to filter out entire secondary data packets. There are currently no capabilities to filter portions of any secondary data packets.

Filtering is done in real time by the FS4430 hardware. It must be stopped to change Filter settings.

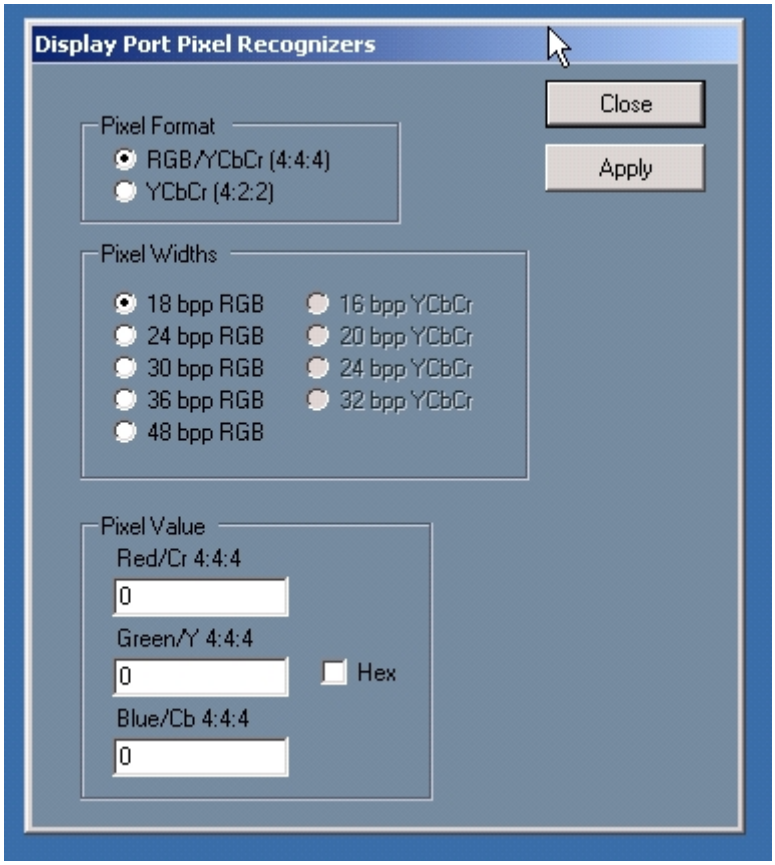
When “Decode Pixel States” is selected in the Protocol Decoder Preferences, then you cannot filter Control Symbols.

Filtering out unwanted traffic such as dummy data symbols can extend the storage capabilities of the logic analyzer. Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

To filter out any particular traffic type, click on the appropriate box so a √ appears and click apply. You must restart the preprocessor by pressing the green run button so the new values will be written to the preprocessor hardware.

DP has only one link and thus there are no controls to specify filters for link A or B.

Pixel recognition



The Pixel recognition function allows the user to trigger on:

- any pixel value or pixel component value
- a pixel value at a specific location
- a specific pixel value at a specific pixel location

The function uses four levels of triggering:
Note: For the following trigger to work, filters must be set so Blanking Dummy data symbols during the active video segment are filtered out

Level 1 - locate the start of the active video frame (BE)
Level 2 - Set up a counter to count N number of states
Level 3 - if Pixel Recognizer is true then trigger
Level 4 - if no trigger then go to Level 1

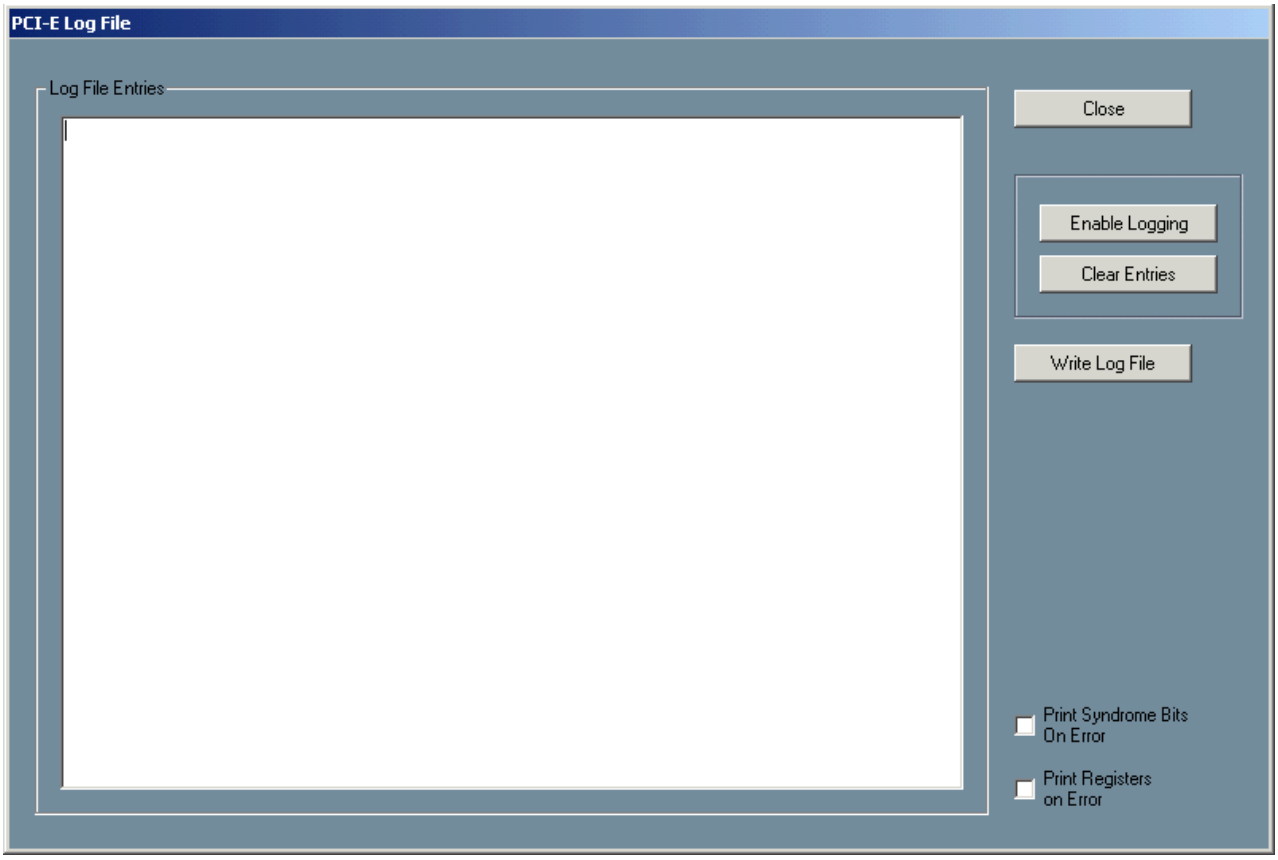
N is an equation that is based on the number of lanes and the index number of the pixel. We will have to document how to calculate N or add this to the Pixel Recognizer screen of the Probe Manager SW. The variables will be:

- Number of lanes
- Format of the pixel
- Pixel value or location

These variables are used to count down the number of states once the start of the frame has been located. If any pixel (completed) in that state matches the recognizer, the condition has been met. By using the trigger statement of the logic analyzer we only call the recognizer into play once we reach the state in question.

Log File

The status of the probe, and the link under test, can be seen in this tab page.



Log File

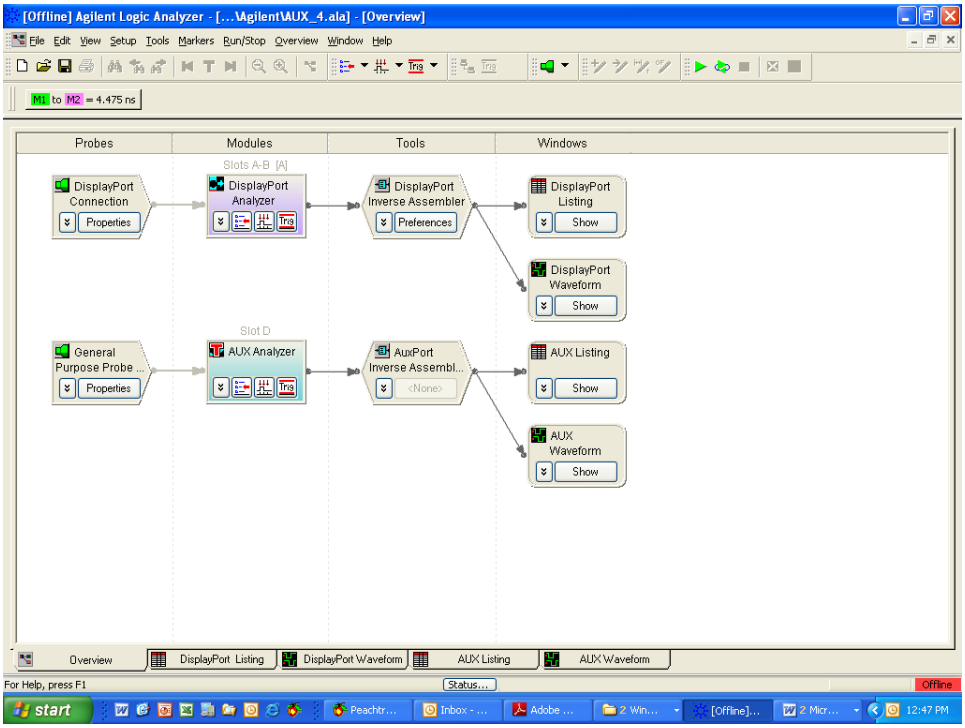
Once started, logging continues even if the preprocessor is stopped and started, or if the log window is closed and re-opened. The log file will not repeat an error that repeats itself constantly.

Once a preprocessor has been stopped, the log entries can be written to a file of the user's choice by clicking the Write Log File button.

State Analysis

This chapter explains how to use the FS4430 to perform state analysis. The configuration file sets up the format specification menu of the logic analyzer for compatibility with the output of the FS4430.

In order to get both the DP and AUX analyzers into the same Logic analyzer workspace as represented in the Overview screen below, first load the appropriate DP configuration file (40 or 90 pin) depending on your analyzer card. Then manually select the appropriate AUX configuration file using the “load” command for the additional card that will show in the workspace.



DP Groups

Besides de-serializing the data stream for the logic analyzer, the FS4430 generates a number of identification and control bits that are used by the Inverse Assembler and logic analyzer. These are also available to the user and are described below. These are the same for any DP link. AUX port is defined separately.

Field	Bits	Definition	Pod	Bits
Storage Flag	1	1= Store this state 0 = Discard	A4 (B4)	16
Data Error	1	1= This state includes an error		15
TRAIN	1	A Training or IDLE sequence has been detected		14
Packet Recognizer	3	1= Packet recognized (pulsed for one clock cycle during packet)		13:11
Event Code	8	Describes what type of packet, signal event or error event. Code is held for duration of packet (Transfer unit?) except that signal and error events can over-write any state except the start state. When start and end coincide, the event code for the starting packet is displayed.		10:3
Sideband signals	3	Spares when in DisplayPort mode.		2:0
Spare	2	Spare	A3 (B3)	16:15
Data Present [3,2,1,0]	4	1= Corresponding lane data byte is present. 0= Data not valid. This might be used to indicate that this lane has been dropped.		14:11
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect Logically named, reflects lane reverse status(?)		10:7
Lane 0 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		6
Lane 0 Control Flag	1	1=K character (control) 0= D character (data)		5
Lane 0 8b Data	8	Decoded 8b value		4:0
			A2 (B2)	16:14
Lane 1 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		13
Lane 1 Control Flag	1	1=K character (control) 0= D character (data)		12
Lane 1 8b Data	8	Decoded 8b value		11:4
Lane 2 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		3
Lane 2 Control Flag	1	1=K character (control) 0= D character (data)		2
Lane 2 8b Data	8	Decoded 8b value		1:0
			A1 (B1)	15:10
Lane 3 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		9
Lane 3 Control Flag	1	1=K character (control) 0= D character (data)		8
Lane 3 8b Data	8	Decoded 8b value		7:0

Clock is on A1 bit 16 and B1 bit 16.

Event Code symbol definitions

Event Code Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							Err bits	Err bits
	Video	Field						
F0 Pixel	1	0	0	0	1	x	0	0
F0 Filler (including FS/FE)	1	0	0	1	0	x	0	Mismatch
BS	1	x	0	1	1	x	0	Mismatch
SR	1	x	1	0	0	x	0	Mismatch
Content Protection BS	1	x	1	0	1	x	0	Mismatch
Content Protection SR	1	x	1	1	0	x	0	Mismatch
F1 Pixel	1	1	0	0	1	x	0	0
F1 Filler (including FS/FE)	1	1	0	1	0	x	0	Mismatch
	Blanking	Horizontal						
Horizontal Blanking BE	0	0	0	0	0	1	Missed SR	Mismatch
Horizontal Blanking VBID	0	0	0	0	1	0	0	Mismatch
Horizontal Blanking MVID	0	0	0	0	1	1	V_err	Mismatch
Horizontal Blanking MAUD	0	0	0	1	0	0	A_err	Mismatch
SR	0	x	0	1	0	1	0	Mismatch
Horizontal Blanking Dummy	0	0	0	1	1	0	0	0
Horizontal Blanking Audio Stream	0	0	1	0	0	0	0	0
Horizontal Blanking Audio TS	0	0	1	0	0	1	0	0
Horizontal Blanking Reserved	0	0	1	0	1	0	0	0
Horizontal Blanking Extension	0	0	1	0	1	1	0	0
Horizontal Blanking Info Frame	0	0	1	1	0	0	0	0
	Blanking	Vertical						
Vertical Blanking BE	0	1	0	0	0	1	Missed SR	Mismatch
Vertical Blanking VBID	0	1	0	0	1	0	0	Mismatch
Vertical Blanking MVID	0	1	0	0	1	1	V_err	Mismatch
Vertical Blanking MAUD	0	1	0	1	0	0	A_err	Mismatch
SR	0	x	0	1	0	1	0	Mismatch
Vertical Blanking Dummy	0	1	0	1	1	0	0	0
Vertical Blanking MSA	0	1	0	1	1	1	0	0
Vertical Blanking Audio Stream	0	1	1	0	0	0	0	0
Vertical Blanking Audio TS	0	1	1	0	0	1	0	0
Vertical Blanking Reserved	0	1	1	0	1	0	0	0
Vertical Blanking Extension	0	1	1	0	1	1	0	0
Vertical Blanking Info Frame	0	1	1	1	0	0	0	0

Event Code Errors:

These signals are asserted for 1 state and are defined as the following:

Mismatch - The mismatch bit is set when there when the KChar or configuration fields of the active lanes don't match. Checks are made on all KChars and the VBID, MVID and MAUD fields.

V_err (MVID Check) - The V_err bit is set when the no_video bit is set in the VBID and the MVID field is not 0.

A_err (MAUD Check) - The A_err bit is set when the audio_mute bit is set in the VBID and the MVAUD field is not 0.

Missed SR - There is a BE counter on each of the four lanes. If 512 BEs are received without receiving an SR on any lane the Missed SR error is asserted.

AUX Group

Aux Port is a half-duplex, bi-directional channel between DisplayPort transmitter (source) and DisplayPort receiver (sink). It consists of 1 differential pair transporting self-clocked data. The AUX CH supports a bandwidth of **1Mbps.** The DisplayPort Source Device is the master (also referred to as AUX CH requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as the replier) is the device that responds to the transaction.

Aux channel has its own clock (67KHz) so that it can be clocked into separate modules in the LA on a separate clock domain. It also has its own Inverse Assembler that has to be loaded separately.

<table>
<tr><th>Field</th><th>Bits</th><th>Definition</th><th>Probe</th><th>Channel</th></tr>
<tr><td>Command</td><td>4</td><td>Command Field</td><td>B1</td><td>3:0</td></tr>
<tr><td>ADDR[11:0]</td><td>12</td><td>Address Field</td><td>B1</td><td>15:4</td></tr>
<tr><td>ADDR[19:12]</td><td>8</td><td>Address Field</td><td>B2</td><td>7:0</td></tr>
<tr><td>Aux CLK</td><td>1</td><td></td><td>B1</td><td>16</td></tr>
<tr><td>DATA[7:0]</td><td>8</td><td>Data field</td><td>B2</td><td>15:8</td></tr>
<tr><td>SYNC</td><td>1</td><td>Sync Bit
First part of the transfer, CMD, ADDR and DATA are all updated, if SYNC is 0 then only DATA is updated.</td><td>B3</td><td>0</td></tr>
<tr><td>STOP
Spare
Spare
Request</td><td>1
1
1
1</td><td>Stop, last byte of the transfer.

High when transaction is request</td><td>B3
B3
B3
B3</td><td>1
2
3
4</td></tr>
<tr><td>Response</td><td>1</td><td>High when transaction is response</td><td>B3</td><td>5</td></tr>
<tr><td>Timeout</td><td>1</td><td>Response Timer timeout period 300us</td><td>B3</td><td>6</td></tr>
<tr><td>HPD event</td><td>2</td><td><table><tr><th>Bit 1</th><th>Bit0</th><th>Meaning</th></tr><tr><td>0</td><td>0</td><td>Unplugged HPD=Low (level)</td></tr><tr><td>0</td><td>1</td><td>HPD pulsed low .25ms to 1.50ms Interrupt event (event signaled on rising edge of HPD)</td></tr><tr><td>1</td><td>1</td><td>Plugged In HPD=High (level)</td></tr></table></td><td>B3</td><td>8:7</td></tr>
<tr><td>HPD Valid</td><td>1</td><td>Indicates a valid HPD event</td><td>B3</td><td>9</td></tr>
<tr><td>Storage</td><td>1</td><td>Indicates Valid states</td><td>B3</td><td>15</td></tr>
<tr><td>Byte Count</td><td>5</td><td>Number of valid bytes received inclusive of current state</td><td>B4</td><td>10:6</td></tr>
</table>

The Storage bit should be used as a qualifier for storing AUX data.

The rate at which Storage is pulsed depends on the packet type. AUX transfers begin with a four bit CMD, a 20 bit address and 8 bits of data. Some packet types contain additional data which will be presented 8 bits at a time. For the additional bytes the Storage bit will be pulsed as each byte is ready, the Command and ADDR Fields will be unchanged.

10 b decode Groups

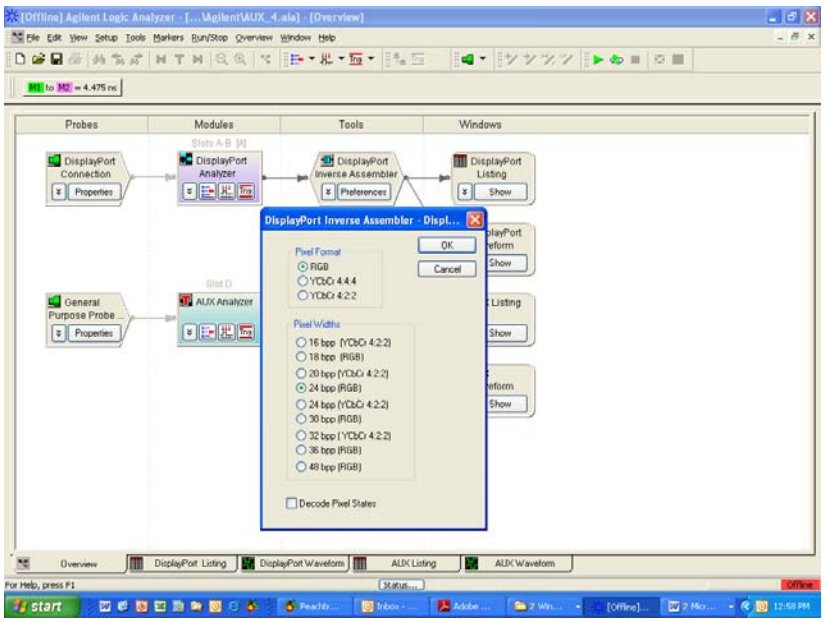
A 10b decode mode is provided in the FS4430. This mode has to be loaded using the Probe Manger at start-up. It requires different connections to the Agilent modules and provides the following labels for the user.

Pre-defined Label	Bits	Definition/Usage	Logic Analyzer Probes
Align Flag	1	1= Alignment of multi-lane link detected	A4[4]
Any Invalid Error Flag	1	1= This state includes an 8b10b code error (either disparity error or decode error in any active lane)	A4[3]
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect on lane (x2 x4 mode only)	A4[2:0] A3[16]
Any LOS	1	1= Loss of Signal detected in any active lane 0= Signal detected in all active lanes	A3[15]
Lane 0 Disparity Error	1	1= Lane 0 data has incorrect 8b10b disparity	A3[14]
Lane 0 Invalid Decode Error	1	1= Lane 0 data is not a valid 8b10b code	A3[13]
Lane0	10	Physical Lane 0 Data, 10-bit encoded	A3[12:3]
Lane 1 Disparity Error	1	1= Lane 1 data has incorrect 8b10b disparity	A3[2]
Lane 1 Invalid Decode Error	1	1= Lane 1 data is not a valid 8b10b code	A3[1]
Lane1	10	Physical Lane 1 Data, 10-bit encoded	A3[0] A2[16:8]
Lane 2 Disparity Error	1	1= Lane 2 data has incorrect 8b10b disparity	A2[7]
Lane 2 Invalid Decode Error	1	1= Lane 2 data is not a valid 8b10b code	A2[6]
Lane2	10	Physical Lane 2 Data, 10-bit encoded	A2[5:0] A1[15:12]
Lane 3 Disparity Error	1	1= Lane 3 data has incorrect 8b10b disparity	A1[11]
Lane 3 Invalid Decode Error	1	1= Lane 3 data is not a valid 8b10b code	A1[10]
Lane3	10	Physical Lane 3 Data, 10-bit encoded	A1[9:0]

Clock is inputted to CK3

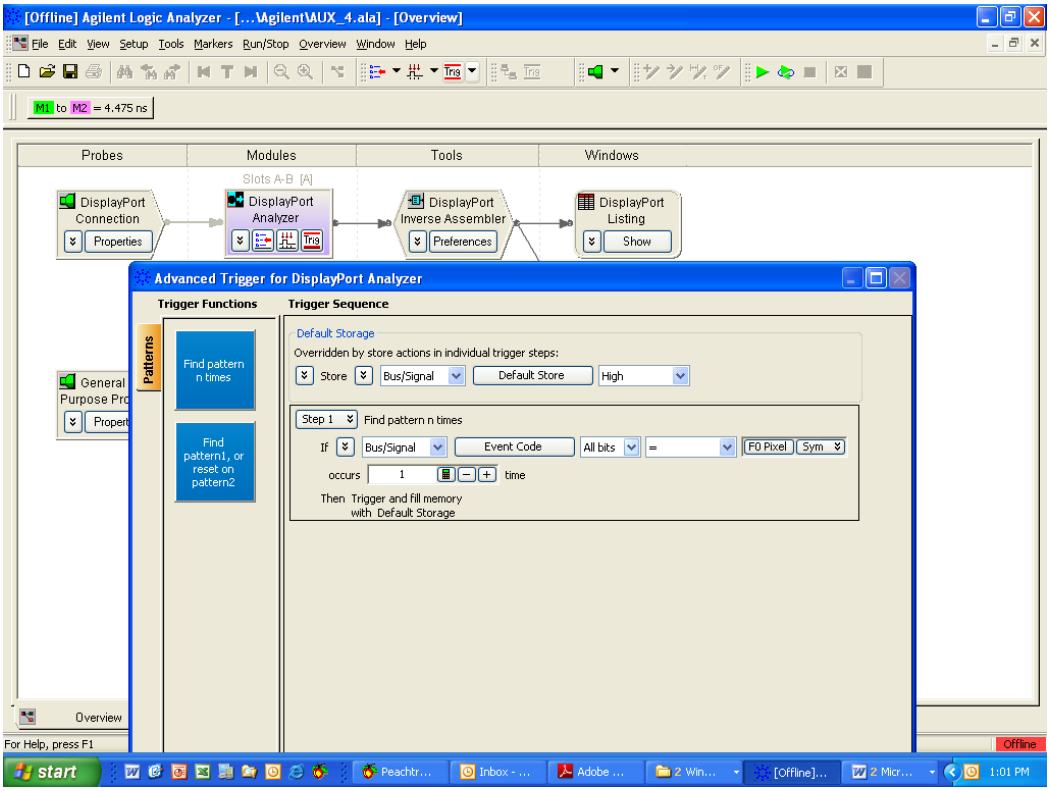
Preferences

The FS4430 Inverse Assembler has Preference settings that are required to insure that it decodes the pixel format properly. These are based on color format and bit width as shown below. They are found on the “Preferences” of the DisplayPort IA as shown.



Triggering

The configuration files provide some logic analyzer based trigger set-ups that utilize the pre defined symbols described earlier. There are Triggers for both the DisplayPort analyzer and the AUX channel analyzer.



- Remember to always use conditional storage for either DisplayPort or AUX. This is because the probe's clock is free running and the Storage bit is used to qualify what is sent to the logic analyzer modules.
- The Event Code field makes it easy to trigger on particular packet types.

To capture specific traffic use the channel signals that can assist in identifying the activity that you want to capture. For example, to capture training use the signal TRAIN, which goes high during training activity. Turning off descrambling when looking at training will properly display the K characters.

Acquiring Data

First, insure that the FS4430 is attached to its external power supply and powered on, which would be indicated by a green Power On LED. Open up the Probe Manager software and insure the appropriate selections are made and applied, finally make sure that the preprocessor is connected via the appropriate cable(s) to the target system.

Once connected, with the link active, open up the Probe Config window and select cable type, lane width, and reference clock options. Verify that lane activity indicators show activity at the correct lanes. Run the preprocessor and observe the LEDs.

If a link's Signal LED is green but its Data LED is orange then there may be a need to select different options for lane width, lane reverse or lane inversion in the Probe Config window.

The FS4430 should show a green Signal LED of any Link being probed, as well as a green or dark data LED.

Configure the analyzer trigger menu to acquire data. Select RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE or when you select STOP.

Link status is communicated by a pair of LEDs as follows:

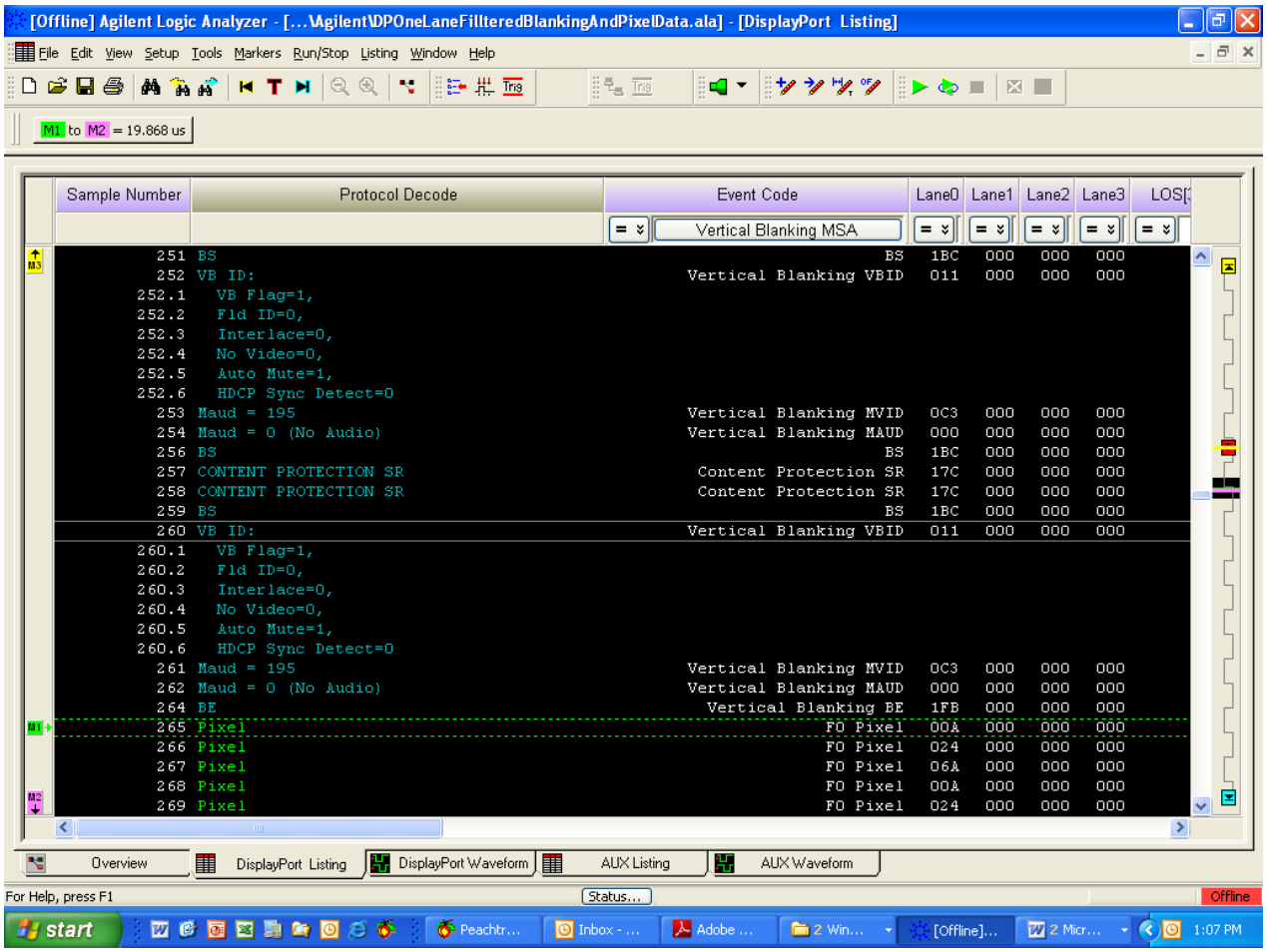
Signal LED State	**Meaning**
Dark	LOS (no signal on an active lane)
Red	RX Fault: Lost Lock on Ref Clock, Lost Synch on Data, FIFO over run or under run. See Log for more information.
Orange	Invalid Symbol or Disparity Error
Green	OK

Data LED State	**Meaning**
Red	FPGA Lost lock on clock(s). Preprocessor needs to stop and run again.
Orange	Any Error: Invalid Symbol or Disparity Error, Align, Framing, Idle.
Green	OK, Data clocking into analyzer.
Dark	No Data (due to filtering or not running)

All transient events, such as a single bit error or a packet clocked into the analyzer, are stretched to short visible pulses on the LEDs.

The Inverse Assembler

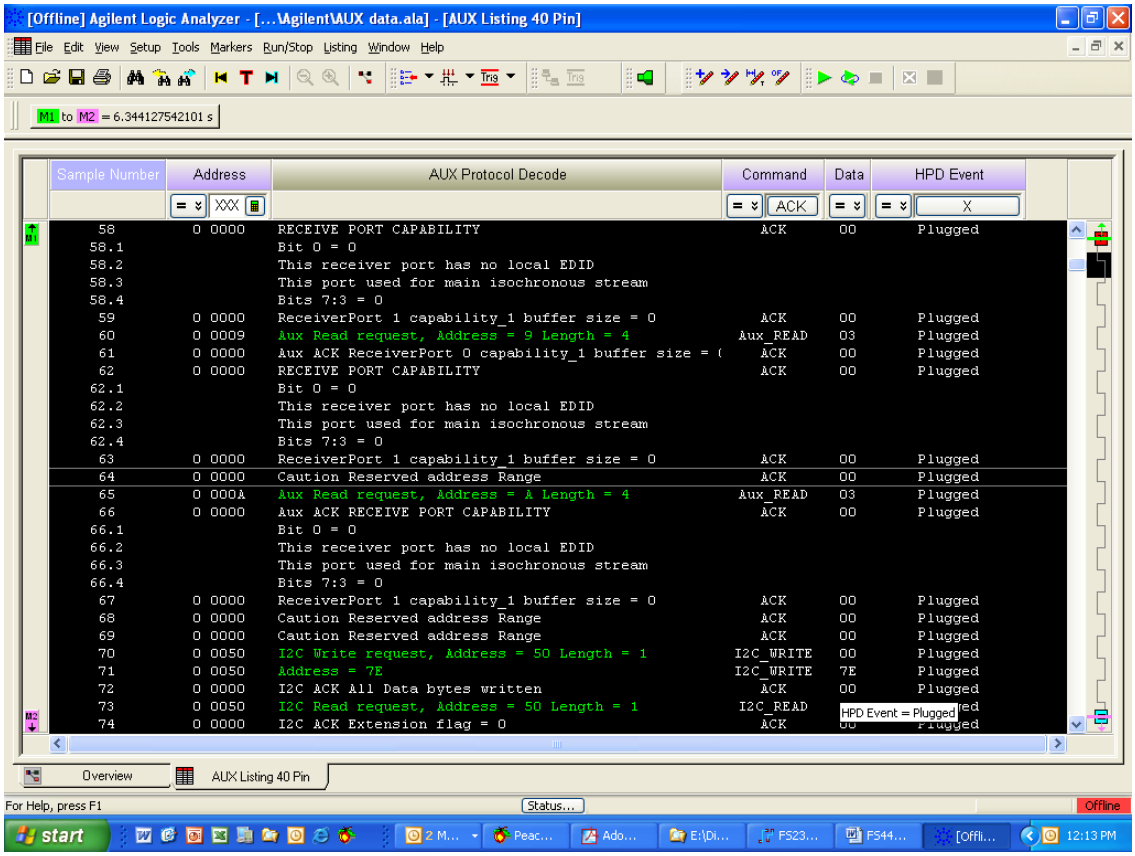
Captured DP data is as shown in the following figure which displays the decoded protocol using the Inverse Assembler.



The FS4430 Inverse Assemblers will perform the following functions:

- Decode all DP or AUX protocol data
- Color code the transaction type. The colors used by the software are as follows:
  - Main Stream Attributes: Blue
  - Secondary Data Packets: Orange
  - All other states: Green

Note: Setting “Decode Pixel States” in the Protocol Decoder Preferences will result in longer processing time for the State Listing.


[Offline] Agilent Logic Analyzer - [...\Agilent\AUX data.ala] - [AUX Listing 40 Pin]
File Edit View Setup Tools Markers Run/Stop Listing Window Help
M1 to M2 = 6.344127542101 s
Sample Number | Address | AUX Protocol Decode | Command | Data | HPD Event
= XXX | ACK | X
58 0 0000 RECEIVE PORT CAPABILITY ACK 00 Plugged
58.1 Bit 0 = 0
58.2 This receiver port has no local EDID
58.3 This port used for main isochronous stream
58.4 Bits 7:3 = 0
59 0 0000 ReceiverPort 1 capability_1 buffer size = 0 ACK 00 Plugged
60 0 0009 Aux Read request, Address = 9 Length = 4 Aux_READ 03 Plugged
61 0 0000 Aux ACK ReceiverPort 0 capability_1 buffer size = (ACK 00 Plugged
62 0 0000 RECEIVE PORT CAPABILITY ACK 00 Plugged
62.1 Bit 0 = 0
62.2 This receiver port has no local EDID
62.3 This port used for main isochronous stream
62.4 Bits 7:3 = 0
63 0 0000 ReceiverPort 1 capability_1 buffer size = 0 ACK 00 Plugged
64 0 0000 Caution Reserved address Range ACK 00 Plugged
65 0 000A Aux Read request, Address = A Length = 4 Aux_READ 03 Plugged
66 0 0000 Aux ACK RECEIVE PORT CAPABILITY ACK 00 Plugged
66.1 Bit 0 = 0
66.2 This receiver port has no local EDID
66.3 This port used for main isochronous stream
66.4 Bits 7:3 = 0
67 0 0000 ReceiverPort 1 capability_1 buffer size = 0 ACK 00 Plugged
68 0 0000 Caution Reserved address Range ACK 00 Plugged
69 0 0000 Caution Reserved address Range ACK 00 Plugged
70 0 0050 I2C Write request, Address = 50 Length = 1 I2C_WRITE 00 Plugged
71 0 0050 Address = 7E I2C_WRITE 7E Plugged
72 0 0000 I2C ACK All Data bytes written ACK 00 Plugged
73 0 0050 I2C Read request, Address = 50 Length = 1 I2C_READ
74 0 0000 I2C ACK Extension flag = 0 ACK
HPD Event = Plugged
Overview
AUX Listing 40 Pin
For Help, press F1
Status...
Offline
start
12:13 PM

General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS4430 probe.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4430 probe.

> If the product is used in a manner not specified by manufacturer, then the protection provided by the equipment may become impaired.

Standards Supported

DisplayPort version 1.1a

Power Requirements

100-240VAC, 2 amps.

Logic Analyzer Required

Agilent 1690x frame and 2 of either 40 or 90 pins modules.

Environmental Temperature

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Operating: 20 to 30 degrees C (68 – 86 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 80% relative humidity. Avoid sudden, extreme temperature changes which would cause condensation on the FS4430 module.

Testing and Troubleshooting Servicing

There are no automatic performance tests or adjustments for the FS4430 module. If a failure is suspected in the FS4430 module contact the factory or your FuturePlus Systems authorized distributor.

The repair strategy for the FS4430 is module replacement. However, if parts of the FS4430 module are damaged or lost contact the factory for a list of replacement parts.