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15LD-1079-03E

LAPIS Semiconductor Errata

ML620Q500 Series

Issue date: Oct. 16th 2015

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1. Introduction

A part of functions on ML620Q500 Series (ML620Q503/504) has a bug. And User's manual has defective descriptions.This document describes the details and the workaround.
Target User's manual : FEUL620Q504-01

1.1 Issue List

No.	Issue Date	Update	Subject
1	2015.04.21	2015.10.16	Interrupt Controller: Interrupt Request Level Control function
2	2015.06.09	-	UART with FIFO: Note in case of stopping clock
3	2015.06.09	-	Port3 :Setting of Port 3 Controll Register
4	2015.10.16	-	High-speed External Clock: Frequency range
5	2015.10.16	-	Power-down/on Procedures
6	2015.10.16	-	Memory mapping of ML620Q503

2. Detail Description

2.1 Interrupt Controller: Interrupt Request Level Control function

A part of interrupt controller has a bug. This document describes the bug details and the workaround. For more details about the function of interrupt controller, see the ML620Q503/504 User's Manual.

2.1.1 Bug (1)

There are conditions that Current Interrupt Request Level Register (CILL) can not be cleared and the CPU does not accept pending interrupts which level is same as (or lower than) the level remained in the CILL.
Conditions :

- When using the "Interrupt Level Control Function" (When the Interrupt Level Control Enable Register ILENL is set to "1").
- When the CPU executes ROM referece instructions & different level interrupts are generated at the same time in oder of "lower level → higher level", or when the CPU executes instructions that clear the CILL at the same time as that WDTINT(Watch dog timer interrupt) is accepted.

2.1.2 Bug (2)

There are condtions that the interrupt level the CPU handles does not equal to the interrupt level the CILL holds. Also, higher level interrupt process have a wait when enabling multiple interrupts or competing with NMI(Non Maskable Interrupt).
Conditions :

- When using the "Interrupt Level Control Function" (When the Interrupt Level Control Enable Register ILENL is set to "1").
- When the CPU executes ROM referece instructions & different level interrupts are generated at the same time in oder of "lower level → higher level".

2.1.3. Workaround

No workaround. Can not propose complete workaround for the all user's application software.
Do not use the "Interrupt level control function".
ML620Q503H/504H have fixed this bug. There have been released on Oct. 2015.

2.2 UART with FIFO: Note in case of stopping clock

A note in 14.3.1 and 14.3.4 of ML620Q503/Q504 User's manual is modified.

(Current description)
[Note]
Transmit FIFO is an empty state, but there is the case that all transmit processing doesn't complete.Confirm that transmit shift register (TSR) became empty in UF0TEMT bit of UAF0LSR register before stopping high-speed clock (Transition to modes such as STOP / DEEP-HALT / HALT-H).

(Modified desctiption)
[Note]
Even if the Transmit FIFO is empty, some transition processing might not be completed.
Before stop the high-speed clock (shift to STOP, DEEP-HALT, HALT-H), confirm the transmit shift register (TSR) becomes empty by UF0TEMT of UAF0LSR register first.
And then wait for 1.5bit transmission time regardless of the setting of Parity and Stop bit.

2.3 Port3 : Setting of Port 3 Control Register

Actions of P34 to P37 are different from bit descriptions of Port 3 control register in 20.2.4 of ML620Q503/ Q504 User's manual. These are dependent on setting to Port 3 mode register.
The bit descriptions is modified.

(Current description)

Setting of P3n pin		When output mode is selected (P3nDIR bit = "0")	When input mode is selected (P3nDIR bit = "1")
P3nC1	P3nC0	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

n = 4 to 7.

(Modified desctiption)

Setting of P3n pin		When output mode is selected (P3nDIR bit = "0")		When input mode is selected (P3nDIR bit = "1")
		When 1st function is selected (P3nMD1,P3nMD0="00")	When 2nd/3rd/4th function is selected (P3nMD1,P3nMD0≠"00")	
P3nC1	P3nC0	Description		
0	0	High-impedance output (initial value)	N-channel open drain output	High-impedance input
0	1	P-channel open drain output	CMOS output	Input with a pull-down resistor
1	0	N-channel open drain output	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	CMOS output	High-impedance input

n = 4 to 7.

2.4 High-speed External Clock : Frequency range

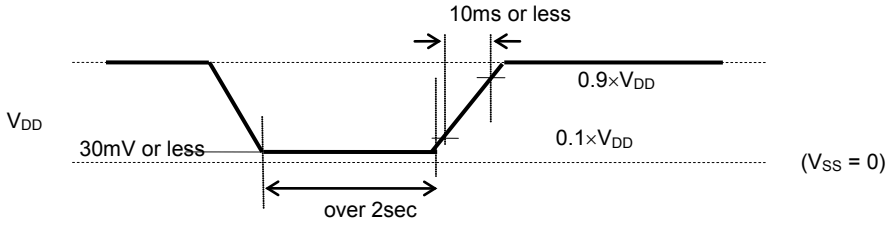
A frequncy range of high-speed external clock input is modified (in section 1.Overview and Appendix C of the User's manual).

(Previous range) : 300kHz to 16MHz
(Modified range) : 2MHz to 16MHz

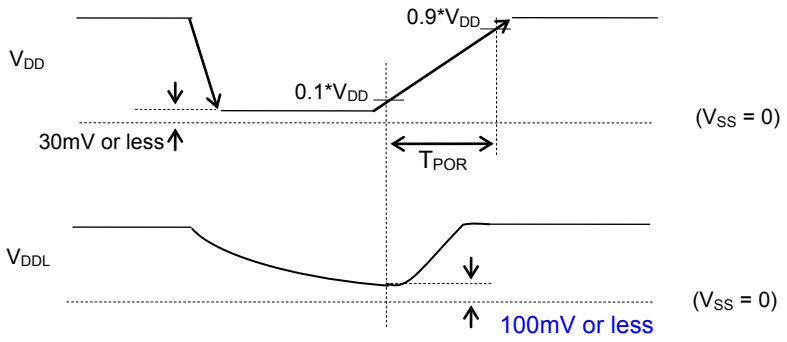
2.5 Power-down/on Procedures

A Power-on procedures and constraints are modified (in Appendix C of the User's manual).

(Previous procedures and consraints)



(Modified procedures and consraints)

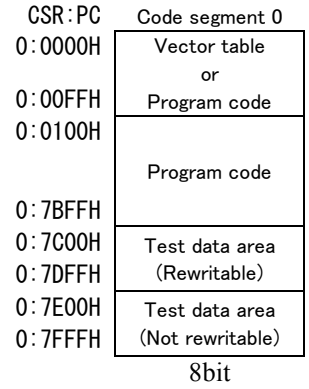


Note:
If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.

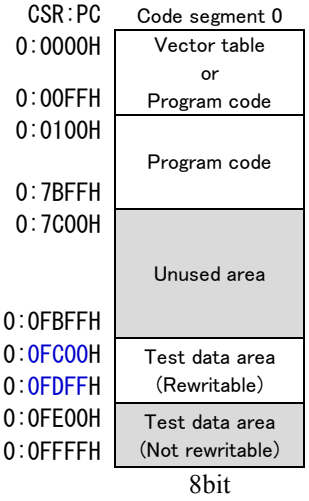
2.6 Memory mapping of ML620Q503

Memory mapping of ML620Q503 is modified (in section 2.CPU and Memory Space of the User's manual).

(Previous mapping) :



(Modified mapping) :



Revision History

Document No.	Issue date	Page		Description
		Before revised	After revised	
15LD-0165-01E	2015.04.21	–	–	First revision
15LD-0165-02E	2015.06.09	–	3	Add Issue No.2,3
15LD-1079-03E	2015.10.16	2	2	Updated description in section 2.1.3.
		–	4,5	Add Issue No. 4,5,6