Freescale Semiconductor
Application Note

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MPC8260 PowerQUICC™II Design Checklist

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Field Applications
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This document provides recommendations for designs based on devices of the PowerQUICC™ II family of integrated communications processors (collectively referred to throughout this document as the MPC8260). The family includes the following devices:

Table 1. PowerQUICC II Family

Process Technology	Devices	
0.29µm (HiP3)	• MPC8260	• MPC8255
0.25µm (HiP4)	• MPC8260A • MPC8250A • MPC8255A	• MPC8264A • MPC8265A • MPC8266A

Refer to Section 10, "References," to review the available information on the functionality, characteristics, and silicon revisions for each device.

This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

Contents

1 Getting Started

This section describes how to simplify the first phase of design. Before designing a system with a PowerQUICC II device, become familiar with the available documentation, silicon revisions, software, microcodes, models, and tools available at the web site listed on the back cover of this document. Refer to Section 10, "References."

1.1 CPM Performance and Bus Usage

The PowerQUICC II CPM runs by time-sharing multiple communication protocols. To estimate the CPM load factor for a particular combination of protocols, use the MPC8260 CPM Performance Evaluator tool (the link "MPC8260SW03.zip" appears in the "Software" table on the MPC8260 product page at the Freescale web site). This tool also estimates the 60x and local bus loads for the combination of protocols selected, bus frequencies, memory speeds, and placement of data structures. At startup, the tool initializes all parameters with default values that are not the recommended values. These values must be changed for each application.

1.2 Pin Assignments

The on-chip serial communications peripherals use four 32-bit parallel ports to exchange data with the physical interfaces. On each pin of the parallel ports several signals are multiplexed. If none of the signals on a given pin are necessary for an application, the pin can be used as an I/O port.

To verify the availability of the I/O functions chosen through pin multiplexing, use the MPC8260 Parallel Ports Configuration tool (the link "MPC8260SW02.zip" appears in the "Software" table on the MPC8260 product page at the Freescale web site). After you select the signals required by an application, this utility assists in defining the pin configuration of each parallel port. A report can then be generated that includes all selections and C-initialization code for the registers associated with the parallel ports.

1.3 Reset Configuration Word

After deciding on the pin multiplexing, review the hard reset configuration word for multiplexing selection and system design decisions (single MPC8260 bus mode versus 60x–compatible bus mode, boot port size, and so on.). The hardware reset configuration word is described in Table 2.

Table 2. Hard Reset Configuration Word

Bits	Name	Description	Comments
0	EARB	Bus arbitration	0 Internal 1 External
1	EXMC	Memory controller	0 Internal 1 External
2	CDIS	Core	0 Enabled 1 Disabled
3	EBM	External bus mode	0 Single MPC8260 bus mode 1 60x-compatible bus mode

Table 2. Hard Reset Configuration Word (continued)

Bits	Name	Description	Comments
4–5	BPS	Boot port size	00 64-bit 01 8-bit 10 16-bit 11 32-bit
6	CIP	Core initial prefix	0 0xFFFn_nnnn 1 0x000n_nnnn
7	ISPS	Internal space port size	0 64-bit 1 32-bit
8–9	L2CPC	L2 cache configuration	00 CI, WT, L2_HIT, CPU_BG active 01 IRQ2, IRQ3, IRQ4, IRQ5 active 10 BADDR(29), BADDR(30), BADDR(31) active
10–11	DPPC	Data parity pin configuration	00 IRQ1-7 active 01 DP(0-7) active 10 RSRV, IRQ1, TLBISYNC, CKSTP_OUT, CORE_SRESET, TBEN, CSE(0), CSE(1) active 11 Additional arbitration lines and IRQ6,7 active
12	—	Reserved	—
13–15	ISB	Initial address of internal RAM IMMR[0-14]	000 0x0000_0000 001 0x00F0_0000 010 0x0F00_0000 011 0x0FF0_0000 100 0xF000_0000 101 0xF0F0_0000 110 0xFF00_0000 111 0xFFF0_0000
16	BMS	Boot memory space	0 HIMEM: 0xFE00_0000–0xFFFF_FFFF 1 LOMEM: 0x0000_0000–0x01FF_FFFF
17	BBD	Bus busy	0 Enabled. ABB and DBB active. 1 Disabled. IRQ2 and IRQ3 active.
18–19	MMR	Mask masters requests	00 No masking on bus request lines 10 Boot master connected to EXT_BR1 11 All external bus requests masked
20–21	LBPC	Local bus pin configuration	00 Local bus pins function as local bus 10 Local bus pins function as core pins
22–23	APPC	Address parity pin configuration	00 TC(0-2), IRQ7/INT_OUT, CS11 active 01 AP(0-3), APE active 10 BNKSEL(0-2), IRQ7/INT_OUT active 11 IRQ7/INT_OUT active
24–25	CS10PS	CS10 pin configuration	00 CS10 active 01 BCTL1 active 10 DBG_DIS active
26–27	—	Reserved	—
28–31	MODCK_H	MODCK[4:7]	See “Clock Configuration Modes” in the relevant hardware specification document (refer to Section 10, “References”).

1.4 Revisions

For current information on chip differences, new features, errata documents, and other updates, refer to *Migration through PowerQUICC II Revisions (MPC82xx/MPC82xxA)* (AN2291), which is available at the web site listed on the back cover of this document.

2 Power

This section provides design considerations for the MPC8260 power supply. For information on AC and DC electrical specifications and thermal characteristics for the MPC8260, refer to the device-specific hardware specification document available at the web site listed on the back cover of this document.

2.1 Power Supply

The MPC8260 has a core voltage VDD which operates at a lower voltage than the I/O voltage VDDH. It is recommended that the core voltage VDD of the MPC8260 be supplied via a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied across VDD and VSS (GND).

Table 3. Core Supply Voltages (VDD)

Device	Core Supply Voltage	Maximum Core Frequency
MPC82xx (HiP3)	2.4V - 2.7V	200 MHz
MPC82xxA (HiP4)	1.7V - 2.1V 1.9V - 2.1V	233 MHz 300 MHz

The I/O section of the MPC8260 is supplied with 3.3V (+/- 5%) across VDDH and VSS (GND). Typically, this is supplied by a simple linear regulator. This increases the complexity of the system because multiple voltage supplies are required for the design (see Section 2.4, “Suggested Power Supply Design,” for recommendations on multi-supply designs). The tolerance on the core and I/O voltages is ±5%. External signals on the MPC8260 are not 5V tolerant. All input signals need to meet the V_{IN} DC spec (-0.3V–3.6V).

2.2 Power Consumption

The device hardware specification documents provide preliminary estimated power dissipation for various configurations. Suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

To estimate the power consumption for the MPC8260, use the MPC8260 Power Consumption Calculator tool, which is available at the Freescale web site (the link “MPC8260SW04.zip” appears in the “Software” table on the MPC8260 product page). Users are required to enter valid clock frequencies and a valid VDD voltage. Even though the tool recognizes individual invalid parameter values, it does not recognize combinations of invalid parameters. To ensure valid combinations, refer to the relevant hardware specification document (see Section 10, “References”). All fields are required in addition to a device

process selection (HiP3 or HiP4). Maximum power consumption values are calculated for the SIU, CPM, CPU, and I/O signals. Overall typical and maximum power consumption values are also calculated.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- VDD/VCCSYN—Must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
- VDDH—Can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 msec. During normal operation, should not exceed VDD/VCCSYN by more than 2.0 V (HiP3) or 2.5V (HiP4).
- VIN—Must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

NOTE

These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased and excessive current can flow through these diodes.

If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 1 (for HiP3 silicon) can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

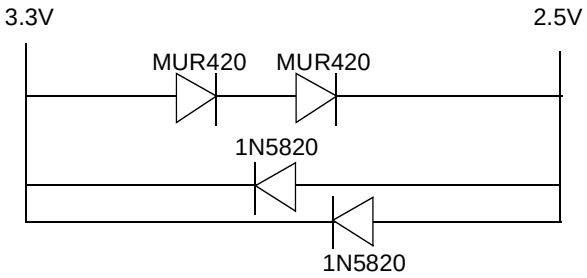


Figure 1. Example Voltage Sequencing Circuit (HiP3 Silicon)

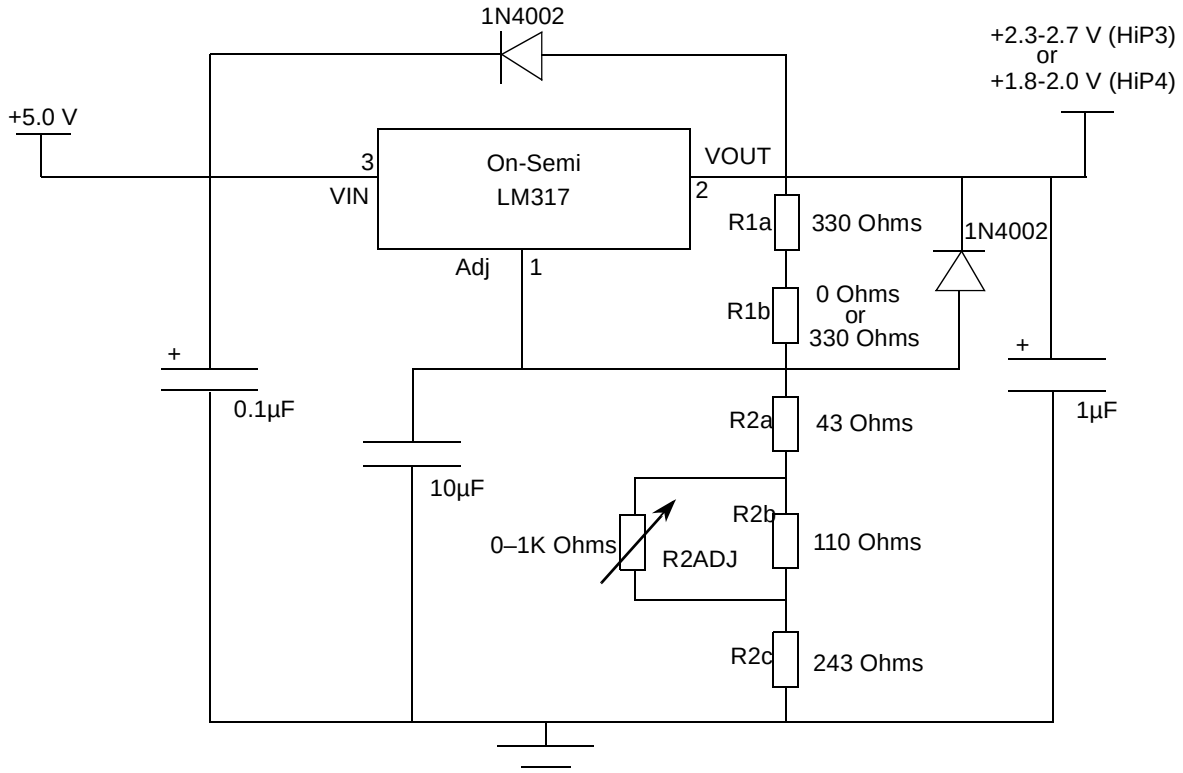
2.4 Suggested Power Supply Design

One common way to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3V supply can be used. However, a separate adjustable supply for the core voltage VDD must be maintained. As shown in Figure 2, an adjustable linear regulator supply can be used. To support future MPC8260 silicon revisions with lower core voltages for lower power, V_{OUT} can be adjusted by modifying the values of R_{2ADJ}.

Consider the following examples:

- HiP3 silicon—R_{1a} = 330Ω, R_{1b} = 0, R_{2a} = 43Ω, R_{2b} = 110Ω, R_{2c} = 243Ω, and R_{2ADJ} = 0–1000Ω generates an output voltage of 2.3-2.7V.

- HiP4 silicon—R_{1a} = 330Ω, R_{1b} = 330Ω, R_{2a} = 43Ω, R_{2b} = 110Ω, R_{2c} = 243Ω, and R_{2ADJ} = 0–1000Ω generates an output voltage of 1.8-2.0V.



Note: $V_{OUT} = V_{REF}(1 + R_1/R_2) + I_{REF}(R_2)$, where V_{REF} = 1.25 V and I_{REF} = 55µA

Figure 2. Core Power Supply Using Adjustable Linear Regulator with Protection Diodes

2.5 Power Planes

Each VCC pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The VCC power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip VCC and ground should be kept to less than half an inch per capacitor lead. A four-layer board that employs two inner layers as VCC and GND planes is recommended.

2.6 Decoupling

Both the I/O voltage (VDDH) and core voltage (VDD) should be decoupled for switching noise. Use standard capacitor values of approximately 0.1 µF and 10 µF. Also, use one high frequency decoupling cap for every two voltage pins. Following this guideline, approximately twenty 0.1 µF and two 10µF capacitors are used on the I/O (VDDH) supply and placed as closely to the MPC8260 as possible. Approximately ten 0.1 µF and one 10µF capacitors are used on the core (VDD) supply and placed as closely to the MPC8260

as possible. Other values and quantities can be substituted for these approximate numbers per designer discretion.

2.7 PLL Power Supply Filtering

The VCCSYN/VCCSYN1 power signals on the MPC8260 provide power to the clock generation phase-locked loops. To ensure stability of the internal clock, the power supplied to these pins should be filtered with capacitors that have low and high frequency filtering characteristics (0.1µF and 10µF). VCCSYN/VCCSYN1 can be connected to VDD through a 10ohm resistor. GNDSYN can be tied directly to the VSS (GND) plane. A circuit similar to the one shown in Figure 3 using surface mount capacitors with minimum effective series inductance (ESL) is recommended.

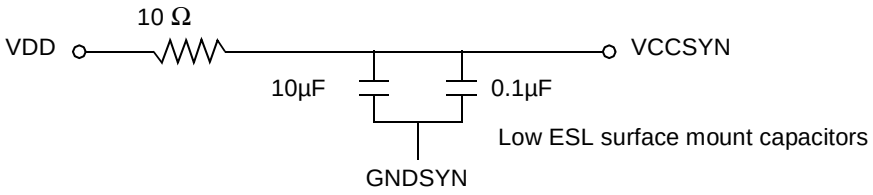


Figure 3. PLL Power Supply Filter Circuit

The PLL also requires a loop filter constructed using a capacitor tied across XFC and VCCSYN. To calculate the XFC Capacitor value in pF, use the appropriate formula in the document entitled *Migration through PowerQUICC II™ Revisions (MPC82xx/MPC82xxA)* (AN2291). The circuit and PLL loop filter should be placed as closely as possible to the pins to minimize noise coupled from nearby circuits.

2.8 Optional PLL Power Planes

A split plane can be created for VCCSYN/VCCSYN1 power supply pins by choosing either a power plane or signal plane and dedicating some area (example: 1 square inch) as a copper plane. On adjacent planes, a signal keepout area can be used to keep this supply clean. The path back from this plane to the power supply should be a low impedance path, and/or the VCCSYN/VCCSYN1 supply can be connected to VDD through a resistor or an inductor.

The GNDSYN can be isolated from the VSS (GND) plane through the use of a split in the VSS (GND) plane. However, this practice is generally not recommended.

3 Clocks

All inputs and outputs except those associated with a serial clock are referenced to the input clock (CLKIN). This clock is provided by a clock buffer such as the MPC940L, a PLL-based zero delay buffer such as a MPC9653, or a clock generator such as a MPC9351. For details on a variety of advanced clock drivers, refer to the timing solutions page at the Freescale web site.

3.1 MODCK[1–3]

The MODCK[1–3] pins are sampled 1024 clocks after the deassertion of $\overline{\text{PORESET}}$ ($\overline{\text{HRESET}}$ is asserted). Their value can be set using either pullups/pulldowns (active driver not needed). Therefore, open

collector drivers are not needed (unlike on the MPC860). This is true even when BNKSEL/TC/AP functions are selected.

3.2 MODCK_H

MODCK_H can be set in the hard reset configuration word (or take the default value). Collectively, the MODCK_H and MODCK fields define the multiplication of the bus clock (CLKIN) to derive the CPU, and the CPM clock rates. Note that the PLL multiplication value is set only during an initial $\overline{\text{HRESET}}$ caused by a $\overline{\text{PORESET}}$, and therefore the PLL does not change during subsequent assertions of $\overline{\text{HRESET}}$. Refer to the relevant hardware specification for the most up-to-date clock configuration mode tables.

4 Reset

The following sections describe the reset recommendations for configuring the MPC8260 device.

4.1 Power-up Reset Circuit

There is no power-up detector on the MPC8260. Use a power-on-reset chip to monitor the power plane and drive $\overline{\text{PORESET}}$.

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector (open-drain) device. When using an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MPC8260 output current, the pull-up value should not be too small.

$\overline{\text{SRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector (open-drain) device. $\overline{\text{SRESET}}$ is driven by the MPC8260 if the $\overline{\text{PORESET}}$ line or the $\overline{\text{HRESET}}$ line is asserted, or if a RESET command is delivered to the debug port.

NOTE

1. $\overline{\text{SRESET}}$ cannot be released until three clocks after $\overline{\text{HRESET}}$ is released.
2. A new reset sequence cannot be started until $\overline{\text{HRESET}}$ is released.
3. $\overline{\text{SRESET}}$ and $\overline{\text{HRESET}}$ must not be tied together.

4.2 Hard Reset Configuration Word Pins

The default hard reset configuration word values (0x0000_0000) can be taken by connecting $\overline{\text{RSTCONF}}$ to a logic “1” during $\overline{\text{HRESET}}$. In this case, no accesses are made to the PROM connected to $\overline{\text{CS0}}$ at location 0x0000_0000. The default case for the device is single-MPC8260 mode.

Both $\overline{\text{BCTL0}}$ and $\overline{\text{BCTL1}}$ are active (functioning as W/$\overline{\text{R}}$ and $\overline{\text{OE}}$) during the hard reset configuration word. Take care to avoid bus contention during this time if buffers on the board are under $\overline{\text{BCTL0/1}}$ control. $\overline{\text{BCTL1}}$ can also be configured as a chip select ($\overline{\text{CS10}}$) and contention during a hard reset configuration word cycle is possible if another device is using it as a chip select and drives the data bus.

Initial values other than the default can be obtained by connecting the $\overline{\text{RSTCONF}}$ pin to logic “0” during $\overline{\text{HRESET}}$. In this case, the hard reset configuration word is read from the PROM connected to $\overline{\text{CS0}}$ at addresses 0x00, 0x08, 0x10, and 0x18. These four bytes are gathered by the MPC8260 core, driven as a word on the 60x data bus, and written to the fields of the hard reset configuration word.

With $\overline{\text{RSTCONF}}$ tied to logic “0”, the MPC8260 also acts as a configuration master to configure up to seven MPC8260 configuration slaves. The $\overline{\text{RSTCONF}}$ lines of up to seven slaves are connected to the most significant 7 address bits of the configuration master address bus. The master continues to read bytes starting at 0x20, configures the next slave while driving the $\overline{\text{RSTCONF}}$ line of the slave, and writes a 32-bit configuration word to that slave while it drives the $\overline{\text{HRESET}}$ asserted to the slave. This is repeated from addresses 0x40, 0x60, 0x80, 0xA0, 0xC0, and 0xE0 for the remaining six slaves.

The configuration master drives the full 32-bit configuration word on the 60x data bus after each of the four byte-reads from the PROM. Avoid any contention on the bus that would affect the configuration word. No pullups are required on the address bus because it is actively driven during this operation.

5 Bit and Byte Lane Ordering

This section describes the 60x bus and local bus bit and byte lane ordering.

5.1 Address/Data Nomenclature

The schematics should use the terminology for the 60x bus and the local bus as defined by the chapter on external signals in the *MPC8260 PowerQUICC II User’s Manual*.

5.2 60x Bus

On the 60x bus, the highest-order address bit is A[0], and the lowest-order address bit is A[31]. All 32 address pins are valid in a byte access. In a 64-bit double word access (that is, cache line fill, castout, SDMA, IDMA), only the upper 29 (A[0–28]) address pins are valid, and A[29–31] are driven low. For the 60x data bus, the highest-order data bit is D[0] and the lowest-order data bit is D[63].

5.3 Local Bus

On the local bus, the highest-order address bit is L_A[14], and the lowest order address bit is L_A[31]. All 18 address pins are valid in a byte access. In a 32-bit word, only L_A[14–29] address pins are valid and L_A[30–31] are driven low. In every access, all 32 bits of address are visible to the internal memory controller. For the local data bus, the highest-order data bit is LCL_D[0], and the lowest-order data bit is LCL_D[31].

5.4 Data Byte Lane Ordering

In PowerPC terminology, D[0–7] is the highest-order byte lane on the data bus, and D[0] is the highest-order bit of that byte lane. D0–D7 correspond to write enable 0 ($\overline{\text{PWE0}}$) and byte lane select (for example, $\overline{\text{PSDDQM0}}$). Table 4 and Table 5 provide the data byte lane ordering for both the 60x bus and the local bus.

Table 4. 60x Bus Data Byte Lane Ordering

Data Bus Signals	Byte Lane	External Pins (Byte Lane Select)
D[0–7]	0	$\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$
D[8–15]	1	$\overline{\text{PWE1}}$/$\overline{\text{PSDDQM1}}$/$\overline{\text{PBS1}}$
D[16–23]	2	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$
D[24–31]	3	$\overline{\text{PWE3}}$/$\overline{\text{PSDDQM3}}$/$\overline{\text{PBS3}}$
D[32–39]	4	$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
D[40–47]	5	$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$
D[48–55]	6	$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
D[56–63]	7	$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$

Table 5. Local Bus Data Byte Lane Ordering

Data Bus Signals	Byte Lane	External Pins (Byte Lane Select)
LCL_D[0–7]	0	$\overline{\text{LWE0}}$/$\overline{\text{LSDDQM0}}$/$\overline{\text{LBS0}}$
LCL_D[8–15]	1	$\overline{\text{LWE1}}$/$\overline{\text{LSDDQM1}}$/$\overline{\text{LBS1}}$
LCL_D[16–23]	2	$\overline{\text{LWE2}}$/$\overline{\text{LSDDQM2}}$/$\overline{\text{LBS2}}$
LCL_D[24–31]	3	$\overline{\text{LWE3}}$/$\overline{\text{LSDDQM3}}$/$\overline{\text{LBS3}}$

5.5 Byte Lanes

The memory controllers can access memories that are 8-, 16-, 32-, and 64-bits wide without creating any holes in the memory space on the 60x bus. This is true for 8-, 16-, and 32-bits wide memories on the local bus as well. In all cases, the memories should be placed in the most significant byte lanes as shown in Table 6.

Table 6. Byte Lanes for Memory Widths

Memory Width	Byte Lanes
Byte (8-bits)	0
Half Word (16-bits)	0, 1
Word (32-bits)	0, 1, 2, 3
Double Word (64-bits)	0, 1, 2, 3, 4, 5, 6, 7 (60x only)

5.6 Boot Memory

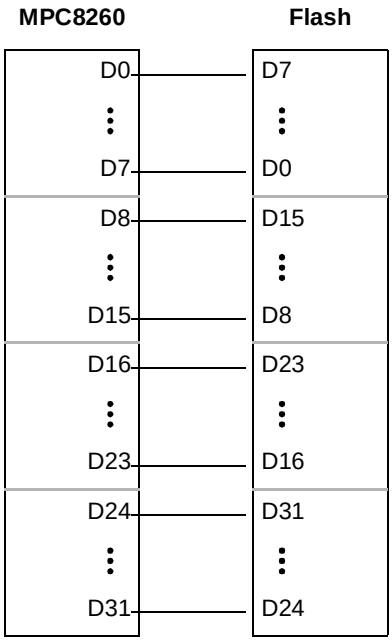
The MPC8260 can boot from memory that is 8-, 16-, 32-, or 64-bits wide. When an internal memory controller is to be used, the memory should be attached to $\overline{\text{CS0}}$, which functions as the global boot select,

and is controlled by a GPCM machine (EPROM or Flash memory). The BPS bit in the hard reset configuration word sets the width of the $\overline{CS0}$ space. After configuration, the 603e core fetches from location 0xFFF0_0100 or 0x0000_0100, depending on the value of the CIP (core initial prefix) bit in the hard reset configuration word. If $\overline{CS0}$ is used for fetching the instruction at this location, the BMS (boot memory space) bit in the hard reset configuration word must have the same value as the CIP bit.

5.7 Using Flash Memory Devices

If 64-bit wide Flash memory is used, there must be floating-point loads/stores for programming. The data lines of most Flash devices are connected to the MPC8260 with byte lanes bit reversed for programming algorithm purposes. A 32-bit example is shown in Figure 4.

Figure 4. MPC8260 to Flash Byte Lane Reversal



Bringing up a board with blank Flash memory requires a switch or other method to force $\overline{RSTCONF}$ to a logic 1 to bring up the MPC8260 in the default state. Otherwise, invalid PLL values can be loaded (for example, MODCK_H = 1111 is invalid). The device cannot boot off the local bus. However, code can execute code off the local bus after the MMU is programmed and the region is marked as cache inhibited.

5.8 UTOPIA Bit Ordering

The numbering of the UTOPIA interface is consistent with the UTOPIA standard.

Table 7. UTOPIA Bit Ordering

UTOPIA Mode	MSB	LSB
16-bit	TxDATA[15]/RxDATA[15]	TxDATA[0]/RxDATA[0]

Table 7. UTOPIA Bit Ordering (continued)

UTOPIA Mode	MSB	LSB
8-bit	TxDATA[7]/RxDATA[7]	TxDATA[0]/RxDATA[0]
16-bit and 8-bit	TxADD/RxADD[4]	TxADD/RxADD[0]

5.9 FCC Nibble Mode Bit Ordering

FCC numbering is consistent with DS3 framers such as TranSwitch TCX-03401. For data moving across the wire, TxD3/RxD3 is transmitted/received first relative to TxD0/RxD0.

6 External Signals

The MPC8260 is not 5V tolerant. All input signals must meet V_{IN} DC Spec (–0.3 to 3.6V).

In 60x bus mode, the bus can be pipelined up to two address cycles deep. For example, it can have a $\overline{\text{TS}}$, an $\overline{\text{AACK}}$, and another $\overline{\text{TS}}$ before the first $\overline{\text{TA}}$. Because the address is valid only during the address phase ending with $\overline{\text{AACK}}$, external latches and multiplexes are necessary for SDRAM, and so on. On accesses to internal slaves such as dual-port RAM, as well as SDRAM page hits, $\overline{\text{TA}}$ can come before $\overline{\text{AACK}}$. In fact, $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ are not guaranteed to be in-order.

In single-MPC8260 bus mode, the bus operation is the same as the 60x bus mode, except the address that is driven on A[0–31] is latched and possibly multiplexed inside the MPC8260. Therefore, the address is valid throughout the data phase of the cycle beginning with $\overline{\text{AACK}}$ and ending with the data phase of the next access. Single-MPC8260 mode does not support mastering of the 60x bus by any other resource, not even an additional MPC8260.

The 60x bus bursts 32 bytes when accessed by the core for I-cache and D-cache line fills and cast outs and for certain CPM SDMA (FCC buffer reads and writes and connection table accesses) and IDMA accesses.

The local bus does not burst when accessed from the 603e core or from an external master through the 60x bus bridge. Accesses to the local bus are not snooped by the 603e core, so regions accessed across the 60x bridge to local bus must be marked as cache inhibited in the 603e core MMU.

Burst accesses by 60x masters to the DPRAM, registers, or local bus are terminated with $\overline{\text{TEA}}$. The local bus bursts 32 bytes for certain CPM SDMA (FCC buffer reads and writes and connection table accesses) and IDMA accesses. Because the local bus is 32 bits wide, it does an eight-beat burst.

The MPC8260 asserts $\overline{\text{AACK}}$ and $\overline{\text{TA}}$ for all accesses to dual-port RAM and CPM registers. It also asserts $\overline{\text{AACK}}$ for all accesses to external memory that match a BR/OR range in the memory controller (and also drives $\overline{\text{TA}}$ unless programmed otherwise).

$\overline{\text{PSDVAL}}$ is driven by the memory controller for an access to an MPC8260-controlled resource (that is, internal space or chip-selects). It is used externally only by external devices that implement the MPC8260 memory bank-based bus sizing protocol (for example, an external MPC8260). Devices that do not implement this protocol (for example, an external MPC7410) do not use $\overline{\text{PSDVAL}}$. Such devices must either provide only 64-bit ports on the 60x bus or must ensure that only MPC8260-initiated transactions can access the 8-, 16-, or 32-bit memory mapped slaves on the 60x bus. Otherwise, any 8-, 16-, or 32-bit memory-mapped slave devices must be located on the MPC8260 local bus.

TBEN defaults to enabled when this function is not selected in the SIUMCR. This results in an interrupt to 0x0000_0900 or 0xFFF0_0900 every five minutes (343.6 seconds at 50 MHz), as the time base register initializes to 0x FFFF_FFFF.

$\overline{\text{PWE}}$[0:7] and $\overline{\text{LWE}}$[0:3] should be used to control the R/$\overline{\text{W}}$ lines of memories, due to timing flexibility. For buffer direction control, $\overline{\text{BCTL0/1}}$ and $\overline{\text{LWR}}$ signals should be used.

7 Memory and Cache

This section discusses design considerations for the MPC8260 associated memories and caches.

7.1 Memory, DRAM, External Master

If an external master device accesses DRAM, the burst address pins, BADDR[27–31], on the MPC8260 should be connected directly to the multiplexer. This is necessary when the external master cannot drive the LSBs of the address bus with appropriate timing in burst accesses.

7.2 BADDR in 60x Mode

In 60x-bus-compatible mode, the BADDR [27–31] pins must be used—not the standard address A[27–31] pins—to address memories when using the GPCM and UPM machines. The BADDR pins are necessary because 60x masters, including the internal 603e core, drive only the starting address on a burst and thus the address lines do not increment. The GPCM memory controller accesses the memory as single accesses. Both the GPCM and the UPM increment the BADDR lines to gather the bytes the 60x master requests.

At the system level, when 16-bit Flash memory and the L2 cache cannot be used together. Because the BADDR pins are multiplexed with the L2 cache control pins, only one set of functionality can be used at a time. One solution is to power up and use BADDR functionality to copy all code from Flash memory to 32-bit SDRAM and then reconfigure the pins for L2 cache operation and run code from SDRAM.

With the SDRAM machine, the BADDR lines must be used for SDRAM regions that are 8- or 16-bits wide. There is no SDRAM burst depth that matches the 32-byte burst the master initiates. Therefore, the SDRAM machine breaks the burst into four 8-beat bursts for the 8-bit case or two 8-beat bursts for the 16-bit case.

In Single MPC8260 mode, the memory controllers drive the address lines for small port sizes and increments for bursts. Therefore, the BADDR pins are not needed in this mode.

UPM differences from the MPC860 include changed polarity of GTA bit and a different array programming algorithm (need to perform dummy read to memory to complete command in MCMR).

7.3 Bank Selects Versus Address Lines

In single-MPC8260 mode, the BNKSEL lines should be used to interface to SDRAM, thus supporting different SDRAM densities without requiring board wiring changes. Also, using the BNKSEL lines and setting the BCR(EAV) bit allows logic analyzers to view the unmultiplexed address of the access. One exception is for external instrumentation that requires the use of the TC lines that are multiplexed with the BNKSEL lines for program trace (not required for standard COP debugging).

7.4 Page Versus Bank Interleaving

Page interleaving is the preferred method for connecting to SDRAM. Bank interleaving generally offers lower performance than page interleaving and is included for compatibility with designs using this mode before page interleaving became available.

7.5 Data Cache Flush

The MPC8260 cannot traverse and flush all the data cache lines without the effective address of each line that is cached (*dcbf* requires an effective address and the cache functions in the HID0 do not include a flush operation). The suggestion is to write an assembly subroutine to accomplish this.

8 COP/JTAG Interface

The MPC8260 implements a common on-chip processor (COP) function, a feature common to all Freescale processors that implement the PowerPC architecture except the MPC8xx family. This feature allows internal access to scan chains for debug purposes and also provides a serial connection to the core for emulator support. Adding a COP connection adds little or no cost to the system but adds significant advantages during early system development. The COP interface is implemented using a standard 16-pin header with the pinout, as shown in Figure 5.

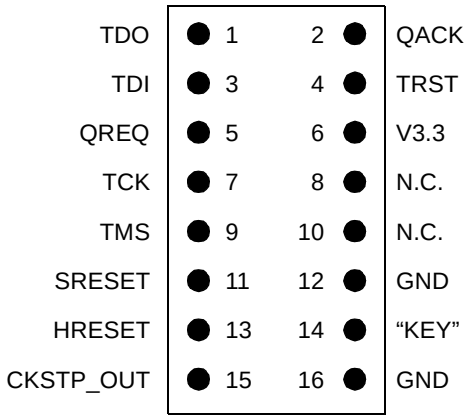


Figure 5. 16-Pin Header for COP/JTAG Interface

The COP interface connects through the JTAG port on the MPC8260 with additional status monitoring signals. Table 8 shows the pin definitions and recommendations.

Table 8. COP/JTAG Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDO	Test Data Out	None
2	QACK	Quiescent Acknowledgement	QACK is not brought out of the G2 core. Leave unconnected or tie directly to GND.
3	TDI	Test Data In	Add 10K pull-up to VDDH = 3.3V.

Table 8. COP/JTAG Interface Pin Definitions (continued)

Pins	Connection	Description	Recommendations
4	$\overline{\text{TRST}}$	Test Reset	Connect to MPC8260 $\overline{\text{TRST}}$ signal. $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ should be tied to VDDH via a 2KΩ external pull-up resistor.
5	QREQ	Quiescent Request	May be optionally connected to MPC8260 $\overline{\text{QREQ}}$ signal. Add 10K pull-up to VDDH = 3.3V in all cases.
6	V3.3	I/O Power Supply	Connect to MPC8260 I/O Voltage VDDH through a 1K current limiting resistor
7	TCK	Test Clock	Add 10K pull-up to VDDH = 3.3V.
8,10	N.C.	No Connect	Leave unconnected.
9	TMS	Test Mode Select	Add 10K pull-up to VDDH = 3.3V.
11	$\overline{\text{SRESET}}$	Soft Reset	Connect to the $\overline{\text{SRESET}}$ and $\overline{\text{HRESET}}$ signals on the MPC8260 using open circuit gates. Refer to Section 8.1, “Merging Reset Signals”
13	$\overline{\text{HRESET}}$	Hard Reset	
14	“KEY”	Mechanical Keying	Pin should be removed.
15	CKSTP_OUT	Check Stop Output	Add 10K pull-up to VDDH = 3.3V.
12, 16	GND	System Ground Plane	Connect to digital ground.

8.1 Merging Reset Signals

The COP interface requires the ability to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently to control the processor. If the target system has multiple independent reset sources, such as voltage monitors, watchdog timers, low voltage detectors, or manual push-button switches that can cause a system reset, the reset signals on the COP header must be merged into these signals with logic. Attempts to wire these reset signals together damage the COP or target system. The arrangement in Figure 6 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently while ensuring that the target system can drive $\overline{\text{HRESET}}$ as well. Both $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ should be tied to VDDH via a 2K external pull-up resistor. If COP is attached, it is responsible for driving $\overline{\text{TRST}}$ when needed.

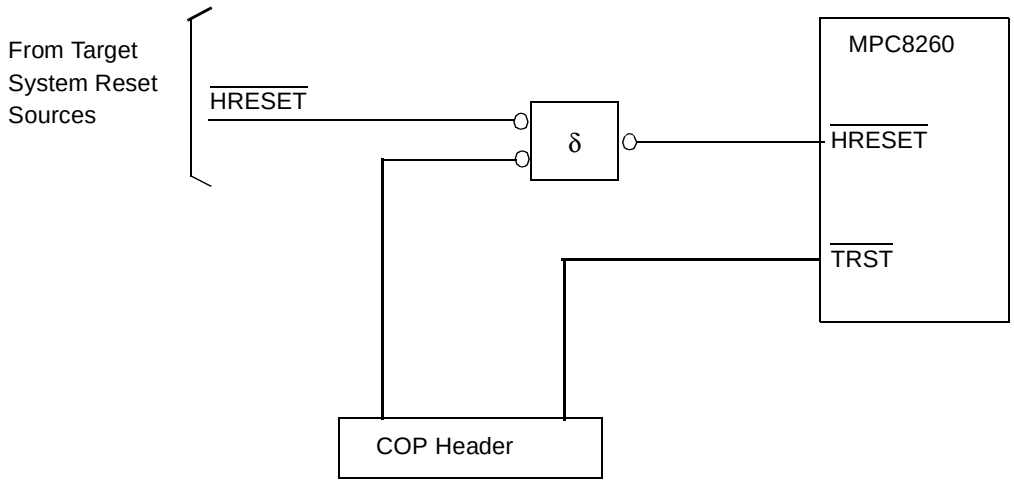


Figure 6. COP Merging Reset Signals

8.2 Nonscan Chain Operation

In nonscan chain operation, the TCK input does not include an internal pull-up resistor, so a 10K pull-up resistor to +3.3V or V_{DDH} should be connected to TCK. To ensure that the scan chain test logic is kept transparent to the system logic, the TAP controller should be forced into a test-logic-reset state. This automatically occurs within the MPC8260 because $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ are connected together internally. A 10K pull-up resistor to 3.3V or VDDH should be connected to TMS and it should not change state. This ensures that the TAP controller does not leave the test-logic-reset state.

9 Signal States and Terminations

This section summarizes the connections and special conditions (such as pullups or pulldowns required) that may be needed for Freescale integrated communications processors. The states of all signals during $\overline{\text{HRESET}}$ along with their recommended terminations are listed in Table 9. If a connection to a specific signal is not named, it may be one of the following terms:

- xx–yyΩ VDDH — A pullup resistor to the VDDH power supply, with a value between xx and yy Ω. The choice of value is selected on the basis of system requirements such as noise immunity and the ability to share pullups.
- xx–yyΩ GND — A pull-down resistor to the ground power connection, with a value between xx and yy Ω. Again, the designer can specify the value.
- “open” — The signal should be left unconnected.
- “as needed” — The system mainly determines the connection. It generally connects to the system controller logic, whether from Freescale or one of several third-parties who make such logic. If not designated, a pullup should be between 1K–10KΩ VDDH and a pull-down between 100-1KΩ GND.

Unused inputs should be tied high or low, but not left floating. Unused inputs can be tied directly to GND, but a pullup is recommended if tied high (generally, any unused inputs are tied to GND or VDDH through a resistor for board testing purposes).

The following signals are active during the reset configuration period of $\overline{\text{HRESET}}$: A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[(0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, and BADDRx. All signals can be three-stated by asserting $\overline{\text{TRIS}}$ or using JTAG commands. Input-only signals (for example, $\overline{\text{PORESET}}$) or signals configured in an input-only mode (for example, $\overline{\text{IRQx}}$, $\overline{\text{EXT\_BRx}}$) do not require pullups/pulldowns if they are actively driven. However, the more conservative pullups are recommended in Table 9. Designers should exercise discretion. The hard reset signal states do not include the states during reset configuration. During the period that $\overline{\text{PORESET}}$ is asserted, configurable signals have their default configuration (and therefore are Hi-Z). During the period of reset configuration, configurable signals still have their default configuration, and certain memory controller signals (A[0–31], $\overline{\text{BCTL0}}$, $\overline{\text{BCTL1}}$, D[0–63], $\overline{\text{CS0}}$, $\overline{\text{POE}}$, BADDRx) operate to perform the reset configuration function.

Table 9. Signal States and Recommended Termination

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
BR	B	Hi-Z, EARB=0 High, EARB=1	1K-10KΩ VDDH		Pullup if EARB=0
BG	B	High, EARB=0 Hi-Z, EARB=1	1K-10KΩ VDDH		Pullup if EARB=1
ABB/IRQ2	B	Hi-Z	1K-10KΩ VDDH		Pullup
TS	B	Hi-Z	1K-10KΩ VDDH		Pullup
A[0-31]	B	Low	as needed	open	No requirement
TT[0-4]	B	Hi-Z	1K-10KΩ VDDH		Pullup
TBST	B	Hi-Z	1K-10KΩ VDDH		Pullup
TSIZ[0-3]	B	Hi-Z	as needed	open	TSIZ bus may be pulled up or down. Pull-down TSIZ0 (100Ω) if external master exists, else no requirement.
AACK	B	Hi-Z	1K-10KΩ VDDH		Pullup
ARTRY	B	Hi-Z	1K-10KΩ VDDH		Pullup
DBG	B	High, EARB=0 Hi-Z, EARB=1	1K-10KΩ VDDH		Pullup
DBB/IRQ3	B	Hi-Z	1K-10KΩ VDDH		Pullup
D[0-63]	B	Hi-Z	as needed	open	No requirement. However, in some design examples, including Scout, 10K pulldowns are used on the 60x and local data buses. This aspect of the implementation is left up to the designer.
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B	High, DPPC=10 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{EXT\_BR2}}$
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	B	High, DPPC=11 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{IRQ1}}$
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/ $\overline{\text{EXT\_DBG2}}$	B	High, DPPC=11 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{IRQ2}}$ or $\overline{\text{TLBISYNC}}$
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/ $\overline{\text{EXT\_BR3}}$	B	High, DPPC=10 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{IRQ3}}$ or $\overline{\text{EXT\_BR3}}$
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/ $\overline{\text{EXT\_BG3}}$	B	High, DPPC=11 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{IRQ4}}$ or $\overline{\text{CORE\_SRESET}}$
$\overline{\text{IRQ5}}$/DP5/TBEN/$\overline{\text{EXT\_DBG3}}$	B	High, DPPC=11 Hi-Z, Otherwise	as needed	open	Pullup if used as $\overline{\text{IRQ5}}$; set as desired if used as TBEN

Table 9. Signal States and Recommended Termination (continued)

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
IRQ6/DP6/CSE0	B	High, DPPC=10 Hi-Z, Otherwise	as needed	open	Pullup if used as IRQ6
IRQ7/DP7/CSE1	B	High, DPPC=10 Hi-Z, Otherwise	as needed	open	Pullup if used as IRQ7
PSDVAL	B	Hi-Z	1K-10KΩ VDDH		Pullup
TA	B	Hi-Z	1K-10KΩ VDDH		Pullup
TEA	OD	Hi-Z	1K-10KΩ VDDH		Pullup
GBL/IRQ1	B	Hi-Z	1K-10KΩ VDDH		Pullup
CI/BADDR29/IRQ2	B	Hi-Z, L2CPC=01 Low, Otherwise	as needed	open	Pullup if used as IRQ2
WT/BADDR30/IRQ3	B	Hi-Z, L2CPC=01 Low, Otherwise	as needed	open	Pullup if used as IRQ3
L2_HIT/IRQ4	I	Hi-Z	1K-10KΩ VDDH		Pullup
CPU_BG/BADDR31/IRQ5	B	Hi-Z, L2CPC=01 Low, Otherwise	as needed	open	Pullup if used as IRQ5
CPU_DBG	O	High	as needed	open	no requirement
CPU_BR	O	Hi-Z, then High	as needed	open	no requirement
CS[0-9]	O	High	as needed	open	no requirement
CS10/BCTL1	B	Hi-Z, CS10PC=10 High, Otherwise	as needed	open	no requirement
CS11/AP0	B	High, APPC=x0 Hi-Z, Otherwise	as needed	open	no requirement
BADDR[27-28]	O	Low	as needed	open	no requirement
ALE	O	High	as needed	open	no requirement
BCTL0	O	Low	as needed	open	no requirement
PWE[0-7]/PSDDQM[0-7]/PBS[0-7]	O	High	as needed	open	no requirement
PSDA10/PGPL0	O	High	as needed	open	no requirement
PSDWE/PGPL1	O	High	as needed	open	no requirement
POE/PSDRAS/PGPL2	O	High	as needed	open	no requirement

Table 9. Signal States and Recommended Termination (continued)

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
PSDCAS/PGPL3	O	High	as needed	open	no requirement
PGTA/PUPMWAIT/PGPL4/PPBS	B	Hi-Z	as needed	open	Pullup if used as PUPMWAIT or PGTA
PSDAMUX/PGPL5	O	Low	as needed	open	no requirement
LWE[0-3]/LSDDQM[0-3]/LBS[0-3]/PCI_CFG[0-3] [2]	O	High	as needed	open	no requirement
LSDA10/LGPL0/PCI_MODCKH0[2]	O	High	as needed	open	no requirement
LSDWE/LGPL1/PCI_MODCKH1[2]	O	High	as needed	open	no requirement
LOE/LSDRAS/LGPL2/PCI_MODCKH2[2]	O	High	as needed	open	no requirement
LSDCAS/LGPL3/PCI_MODCKH3[2]	O	High	as needed	open	no requirement
LGTA/LUPMWAIT/LGPL4/LPBS	B	Hi-Z	as needed	open	Pullup if used as LUPMWAIT or LGTA
LGPL5/LSDAMUX[3]/PCI_MODCK[2]	O	Low	as needed	open	no requirement
LWR	O	High	as needed	open	no requirement
L_A14/PAR[2]	B	Low	as needed	open	no requirement
L_A15/FRAME[2]/SMI	B	Low	as needed	open	no requirement
L_A16/TRDY[2]	B	Low	as needed	open	no requirement
L_A17/IRDY[2]/CKSTP_OUT	B	Low	as needed	open	no requirement
L_A18/STOP[2]	B	Low	as needed	open	no requirement
L_A19/DEVSEL[2]	B	Low	as needed	open	no requirement
L_A20/IDSEL[2]	B	Low	as needed	open	no requirement
L_A21/PERR[2]	B	Low	as needed	open	no requirement
L_A22/SERR[2]	B	Low	as needed	open	no requirement
L_A23/REQ0[2]	B	Low	as needed	open	no requirement
L_A24/REQ1[2]/HSEJSW[2]	B	Low	as needed	open	no requirement
L_A25/GNT0[2]	O	Low	as needed	open	no requirement
L_A26/GNT1[2]/HSLED[2]	O	Low	as needed	open	no requirement
L_A27/GNT2[2]/HSENUM[2]	O	Low	as needed	open	no requirement

Table 9. Signal States and Recommended Termination (continued)

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
L_A28/RST[2]/ CORE_SRESET	B	Low	as needed	open	no requirement
L_A29/INTA[2]	B	Low	as needed	open	no requirement
L_A30/REQ2[2]	O	Low	as needed	open	no requirement
L_A31/DLLOUT[2]	B	Low	as needed	open	no requirement
LCL_D[0-31]/AD[0-31][2]	B	Hi-Z	as needed	open	no requirement
LCL_DP[0-3]/C[0-3][2]/ BE[0-3][2]	B	Hi-Z	as needed	open	no requirement
IRQ0/NMI_OUT	B	Hi-Z, CDIS=0 High, CDIS=1	as needed	open	Pullup if used as IRQ0
IRQ7/INT_OUT/APE	B	High, APPC=01 Otherwise: Hi-Z, CDIS=0 High, CDIS=1	as needed	open	Pullup if used as IRQ7
TRST	I	Internal pullup	Actively drive with HRESET, logically OR'ed with COP TRST, if any. 100-1KΩ GND		TRST is internally connected to PORESET and thus the JTAG TAP controller is guaranteed to be in the test-logic-reset state after each power up. Therefore, it is not necessary to connect TRST to PORESET through a gate or diode to ensure that the JTAG TAP controller is properly reset after each power up, as was the case with the MPC860. See Section 8, "COP/JTAG Interface."
TCK	I	Hi-Z	1K-10KΩ VDDH		Pullup. Refer to Section 8, "COP/JTAG Interface."
TMS	I	Internal pullup	1K-10KΩ VDDH		Pullup. Refer to Section 8, "COP/JTAG Interface."
TDI	I	Internal pullup	1K-10KΩ VDDH		Pullup. Refer to Section 8, "COP/JTAG Interface."
TDO	O	Hi-Z	as needed	open	no requirement
TRIS	I	Hi-Z	1K-10KΩ VDDH		Pull up
PORESET	I	Hi-Z	1K-10KΩ VDDH		Pullup. Refer to Section 8, "COP/JTAG Interface."
HRESET	OD	Low	1K-10KΩ VDDH		
SRESET	OD	Low	1K-10KΩ VDDH		
QREQ	O	Hi-Z, then High	1K-10KΩ VDDH		Pullup. Refer to Section 8, "COP/JTAG Interface."

Table 9. Signal States and Recommended Termination (continued)

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
RSTCONF	I	Hi-Z	As required by reset configuration mode	—	RSTCONF can be tied to ground if the Hard Reset Word is to be read from a boot EPROM, and it is a Configuration Master. If it is a Configuration Slave, the RSTCONF should be connected to one of the Master's seven most significant address bits. Otherwise a 4.7K Ohm pullup resistor to VDDH is recommended to accept the default Hard Reset Word.
MODCK1/AP1/TC0/ BNKSEL0	B	Hi-Z	as needed	—	Pullup or pull-down per desired clock configuration. Refer to the appropriate hardware specification for settings.
MODCK2/AP2/TC1/ BNKSEL1	B	Hi-Z	as needed		Pullup or pull-down per desired clock configuration. Refer to the appropriate hardware specification for settings.
MODCK3/AP3/TC2/BN KSEL2	B	Hi-Z	as needed		Pullup or pull-down per desired clock configuration. Refer to the appropriate hardware specification for settings.
XFC	Analog	Analog voltage	analog voltage		Provide appropriate XFC filter capacitor.
CLKIN1	I	Hi-Z	as needed		Provide appropriate clock
PA[0-31]	B	Hi-Z	as needed	none	The parallel port (Port A, B, C, D) pins on the MPC8260 do not have internal pull-ups or pulldowns. Unused parallel I/O pins can be configured as outputs after reset and left unconnected.
PB[4-31]	B	Hi-Z	as needed	none	"
PC[0-31]	B	Hi-Z	as needed	none	"
PD[4-31]	B	Hi-Z	as needed	none	"
VCCSYN	Analog		filtered VDD		Refer to Section 2.7, "PLL Power Supply Filtering."
VCCSYN1	Analog		filtered VDD		Refer to Section 2.7, "PLL Power Supply Filtering."
GNDSYN	Analog		filtered VDD		Refer to Section 2.7, "PLL Power Supply Filtering."
SPARE1/CLKIN2[2] (Pin AE11)	I	Hi-Z	as needed	none	AE11 should be asserted if the PCI function is desired. If PCI is not desired or on non-PCI devices, AE11 should be pulled down, but it can be left floating.
SPARE4 (pin U5), SPARE6 (pin V4)	Undefined	Undefined	—	none	Tying SPAREs to ground using a resistor is recommended, but they can be left floating.

Table 9. Signal States and Recommended Termination (continued)

Signal	Function [1]	State at Hard Reset	Connection		Notes
			if used	if not used	
SPARE5/$\overline{\text{PCI\_MODE}}$[2] (pin AF25)	I	Hi-Z	as needed	none	AF25 should be asserted if the PCI function is desired. If PCI is not desired or on non-PCI devices, this pin must be pulled up or left floating.
THERMAL[0-1]	Thermal	Thermal	as needed	100-1KΩ GND	These pins should be grounded in regular system operation as they do not have ESD protection. For information on how to use these pins, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide*.

1 I = input, O = output, B = bidirectional three-state, OD = open-drain. Most multi-function pins are bidirectional three-state. This does not imply that they are all shared signals—only that they may be used as inputs or outputs.

2 MPC8250A, MPC8265A, and MPC8266A only.

3 Only on HiP3 Rev C.2 silicon and forward.

10 References

The reference documents listed in Table 10 are available at the web site listed on the back cover of this document. Visit the relevant product summary page or search by title or document ID.

Table 10. References

Document Category	Document Title	Document ID
Data Sheet (Hardware Specifications)	MPC8260 (HiP3) Hardware Specifications	MPC8260EC/D
	MPC826xA (HiP4) Family Hardware Specifications	MPC8260AEC/D
	MPC8250 Hardware Specifications	MPC8250EC/D
	MPC8255 Hardware Specifications	MPC8255EC/D
Errata (device)	MPC826x Family Device Errata Reference	MPC8260CE/D
	MPC8260/XPC8260A Family Device Errata Summary	MPC82660CESUMM/D
	RAM Microcode Patches for MPC8260 Device Errata	MPC8260MC05
	XPC826xA Family Device Errata Reference	XPC8260ACE/D

Table 10. References

Document Category	Document Title	Document ID
Reference Manual (User's Manuals, Manual Errata, Manual Addenda)	MPC8260 User's Manual	MPC8260UM/D
	MPC8260 User's Manual Errata	MPC8260UMAD/D
	MPC8260 HiP4 Supplement to the User's Manual	MPC8260AUMAD/D
	TC Layer Functional Specification: Addendum to the MPC8260 User's Manual	MPC8264AUMAD/D
	PCI Bridge Functional Specification: Addendum to the MPC8260 User's Manual	MPC8265AUMAD/D
	IMA Functional Specification: Addendum to the MPC8260 User's Manual	MPC8266AUMAD/D
	MPC603e RISC Microprocessor User's Manual	MPC603EUMAD/D
Application Notes	Minimal MPC8260 PowerQUICC IITM System Configuration	AN1819/D
	Migration through PowerQUICC II™ Revisions (MPC82xx/MPC82xxA)	AN2291/D
	Design Checklist for Freescale PowerPC ISA Processors	AN2077/D
	Instruction and Data Cache Locking on the G2 Processor Core	AN2129/D
	Excimer MPC603 Minimum System Reference Design	AN1769/D
	MPC8260 PowerQUICC II Thermal Resistor Guide	AN2271/D
Schematics	MPC8260 Example Schematics	MPC8260SCH1
Reference Design	MPC8260-MPC750 Reference Design (The Scout)	MPC8260RD4/SCH2

11 Revision History

Table 11 shows the revision history of this document.

Table 11. Revision History

Revision Number	Changes
0	Initial release
1	• Added technical notes to document. • Nontechnical reformatting
1.1	• Document did not change. This note is to clarify the Technical Notes added for Rev 1. • For Rev. 1, Added 3 Notes below Section 4.1 Power-Up Reset Circuit.
2	Corrected Figure 6 to show that TRST should be tired to VDDH via a 2KΩ external pullup resistor.

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