Acromag®

Series APC341 Simultaneous Sampling Analog Input Board, PCI Bus

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.
Tel: (248) 295-0310
Fax: (248) 624-9234

8500-685-13C010

Table of Contents

IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Series APC341 (14-bit) analog input board is a precision, short size PCI board with simultaneous sampling of analog input signals. Sixteen differential analog input channels are provided with an input range of ±10 volts.

The 16 differential analog voltage input channels are converted as two banks of eight channels. After the first bank of eight channels are simultaneously converted, the second bank of 8 channels can then be simultaneously converted at the time specified in a user programmable delay counter.

All 16-channels share two generous 512-sample memory buffers, from which digitized values are read. Since all channels share the same memory buffer, data tagging is implemented for easy identification of corresponding channel data. To minimize CPU interaction, interrupt generation is also supported upon reaching a programmable memory full threshold condition.

The APC341 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial and scientific applications that require, high-performance analog inputs.

The APC341 boards are available in standard or extended temperature range as follows:

Model	Resolution	512 Sample Momery Buffer	Temperature Range
APC341	14-bit	Yes	0 to +70°C
APC341E	14-bit	Yes	-40 to +85°C

KEY APC341 FEATURES

- **14-Bit ADC Resolution** - Eight individual 14-bit successive approximation Analog to Digital Converters (ADC) with integral sample and hold are utilized.
- **8μsec Conversion Time** - A maximum conversion rate of 125KHz is supported.
- **Two 512 Sample Memory Buffers –** Two 512 sample deep memory buffers are available to reduce CPU interactions. While new digitized data is written to one memory buffer, data can be read from the other at burst data rates. This allows the external processor to service more tasks within a given time. Data tagging is also implemented for easy channel data identification.
- **Memory Buffers Switch Condition –** When the number of new data samples exceed a programmable threshold value the input buffer switches to the data read buffer which allows reading of the new data. The old read buffer will simultaneously switch from the data read to the data input buffer.
- **Interrupt Upon Reaching a Memory Threshold Condition –** An interrupt can be generated when the number of new data samples reaches a programmable threshold condition. This feature can be used to minimize CPU interaction.
- **Programmable Control of Channels Converted** - Up to 16 differential analog inputs are monitored. Channels 0 to 7 are simultaneously converted followed by the simultaneous conversion of channels 8 to 15. Channels may be individually enabled/disabled for simultaneous conversion.
- **User Programmable Conversion Timer** - A programmable conversion timer is available to control the time between simultaneous conversion of new banks of channel data. For example, channels 0-7 are converted immediately upon trigger and then channels 8-15 are converted after a user programmable delay from the start of the first eight channels. An overall count value is also used to control when conversions will start again for the first eight channels. Supports a maximum interval of 2.09 seconds.
- **Continuous Conversion Mode** - All channels selected for conversion are continually digitized with the interval between conversions controlled by the user programmed conversion timer registers. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Single Cycle Conversion Mode** - All channels selected for conversion are digitized once with the time between channels 0 to 7 and 8 to 15 controlled by a programmable timer. Single cycle conversion mode is initiated by a software or external trigger.
- **External Trigger Input or Output** - The external trigger is assigned to a field I/O line. This external trigger may be configured as an input, output, or disabled. As an output this signal provides a means to synchronize other boards to a single APC341 timer reference. As an input the signal will trigger the APC341 hardware to initiate data conversions.
- **Precision On Board Calibration Voltages** - Calibration autozero and autospan precision voltages are available to permit host computer correction of conversion errors. The calibration voltages can be converted and then compared to the expected value stored in on board memory. Calibration voltages include: 0V (local analog ground), and a precision 5 volt reference.
- **Fault Protected Input Channels** - Analog input overvoltage protection to +/-25V with power on and +/-40V with power off.

PCI BUS INTERFACE FEATURES

- **Slave Module**- All read and write accesses are implemented as either a 32-bit, 16-bit or 8-bit single data transfer.
- **Immediate Disconnect on Read** - The PCI bus will immediately disconnect after a read. The read data is then stored in a read FIFO. Data in the read FIFO is then accessed by the PCI bus when the read cycle is retried. This allows the PCI bus to be free for other system operations while the read data is moved to the read FIFO.
- **Interrupt Support** - PCI bus INTA# interrupt request is supported. All board interrupts are mapped to INTA#. The APC341 board software programmable registers are utilized as interrupt request control and status monitors.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

The APC341 field I/O is accessed from a SCSI-2 (50-pin) front panel connector. This board only supports front I/O access.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the APC341 analog input board, use of the shortest possible length of shielded input cable is recommended.

Cables:

Model 5025-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting the APC341 board to Model 5025-552 termination panels.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag APC341, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

APC341 ActiveX CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of APC341 ActiveX (Object Linking and Embedding) drivers for Windows 95® and newer compatible application programs (Model PMCSW-ATX). This software provides individual drivers that allow Acromag APC341 boards to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® applications and others. The ActiveX controls provide a high-level interface to APC341 boards, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC board (APC products use the corresponding PMC Module software).

APC341 VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of APC341 VxWorks® library. This software (Model PMCSW-API-VXW) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

APC341 QNX SOFTWARE

Acromag provides a software product (sold separately) consisting of APC341 QNX® library. This software (Model PCISW-API-QNX) is composed of QNX® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, Inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the APC341 board, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the APC341 board when installing cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-925 and the following discussion for configuration and assembly instructions.

Software Configuration

Software configurable control registers are provided for control of external trigger mode, conversion mode, timer control, channel enable, and interrupt mode selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as needed for the application before starting analog input conversions. Refer to section 3 for programming details.

CONNECTORS

Connectors of the APC341 board consist of one 50-pin front panel SCSI-2 field I/O connector, and one P1 PCI local bus connector. These interface connectors are discussed in the following sections.

Front Panel Field I/O Connector

The front panel connector provides the field I/O interface connections. The front panel connector is a SCSI-2 50-pin female connector (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the front panel via round shielded cable (Model 5028-187).

Front panel connector pin assignments are shown in Table 2.1. When reading Table 2.1 note that channel designations are abbreviated to save space. . For example, channel 0 is abbreviated as "+CH00" & "-CH00" for the + & - connections, respectively.

Table 2.1: APC341 Field I/O Pin Connections

Pin Description	Number	Pin Description	Number
+CH00	1	-CH08	26
-CH00	2	COMMON	27
COMMON	3	+CH09	28
+CH01	4	-CH09	29
-CH01	5	COMMON	30
COMMON	6	+CH10	31
+CH02	7	-CH10	32
-CH02	8	COMMON	33
COMMON	9	+CH11	34
+CH03	10	-CH11	35
-CH03	11	COMMON	36
COMMON	12	+CH12	37
+CH04	13	-CH12	38
-CH04	14	COMMON	39
COMMON	15	+CH13	40
+CH05	16	-CH13	41
-CH05	17	COMMON	42
COMMON	18	+CH14	43
+CH06	19	-CH14	44
-CH06	20	COMMON	45
COMMON	21	+CH15	46
+CH07	22	-CH15	47
-CH07	23	COMMON	48
COMMON	24	EXT TRIGGER*	49
+CH08	25	SHIELD	50

***** Indicates that the signal is active low.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the APC341 board and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Drawing 4501-928 for analog input connections for differential-ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

The APC341 is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the APC341 board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed.

External Trigger Input/Output

The external trigger signal on pin 49 of the front panel connector can be programmed as an input, output, or disabled.

As an input, the external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The external trigger signal is an active low edge sensitive signal. That is, the external trigger signal will trigger the APC341 hardware on the falling edge. Once the external trigger signal has been driven low, it should remain low for a minimum of 500 nano seconds.

As an output an active-low TTL signal can be driven to additional APC341s, thus providing a means to synchronize the conversions of multiple APC341s. The additional APC341s must program their external trigger for signal input and convert on external trigger only mode. See section 3.0 for programming details to make use of this signal.

The external trigger signal can also be disabled. This prevents external noise from falsely triggering the board. See section 3.0 for programming details to make use of this signal.

PCI Bus Connections for P1

Table 2.3 indicates the pin assignments for the PCI bus signals at the card edge connector. Connector pins are designated by a letter and a number. The letter indicates which side of a particular connector the pin contact is on. “B” is on the component side of the board while “A” is on the solder side. Connector “gold finger” numbers increase with distance from the bracket end of the printed circuit board.

Refer to the PCI bus specification for additional information on the PCI bus signals.

TABLE 2.2: PCI Bus P1 CONNECTIONS

Signal	Pin	Pin	Signal
-12V	B01	A01	***TRST#***
TCK	B02	A02	***+12V***
Ground	B03	A03	***TMS***
TDO	B04	A04	TDI
+5V	B05	A05	+5V
+5V	B06	A06	INTA#
INTB#	B07	A07	***INTC#***
INTD#	B08	A08	+5V
PRSNT1#	B09	A09	***Reserved***
Reserved	B10	A10	+5V
PRSNT2#	B11	A11	***Reserved***
Ground	B12	A12	Ground
Ground	B13	A13	Ground
Reserved	B14	A14	***Reserved***
Ground	B15	A15	RST#
CLK	B16	A16	+5V
Ground	B17	A17	***GNT#***
REQ#	B18	A18	Ground
+5V	B19	A19	***Reserved***
AD[31]	B20	A20	AD[30]
AD[29]	B21	A21	***+3.3V***
Ground	B22	A22	AD[28]
AD[27]	B23	A23	AD[26]
AD[25]	B24	A24	Ground
+3.3V	B25	A25	AD[24]
C/BE[3]#	B26	A26	IDSEL
AD[23]	B27	A27	***+3.3V***
Ground	B28	A28	AD[22]
AD[21]	B29	A29	AD[20]
AD[19]	B30	A30	Ground
+3.3V	B31	A31	AD[18]
AD[17]	B32	A32	AD[16]
C/BE[2]#	B33	A33	***+3.3V***
Ground	B34	A34	FRAME#
IRDY#	B35	A35	Ground
+3.3V	B36	A36	TRDY#
DEVSEL#	B37	A37	Ground
Ground	B38	A38	STOP#
LOCK#	B39	A39	***+3.3V***
PERR#	B40	A40	***SDONE***
+3.3V	B41	A41	***SBO#***
SERR#	B42	A42	Ground
+3.3V	B43	A43	PAR
C/BE[1]#	B44	A44	AD[15]
AD[14]	B45	A45	***+3.3V***
Ground	B46	A46	AD[13]
AD[12]	B47	A47	AD[11]
AD[10]	B48	A48	Ground
Ground	B49	A49	AD[09]
KEYWAY			KEYWAY
KEYWAY			KEYWAY
AD[08]	B52	A52	C/BE[0]#
AD[07]	B53	A53	***+3.3V***
+3.3V	B54	A54	AD[06]
AD[05]	B55	A55	AD[04]
AD[03]	B56	A56	Ground
Ground	B57	A57	AD[02]
AD[01]	B58	A58	AD[00]
+5V	B59	A59	+5V
ACK64#	B60	A60	***REQ64#***
+5V	B61	A61	+5V
+5V	B62	A62	+5V

Bracket End

(#) s used to indicate an active-low signal.

BOLD ITALIC Logic Lines are NOT USED by this board.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the APC341 board.

This Acromag APC341 board complies with PCI Specification Version 2.2. It is a PCI bus slave board.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The APC341 board can be accessed via the PCI bus memory space and configuration spaces only.

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PCI is a Plug-and-Play card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to access a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the board requires. It then programs the boards configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PCI board requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PCI board.

Since this PCI board is relocatable and not hardwired in address space, this board's mapping and IRQ information is stored in the board's Configuration Space registers.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This board provides 256 bytes of configuration registers for this purpose. The APC341 contains the configuration registers, shown in Table 3.1, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the APC341 and the interrupt request line that goes active on an APC341 interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=4D4D		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for APC341 4K-Byte Block			
5 : 10	Not Used			
11	Subsystem ID=0000		Subsystem Vendor ID=0000	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCI bus memory space to control the acquisition of analog inputs from the field. As such, three types of information are stored in the memory space: control, status, and data.

The memory space address map for the APC341 is shown in Table 3.2. Note that the base address for the APC341 in memory space must be added to the addresses shown to properly access the APC341 registers. Register accesses as 32, 16, and 8-bit in memory space are permitted.

Table 3.2: APC341 Memory Map[2]

Base Addr+	D31 D16	D15 D00	Base Addr+
03	Not Used[1]	Interrupt Register	00
07	Control Register		04
0B	Not Used[1]	Channel Enable Control	08
0F	Low Bank Timer		0C
13	High Bank Timer		10
17	Not Used[1]	Memory Threshold Register	14
1B	Not Used Bits-31 to 01	Start Convert Bit-0	18
1F	Not Used[1]	Reference Voltage Access Register	1C
23	Not Used[1]	Reference Voltage Data & Status	20
27	Not Used[1]	Reference Voltage Write Enable Code[3]	24
29	Not Used[1]		28
↓	↓		↓
7FF	Not Used[1]		7FC
803	1st Memory Location Not Used(31:20), Tag bits(19:16), Data(15:0)		800
↓	↓		↓
FFF	512th Memory Location Not Used(31:20), Tag bits(19:16), Data(15:0)		FFC

Notes (Table 3.2):

1. The APC341 will return 0 for all addresses that are "Not Used".
2. All Reads and writes are 8 clock cycles.
3. This byte is reserved for use at the factory to enable writing of the reference voltage.

This memory map reflects byte accesses using the “Little Endian” byte ordering format. Little Endian uses even-byte addresses to store the low-order byte. The Intel x86 family of microprocessors uses “Little Endian” byte ordering. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses.

Interrupt Register, (Read/Write) - (Base + 00H)

This read/write register is used to enable board interrupt, determine the pending status of interrupts, and release an interrupt.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.3: Interrupt Register

BIT	FUNCTION
0	Board Interrupt Enable Bit. (Read/Write Bit) 0 = Disable Interrupt 1 = Enable Interrupt If enabled via this bit an interrupt request from the board will be issued to the system if the Memory contains more than the threshold number of bytes selected via the Memory Threshold register. The interrupt request will remain active until the interrupt release bit is set, or by disabling interrupts via this bit.
1	Board Interrupt Pending Status Bit. (Read Only Bit) 0 = Interrupt Not Pending 1 = Interrupt Pending This bit can be read to determine the interrupt pending status of the APC341. When this bit is logic “1” an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is a logic “0” an interrupt is not being requested. This bit will only indicate a pending status if the board is enabled for interrupt via bit-0. Once the bit is in the pending status it will remain until the pending interrupt is removed even if interrupts are disabled via bit-0.
14 to 2	Not Used[1]
15	Board Interrupt Release Bit. (Write Only Bit) 0 = Interrupt Not Released 1 = Interrupt Released This bit must be set to a logic “1” to release an interrupt request. This bit is typically set in the interrupt service routine to remove the interrupt request. Once an interrupt request is generated on the APC341, it will continue to assert the interrupt request until this Interrupt Release bit is set to logic “1” or interrupts are disabled via bit-0 of this register.

Notes (Table 3.3):
1. All bits labeled "Not Used" will return logic "0" when read.

Control Register, (Read/Write) - (Base + 04H)

This read/write register is used to enable single or continuous conversions, select conversion of calibration voltages or field analog signals, control external trigger input/output mode, monitor Memory status, and issue a software reset to the board.

The function of each control register bit is described in Table 3.4. This register can be read or written via 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all control register bits to 0.

Table 3.4: Control Register

BIT	FUNCTION
1, 0 (Read/ Write Bits)	00 = Conversions are disabled. 01 = Enable Single Conversion Mode. A single conversion is initiated per software start convert or external trigger. The internal channel timer controls the start conversion of channels 8-15. 10 = Enable Continuous Conversion Mode. Conversions are initiated by a software start convert or external trigger and continued by internal hardware triggers generated at the frequency set by the interval timer registers. 11 = Reserved
3, 2 (Read/ Write Bits)	00 = All Channels Differential Input. 01 = Auto Zero Calibration Voltage Input. 10 = Auto Span Calibration Voltage. 11 = Reserved
5, 4 (Read/ Write Bits)	00 = External Trigger Disable. 01 = External Trigger Set as Input. 10 = External Trigger Set as Output. 11 = Reserved. As an output Internal Timer triggers are driven on the External trigger pin of the field I/O connector. The External Trigger output signal can be used to synchronize the conversion of multiple boards. A single master APC341 must be selected for External Trigger output and Continuous Conversion mode while all other boards are selected for External Trigger input and Single Conversion mode. The external trigger signals (pin 49 of the field I/O) must be wired together for all synchronized boards. Also, the High Bank Timer must be programmed with the same value on all synchronized boards. The External Trigger input can be sensitive to external EMI noise which can cause erroneous external triggers. If External Trigger input or output is not required, the External Trigger should be configured as Disabled.
6 (Read/ Write Bit)	0 = Enable Continued Analog Input 1 = Disable Conversions on Memory Bank Switch If the system cannot read all valid data values available in the memory buffer before the rate of new input data acquisition causes the buffers to switch, then the automatic disabling of analog input acquisition upon memory bank switching can be selected via this control register bit. If this bit is set to 1, analog input conversions will be disabled upon a memory bank switch. Also, bits 0 and 1 of this register will be set to 00 to reflect the disabled analog input mode.
7	Not Used
8 (Read Only Bit)	Transition Status Bit 1 = Valid Data in Memory 0 = Waiting for New Valid Data in Memory This transition status bit can be polled to insure the Memory buffer data is valid. The transition status bit will be set when the memory buffer switches causing new valid data to be available in the read memory buffer. The transition status bit is cleared upon the first read of the memory buffer and will not be set again until new valid data is available.
14-9	Not Used
15 (Write Only Bit)	0 = Software Reset Inactive. 1 = Software Reset Issued. Reset signal is held active for 300ns.

Notes (Table 3.4):
1. All bits labeled "Not Used" will return logic "0" when read.

The software reset will clear this control register, the channel enable register, counters, and the Memory Threshold register.

Channel Enable Control Register (Read/Write, 08H)

The Channel Enable Control register (bits-15 to 0) is used to select the channels desired for conversion. Only those channels enabled are stored into the data Memory buffer. When the channel's corresponding bit is set high, per the table below, the channel's converted data is tagged and stored into the Memory buffer. For example, to enable channels 15, 11, and 7 through 0 the Channel Enable register must be set as 88FF hex.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

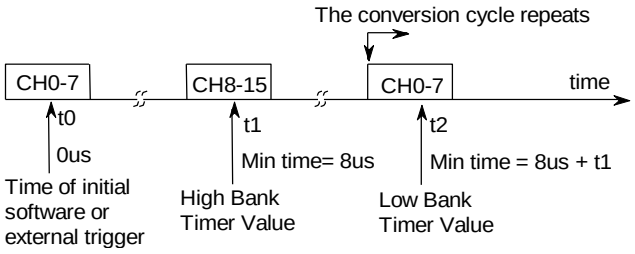
Channel Enable Control Register							
MSB							LSB
15	14	13	12	11	10	09	08
Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08
MSB							LSB
07	06	05	04	03	02	01	00
Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Low Bank Timer Register (Read/Write, 0CH)

Timed periodic triggering can be used to achieve precise time intervals between conversions. The Low Bank Timer register is a 24 bit register value that controls the interval time between conversions of all enabled channels.

The Low Bank Timer is used to control the frequency at which the conversion cycle is repeated for all enabled channels. For example, upon software or external trigger, channels 0 to 7 are simultaneously converted. The time programmed into the High Bank Timer Register then determines when channels 8 to 15 are simultaneously converted. The cycle repeats when the time programmed into Low Bank Timer has lapsed. At this time, channels 0 to 7 will again be simultaneously converted. Thus, the Low Bank Timer value must always be greater then the High

Bank Timer value by at least 8μ seconds. If Continuous Conversions are selected via the Control register, then conversions will continue until disabled. See figure 1 for an illustration of the sequence of conversions described in this paragraph.



Where: High Bank Timer Value must be > 8μ seconds
Low Bank Timer Value must be > t1 + 8μ seconds

Figure1: Time line of channel bank conversions

The 24-bit Low Bank Timer value divides an 8 MHz clock signal. The output of this Low Bank Timer is used to precisely generate periodic trigger pulses to control the frequency at which all enabled channels are converted. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Low Bank Timer Value} + 1}{8{,}000{,}000 Hz} = \text{T in seconds}$$

The following equation can be used to calculate the Low Bank Timer value. Note, this gives the value in decimal. It must still be converted to hex before it is written to the Low Bank Timer register.

$$\text{Low Bank Timer Value} = (\text{T seconds} \times 8{,}000{,}000 \text{Hz}) - 1$$

Where:
T = the desired time period between trigger pulses in seconds.
Low Bank Timer Value can be a minimum of 63 decimal if only channels 0 to 7 are enabled for conversion. If any channels in the upper bank (channels 8 to 15) are also enabled, then the minimum value is 127 decimal. The maximum value is 16,777,214 decimal.

The maximum period of time which can be programmed to occur between simultaneous conversions is (16,777,214 + 1) ÷ 8,000,000 = 2.097151875 seconds. The minimum time interval which can be programmed to occur is (63 + 1) ÷ 8,000,000 = 8.0μ seconds. This minimum of 8.0μ seconds is defined by the minimum conversion time of the hardware given only channels 0 to 7 are enabled for conversions. If any of channels 8 to 15 are enabled for conversion, then the minimum time that the Low Bank Timer can be programmed is 127 decimal. The minimum time of 16μ seconds allows 8μ seconds for channels 0 to 7 and 8μ seconds for channels 8 to 15.

The 8μ seconds maximum sample rate corresponds to a maximum sample frequency of 125KHz. The maximum analog input frequency should be band limited to one half the sample frequency. An anti-aliasing filter should be added to remove unwanted signals above 1/2 the sample frequency in the input signal for critical applications.

Reading or writing the Low Bank Timer register is possible with 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

High Bank Timer Register (Read/Write, 10H)

The High Bank Timer register is a 24 bit register that controls when the upper bank of channels 8 to 15 are converted.

The High Bank Timer is used to control the delay after channels 0 to 7 are converted until channels 8 to 15 are simultaneously converted. For example, upon software or external trigger channels 0 to 7 are simultaneously converted. Then, the time programmed into this counter determines when channels 8 to 15 will be simultaneously converted. See figure 1 for an illustration of this sequence of events.

If a channel within the 8 to 15 bank is enabled in the Channel Enable Control register, then the High Bank Timer register must be programmed with a delay. If this register is left as zero erroneous operation will result.

The 24-bit High Bank Timer value is divided by an 8 MHz clock signal. The output of this Timer is used to precisely generate periodic trigger pulses to control the frequency at which the bank of channels 8 to 15 are simultaneously converted. The time period between trigger pulses is described by the following equation:

$$\frac{\text{High Bank Timer Value} + 1}{8{,}000{,}000 Hz} = \text{T in seconds}$$

Where:
T = the desired time period between trigger pulses in seconds.
The **High Bank Timer Value** can be minimum of 63 decimal. The maximum value is 16,777,150 decimal.

The maximum period of time which can be programmed to occur between conversions is (16,777,150 + 1) ÷ 8,000,000 = 2.097143875 seconds. The minimum time interval which can be programmed to occur is (63 + 1) ÷ 8,000,000 = 8.0μ seconds. This minimum of 8.0μ seconds is defined by the minimum conversion time of the hardware. This gives channels 0 to 7 eight micro seconds to complete their simultaneous conversion. Then, channels 8 to 15 can be simultaneously converted.

Reading or writing the High Bank Timer register is possible with 32-bit, 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Memory Threshold Register (Read/Write, 14H)

The Memory Threshold register is an 8-bit register that is used to control transition between two 512 deep memory banks. One memory bank is used to store converted analog input data while the other is accessible for reading of converted analog input data. When the analog input memory buffer contains more samples than the Memory Threshold value the memory banks will switch. This allows software to read the new converted analog input data. The new data must be read before the memory banks switch again. If the system cannot keep up by reading the memory buffer before they switch, then the automatic disabling of analog input upon memory bank switching can be selected via the control register bit-6.

The number of valid analog input data samples available in the memory buffer will be one more than the value set in the Memory Threshold register. Thus, if the memory threshold value is 33 then 34 valid data entries will be present in memory when the memory buffer switch occurs. The Memory Threshold register value can be any value between 1 and 511.

An interrupt can also be issued upon exceeding the specified threshold level, if enabled via bit-0 of the interrupt register. This interrupt indicates that new data is available in the memory buffer. An interrupt request can be released by setting bit-15 of the Interrupt register to a logic one. The interrupt request can also be disabled by setting bit-0 to a logic zero; however, the interrupt request will remain active on the APC341 until released via bit-15.

Reading or writing to this register is possible via 32-bit, 16-bit or 8-bit data transfers. This register's contents are set to 1FF hex (511 decimal) upon reset.

Start Convert Register (Write Only, 18H)

The Start Convert register is write-only and is used to trigger conversions by setting data bit-0 to a logic one. This method of starting conversions is most useful for its simplicity and for when precise time of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The APC341 control and timer register bits must first be configured before the Start Convert bit is set.

This register can be written via 32-bit, 16-bit or 8-bit data transfer. Data bit-0 must be a logic one to initiate data conversions.

Start Convert Register			
Not Used			Start Convert
31	• • •	01	00

Memory Buffer (Read Only, 800H to FFCH)

In order to support burst data acquisition of digitized converted data, two 512-sample memory buffers are used. While one buffer functions to acquire new data input from the converters, the other functions as a read buffer. Data can be read at burst rates via the PCI bus to obtain new digitized data. The two memory buffers switch functions based upon the Memory Threshold register value, when the number of new input digitized data samples exceeds the Memory Threshold value.

Since all channels share the same memory, channel data tagging is implemented. The tag value identifies the channel to which the data corresponds. The hardware tags each memory location with a channel number, so the data can easily match with its source channel.

The Memory samples are 20-bit data values. The least significant bits, 15 to 0, represent the digitized data while bits 19 to 16 represent the channel tag.

Care should be taken when reading data from the memory buffer. To insure the memory buffer data is valid the Transition Status bit (bit-8 of the Control Register) can be polled. The Transition Status bit will be set when valid data is available in the memory buffer. The Transition Status bit is cleared upon the first read of the memory buffer and will not be set again until the memory buffers switch, based upon the Threshold register value. Alternatively, an interrupt upon threshold met condition can be used to start reading of valid data.

Reading of the Memory is possible via 32-bit, 16-bit, or 8-bit data transfers.

Analog Input and Corresponding Digital Codes

The data coding is in binary two's compliment. The digital code corresponding to each of the given ideal analog input values is given in binary two's complement format in Table 3.5. Note that the 14 bit data values are left justified within the 16-bit word. For the APC341 the least significant 2 bits will be returned as zero when read.

Table 3.5: Digital Output Codes and Input Voltages

DESCRIPTION	ANALOG INPUT	
Model	**APC341 (14-bit)**	
Least Significant Bit Weight	1.22mV	
+ Full Scale Minus One LSB	9.998779 Volts	7FFC hex
Midscale	0V	0000h
One LSB Below Midscale	-1.22mV	FFFC hex
Minus Full Scale	-10V	8000 hex

Reference Voltage Access Register (Write, 1CH)

This register is used to initiate a read of the reference voltage value. The reference voltage value is provided so that software can adjust and improve the accuracy of the analog input voltage over the uncalibrated state. The reference voltage is precisely measured at the factory and then stored to this location at the addresses given in table 3.6.

The Reference Voltage Access Register is a write-only register and is used to configure and initiate a read cycle to the Reference Voltage memory. Setting bit-15 of this register high, to a "1'', initiates a read cycle.

The address of the Reference Voltage to be read must be specified on bits 14 to 8 of the Reference Voltage Access register.

Most Significant Byte of Reference Voltage Access Reg	
Read or Write~	Address
15	14, 13, 12, 11, 10, 9, 8

The reference voltage is stored in memory as a null terminated ASCII character string. For example if the value 4.99835 were stored to memory the corresponding ASCII characters would be 34, 2E, 39, 39, 38, 33, 35, 00 as shown in Table 3.6. Note, the ASCII equivalent of a decimal point is 2E and the null character is 00. The memory should be read starting at address 00 until the null ASCII character is read. This string can then be converted into a float by using your compiler's ATOF function.

Table 3.6: Reference Voltage Address Memory Map

Address (Hex)							
00	01	02	03	04	05	06	07
Example Reference Value							
4	.	9	9	8	3	5	null
ASCII Characters As Stored In Memory							
34	2E	39	39	38	33	35	00

The address corresponding to each of the reference voltage digits is given in hex. The most significant digit is stored at address 00 hex.

For additional details on the use of the reference voltage, refer to the “Data Correction” section.

Write accesses to the Reference Voltage Access register are possible via 32-bit or 16-bit data transfers, only. Storing the reference voltage value to memory is normally only performed at the factory.

A software or hardware reset has no affect on this register.

Reference Voltage Read Data/Status Register (Read, 20H)

The Reference Voltage Read Data/Status register is a read-only register and is used to access the read data and determine the status of a read cycle initiated by the Reference Voltage Access register. In addition, this register is used to determine the status of a write cycle to the memory. When bit-1 of this register is set it indicates the memory is busy completing a write cycle.

All read accesses to this Data/Status register initiate an approximately 1millisecond access to the memory. **Thus, you must wait 1 millisecond after reading this Data/Status register before a new read or write cycle to the memory can be initiated, (an EEPROM latency limitation).**

A read request, initiated through the Reference Voltage Access register, will provide the addressed digit of the reference voltage on data bits 15 to 8 of the Reference Voltage Data/Status register. Although the read request via the Reference Voltage Access register is accomplished in 200 nano seconds, typically, the reference voltage digit will not be available in the Reference Voltage Data/Status register for approximately 2.5 milliseconds.

Bit-0 of the Reference Voltage Data/Status register is the read complete status bit. This bit will be set high to indicate that the requested reference voltage digit is available on data bits 15 to 8 of the Reference Voltage Data/Status register. This bit is cleared upon initiation of a new read access of the memory or upon issue of a hardware reset.

Writes to Reference Voltage memory require a special enable code and are normally only performed at the factory. The board should be returned to Acromag if the reference voltage must be re-measured and stored to memory.

A write operation to the memory, initiated via the Reference Voltage Access register, will take approximately 5 milliseconds. Bit-1 of the Reference Voltage Data/Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation and will remain high until the requested write operation has completed. New read or write accesses to the memory, via the Reference Voltage Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A hardware reset of the IP board will also clear this bit.

Read accesses to the Reference Voltage Data/Status register are possible via 32-bit or 16-bit data transfers, only. A software or hardware reset will clear all bits to zero.

MODES OF CONVERSION

The APC341 provides two methods of analog input operation for maximum flexibility with different applications. The following sections describe the features of each method and how to best use them.

Single Conversion Mode

In the Single Conversion mode, conversions are initiated by a software or external trigger. Upon the trigger, channels 0 to 7 will be simultaneously converted. Then, after the time programmed into the High Bank Timer has been reached, channels 8 to 15 will be converted. All channels enabled in the Channel Enable Control register will be tagged with their channel number and stored to the memory buffer. No additional conversions will be initiated unless a new software or external trigger is generated.

To select this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code “01”. Then, issuing a software start convert or external trigger will initiate conversions. The Low Bank Timer is not used in this mode of operation. Also, the High Bank Timer is not needed if channels 8 to 15 are disabled.

This mode of operation can be used to initiate conversions based on external triggers. This can be used to synchronize multiple boards to a single board running in a continuous conversion mode. The external trigger of a APC341 “master” must be programmed as an output. The external trigger signal of that board must then be connected to the external trigger signal of all other boards that are to be synchronized. These other boards must be programmed for Single Conversion mode and external trigger input. Also, the High Bank Timer must be programmed with the same value on all synchronized boards. Data conversion can then be initiated via the Start Convert bit of the master board configured for continuous conversion mode.

Continuous Conversion Mode

In the Continuous Conversion mode, the hardware controls the continuous conversions of all enabled channels. All channels 0 to 15 are converted at the rate specified by the Low Bank Timer. Channels, 8 to 15, are converted after channels 0 to 7. The time programmed into the High Bank Timer specifies how long after channels 0 to 7 are converted before channels 8 to 15 are converted.

To initiate this mode bits 1 and 0 of the Channel Control register must be set to digital code “10”. Then, issuing a software start convert or external trigger will initiate the continuous conversions of all enabled channels.

The interrupt capability of the board can be employed as a means to indicate to the system that up to 512 samples (depending on the threshold selected via the Threshold register) are available to be read.

Alternatively, a polling method could be used. The Transition Status bit (bit-8 of the Control Register) can be polled to insure the memory buffer data is valid. The Transition Status bit will be set when valid data is available in the memory buffer. The Transition Status bit is cleared upon the first read of the memory buffer and will not be set again until the memory buffers switch again based upon the Threshold register value.

PROGRAMMING CONSIDERATIONS

The APC341 provides different methods of analog input acquisition to give the user maximum flexibility for their application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion Mode Example

This example will enable channels 0, 3, and 8 through 15 for the single conversion mode of operation. Conversions can be initiated via software or external trigger. Channels 8 to 15 will be simultaneously converted 16μ seconds after channels 0 and 3.

1. Execute Write of 0011H to the Control Register at Base Address + 04H.
   a) Single Conversion is enabled.
   b) External and Software generated triggers are enabled.

2. Execute Write of FF09H to the Channel Enable Control register at Base Address + 08H. This will enable channels 0, 3, and 8 through 15 for conversion.

3. Execute Write of 007FH to the High Bank Timer at Base Address + 10H. Channels 8 to 15 will be converted 16μ seconds after channels 0, and 3.

4. Execute Write of 0001H to the Start Convert Bit at Base Address + 18H. This starts the simultaneous conversion of channels 3 and 0. Then, 16μ seconds later, channels 8 to 15 are simultaneously converted.

Continuous Conversion Mode with Interrupt Example

This example will enable channels 0 through 13 for the continuous conversion mode of operation. Interrupts are enabled and an interrupt threshold of 430 samples is programmed. The Low Bank Timer will be set for an 80μ second interval. The High Bank Timer is set to activate the simultaneous conversion of channels 8 through 13 at 23μ seconds after channels 0 to 7. Conversions can be initiated via software or external trigger.

1. Enable interrupts for the APC board by writing a “1” to bit 1 of the Interrupt Register at Base Address + 00H.

2. Execute Write of 0012H to the Control Register at Base Address + 04H.
   a) Continuous Conversion mode is selected.
   b) External and Software generated triggers are enabled.

3. Execute Write of 3FFFH to the Channel Enable Control register at Base Address + 08H. This will enable channels 0 through 13 for conversion.

4. Execute Write of 027FH to the Low Bank Timer Register at Base Address + 0CH.
   a) This sets the Conversion Timer to 639 decimal as needed for an 80μ second interval.

5. Execute Write of 00B7H to the High Bank Timer Register at Base Address + 10H.
   a) This sets the High Bank Timer to 183 decimal as needed for a 23μ seconds delay after channels 0 through 7. Note: (183+1) ÷ 8,000,000 = 23μ seconds.

6. Execute Write of 1AEH to the Memory Threshold register at Base Address + 14H.
   a) The APC341 will issue an interrupt to the system when more than 430 samples are present in the Memory buffer.

7. Execute Write of 0001H to the Start Convert Bit at Base Address + 18H.
   a) This starts the simultaneous conversion of channels 0 to 7. Then, after 23μ seconds channels 8 through 13 are simultaneously converted. The cycle repeats every 80μ seconds.

USE OF CALIBRATION REFERENCE SIGNAL

A Reference voltage signal for analog input calibration has been provided for use to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Software calibration uses some fairly complex equations. **Acromag recommends purchase of our ActiveX, QNX or VxWorks software to make communication with the board and calibration easy. It relieves you from having to turn the equations in the following sections into debugged software calibration code.**

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Instrumentation Amplifier (IN-AMP) and the Analog to Digital Converter (ADC). The untrimmed IN-AMP and ADC have significant offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the APC341 can be accomplished by using the calibration reference voltage and auto zero (analog ground reference) present on the board. The five volt and the analog ground references are used to determine two points of a straight line which defines the analog input characteristic. The exact value of the five volt reference is stored in on board memory to provide the most accurate calibration.

The APC341 has eight separate ADC circuits. As such, each of the first eight channels will have their own unique offset and gain errors. Note, channels 8 through 15 share the gain and offset values of channels 0 through 7. The five volt reference (Auto Span Calibration Voltage) and the ground reference (Auto Zero voltage) will need to be selected and converted through each of the eight channels to determine the corrected value as given in equation 1.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the stored reference voltage.

$$CorrectValue = \left[CountRead - Count_{0V}\right] \times \left[\frac{5VRefValue}{Count_{5V} - Count_{0V}}\right] \quad (1)$$

Where:

$Count_{5V}$ = Actual ADC Data Read With 5 Volt Calibration Voltage Applied

$Count_{0V}$ = Actual ADC Data Read With Auto Zero Calibration Voltage Applied

CountRead = Uncorrected ADC Data Read For Channel Undergoing Correction.

The **5VRefValue** represents the five volt reference value as it is read from stored memory via the Reference Voltage Access register and the Reference Voltage Read Data/Status register.

The $Count_{5V}$ and $Count_{0V}$ reference voltages should not be determined immediately after startup but after the board has reached a stable temperature (about 20 minutes) and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 100) of the reference voltages should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

Calibration Programming Example

Assume that channels 0 through 3 are enabled, and corrected input channel data is desired. The calibration parameters ($Count_{5V}$ and $Count_{0V}$) need to be determined for channels 0 through 3 before the analog field signals can be corrected. Note that channel 0 and 8 share the same INAMP and ADC and thus share the same $Count_{5V}$ and $Count_{0V}$ values. This is also true for channels 1 and 9, 2 and 10, etc..

Determination of the $Count_{0V}$ Value

1. Execute Write of 01H to the Interrupt Register at Base Address + 00H.
   a) Interrupts Enabled

2. Execute Write of 0046H to the Control Register at Base Address + 04H.
   a) Continuous Mode Enabled
   b) Auto Zero Calibration Voltage Selected ($Count_{0V}$)
   c) External Trigger Disabled
   d) Analog Input is Disabled on Memory Bank Switch

3. Execute Write of 000FH to the Channel Enable Control Register at Base Address + 08H. This will permit the Auto Zero values corresponding to channels 0 to 3 to be stored in the memory buffer.

4. Execute Write of BFH to the Low Bank Timer register at Base Address + 0CH. This sets the interval time between conversions to 24μ seconds.

5. Execute Write of 18FH to the Memory Threshold register at Base Address + 14H. Since interrupts are enabled in the control register, an interrupt request will be issued when 400 values of the Auto Zero calibration voltage have been stored in the memory buffer. This corresponds to 100 values for each of the four channels enabled.

6. Execute Write of 0001H to the Start Convert Bit at Base Address + 18H. This starts the continuous mode of conversions.

7. Upon system interrupt, Analog input is disabled as requested via bit-6 of the Control register. Execute Write of 8000H to the Interrupt Register at Base Address + 00H.
   a) Interrupts are disabled, and the Interrupt request is released.

8. Software must read the memory buffer and calculate a $Count_{0V}$ value for each channel 0 to 3, by averaging the 100 values for each channel.

Determination of the $Count_{5V}$ Value

9. Execute Write of 01H to the Interrupt Register at Base Address + 00H.
   a) Interrupts Enabled

10. Execute Write of 004AH to the Control Register at Base Address + 04H.
    a) Continuous Mode Enabled
    b) Auto Span Calibration Voltage Selected ($Count_{5V}$)
    c) External Trigger Disabled
    d) Analog Input is Disabled on Memory Bank Switch

11. Writing the Channel Enable register, Low Bank Timer Value, and the Memory Threshold is not necessary because they need not change from that programmed in the previous steps.

12. Execute Write of 0001H to the Start Convert Bit at Base Address + 18H. This starts the continuous mode of conversions.

13. Upon system interrupt, Analog input is disabled as requested via bit-6 of the Control register. Execute Write of 8000H to the Interrupt Register at Base Address + 00H.
    a) Interrupts are disabled, and the Interrupt request is released.

14. Software must read the memory buffer and calculate a $Count_{5V}$ value for each channel 0 to 3, by averaging the 100 values for each channel.

Read the Reference Voltage Value From Memory

15. Read the reference voltage memory to retrieve the unique reference voltage value (5VRefValue). To obtain the reference voltage value the ASCII characters comprising the reference voltage must be read until the null (terminating) character “00” is read. To read the most significant digit, the Reference Voltage Access register must be written with data value 8000H at Base

Address + 1CH. The data can be read by polling the Reference Voltage Read Data/Status register. When bit 0 of the Reference Voltage Read Data/Status register is set to logic high, then the data on bits 15 to 8 contains the most significant digit of the reference voltage value, represented as an ASCII character.

To initiate a read of the second memory location of the reference voltage value, the Reference Voltage Access register must be written with data value 8100H at Base Address + 1CH. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the decimal point digit of the reference voltage value.
This procedure must continue until the null ASCII character is read from memory. The string can then be converted into a float by using your compiler's atof function.

16. Since $Count_{0V}$, $Count_{5V}$, and 5VRefValue are known, corrected input data values can now be determined.

Start Conversion Of Differential Input Channel Data

17. Execute Write of 01H to the Interrupt Register at Base Address + 00H.
    a) Interrupts Enabled

18. Execute Write of 0042H to Control Register at Base Address + 04H.
    a) Continuous Mode Enabled
    b) Channel Differential Input Selected
    c) External Trigger Disabled
    d) Analog Input is Disabled on Memory Bank Switch

19. Execute Write 0001H to the Start Convert Bit at Base Address + 18H. This starts the continuous mode of conversions. Continuous simultaneous conversions of channels 0 to 3 are implemented and corresponding results are stored in the Memory buffer.

20. Upon system interrupt the Memory buffer at Base Address + 800H must be read. The data read should be corrected per equation 1 of this section.

Programming Interrupts

Interrupts can be enabled for generation after the Memory buffer contains more new data values than that set by the Memory Threshold register. Interrupts generated by the APC341 use interrupt request line INTA# . The interrupt release mechanism is release on register access. That is, the APC341 will release the INTA# signal when bit-15 of the Interrupt Register at Base Address + 00H is set to logic "1".

Interrupt Programming Example

1. Enable APC341 board interrupt by writing a "1" to bit 0 of the Interrupt register at Base Address + 00H.
2. Set the Memory Threshold register as desired at Base Address + 14H.
3. Interrupts can now be generated after more samples than that set in the Memory Threshold register are available in the Memory buffer.

General Sequence of Events for Processing an Interrupt

1. The APC341 asserts the Interrupt Request Line (INTA#) in response to an interrupt condition.
2. Determine the IRQ line assigned to the APC341 during system configuration (read configuration register number 15).
3. Set up the system interrupt vector for the appropriate interrupt.
4. Unmask the IRQ in the system interrupt controller.
5. The interrupt service routine pointed to by the vector set up in step 3 starts.
6. Interrupt service routine determines if the APC341 has a pending interrupt request by reading the Interrupt pending bit-1 of the Interrupt register.
7. Example of Generic Interrupt Handler Actions:
   a) Disable the interrupting APC341 by writing "0" to bit-0 of the Interrupt Register to disable interrupts on the APC341.
   b) Service the interrupt by reading converted data resident in the Memory buffer of the APC341.
   c) Clear the interrupt request by writing a "1" to bit-15 of the Interrupt register.
   d) Enable the APC341 for interrupts by writing "1" to bit-0 of the Interrupt register.
8. Write "End-Of-Interrupt" command to systems interrupt controller.
9. If the APC341's interrupt stimulus has been removed, the interrupt cycle is completed and the board holds the INTA# inactive.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the APC341. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-927 as you review this material.

FIELD ANALOG INPUTS

The field I/O interface to the board is provided through front panel connector (refer to Table 2.1). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operational errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-928 for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. APC341board control logic drives the select signals of the multiplexer as required per the programming of the control register.

Up to 16 differential inputs can be monitored. The multiplexer stage directs one of two groups of eight channels for simultaneous conversion. Channels 0 to 7 are simultaneously selected and converted by eight individual ADC's, and channels 8 to 15 are also simultaneously converted.

The output of the multiplexer stage feeds an instrumentation amplifier (INAMP) stage. The INAMP has a fixed gain of one. The INAMPs high input impedance allows measurement of analog input signals without loading the source. The INAMP

takes in the channel's + and - inputs and outputs a single ended voltage proportional to it.

The output of the INAMP feeds an Analog to Digital Converter (ADC). The ADC is a state of the art 14-bit (APC341) successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then, it returns to sample mode to acquire the next analog input signal. Once a conversion has been completed, control logic on the board automatically and simultaneously serially reads the digitized values corresponding to the eight channels. While the digitized values are read the inputs are in the acquire mode. Digital noise generated by reading the newly digitized values will not be present when the ADC transitions into the hold mode since the analog signals are allowed to settle for an interval after the digitized values are read. This pipelined mode of operation facilitates a maximum system throughput with minimum system noise.

The board contains two precision voltage references and a ground (autozero) reference for use in calibration. A 2.5 volt reference is used by the ADC. A 5 volt reference is used to provide accurate auto span voltage for offset and gain correction of the ADC and INAMP.

LOGIC/POWER INTERFACE

The logic interface to the board is made through and one P1 PCI connector (refer to Table 2.2). This connector also provides +5V and ±12V power to the board. Note that the signals in bold italic are not used.

A Field Programmable Gate-Array (FPGA) installed on the APC Module provides an interface to the board per PCI Local Bus Specification 2.2. The interface to the CPU board allows complete control of all APC341 functions.

PCI INTERFACE LOGIC

The PCI bus interface logic is imbedded within the FPGA. This logic includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCI target interface performs parity error detection, uses a single 4K base address register, and implements target abort, retry, and disconnect. The APC341 logic also implements interrupt requests via interrupt line INTA#.

All register accesses to the APC341 require 8 PCI clock cycles with the exception of burst read operations which will be implemented in three PCI clock cycles.

BURST READ OF APC341 MEMORY

Burst read of APC341 memory buffer will allow a 40Mbyte per second data read rate. With every three PCI clock cycles a new data sample is read from the memory buffer. The APC341 will automatically stop the burst operation upon reaching the end of the Memory buffer.

Note that, burst mode read operations can only be used on hardware that is prefetchable. The APC341 is prefetchable since it makes use of RAM, not FIFO, memory to retrieve sample data. Prefetchable hardware requires read operations that do not destroy the data. In burst read operations, it is possible for the system to read more data from a PCIbus board than is actually delivered to its destination. When this happens, given a FIFO implementation, the data would be forever destroyed/lost. However with the APC341 RAM implementation, the undelivered data could be read again. Reading of Memory buffer can start at any address location allowing access to any of the 512 available samples.

CONVERSION CONTROL LOGIC

All logic to control data conversions is imbedded in the APC board's FPGA. The control logic of the board is responsible for controlling the programmed mode of operation. Once the APC board has been configured, the control logic performs the following:

- Controls Multiplexers for selection of channel data.
- Controls serial transfer of data from the eight ADC's to the FPGA memory buffer.
- Controls conversion rate as user programmed.
- Provides memory buffer switch control.
- Provides external or internal trigger control.
- Controls read and write access to the reference voltage value stored in memory.
- Controls interrupt requests to the CPU and responds to interrupt select cycles.

MULTIPLEXER CONTROL CIRCUITRY

Analog channels are multiplexed into the ADC's. The multiplexers allows the programmable selection of analog channel data or the auto span and auto zero calibration voltages. When selected for differential analog input of channel data, channels 0 to 7 are automatically selected for simultaneous conversion first. Channels 0 to 7 are converted upon an external trigger or software start convert. Then, 1.25μ seconds after channels 0 to 7 are converted the multiplexers swith to channels 8 to 15 for input to the ADC's. This provides a setup time, for channels 8 to 15, of the High Bank time minus 1.25μ seconds.

DATA TRANSFER FROM ADC TO FPGA

A 16-bit serial shift register is implemented in the board's FPGA for each of the eight channels. Internal FPGA counters are used to synchronize the transfer of digitized data from the A/D converters to the memory buffer. Only the channels enabled for conversion are stored in memory and tagged for channel identification.

CONVERSION COUNTER

The ADC conversion rate is controlled by a conversion counter, which is a 24-bit counter implemented in the FPGA. The counter provides variable time periods up to 2.0889 seconds. The output of this counter is compared to the value stored in the Low Bank Timer register to trigger the start of new conversions for the continuous mode of operation. The output of the conversion counter is also compared to the value stored in the High Bank Timer register to determine when the second bank of channels (8 through 15) are to be simultaneously triggered for conversion.

MEMORY BUFFER SWITCH CONTROL

Two 512 sample memory buffers are provided in the FPGA logic to control simultaneous data acquisition and data reading via the PCI bus. One memory buffer accepts new data input samples along with a channel tag value. The other memory buffer is available for data reading at PCI burst data rates over the PCI bus. The Memory Threshold value is used to control transition between the two 512 sample memory buffers. When the analog input memory buffer contains more samples then the Memory Threshold value the memory banks will switch. See section 3.0 for programming details and use of the Memory Threshold register.

EXTERNAL TRIGGER

The external trigger connections are made via pin 49 of the Field I/O Connector. For all modes of operation, when the external trigger is enabled as an input via bits 4 and 5 of the control register, the falling edge of the external trigger will initiate simultaneous conversions for channels 0 to 7. Once the external trigger signal has been driven low, it should remain low for a minimum of 250n seconds for proper external trigger operation. The external trigger input signals must be TTL compatible. The APC341 uses a diode clamping circuit to protect the board from external trigger signals that violate the 5 volt logic (TTL) requirement.

As an output, an active-low TTL signal is driven from the APC board. The trigger pulse generated is low for 500n seconds, typical. See section 3.0 for programming details to make use of this signal.

INTERRUPT CONTROL LOGIC

The APC341 can be configured to generate an interrupt using a programmable Memory Threshold level. When the memory buffer has more samples than set in the Memory Threshold register the APC interrupt signal INTA# is driven active to the CPU to request an interrupt. Bit-1 of the Interrupt register (at Base Address + 0H) can be read to identify a pending interrupt. The interrupt release mechanism employed is release on register access. The APC341 will release the interrupt request when bit-15 of the Interrupt register (at Base Address + 0H) is set to a logic “1”.

REFERENCE VOLTAGE MEMORY CONTROL LOGIC

The FPGA of the APC341 board contains control logic that implements read and write access to reference voltage memory. The reference voltage memory (EEPROM) contains an ASCII null terminated string that represents the exact voltage of the on board reference circuit as measured and stored at the factory.

APC Software

Acromag also provides a software product (sold separately) consisting of APC341 ActiveX (Object Linking and Embedding) drivers for Windows 95® and newer compatible application programs (Model PMCSW-ATX). This software provides individual drivers that allow Acromag APC341 boards to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® applications and others. The ActiveX controls provide a high-level interface to APC341 boards, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC board (APC products use the corresponding PMC Module software).

In addition, Acromag provides a software product (sold separately) consisting of APC341 VxWorks® library or QNX® library. This software (Model PMCSW-API-VXW or Model PCISW-API-QNX) is composed of VxWorks® or QNX® (real time operating system) libraries for all Acromag PMC boards. The software is implemented as a library of “C” functions which link with existing user code to make possible simple control of all Acromag PMC boards (APC products use the corresponding PMC Module software).

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

The APC341 is shipped pre-calibrated by Acromag and may be returned at the discretion of the customer to measure the accuracy of the calibration at some defined period. Recalibration, if required, can be performed by the customer if the proper equipment is available to them and is otherwise offered through the Service Department at Acromag for a fee.

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your CPU board to verify that it is correctly configured. Replacement of the board with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag’s Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration…… Short PCI 5 Volt Board
Height..... 4.200 inches (106.68 mm).
Depth…….. 6.600 inches (167.64 mm).
Board Thickness..... 0.062 inches (1.59 mm).
Max Component Height….. 0.570 inches (14.48 mm).
Recommended Card Spacing…….. 0.800 inches (20.32 mm).
Connectors:
P1 (PCI Bus)…… PCI Specification Version 2.2. 5 V card "finger" edge spacing.

P2 (Field I/O)…… 50-pin, SCSI-2, female receptacle header (AMP 787082-5 or equivalent).

Power Requirements		Board APC341
5V[2]	Typical	265 mA
(±5%)	Max.	320 mA
+12V[3]	Typical	0 mA
(±5%)	Max.	0 mA
-12V[3]	Typical	0 mA
(±5%)	Max.	0 mA

Note:
1. Circuit board is selectively coated with a fungus resistant acrylic conformal coating.
2. Maximum rise time of 100m seconds.
3. The +/-12 volt power supplies on the PCI bus interface connector are not used. This board uses a DC-DC converter, which uses the 5V supply from the PCI bus interface connector and generates +/-15 volt supplies for the board.

ENVIRONMENTAL

Operating Temperature..... 0 to +70°C.
-40 to +85°C (E Versions)
Relative Humidity…..... 5-95% Non-Condensing.
Storage Temperature…..... -55°C to 100°C.
Non-Isolated..... Logic and field commons have a direct electrical connection.

Radiated Field Immunity[3](RFI).. Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.50% of FSR.

Electromagnetic Interference… Error is less than ±0.25% of FSR
Immunity[3] (EMI) under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Surge Immunity…… Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient
Immunity[3](EFT)…… Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions[3]…….. Meets or exceeds European Norm EN50081-1 for class A equipment.

CE Mark…… All models are designed to comply with EMC Directive 89/336/EEC per **European Standard EN 61000-6-1:2001** Electromagnetic compatibility (EMC) – Part 6-1: Generic standards - Immunity for residential, commercial and light-industrial environments and **European Standard EN 61000-6-3:2001** Electromagnetic compatibility (EMC) – Part 6-3: Generic standards - Emission standard for residential, commercial and light-industrial environments.

Note: Only the APC Models have the CE Mark.
FCC…….. Only the APC Models are compliant to standard FCC PART 15, Subpart.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this installation does cause harmful interference to the radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or experienced radio/TV technician for help.*

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures to suppress.

Note:
3. Reference Test Conditions: Temperature 25°C, 100K conversions/second, using a 1 meter shielded cable length connection to the field analog input channels 0-7.

Reliability Prediction

Mean Time Between Failure….. MTBF = TBD hours (not available at time of printing) @ 25°C, Using MIL-HDBK-217F, Notice 2.

ANALOG INPUTS

Input Channels (Field Access).. Two Banks of Eight Channels (Channels 0-7 and 8-15). The Channels of Each Bank are Simultaneously Converted.
Analog Input Memory Buffer….. 512 Sample Memory
Input Signal Type..... Voltage (Non-isolated).
Input Range…….. Bipolar -10 to +10 Volts
Input Overvoltage Protection…. +/-25 Volts Power On
+/-40 Volts Power Off
Data Format……. Binary two's complement format left justified within the 16-bit word

Maximum Source Impedance[4]	Maximum Operating Frequency	Channels in Operation
2.2KΩ	125KHz	0 to 7 & 8 to 15
6KΩ	50KHz	0 to 7 & 8 to 15
25KΩ	12.5KHz	0 to 7 & 8 to 15
50KΩ	6.25KHz	0 to 7 & 8 to 15
100KΩ	3.12KHz	0 to 7 & 8 to 15
1MΩ	125KHz	0 to 7 only

Note:
4. A low source impedance is required at the maximum operating frequency when channels 0 to 7 and 8 to 15 are in use. This is due to the leakage current experienced when the input multiplexer switches between the lower bank channels 0 to 7 and the high bank channels 8 to 15.

ADC Spec's

Conversion Rate…….. 125KHz
Input Voltage Range…… ±10 Volts
Data Format……. Binary 2's Complement

APC341
ADC…… Analog Devices AD7894
ADC Resolution…….. 14 Bits
No Missing Codes…… 14 Bits
Differential Nonlinearity…….. -1 to +1.5 LSB Maximum
Gain Error[5]…… ±6 LSB Maximum
Bipolar Zero Error[5]…….. ±8 LSB Maximum

Instrumentation Amplifier

INAMP…….. Burr-Brown INA128
Nonlinearity…….. ±0.001% of FSR Maximum
Offset Voltage[5]…… ±550μ Volt Maximum
Gain Error[5]…….. ±0.024% Maximum
Settling Time…… 7μ seconds Typical to 0.01%

Note:
5. Software calibration minimizes these error components.

5 Volt Calibration Reference Voltage

Temperature Drift…….. 2ppm/°C Typical, 5ppm/°C Max.

Maximum Overall Calibrated Error @ 25°C

APC341 Max. Total Error[6]
±2.4 LSB
0.014% Span

The maximum corrected (i.e. calibrated) error is the worst case accuracy. It is the sum of error components due to ADC quantization of the low and high calibration signals, instrumentation amplifier, and ADC linearity error at 25°C. For critical applications multiple input samples should be averaged to improve performance.

Note:
6. Software calibration must be performed in order to achieve the specified accuracy. Follow the output connection recommendations of Chapter 2, to keep non-ideal grounds from degrading overall system accuracy.

Input Noise APC341[7]…… 1 LSB rms, Typical.

Note:
7. Reference Test Conditions: Temperature 25°C, 125K conversions/second, using test PC with a 2 meter cable length connection to the field analog input signal.

External Trigger Input/Output

As An Input:…… Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered on the falling edge of this trigger signal. Minimum pulse width 250nano seconds
As An Output:…… Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for typically 500nano seconds

PCI BUS COMPLIANCE

Specification.....	This device meets or exceeds all written PCI Specification Version 2.2.
Electrical/Mechanical Interface.	Short 5V Board
PCI Target	Implemented by Altera FPGA
4K Memory Space Required...	One Base Address Register
PCI commands Supported.....	Configuration Read/Write, Memory Read/Write, 32,16, and 8-bit data transfer types supported.
Signaling.....	5V Compliant, 3.3V Tolerant.
INTA#.....	Interrupt A is used to request an interrupt. Interrupt will occur when the amount of new converted data in the memory buffer exceeds that set by the Memory Threshold register.
Access Times.....	8 PCI Clock Cycles for all non-burst register accesses. Burst read of the 512 sample memory buffer implements three PCI clock cycles for each sample read.

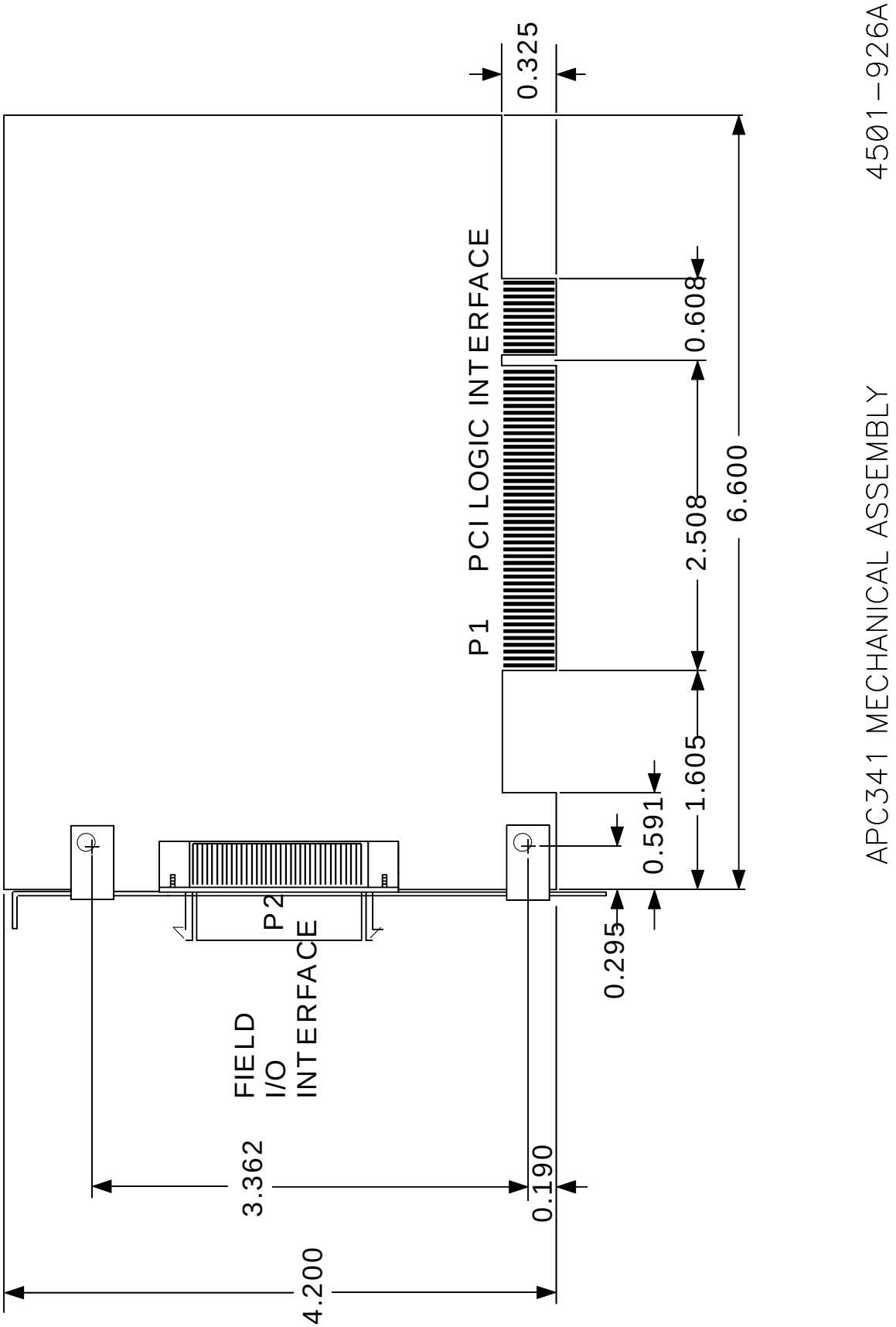
APPENDIX

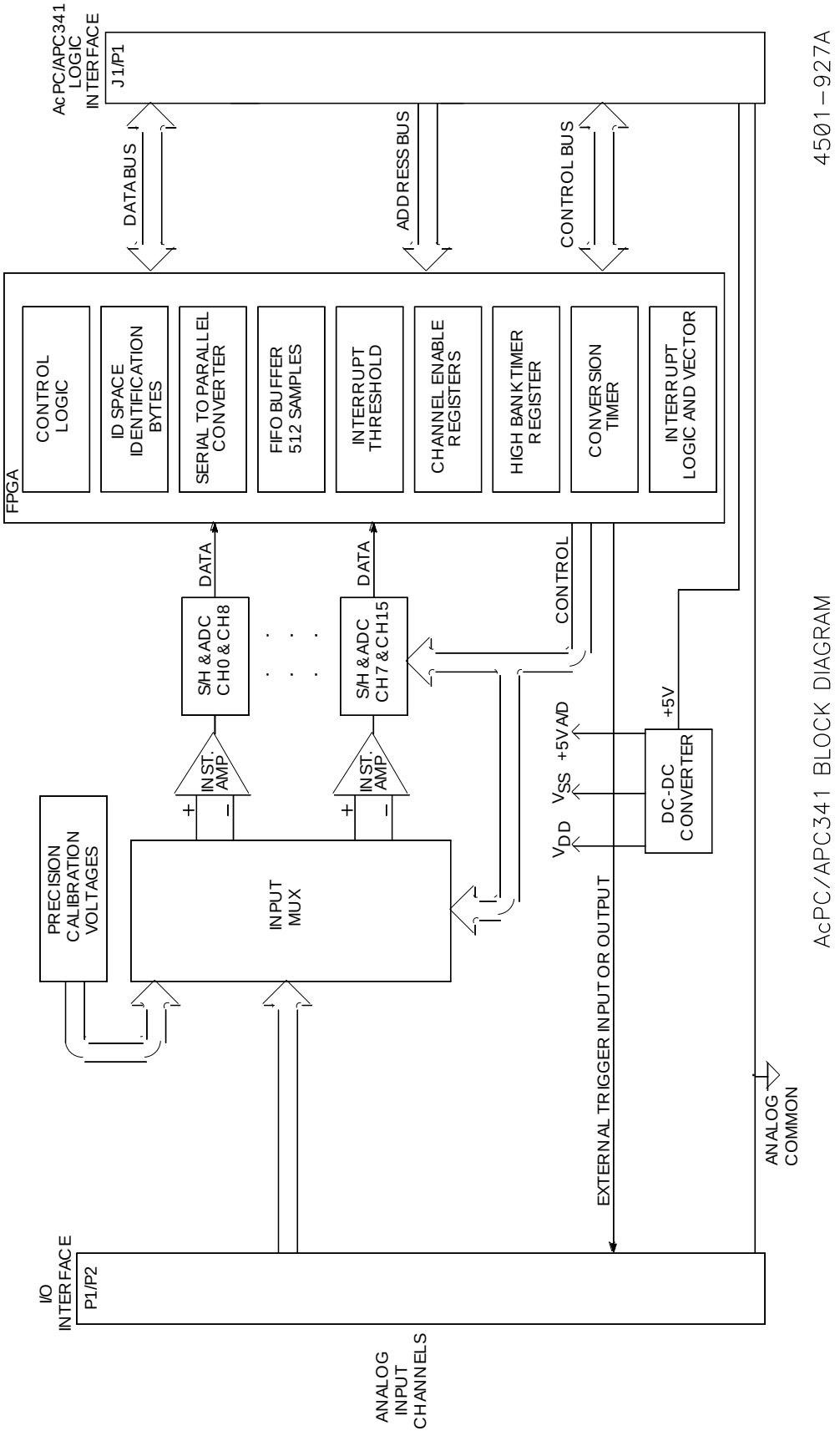
CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

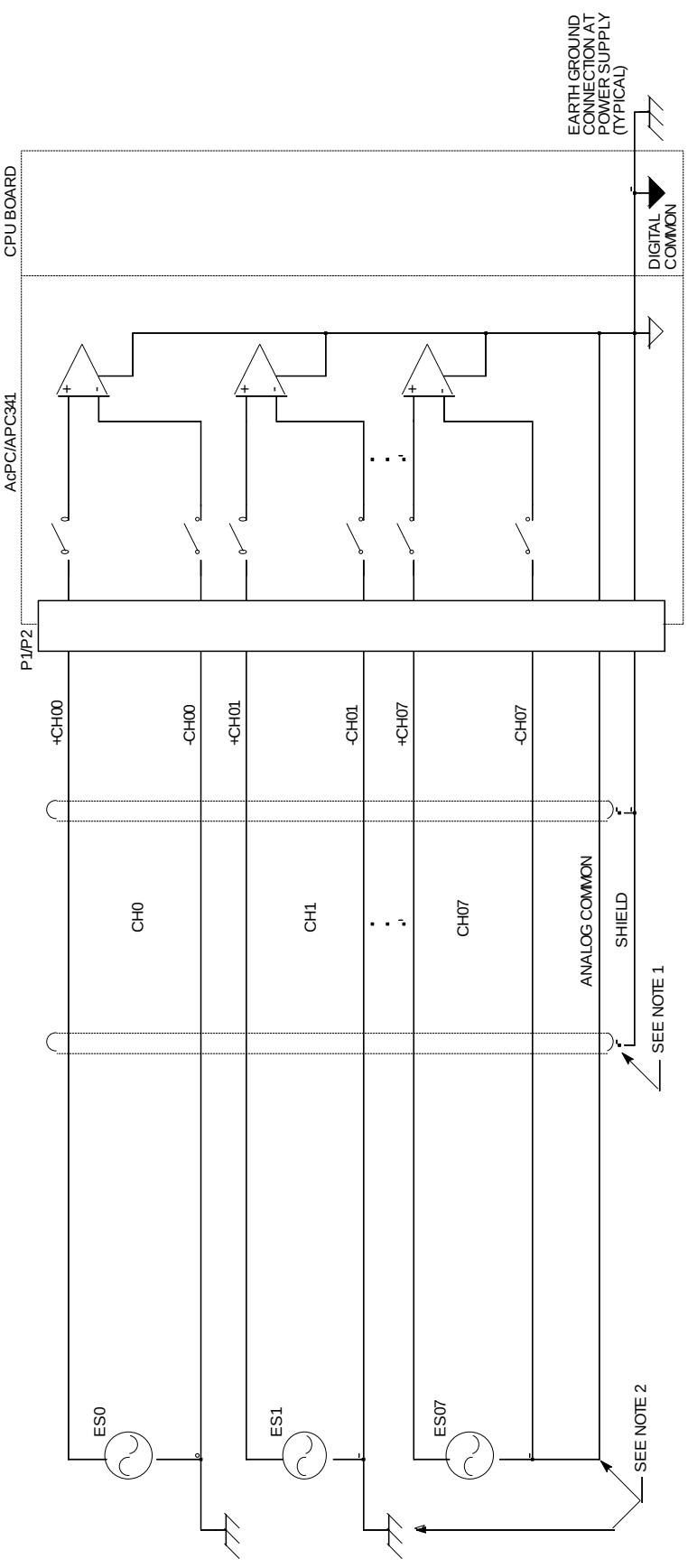
Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the APC341 Module.
Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other lenghts. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a “D Shell” and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.’s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For APC Module Boards
Application: To connect field I/O signals to the APC Module. *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the APC Module (connectors only) via a flat ribbon cable (Model 5025-551-x). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to field I/O (pins 1-50) on the APC board. Each APC board has its own unique pin assignments. Refer to the APC board manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.


4501-926A
APC341 MECHANICAL ASSEMBLY
0.325
P1 PCI LOGIC INTERFACE
0.608
2.508
6.600
1.605
0.591
0.295
P2
FIELD I/O INTERFACE
3.362
0.190
4.200

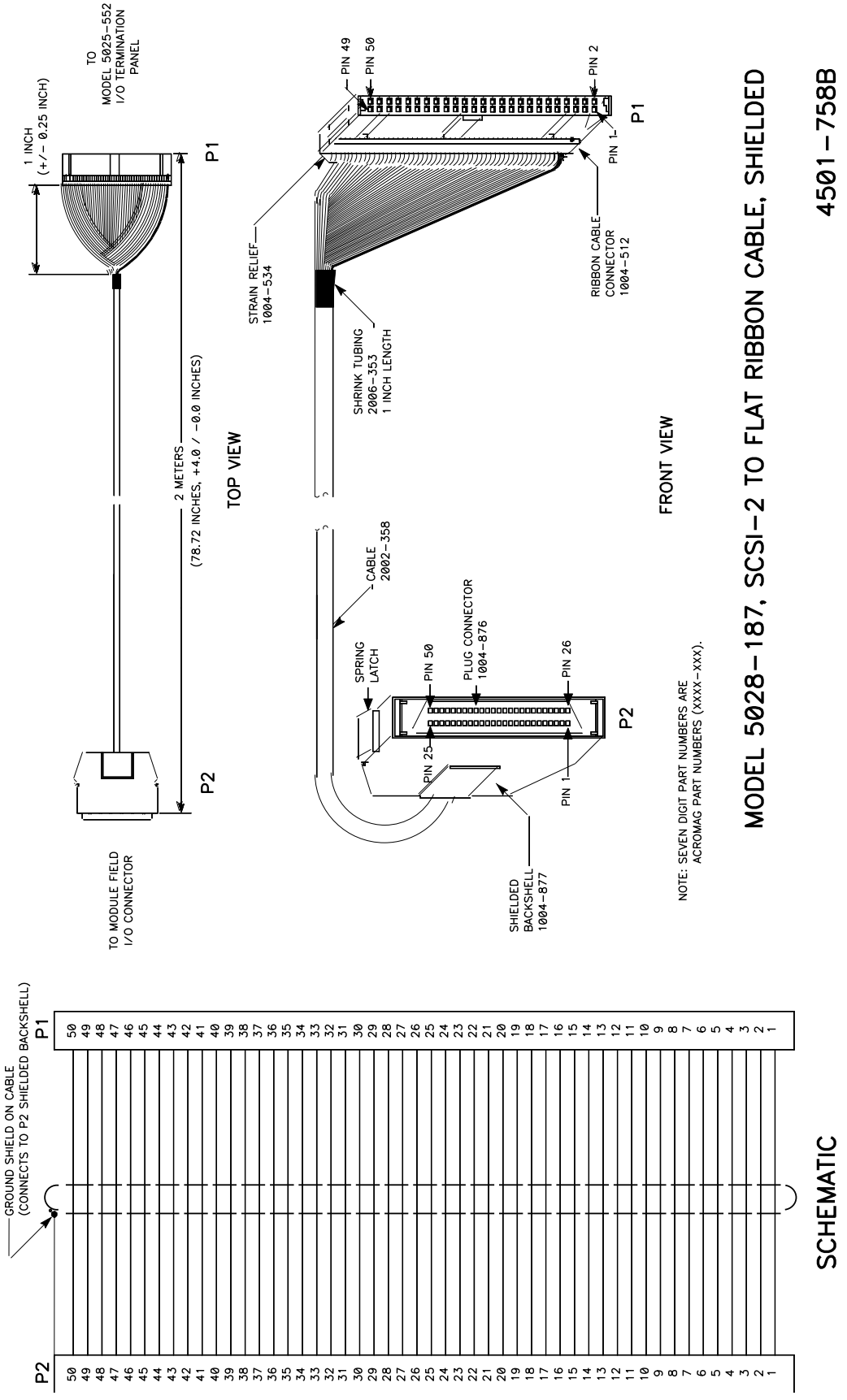

AcPC/APC341
LOGIC
INTERFACE
J1/P1
DATA BUS
ADDRESS BUS
CONTROL BUS
FPGA
CONTROL LOGIC
ID SPACE IDENTIFICATION BYTES
SERIAL TO PARALLEL CONVERTER
FIFO BUFFER 512 SAMPLES
INTERRUPT THRESHOLD
CHANNEL ENABLE REGISTERS
HIGH BANK TIMER REGISTER
CONVERSION TIMER
INTERRUPT LOGIC AND VECTOR
DATA
DATA
CONTROL
S/H & ADC CH0 & CH8
S/H & ADC CH7 & CH15
INST. AMP
INST. AMP
+5V
+5V A/D
VSS
VDD
DC-DC CONVERTER
PRECISION CALIBRATION VOLTAGES
INPUT MUX
EXTERNAL TRIGGER INPUT OR OUTPUT
ANALOG COMMON
I/O
INTERFACE
P1/P2
ANALOG INPUT CHANNELS
4501-927A
AcPC/APC341 BLOCK DIAGRAM

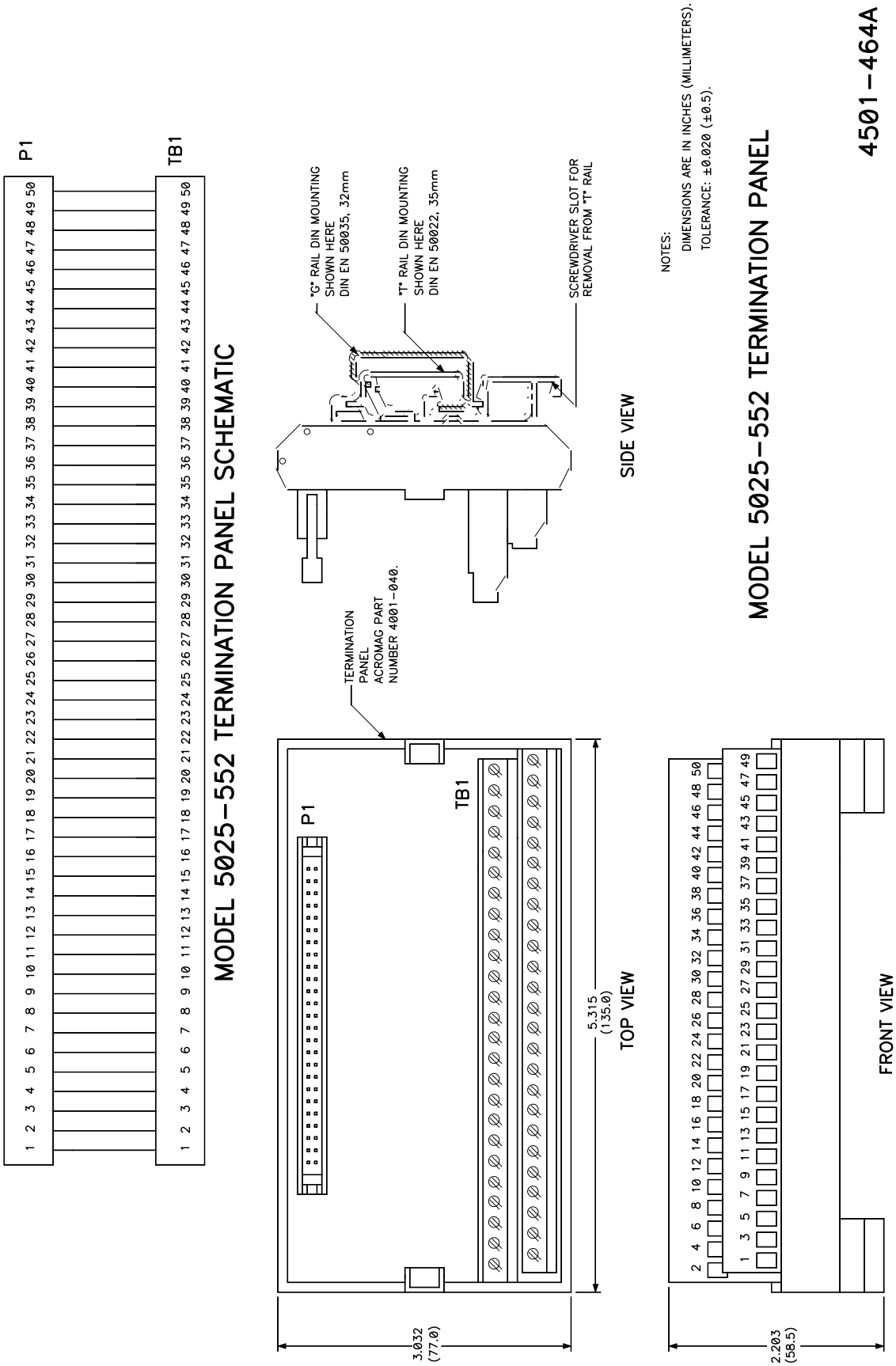


4501-928A

AcPC/APC341 DIFFERENTIAL VOLTAGE INPUT CONNECTION DIAGRAM

NOTES:
1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.


MODEL 5028-187, SCSI-2 TO FLAT RIBBON CABLE, SHIELDED
4501-758B
TOP VIEW
FRONT VIEW
SCHEMATIC
TO MODEL 5025-552 I/O TERMINATION PANEL
1 INCH (+/- 0.25 INCH)
2 METERS (78.72 INCHES, +4.0 / -0.0 INCHES)
TO MODULE FIELD I/O CONNECTOR
P1
P2
PIN 49
PIN 50
PIN 2
PIN 1
STRAIN RELIEF 1004-534
SHRINK TUBING 2006-353 1 INCH LENGTH
RIBBON CABLE CONNECTOR 1004-512
CABLE 2002-358
SPRING LATCH
PIN 50
PLUG CONNECTOR 1004-876
PIN 26
PIN 25
PIN 1
SHIELDED BACKSHELL 1004-877
NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX-XXX).
GROUND SHIELD ON CABLE (CONNECTS TO P2 SHIELDED BACKSHELL)


P1
TB1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
SIDE VIEW
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
5.315 (135.0)
3.032 (77.0)
TOP VIEW
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
MODEL 5025-552 TERMINATION PANEL
4501-464A
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
2.203 (58.5)
FRONT VIEW