SYCARD TECHNOLOGY

PCChost 1420
PCI-CardBus Host Adapter
User's Manual

Preliminary

M200157-00
January 2005

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1.0 Introduction

The PCChost 1420 host adapter is a PCI plug-in board designed evaluate the Texas Instruments PCI1420 PCI-CardBus bridge device. The PCI1420 is the 4th generation of TI's CardBus controllers and offers high performance and low power. The PCChost 1420 has the following features:

- Based on the high performance PCI1420 PCI to CardBus bridge
- ACPI compliant
- Dual sockets support both 16 bit and CardBus cards
- Support for both ISA and PCI interrupts
- LEDs indicate slot power and activity
- Supports Zoomed Video on both slots
- Overcurrent LED informs user of error condition
- TPS2206 Vpp and Vcc switch supports all Vpp and Vcc options
- On-board 12V Vpp supply eliminates problems caused by poorly regulated host power
- Adjustable 3.3V Power supply for voltage margin testing
- On-board speaker
- All PCI1420 signals accessible through test points for easy logic analyzer connection.

1.1 Packing List

The PCChost 1420 package includes the following:

- PCChost 1420 PC Board
- PCChost 1010 ISA Interrupt Board
- 10 pin ribbon cable
- PCI1420 Data Sheet
- PCChost 1420 User's Manual
- Registration Card

1.2 Specifications

Electrical

Supply Voltage: 5V +-5%
Supply Current: TBD

Physical

Width:	5.0"
Length:	8.75"
Thickness:	0.8" Max
Weight:	5.5 oz

1.3 Related Documentation

Sycard Technology's PCMCIA Developer's Guide - Third Edition
Texas Instruments PCI1420 Data Sheet
TPS2206 Data Sheet
The PC Card Specification - Release 7.0

1.4 Technical Support

Technical support for the PCChost 1420 can be obtained directly from Sycard Technology. You may reach Sycard via phone or FAX at the following:

(408) 749-0130
(408) 749-1323 FAX

Commonly asked questions and answers can be found on Sycard's web site at the following URL:

http://www.sycard.com/h1420_qa.html

You may also direct questions, comments, suggestions or any other issues to the following email address:

support@sycard.com

2.0 PCChost 1420 Installation

The PCChost 1420 is designed to work in most Windows 98/ME/2000/XP based systems. The PCChost 1420 package contains the PCChost 1420 PCI-CardBus interface and associated documentation.

2.1 Configuring the Hardware

As shipped from the factory the PCChost 1420 is ready to be installed in a standard PC Architecture machine. The following jumpers are configured at the factory:

Jumper	Setting	Description
JP6	1-2 shorted	Adjustable 3.3V Vcc
JP7	1-2 shorted	ZV Buffer Enable 0
JP7	3-4 open	
JP7	5-6 shorted	Slot 1 Activity LED
JP7	7-8 shorted	IRQSER Signal
JP7	9-10 open	
JP7	11-12 shorted	Slot 0 Activity LED
JP7	13-16 shorted	External EEPROM
JP7	15-14 shorted	External EEPROM

Table 2.1-1 Factory Jumper Settings

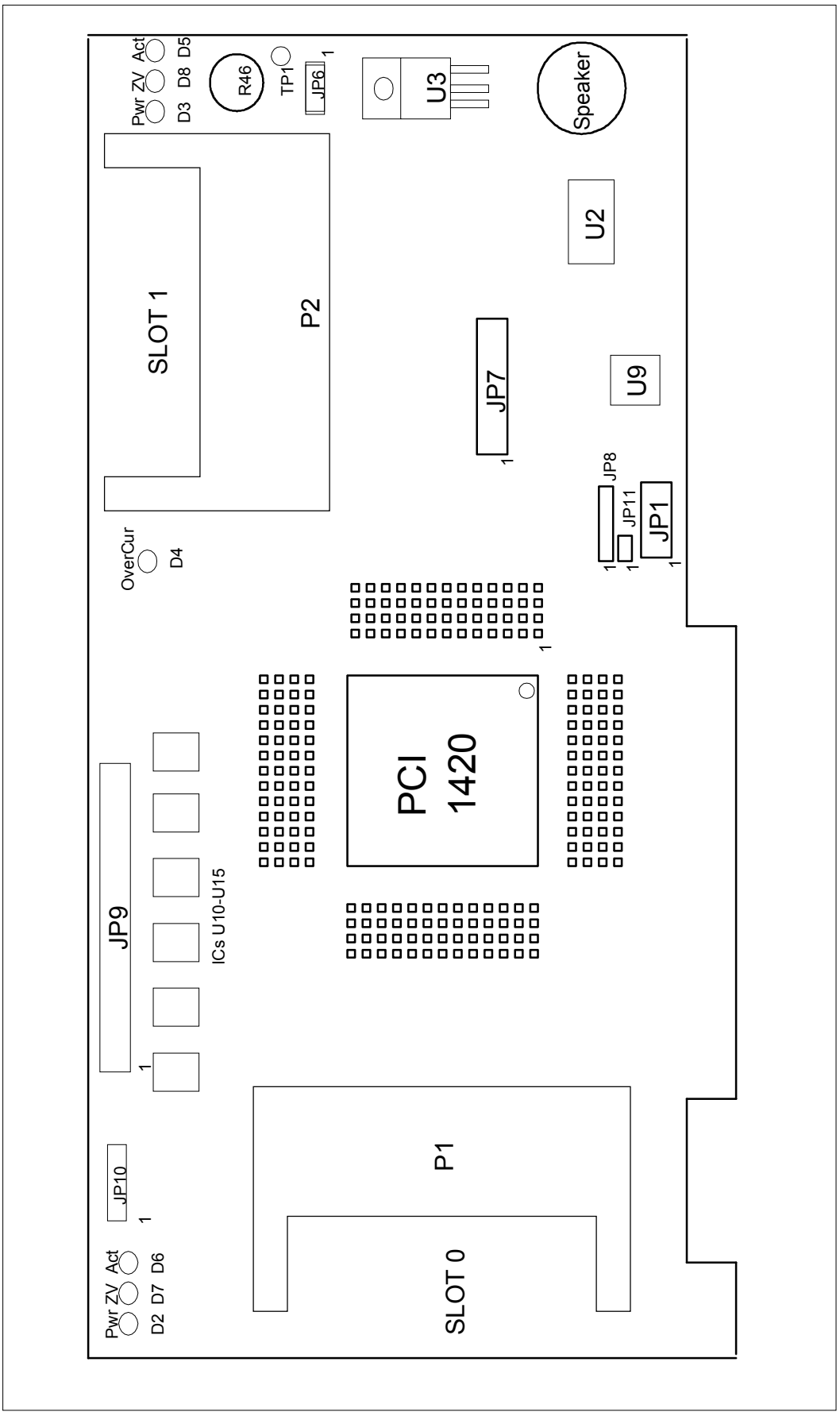
Other jumpers and test points integrated on the board are used to access advanced features. These features are listed in section 3.0 and 4.0.

2.2 Installing the Hardware

The PCChost 1420 can be installed in any available PCI slot. Insure that the bracket is properly fastened to the chassis with a screw or other device. This will prevent the PCChost 1420 from being pulled from the slot when a PC Card is inserted.

2.3 Installing the Software Driver

The on-board EEPROM on the PCChost 1420 will initialize the board for Window 98/ME/2000 and XP. These versions of windows have built-in support for the PCI-1420 chip used on the PCCHost 1420. No other software drivers are required.


Pwr ZV Act
D3 D8 D5
R46
TP1
JP6
1
U3
Speaker
SLOT 1
P2
U2
JP7
U9
JP8
JP11
JP1
OverCur
D4
PCI
1420
JP9
ICs U10-U15
P1
JP10
Pwr ZV Act
D2 D7 D6
SLOT 0

3.0 Using the PCChost 1420

In most applications the PCChost 1420 requires no adjustments or jumper changes. The following sections describe the operation of some of the less frequently used features.

3.1 Adjusting the 3.3V Vcc

A single 3.3V on-board power supply provides power for both PC Card slots. Via jumper JP6, the power supply can be configured for fixed or adjustable operation. In the fixed position (JP6 pins 2-3 shorted), the power supply supplies a fixed 3.3V output. When JP6 pins 1-2 are shorted the 3.3V power supply is adjustable from approximately 3.0 to 3.6 volts to allow for voltage margin testing of a PC Card.

JP6 Position	Description
1-2	Adjustable 3.3V
2-3	Fixed 3.3V

Table 3.1-1 Fixed/Adjustable Vcc Select

***Caution**: Do not change the position of JP6 when power is applied to the PCChost unit. Damage to the PCChost and the host system may occur.*

The trimpot (R46) adjusts the voltage. To adjust the power supply, connect a voltmeter between the 3.3V test point at TP1 and ground. Remove any installed PC Cards from the slot. Apply power to the board and adjust the trimpot until the desired voltage is obtained.

***Note**: The trimpot only adjusts the 3.3V power to the PC Card slots. Another fixed 3.3V regulator powers the PCI1420 core functions.*

***Note**: 5V power to the PC Card slots is derived directly from the PCI Vcc rails. No adjustments to the 5V slot voltage is possible.*

3.2 Zoomed Video connection

Zoomed Video PC Cards output digital video signals compatible with ZV ports of many video controllers. The Zoomed Video signals are shared with the 16-bit PC Card signals. Buffers on the PCChost 1420 board isolate the card slots from the ZV connectors at JP9 and JP10. The buffers allow the ZV signals from either slot to be routed to the JP9 and JP10. JP9 is a 40 pin connector that contains the ZV digital video signals. JP10 contains the I^2S stereo audio signal. Pinouts of these connectors can be found on the schematics in Appendix C.

4.0 Hardware Description

This section will describe the major operational blocks that make up the PCChost 1420. Additional details can be found in the TI PCI1420 datasheet included in the documentation package.

4.1 PCI-1420 PCI to CardBus Bridge

The heart of the PCChost 1420 is Texas Instruments PCI1420 PCI to CardBus bridge. The PCI1420 chips directly connect to the PCI bus and PC Card slots to provides a true-single chip CardBus host implementation. A full detailed description of the PCI1420 can be found in the accompanying PCI1420 data sheet. The PCChost 1420 provides 0.1" spaced headers for accessing all PCI1420 signal pins. These pins can be probed by an oscilloscope or connected directly to a logic analyzer for system debug. A pin map for this header is shown in appendix A.

4.2 Power Supply and Power Distribution

The PCChost 1420 contains eight separate power planes. They are as follows:

- 5 Volt PCI power supply
- 3.3 Volt PCI1420 "core" power supply
- Adjustable 3.3 Volt card power supply
- 12 Volt programming voltage power supply (Vpp)
- Slot A Vcc supply
- Slot B Vcc supply
- Slot A Vpp supply
- Slot B Vpp supply

The following diagram illustrates the connection of the various power planes.

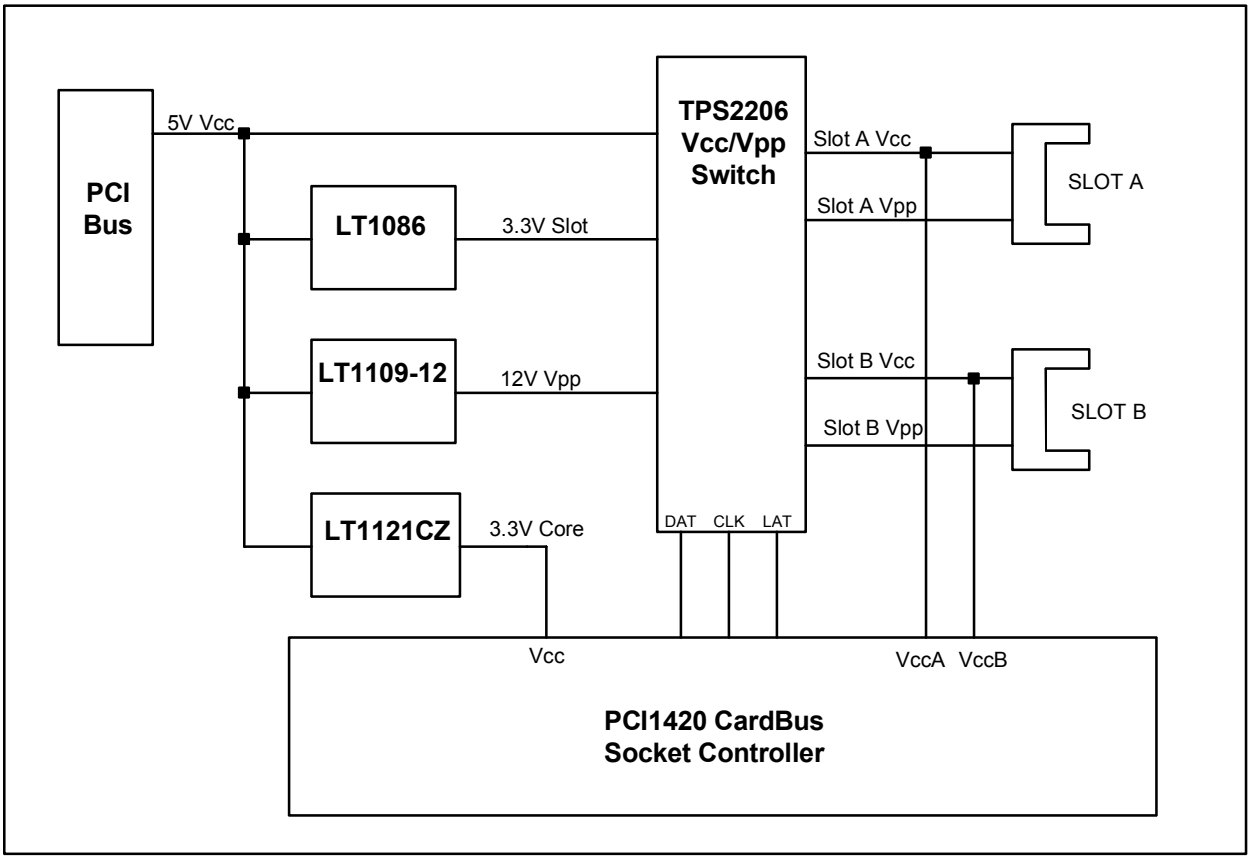


Figure 4.2-1 PCChost 1420 power distribution

4.2.1 3.3 Volt PC Card Slot Power Supply

The 3.3V card slot power supply is responsible for supplying power to both PC Card slots. The 3.3V power supply is based on a Linear Technology LT1086 low dropout adjustable regulator. Input to the LT1086 is the PCI 5V supply. The output voltage is determined by a resistor divider across the output pins of the device. The PCChost 1420 includes a jumper (JP6) to select a fixed 3.3V output or an adjustable 3.3V supply capable of supplying 3.0V to 3.6V. 3.3V PC Card slot power is connected to the TPS2206 Vcc/Vpp switch.

4.2.2 3.3 Volt PCI1420 "Core" Power Supply

The 3.3V PCI1420 "core" power supply provides power for the core portion of the PCI1420. The core power supply is separately regulated by a LT1121CZ-3.3 fixed 3.3V regulator. The input to the LT1121CZ is the PCI 5V supply. The output connects directly to the PCI1420 core Vcc pins.

4.2.3 12 Volt Power Supply

A Linear Technology LT1109-12 Vpp generator chip and associated circuitry provide 12 volt power for the Vpp1 and Vpp2 pins on each PC card slot. The input to the LT1109-12 is from the host system 5.0V Vcc. The output connects directly to the TPS2206 Vcc/Vpp switch.

4.2.4 Vcc/Vpp switch

Slot Vcc and Vpp are controlled by the PCI1420 via a external power switch chip. The PCChost 1420 takes advantage of a single chip power switching chip specifically designed for the PC Card environment, the Texas Instruments TPS2206. The TPS2206 supports Vcc and Vpp switching for two PC Card slots and provides over-current protection. The control interface to the TPS2206 is via a three wire serial connection to the PCI1420.

4.2.5 LED Indicators

Three power indicators display the current slot power status and any overcurrent situation on either slot. Green LEDs adjacent to each slot indicate the present slot power status. A single red LED at D4 labeled "OVC" indicates an overcurrent situation on either socket A RED LED indicates socket activity and a YELLOW led indicates Zoomed Video status.

4.3 Interrupt Deserializer

Because of pin limitations on the PCI1420, interrupts are converted to a serial bitstream and converted to parallel interrupt in an external chip. This chip, the PCI950, is located at U9. Figure 4.3-1 illustrates the connections between the PCI1420 and the PCI950. The PCI950 converts the serial bitstream into the ISA and PCI style interrupts.

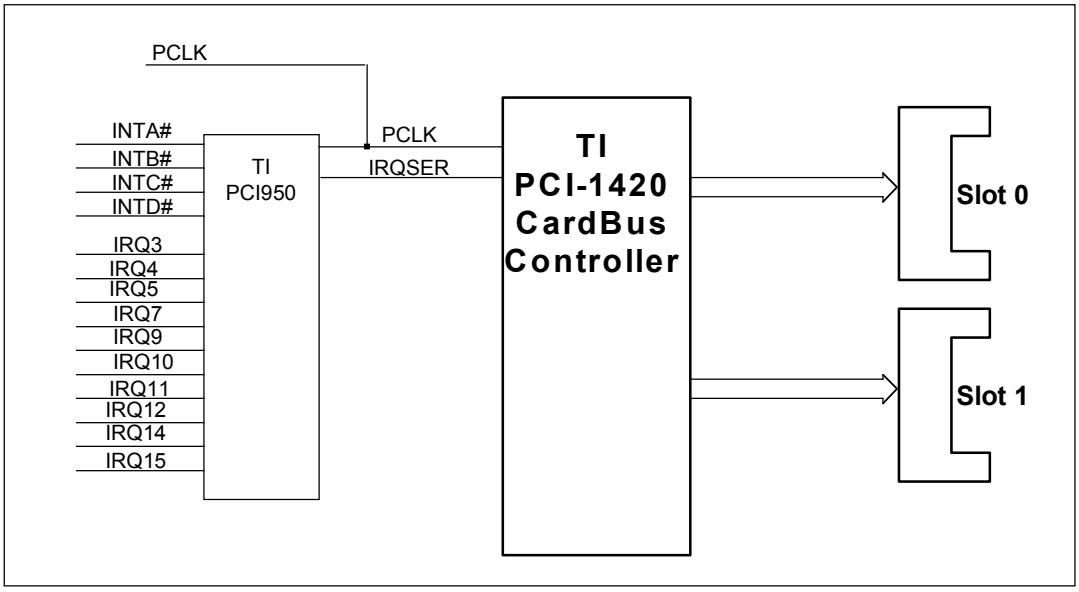


Figure 4.3-1 PCI950 Interrupt Deserializer

The PCI interrupts are routed directly to the corresponding pins on the PCI connector. Since ISA interrupts are not available on the PCI connector, these must be routed through a 10-pin ribbon cable to a plug-in ISA interrupt board. See Figure 4.3-2. Since most new motherboards do not support ISA slots all later Microsoft operating systems configure the CardBus controller to route 16-bit ISA interrupts to the PCI interrupt mechanism.

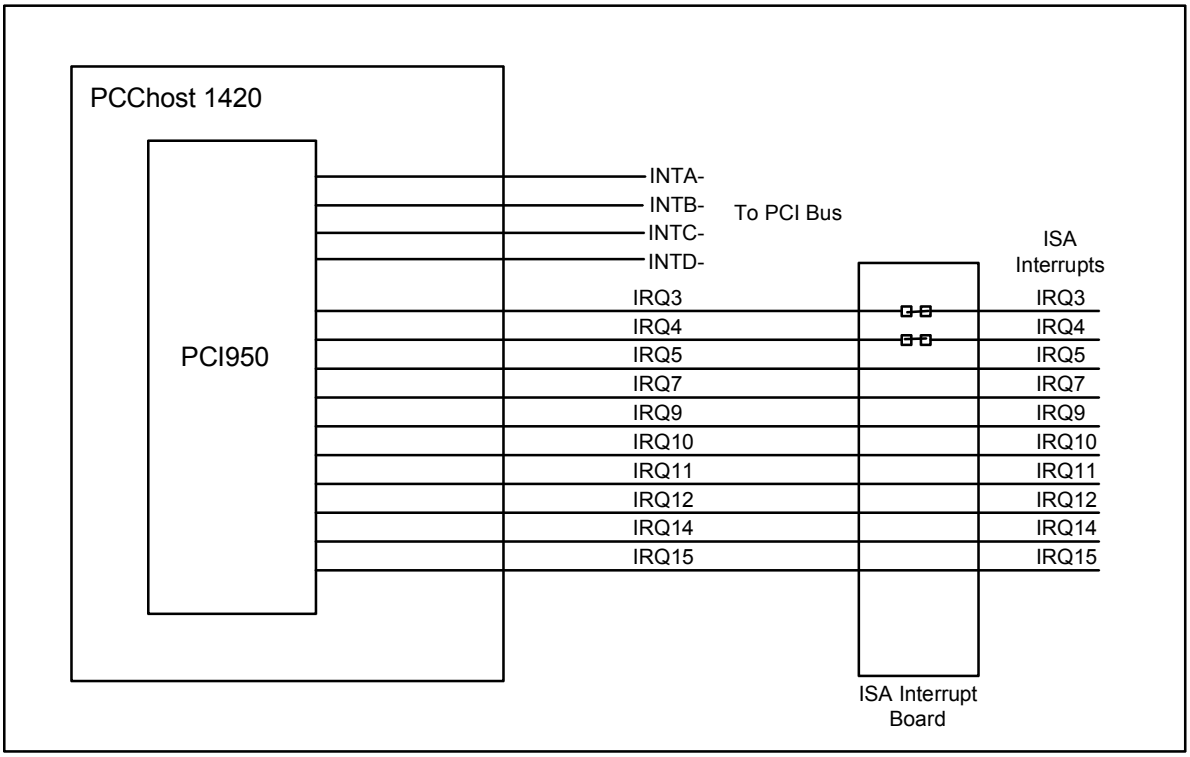
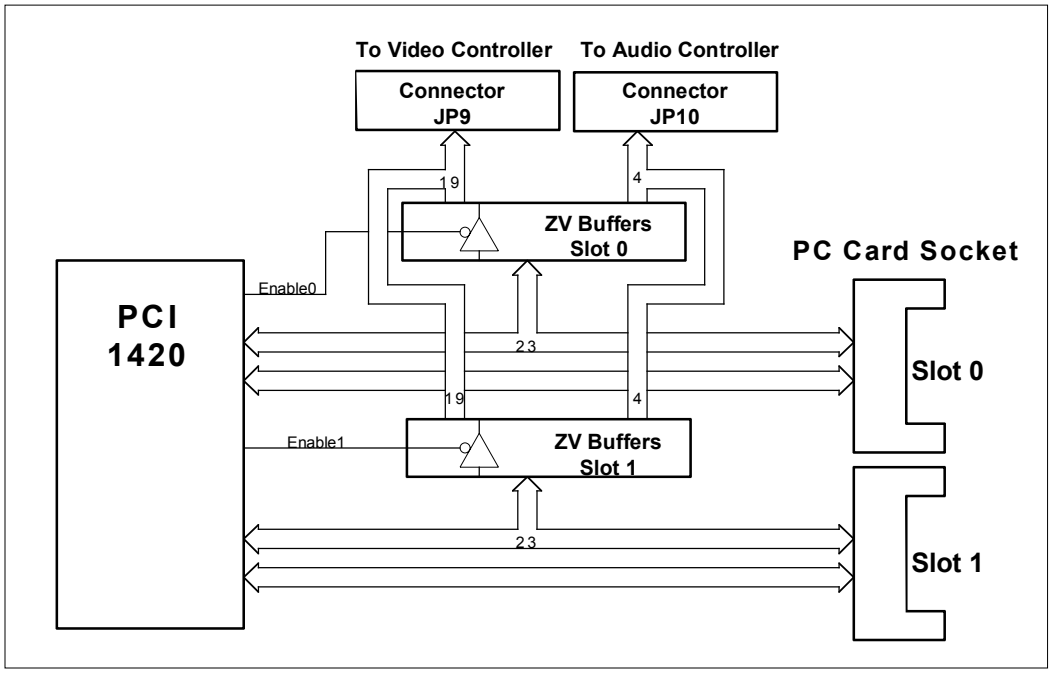


Figure 4.3-2 ISA Interrupt Routing

4.4 Zoomed Video Buffers

In order to isolate the PC Card slot from potentially long traces to the Zoomed video capable video controller the PCChost 1420 implements Zoomed Video buffers. These buffers, implemented with several 74VHC245, are implemented on both slots. The buffers are controlled via programmable I/O pins on the PCI1420. See section 4.6 for information on how the buffers are controlled.



4.5 Speaker Driver

An on-board speaker and driver is connected to the SPKROUT pin of the PCI1420. The speaker driver is designed to support the audio digital waveform output from a PC Card.

4.6 Programmable I/O Pins

The PCI-1420 incorporates a number of programmable I/O pins. These pins can be configured through software for various control functions. On power-up these pins are programmed by the external EEPROM. In order to use these pins for other function, software must program certain registers in the PCI1420. The PCChost 1420 uses the pins for the following:

- Serial Interrupt connection to the PCI950 interrupt deserializer
- Zoomed Video Buffer Control
- Activity LEDs
- EEPROM configuration

These programmable I/O pins (MFUNC[6:0]) must be configured prior to loading the operating system drivers. In notebook computers and other systems with integrated CardBus controllers, this is typically handled in the ROM BIOS. However, in a plug-in board environment, the BIOS usually will not know about the presence of the CardBus controller. Although there may be O/S level drivers, they know how to handle the core functions of the PCI1420 chip but don't know how the programmable I/O pins need to be configured. The EEPROM on the PCChost 1420 will setup the PCI1420's programmable I/O for use with the various versions of Windows. Other O/S and non-PC platforms may need to initialize these registers in another way. The following table lists the functions used for each multifunction pin and the register setting in PCI Configuration spaced used to enable that pin.

Pin	Name	Access Point	PCChost 1420 Function	PCI Config Register	Setting
154	MFUNC0	JP7-1	ZV Buffer Enable 0	8CH	Bits [3:0] = 0111
155	MFUNC1	JP7-3	EEPROM Clock	8CH	Bits [7:4] = 0000
157	MFUNC2	JP7-5	Slot 1 Activity LED	8DH	Bits [3:0] = 1101
158	MFUNC3	JP7-7	IRQSER Signal	8DH	Bits [7:4] = 0001
159	MFUNC4	JP7-9	EEPROM Data	8EH	Bits [3:0] = 0000
160	MFUNC5	JP7-11	Slot 0 Activity LED	8EH	Bits [7:4] = 1100
161	MFUNC6	JP8-3	Not Used - Tied to JP8-3	8FH	Bits [3:0] = 0000

Table 4.6-1 Multifunction Pin Assignments

***Note**: The configuration described in table 4.6-1 is configured by the on-board EEPROM on power-up.*

4.7 Configuration EEPROM

The PCChost 1420 uses a serial configuration EEPROM (24C01) that is used to initialize certain PCI configuration registers on power-up. These PCI configuration registers are used to configure the 7 multi-function I/O pins and setup default values in certain control registers. Table 4.7-1 describes the settings made by the PCChost 1420's EEPROM. See page 34 of the PCI-1420 manual for more information on the serial EEPROM feature.

ROM Offset	Value	Register Description	Setting
00	0x01	Reference 1	
01	0x00	Sub-System Identification (byte 3)	Do not set Sub-system ID
02	0x00	Sub-System Identification (byte 2)	
03	0x00	Sub-System Identification (byte 1)	
04	0x00	Sub-System Identification (byte 0)	
05	0x00	Reserved	
06	0x00	Reserved	
07	0x00	Reserved	
08	0x02	Reference 2	
09	0x08	System Control (3)	Enable P2C clock for Power control switch (TPS-2206)
0a	0x44	System Control (2)	Set system control byte 2 to default
0b	0x90	System Control (1)	Set system control byte 1 to default
0c	0x60	System Control (0)	Set system control byte 0 to default
0d	0x00	Reserved	
0e	0x00	Reserved	
0f	0x00	Reserved	
10	0x03	Reference 3	
11	0x00	Multifunction Routing (byte 3)	Set MFUNC6 to input
12	0xc0	Multifunction Routing (byte 2)	Set MFUNC5 to Socket 0 Activity LED Set MFUNC4 to input
13	0x1d	Multifunction Routing (byte 1)	Set MFUNC3 to IRQSER Set MFUNC2 to Socket 1 Activity LED
14	0x07	Multifunction Routing (byte 0)	Set MFUNC1 to input Set MFUNC0 to Zoomed Video Buffer enable
15	0x00	Reserved	
16	0x00	Reserved	
17	0x00	Reserved	
18	0x04	Reference 4	
19	0x61	PCI-1420 Diagnostic Register	Set diagnostic register to default values
1a	0x66	PCI-1420 Device Control Register	Set device control register to default values
1b	0x00	PCI-1420 Card Control Register	Set card control register to default values
1c	0xc0	PCI-1420 Retry Status Register	Set retry status register to default values
1d	0x00	Reserved	
1e	0x00	Reserved	
1f	0x00	Reserved	
20	0xff	EOL	

Table 4.7-1 PCChost 1420 EEPROM Contents

5.0 PCChost 1420 Manual Setup

This section will describe a step-by-step manual configuration process for setting up the PCChost 1420 for operation. This information is intended for the user that is writing software to directly access the registers of the PCI1420 chip.

Find the socket controller - The first setup in configuring the CardBus controller to locate the specific controller using the PCI BIOS. By using the manufacturer and device ID, the PCI BIOS will return the PCI bus, function and device ID. Each CardBus slot will be controlled by a different PCI function.

Configuring programmable I/O pins, power control and interrupts - The PCChost 1420 uses the programmable pin definitions in table 4.6.1. These controls are located in PCI configuration space.

Configure the PCI bus numbers - There are three PCI bus registers that must be programmed. The PCI bus number located at offset 18H in the controller's PCI configuration space is programmed with the bus number that the controller is connected. The CardBus bus number located at offset 19H is programmed with the bus number of the CardBus bus. Each function (slot) has separate register. The Subordinate bus number is programmed with the highest numbered bus below the CardBus bus. Each function (slot) has separate register.

Set the latency timers - There are two latency timer, one for the PCI interface and one for the CardBus bus.

Enable the CardBus socket registers - The next step is to assign memory space resources for the CardBus socket registers. These registers provide socket status and control power to the slot. The memory location of the CardBus socket registers is controlled by registers 10-13H in the socket controller's PCI configuration space. Each socket has its own set of CardBus socket registers.

Enable PCI memory, I/O and master accesses - In order to access the CardBus socket registers, PCI memory accesses must be enabled through the socket controller's PCI command register.

Configure the Socket Registers - Once configured, the next step is to setup the socket controller registers. The socket controller registers show the slot status and control the power-on status.

Determine if a CardBus card is plugged in - Bits in the Present State Register will show if the card is inserted, the card type and what voltage is supported. The bits in the Present State Register are determined by a state machine that tests the Voltage Sense (VS[2:1]) and the Card Detect (#CD[2:1]) when a card insertion is detected. If the bits in the Present State Register show that an invalid card has been inserted, software may request that the state machine re-interrogate the card type. This is accomplished by setting the CVSTEST bit in the Socket Force Event Register.

If the CardBus card is detected, then power may be applied - Power is controlled through the Socket Control Register at offset 10H in CardBus socket register memory space. Wait until the PWRCYCLE bit in the Socket Present State Register is set.

Reset the card - The reset bit is located in the socket controller's Bridge Control Register located at offset 3EH in PCI configuration space. Allows an appropriate delay for the card to perform its reset sequence before performing any other accesses.

Verify the correct card is inserted - The CardBus card's PCI ID may be read using the PCI configuration read BIOS mechanism.

Configure the Card's memory and I/O windows - Enable memory and I/O windows through the PCI configuration space.

Enable memory and/or I/O accesses - Enable memory and I/O accesses through the card's PCI Command register.

At this point, the card specific hardware may be accessed.

Appendix A

PCChost 1420 Header Pinout

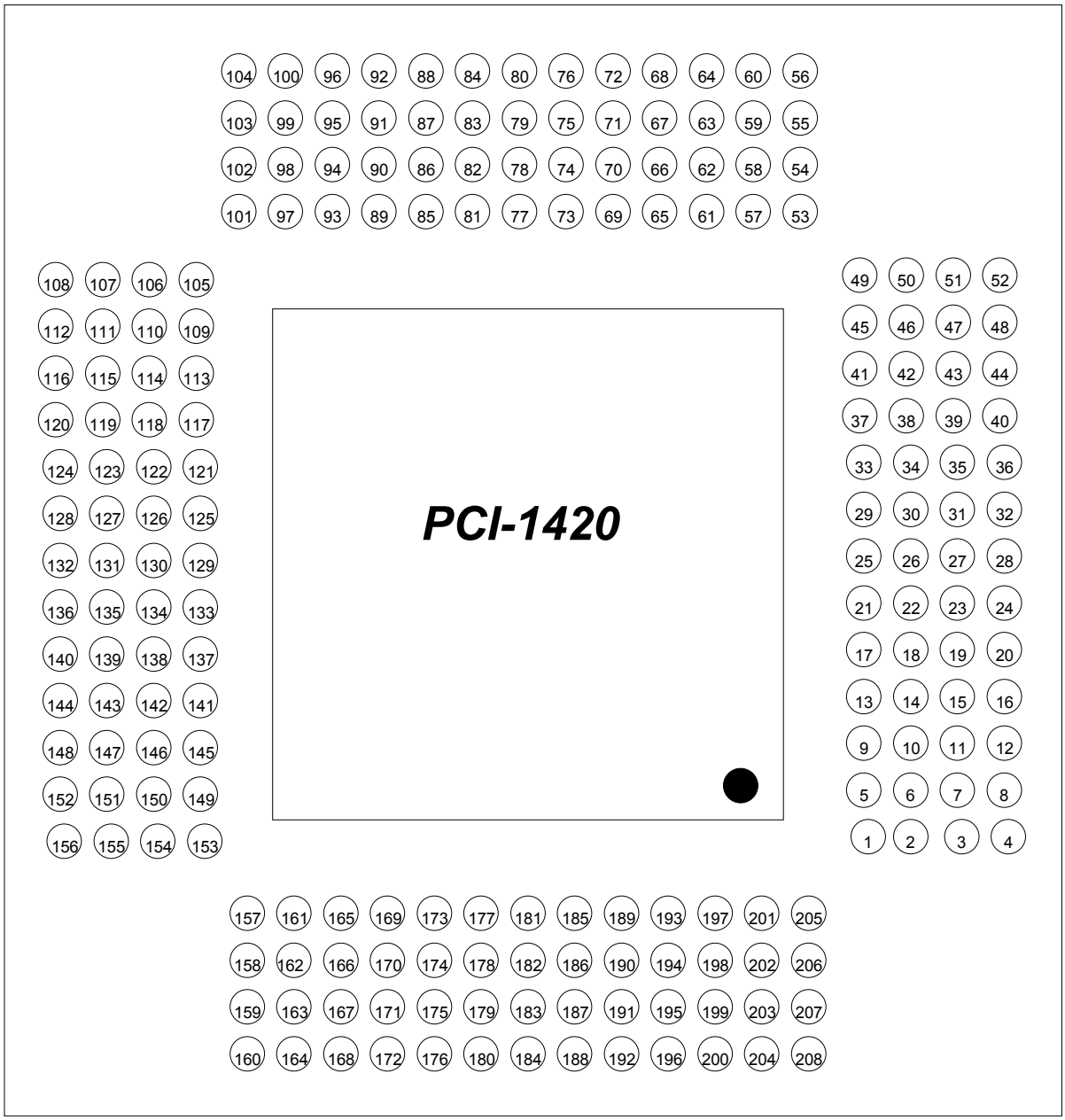


Figure A-1 PCChost 1420 Header

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
1	VccP	53	B_CAD17	105	A_RSVD	157	MFUNC2
2	AD10	54	B_CAD18	106	A_CPAR	158	MFUNC3
3	AD9	55	B_CAD19	107	A_CBLOCK#	159	MFUNC4
4	AD8	56	B_CVS2	108	A_CPERR#	160	MFUNC5
5	C/BE0#	57	B_CAD20	109	A_CSTOP#	161	MFUNC6
6	AD7	58	B_CRST#	110	A_CGNT#	162	C/BE3#
7	V_{CC}	59	B_CAD21	111	A_CDEVSEL#	163	RI_OUT#/PME#
8	AD6	60	B_CAD22	112	A_CCLK	164	V_{CC}
9	AD5	61	B_CREQ#	113	V_{CC}	165	AD25
10	AD4	62	B_CAD23	114	A_CTRDY#	166	PRST#
11	AD3	63	B_CC/BE3#	115	A_CIRDY#	167	GND
12	AD2	64	V_{CC}	116	A_CFRAME#	168	GNT#
13	GND	65	B_CAD24	117	A_CC/BE2#	169	REQ#
14	AD1	66	B_CAD25	118	A_CAD17	170	AD31
15	AD0	67	B_CAD26	119	A_CAD18	171	AD30
16	B_CCD1#	68	B_CVS1	120	V_{CCA}	172	AD11
17	B_CAD0	69	B_CINT	121	A_CAD19	173	AD29
18	B_CAD2	70	B_CSERR#	122	A_CVS2	174	AD28
19	B_CAD1	71	B_CAUDIO	123	A_CAD20	175	GRST#
20	B_CAD4	72	B_CSTSCHG	124	A_CRST#	176	AD27
21	B_CAD3	73	B_CCLKRUN#	125	A_CAD21	177	AD26
22	GND	74	B_CCD2#	126	A_CAD22	178	VCC_P
23	B_CAD6	75	GND	127	A_CREQ#	179	AD24
24	B_CAD5	76	B_CAD27	128	A_CAD23	180	PCLK
25	B_RSVD	77	B_CAD28	129	GND	181	GND
26	B_CAD7	78	B_CAD29	130	A_CC/BE3#	182	IDSEL
27	B_CAD8	79	B_CAD30	131	A_CAD24	183	AD23
28	B_CC/BE0#	80	B_RSVD	132	A_CAD25	184	AD22
29	B_CAD9	81	B_CAD31	133	A_CAD26	185	AD21
30	B_CAD10	82	A_CCD1#	134	A_CVS1	186	AD20
31	V_{CC}	83	A_CAD0	135	A_CINT#	187	V_{CC}
32	B_CAD11	84	A_CAD2	136	A_CSERR#	188	AD19
33	B_CAD13	85	A_CAD1	137	A_CAUDIO	189	AD18
34	B_CAD12	86	V_{CC}	138	A_CSTSCHG	190	AD17
35	B_CAD15	87	A_CAD4	139	A_CCLKRUN#	191	AD16
36	B_CAD14	88	A_CAD3	140	A_CCD2#	192	C/BE2#
37	B_CAD16	89	A_CAD6	141	A_CAD27	193	FRAME#
38	V_{CCB}	90	A_CAD5	142	A_CAD28	194	GND
39	B_CC/BE1#	91	A_RSVD	143	V_{CC}	195	IRDY#
40	B_RSVD	92	A_CAD7	144	A_CAD29	196	TRDY#
41	B_CPAR	93	A_CAD8	145	A_CAD30	197	DEVSEL#
42	B_CBLOCK#	94	A_CC/BE0#	146	A_RSVD	198	STOP#
43	B_CPERR#	95	A_CAD9	147	A_CAD31	199	PERR#
44	GND	96	GND	148	V_{CCI}	200	SERR#
45	B_CSTOP#	97	A_CAD10	149	SPKROUT#	201	V_{CC}
46	B_CGNT#	98	A_CAD11	150	LATCH	202	PAR
47	B_CDEVSEL#	99	A_CAD13	151	CLOCK	203	C/BE1#
48	B_CCLK	100	A_CAD12	152	DATA	204	AD15
49	B_CTRDY#	101	A_CAD15	153	GND	205	AD14
50	B_CIRDY#	102	A_CAD14	154	MFUNC0	206	AD13
51	B_CFRAME	103	A_CAD16	155	MFUNC1	207	GND
52	B_CC/BE2#	104	A_CC/BE1#	156	SUSPEND#	208	AD12

Table A-1 CardBus PC Card Signal Names Sorted by Terminal Number

Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name	No.
A_CAD0	83	A_CSTOP#	109	B_CAD12	34	CLOCK	151
A_CAD1	85	A_CSTSCHG#	138	B_CAD13	33	DATA	152
A_CAD2	84	A_CTRDY#	114	B_CAD14	36	DEVSEL#	197
A_CAD3	88	A_CVS1	134	B_CAD15	35	FRAME#	193
A_CAD4	87	A_CVS2	122	B_CAD16	37	GND	13
A_CAD5	90	A_RSVD	91	B_CAD17	53	GND	22
A_CAD6	89	A_RSVD	105	B_CAD18	54	GND	44
A_CAD7	92	A_RSVD	146	B_CAD19	55	GND	75
A_CAD8	93	AD0	15	B_CAD20	57	GND	96
A_CAD9	95	AD1	14	B_CAD21	59	GND	129
A_CAD10	97	AD2	12	B_CAD22	60	GND	153
A_CAD11	98	AD3	11	B_CAD23	62	GND	167
A_CAD12	100	AD4	10	B_CAD24	65	GND	181
A_CAD13	99	AD5	9	B_CAD25	66	GND	194
A_CAD14	102	AD6	8	B_CAD26	67	GND	207
A_CAD15	101	AD7	6	B_CAD27	76	GNT#	168
A_CAD16	103	AD8	4	B_CAD28	77	IDSEL	182
A_CAD17	118	AD9	3	B_CAD29	78	IRDY#	195
A_CAD18	119	AD10	2	B_CAD30	79	LATCH	150
A_CAD19	121	AD11	172	B_CAD31	81	MFUNC0	154
A_CAD20	123	AD12	208	B_CAUDIO	71	MFUNC1	155
A_CAD21	125	AD13	206	B_CBLOCK#	42	MFUNC2	157
A_CAD22	126	AD14	205	B_CC/BE0#	28	MFUNC3	158
A_CAD23	128	AD15	204	B_CC/BE1#	39	MFUNC4	159
A_CAD24	131	AD16	191	B_CC/BE2#	52	MFUNC5	160
A_CAD25	132	AD17	190	B_CC/BE3#	63	MFUNC6	161
A_CAD26	133	AD18	189	B_CCD1#	16	PAR	202
A_CAD27	141	AD19	188	B_CCD2#	74	PCLK	180
A_CAD28	142	AD20	186	B_CCLK	48	PERR#	199
A_CAD29	144	AD21	185	B_CCLKRUN#	73	PRST#	166
A_CAD30	145	AD22	184	B_CDEVSEL#	47	REQ#	169
A_CAD31	147	AD23	183	B_CFRAME#	51	RI_OUT#/PME#	163
A_CAUDIO	137	AD24	179	B_CGNT#	46	SERR#	200
A_CBLOCK#	107	AD25	165	B_CINT#	69	SPKROUT	149
A_CC/BE0#	94	AD26	177	B_CIRDY#	50	STOP#	198
A_CC/BE1#	104	AD27	176	B_CPAR	41	SUSPEND#	156
A_CC/BE2#	117	AD28	174	B_CPERR#	43	TRDY#	196
A_CC/BE3#	130	AD29	173	B_CREQ#	61	Vcc	7
A_CCD1#	82	AD30	171	B_CRST#	58	V_{CC}	31
A_CCD2#	140	AD31	170	B_CSERR#	70	V_{CC}	64
A_CCLK	112	B_CAD0	17	B_CSTOP#	45	V_{CC}	86
A_CCLKRUN#	139	B_CAD1	19	B_CSTSCHG#	72	V_{CC}	113
A_CDEVSEL#	111	B_CAD2	18	B_CTRDY#	49	V_{CC}	143
A_CFRAME#	116	B_CAD3	21	B_CVS1	68	V_{CC}	164
A_CGNT#	110	B_CAD4	20	B_CVS2	56	GRST	175
A_CINT#	135	B_CAD5	24	B_RSVD	25	V_{CC}	187
A_CIRDY#	115	B_CAD6	23	B_RSVD	40	V_{CC}	201
A_CPAR	106	B_CAD7	26	B_RSVD	80	V_{CCA}	120
A_CPERR#	108	B_CAD8	27	C/BE0#	5	V_{CCB}	38
A_CREQ#	127	B_CAD9	29	C/BE1#	203	Vccl	148
A_CRST#	124	B_CAD10	30	C/BE2#	192	V_{CCP}	1
A_CSERR#	136	B_CAD11	32	C/BE3#	162	V_{CCP}	178

Table A-2 CardBus PC Card Signal Names Sorted Alphabetically

No.	Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name
1	V_{CCP}	53	B_A24	105	A_A18	157	MFUNC2
2	AD10	54	B_A7	106	A_A13	158	MFUNC3
3	AD9	55	B_A25	107	A_A19	159	MFUNC4
4	AD8	56	B_VS2#	108	A_A14	160	MFUNC5
5	C/BE0#	57	B_A6	109	A_A20	161	MFUNC6
6	AD7	58	B_RESET	110	A_WE#	162	C/BE3#
7	V_{CC}	59	B_A5	111	A_A21	163	RI_OUT#/PME#
8	AD6	60	B_A4	112	A_A16	164	V_{CC}
9	AD5	61	B_INPACK	113	V_{CC}	165	AD25
10	AD4	62	B_A3	114	A_A22	166	PRST#
11	AD3	63	B_REG#	115	A_A15	167	GND
12	AD2	64	V_{CC}	116	A_A23	168	GNT#
13	GND	65	B_A2	117	A_A12	169	REQ#
14	AD1	66	B_A1	118	A_A24	170	AD31
15	AD0	67	B_A0	119	A_A7	171	AD30
16	B_CD1#	68	B_VS1#	120	V_{CCA}	172	AD11
17	B_D3	69	B_READY(IREQ#)	121	A_A25	173	AD29
18	B_D11	70	B_WAIT#	122	A_VS2#	174	AD28
19	B_D4	71	B_BVD2(SPKR#)	123	A_A6	175	V_{CC}
20	B_D12	72	B_BVD1(STSCHG/RI#)	124	A_RESET	176	AD27
21	B_D5	73	B_WP(IOIS16#)	125	A_A5	177	AD26
22	GND	74	B_CD2#	126	A_A4	178	V_{CCP}
23	B_D13	75	GND	127	A_INPACK	179	AD24
24	B_D6	76	B_D0	128	A_A3	180	PCLK
25	B_D14	77	B_D8	129	GND	181	GND
26	B_D7	78	B_D1	130	A_REG#	182	IDSEL
27	B_D15	79	B_D9	131	A_A2	183	AD23
28	B_CE1#	80	B_D2	132	A_A1	184	AD22
29	B_A10	81	B_D10	133	A_A0	185	AD21
30	B_CE2#	82	A_CD1#	134	A_VS1#	186	AD20
31	V_{CC}	83	A_D3	135	A_READY(IREQ#)	187	V_{CC}
32	B_OE#	84	A_D11	136	A_WAIT#	188	AD19
33	B_IORD#	85	A_D4	137	A_BVD2(SPKR#)	189	AD18
34	B_A11	86	V_{CC}	138	A_BVD1(STSCHG/RI#)	190	AD17
35	B_IOWR#	87	A_D12	139	A_WP(IOIS16#)	191	AD16
36	B_A9	88	A_D5	140	A_CD2#	192	C/BE2#
37	B_A17	89	A_D13	141	A_D0	193	FRAME#
38	V_{CCB}	90	A_D6	142	A_D8	194	GND
39	B_A8	91	A_D14	143	V_{CC}	195	IRDY#
40	B_A18	92	A_D7	144	A_D1	196	TRDY#
41	B_A13	93	A_D15	145	A_D9	197	DEVSEL#
42	B_A19	94	A_CE1#	146	A_D2	198	STOP#
43	B_A14	95	A_A10	147	A_D10	199	PERR#
44	GND	96	GND	148	V_{CCI}	200	SERR#
45	B_A20	97	A_CE2#	149	SPKROUT#	201	V_{CC}
46	B_WE#	98	A_OE#	150	LATCH	202	PAR
47	B_A21	99	A_IORD#	151	CLOCK	203	C/BE1#
48	B_A16	100	A_A11	152	DATA	204	AD15
49	B_A22	101	A_IOWR#	153	GND	205	AD14
50	B_A15	102	A_A9	154	MFUNC0	206	AD13
51	B_A23	103	A_A17	155	MFUNC1	207	GND
52	B_A12	104	A_A8	156	SUSPEND#	208	AD12

Table A-3 16-bit PC Card Signal Names Sorted by Terminal Number

Signal Name	No.	Signal Name	No.	Signal Name	No.	Signal Name	No.
A_A0	133	A_READY(IREQ#)	135	B_A12	52	CLOCK	151
A_A1	132	A_REG#	130	B_A13	41	DATA	152
A_A2	131	A_RESET	124	B_A14	43	DEVSEL#	197
A_A3	128	A_VS1#	134	B_A15	50	FRAME#	193
A_A4	126	A_VS2#	122	B_A16	48	GND	13
A_A5	125	A_WAIT#	136	B_A17	37	GND	22
A_A6	123	A_WE#	110	B_A18	40	GND	44
A_A7	119	A_WP(IOIS16#)	139	B_A19	42	GND	75
A_A8	104	AD0	15	B_A20	45	GND	96
A_A9	102	AD1	14	B_A21	47	GND	129
A_A10	95	AD2	12	B_A22	49	GND	153
A_A11	100	AD3	11	B_A23	51	GND	167
A_A12	117	AD4	10	B_A24	53	GND	181
A_A13	106	AD5	9	B_A25	55	GND	194
A_A14	108	AD6	8	B_BVD1(STSCHG/RI#)	72	GND	207
A_A15	115	AD7	6	B_BVD2(SPKR#)	71	GNT#	168
A_A16	112	AD8	4	B_CD1#	16	IDSEL	182
A_A17	103	AD9	3	B_CD2#	74	IRDY#	195
A_A18	105	AD10	2	B_CE1#	28	LATCH	150
A_A19	107	AD11	172	B_CE2#	30	MFUNC0	154
A_A20	109	AD12	208	B_D0	76	MFUNC1	155
A_A21	111	AD13	206	B_D1	78	MFUNC2	157
A_A22	114	AD14	205	B_D2	80	MFUNC3	158
A_A23	116	AD15	204	B_D3	17	MFUNC4	159
A_A24	118	AD16	191	B_D4	19	MFUNC5	160
A_A25	121	AD17	190	B_D5	21	MFUNC6	161
A_BVD1(STSCHG/RI#)	138	AD18	189	B_D6	24	PAR	202
A_BVD2(SPKR#)	137	AD19	188	B_D7	26	PCLK	180
A_CD1#	82	AD20	186	B_D8	77	PERR#	199
A_CD2#	140	AD21	185	B_D9	79	PRST#	166
A_CE1#	94	AD22	184	B_D10	81	REQ#	169
A_CE2#	97	AD23	183	B_D11	18	RI_OUT#/PME#	163
A_D0	141	AD24	179	B_D12	20	SERR#	200
A_D1	144	AD25	165	B_D13	23	SPKROUT	149
A_D2	146	AD26	177	B_D14	25	STOP#	198
A_D3	83	AD27	176	B_D15	27	SUSPEND#	156
A_D4	85	AD28	174	B_INPACK	61	TRDY#	196
A_D5	88	AD29	173	B_IORD#	33	Vcc	7
A_D6	90	AD30	171	B_IOWR#	35	V_{CC}	31
A_D7	92	AD31	170	B_OE#	32	V_{CC}	64
A_D8	142	B_A0	67	B_READY(IREQ#)	69	V_{CC}	86
A_D9	145	B_A1	66	B_REG#	63	V_{CC}	113
A_D10	147	B_A2	65	B_RESET	58	V_{CC}	143
A_D11	84	B_A3	62	B_VS1#	68	V_{CC}	164
A_D12	87	B_A4	60	B_VS2#	56	GRST	175
A_D13	89	B_A5	59	B_WAIT#	70	V_{CC}	187
A_D14	91	B_A6	57	B_WE#	46	V_{CC}	201
A_D15	93	B_A7	54	B_WP(IOIS16#)	73	V_{CCA}	120
A_INPACK	127	B_A8	39	C/BE0#	5	V_{CCB}	38
A_IORD#	99	B_A9	36	C/BE1#	203	V_{CCI}	148
A_IOWR#	101	B_A10	29	C/BE2#	192	V_{CCP}	1
A_OE#	98	B_A11	34	C/BE3#	162	V_{CCP}	178

Table A-4 16-bit PC Card Signal Names Sorted Alphabetically

Appendix B

68 Pin PC Card Socket

Zoomed Video	16-Bit	CardBus			CardBus	16-Bit	Zoomed Video
GND	GND	GND	35	1	GND	GND	GND
CD#1	CD1#	CCD1#	36	2	CAD0	D3	D3
D11	D11	CAD2	37	3	CAD14	D4	D4
D12	D12	CAD4	38	4	CAD3	D5	D5
D13	D13	CAD6	39	5	CAD5	D6	D6
D14	D14	RFU	40	6	CAD7	D7	D7
D15	D15	CAD8	41	7	CC/BE0#	CE1#	CE#1
CE#2	CE2#	CAD10	42	8	CAD9	A10	HREF
VS1#	VS1#	CVS1	43	9	CAD11	OE#	OE#
RSVD	RSVD	CAD13	44	10	CAD12	A11	VSYNC
RSVD	RSVD	CAD15	45	11	CAD14	A9	Y0
Y1	A17	CAD16	46	12	CC/BE1#	A8	Y2
Y3	A18	RFU	47	13	CPAR	A13	Y4
Y5	A19	CBLOCK#	48	14	CPERR#	A14	Y6
Y7	A20	CSTOP#	49	15	CGNT#	WE#	WE#
UV0	A21	CDEVSEL#	50	16	CINT#	READY	READY
Vcc	Vcc	Vcc	51	17	Vcc	Vcc	Vcc
Vpp2	Vpp2	Vpp2	52	18	Vpp1	Vpp1	Vpp1
UV1	A22	CTRDY#	53	19	CCLK	A16	UV2
UV3	A23	CFRAME#	54	20	CIRDY#	A15	UV4
UV5	A24	CAD17	55	21	CC/BE2#	A12	UV6
UV7	A25	CAD19	56	22	CAD18	A7	SCLK
VS2#	VS2#	CVS2	57	23	CAD20	A6	MCLK
RESET	RESET	CRST	58	24	CAD21	A5	RSVD
WAIT#	WAIT#	CSERR#	59	25	CAD22	A4	RSVD
LRCLK	RSVD	CREQ#	60	26	CAD23	A3	A[3::0]
REG#	REG#	CC/BE3#	61	27	CAD24	A2	A[3::0]
SDATA	BVD2	CAUDIO#	62	28	CAD25	A1	A[3::0]
BVD1	BVD1	CSTSCHG	63	29	CAD26	A0	A[3::0]
D8	D8	CAD28	64	30	CAD27	D0	D0
D9	D9	CAD30	65	31	CAD29	D1	D1
D10	D10	CAD31	66	32	RFU	D2	D2
CD2#	CD2#	CCD2#	67	33	CCLKRUN#	WP	PCLK
GND	GND	GND	68	34	GND	GND	GND

Figure C-1 PC Card Socket Pinouts Host Socket's View

Appendix C

Schematics

Page 1 - PCI 1420 Chip

Page 2 - PCI Bus Interface, Zoomed Video connectors, and ISA Interrupt connector.

Page 3 - Slot A interface and zoomed video buffers

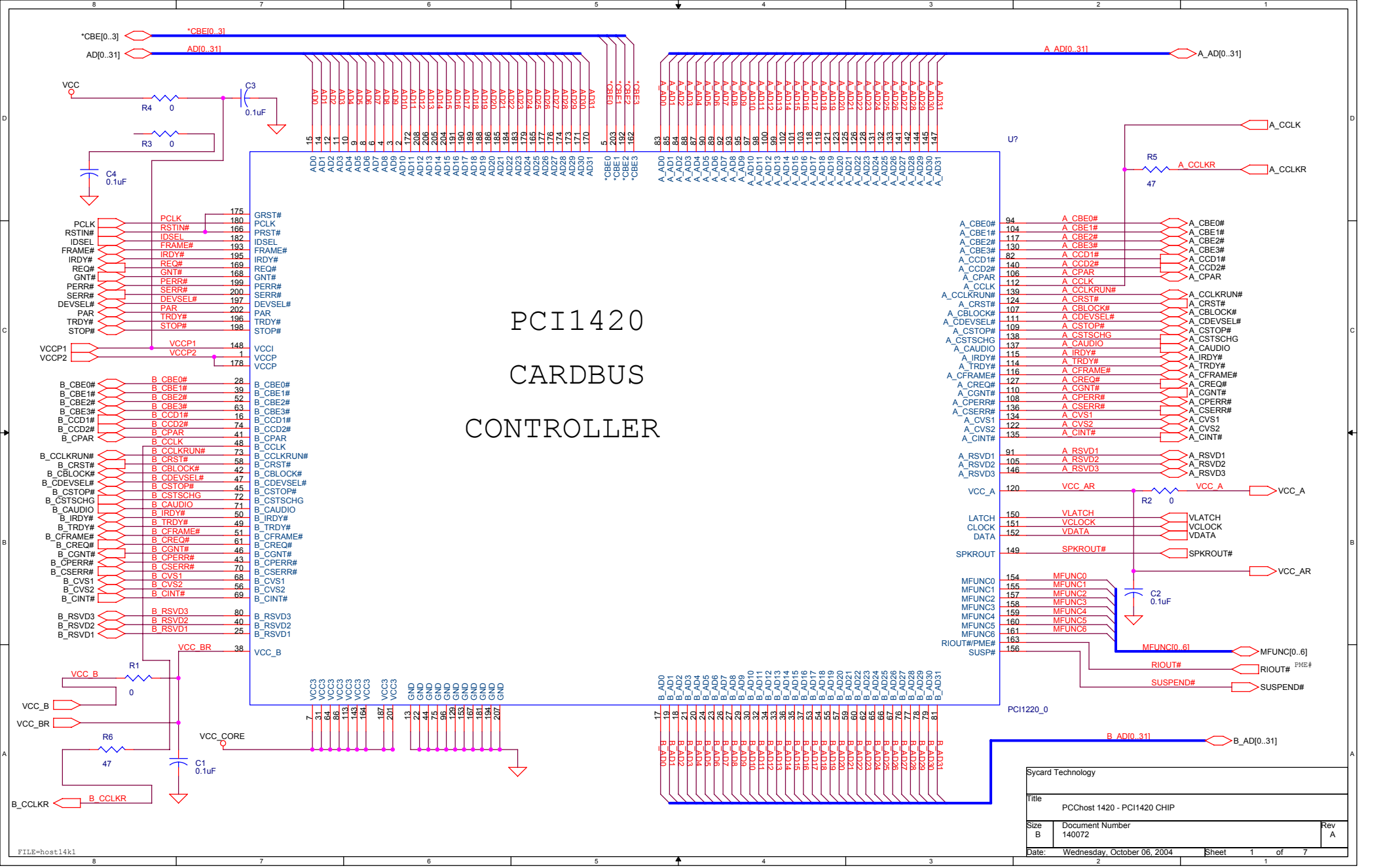
Page 4 - Slot B interface and zoomed video buffers

Page 5 - Power Supply, power routing logic and speaker driver

Page 6 - PCI 1420 Header

Page 7 - IRQ Deserializer and multifunction pin select

Page 8 - PCChost 1010 ISA IRQ interrupt board


PCI1420
CARDBUS
CONTROLLER
U?
PCI1220_0
*CBE[0..3]
AD[0..31]
A_AD[0..31]
B_AD[0..31]
VCC
VCC_A
VCC_B
VCC_BR
VCC_AR
VCC_CORE
B_CCLKR
A_CCLK
A_CCLKR
R1
R2
R3
R4
R5
R6
C1
C2
C3
C4
0.1uF
47
0
MFUNC[0..6]
RIOUT#
SUSPEND#
SPKROUT#
VLATCH
VCLOCK
VDATA
Sycard Technology
PCChost 1420 - PCI1420 CHIP
Document Number
140072
Rev
A
Size
B
Date:
Wednesday, October 06, 2004
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1
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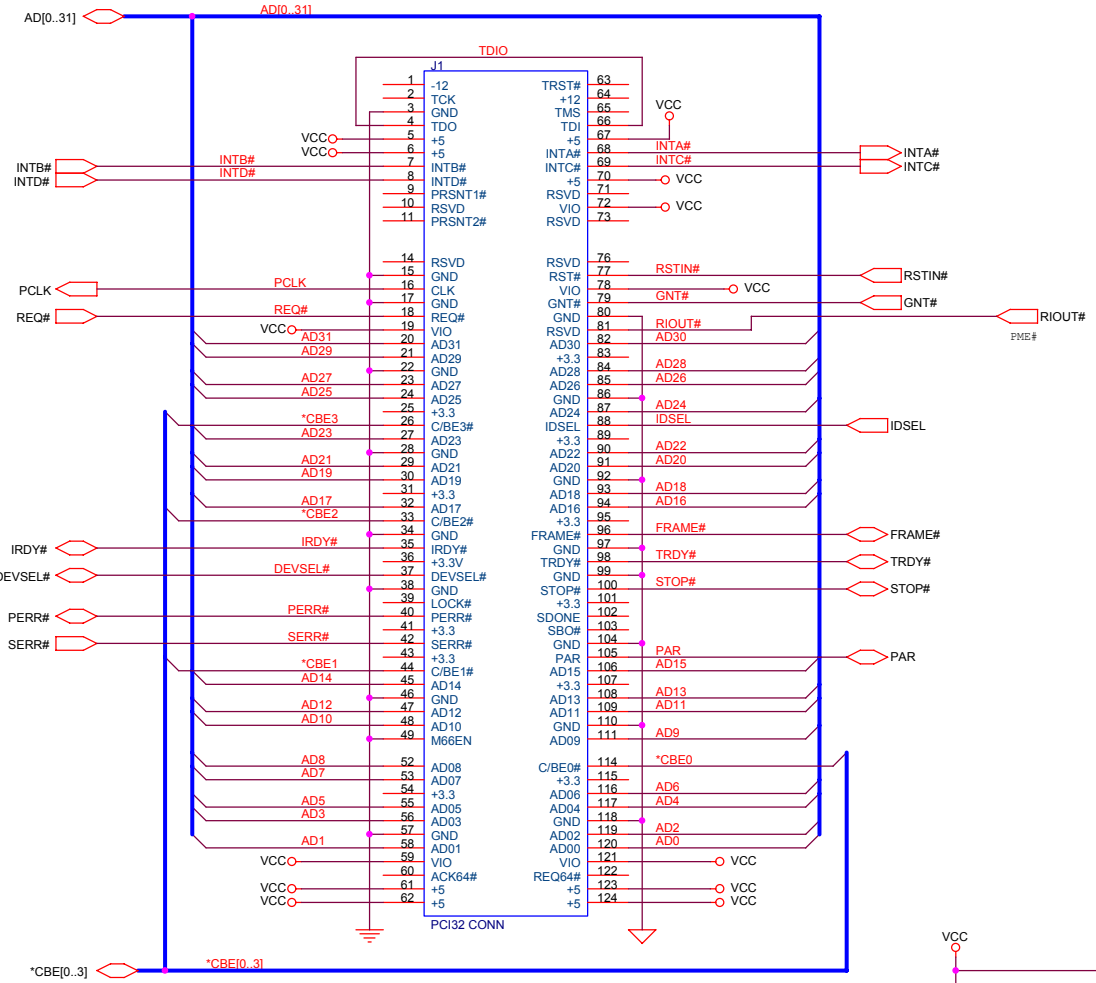
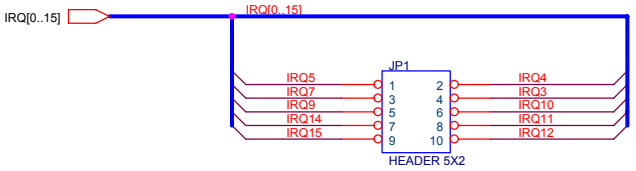
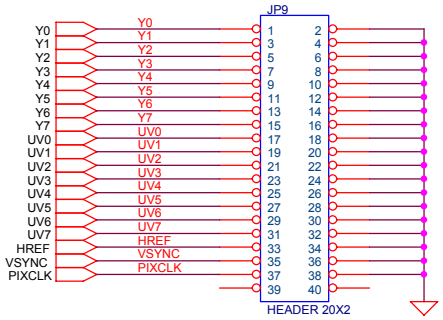
FILE=host14k1



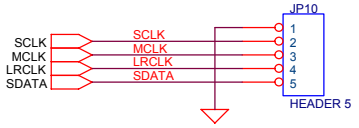
PCI BUS



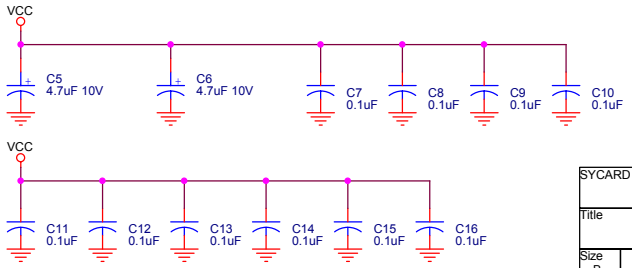
ISA INTERRUPT CONNECTOR



ZOOMED VIDEO CONNECTOR

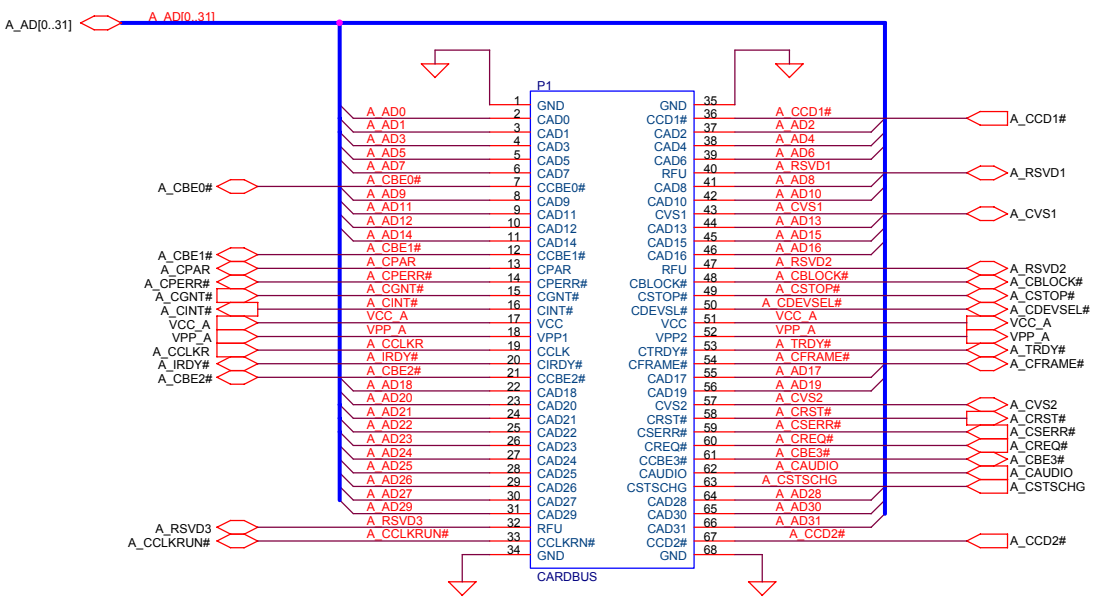


ZOOMED VIDEO AUDIO CONNECTOR

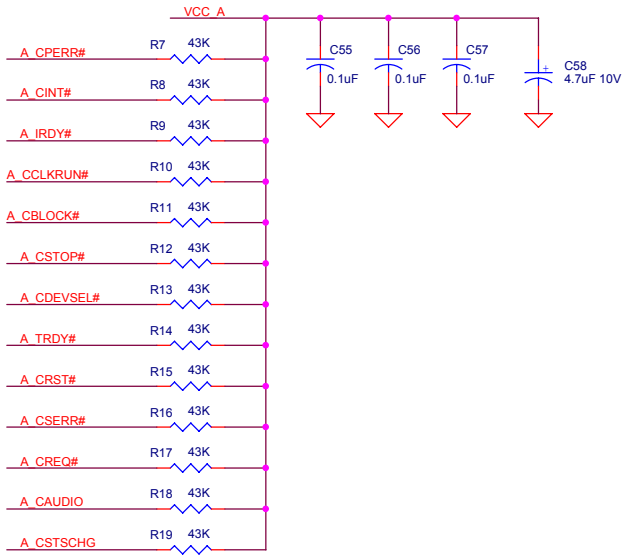


SYCARD TECHNOLOGY		
Title: PCCHOST 1420 - PCI Interface		
Size: B	Document Number: 140072	Rev: A
Date: Wednesday, October 06, 2004	Sheet 2 of 7	

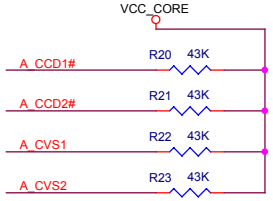
FILE=HOST14K2

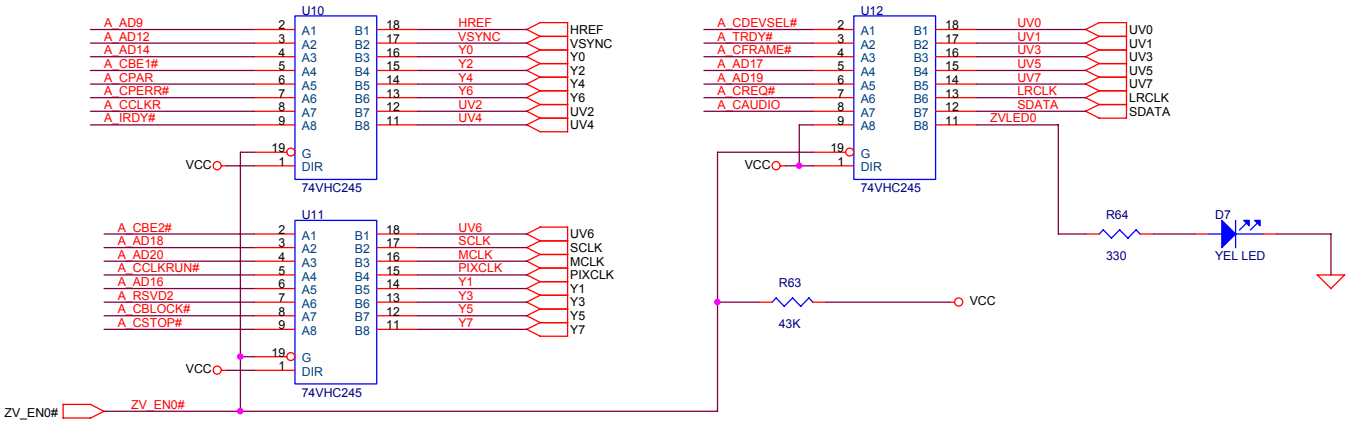


Pullups to Card VCC



Pullups to System 3.3V

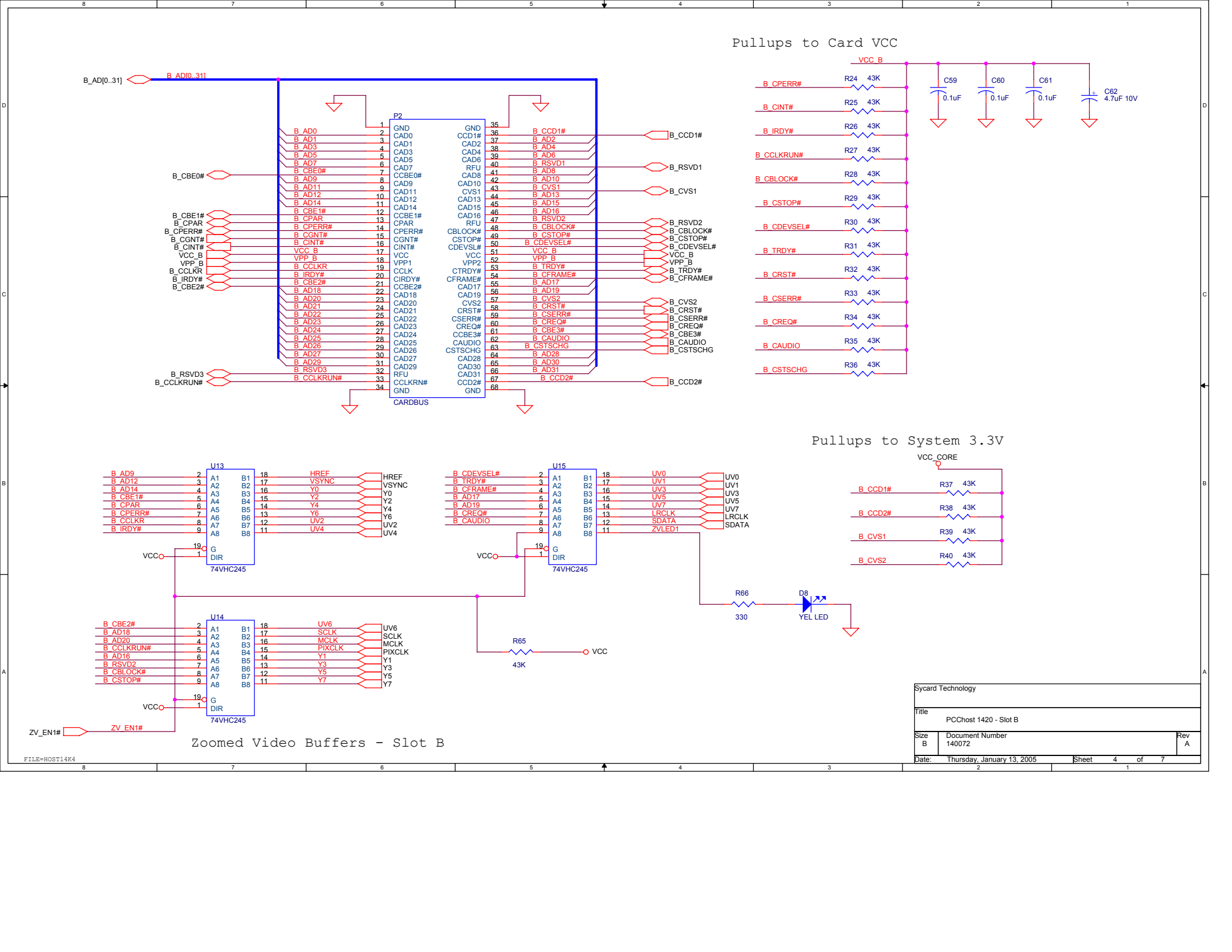


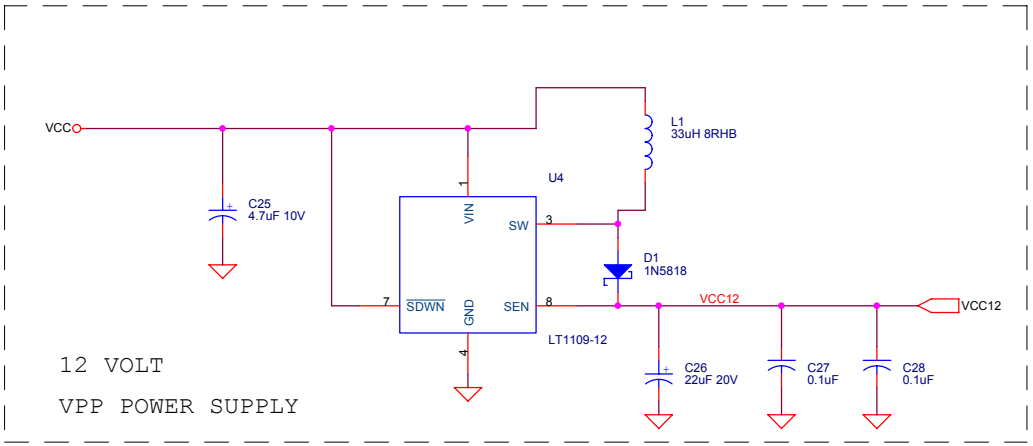


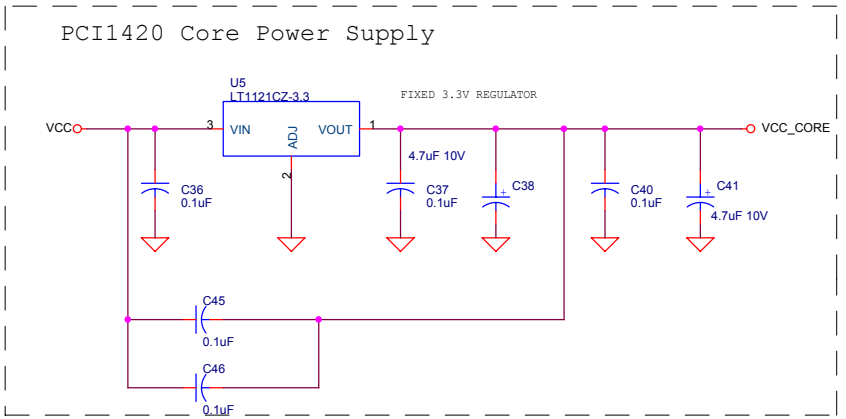
Zoomed Video Buffers - Slot A

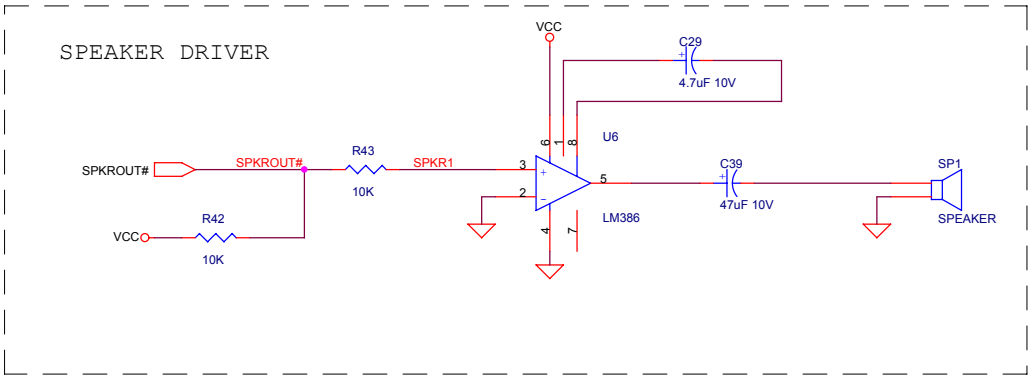
Sycard Technology		
Title: PCChost 1420 - Slot A		
Size: B	Document Number: 140072	Rev: A
Date: Wednesday, October 06, 2004	Sheet 3 of 7	

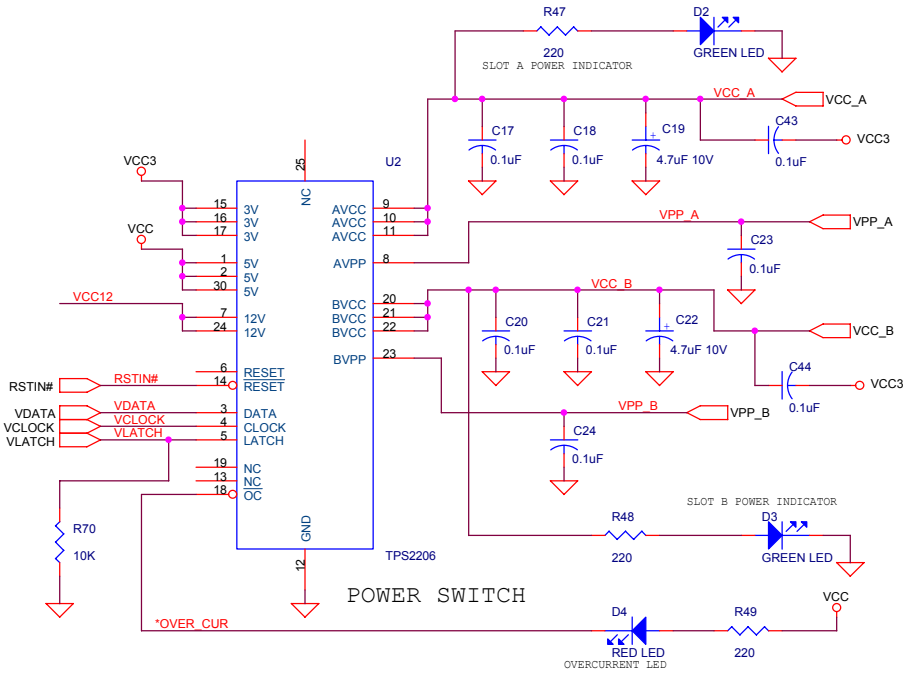
FILE=HOST14K3

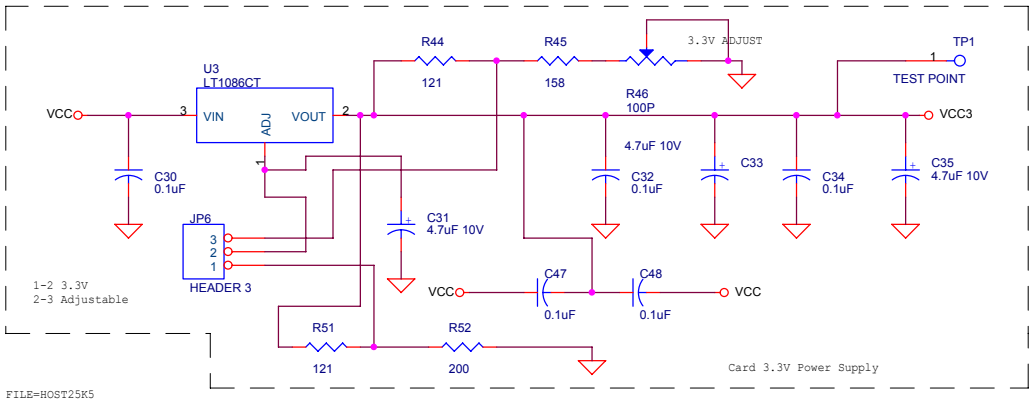

Pullups to Card VCC
B_AD[0..31]
B_AD[0..31]
P2
CARDBUS
B_CBE0#
B_CBE1#
B_CPAR
B_CPERR#
B_CGNT#
B_CINT#
VCC_B
VPP_B
B_CCLKR
B_IRDY#
B_CBE2#
B_RSVD3
B_CCLKRUN#
B_CCD1#
B_RSVD1
B_CVS1
B_RSVD2
B_CBLOCK#
B_CSTOP#
B_CDEVSEL#
B_TRDY#
B_CFRAME#
B_CVS2
B_CRST#
B_CSERR#
B_CREQ#
B_CBE3#
B_CAUDIO
B_CSTSCHG
B_CCD2#
VCC_B
B_CPERR#
B_CINT#
B_IRDY#
B_CCLKRUN#
B_CBLOCK#
B_CSTOP#
B_CDEVSEL#
B_TRDY#
B_CRST#
B_CSERR#
B_CREQ#
B_CAUDIO
B_CSTSCHG
R24 43K
R25 43K
R26 43K
R27 43K
R28 43K
R29 43K
R30 43K
R31 43K
R32 43K
R33 43K
R34 43K
R35 43K
R36 43K
C59 0.1uF
C60 0.1uF
C61 0.1uF
C62 4.7uF 10V
Pullups to System 3.3V
VCC_CORE
B_CCD1#
B_CCD2#
B_CVS1
B_CVS2
R37 43K
R38 43K
R39 43K
R40 43K
U13
74VHC245
U15
74VHC245
U14
74VHC245
HREF
VSYNC
Y0
Y2
Y4
Y6
UV2
UV4
UV0
UV1
UV3
UV5
UV7
LRCLK
SDATA
ZVLED1
UV6
SCLK
MCLK
PIXCLK
Y1
Y3
Y5
Y7
VCC
R66 330
D8 YEL LED
R65 43K
ZV_EN1#
ZV_EN1#
Zoomed Video Buffers - Slot B
Sycard Technology
Title
PCChost 1420 - Slot B
Size B
Document Number 140072
Rev A
Date: Thursday, January 13, 2005
Sheet 4 of 7
FILE=HOST14K4





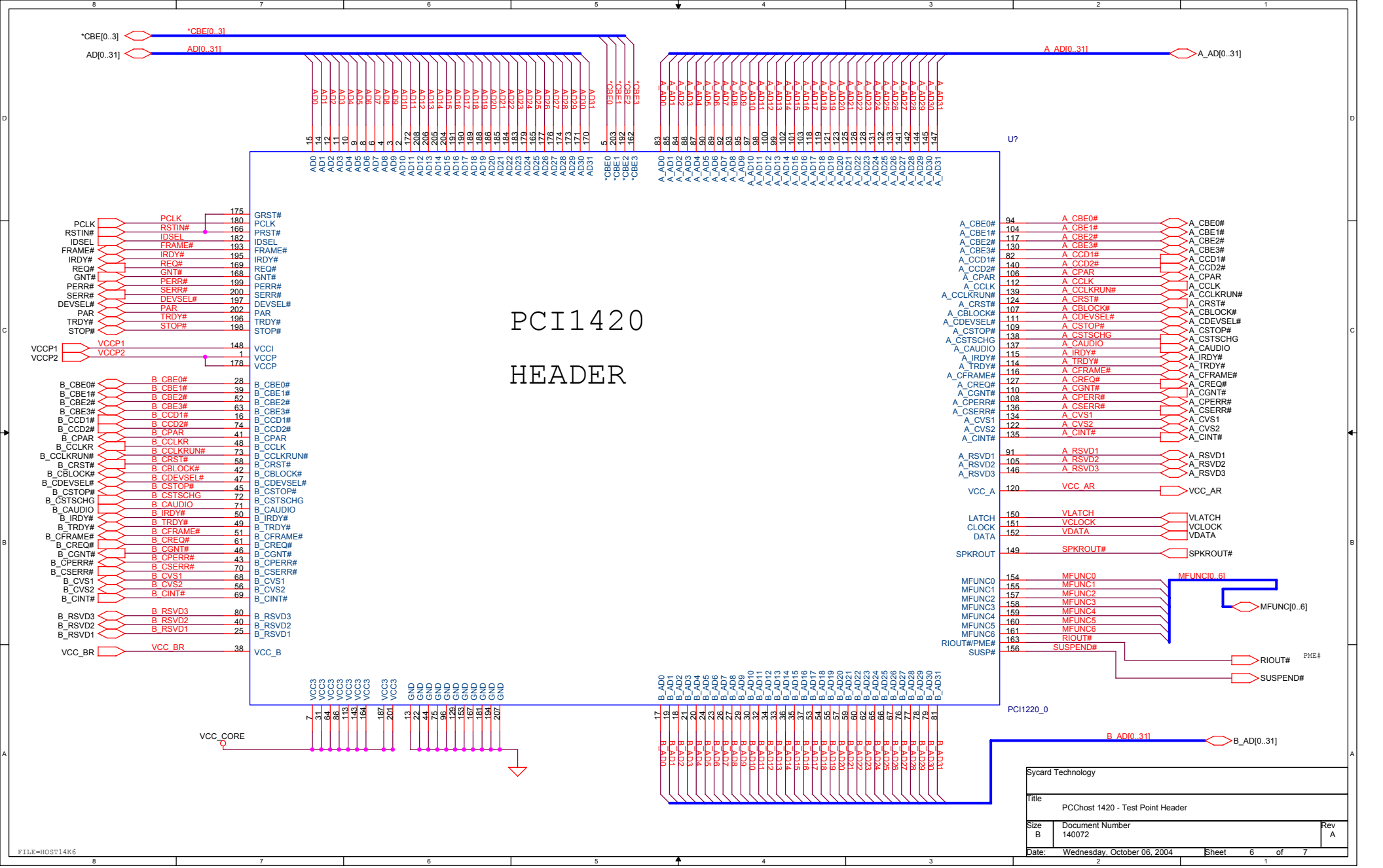






FILE=HOST25K5

Sycard Technology		
Title: PCChost 1420 - Power Control		
Size: B	Document Number: 140072	Rev: A
Date: Wednesday, October 06, 2004	Sheet 5 of 7	



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Title: PCChost 1420 - Test Point Header

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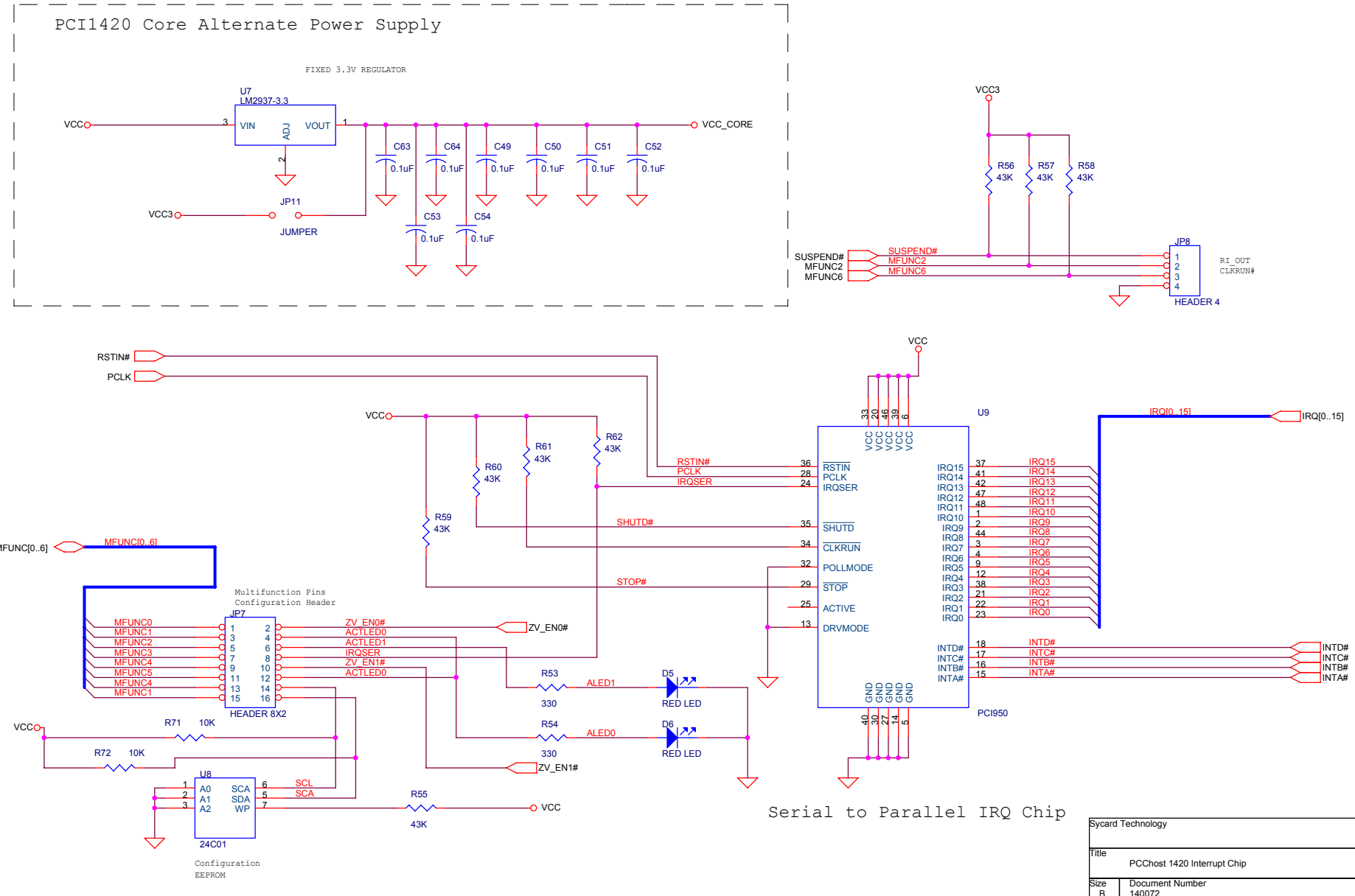

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Title: PCChost 1420 Interrupt Chip		
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FILE=HOST14K7