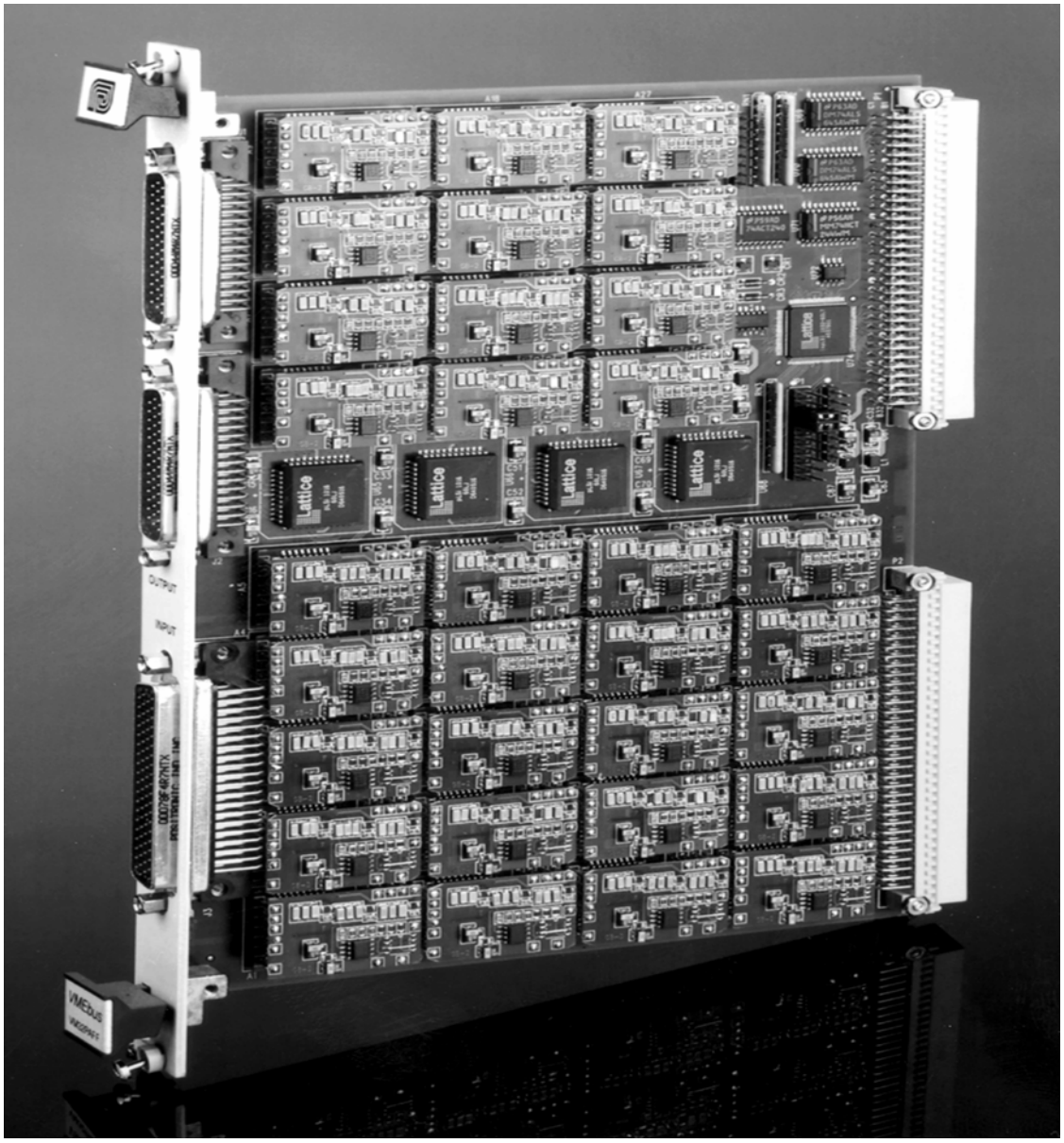
FREQUENCY DEVICES™, INC.

Model VM2.0PAFF

32 Channel VME Module

Programmable Amplifier
With Fixed Frequency Filter

USER'S MANUAL



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1. Introduction

The VM2.0PAFF VMEbus family of amplifier/filter boards from Frequency Devices Inc. offer up to thirty-two channels of software programmable differential input amplifiers combined with precision 4-pole fixed frequency Butterworth or Bessel linear analog filters on each channel. The boards are available in a single width B-size (6U) VME form factor and fully conform to VME Revision C.1 as an A16/D16 Slave.

VM2.0PAFF's provide simultaneous access to DC-coupled wideband signals. The boards receive up to thirty-two differential signal inputs through two shielded front panel connectors and provide signal buffering, software programmable gain from -12dB to +36dB in 6dB steps, and fixed frequency 4-pole low pass filtering for each channel. The boards may be configured with Butterworth or Bessel filters with cutoff frequencies from >100 kHz to 2.0 MHz. Available option includes AC coupled input.

Features/Benefits

- Simultaneous access over 32 channels offers a low cost, versatile and convenient way to provide amplification and filtering.
- Three active read/write registers provide programming and set-up verification.
- Phase match of ±2.0° and gain accuracy of ±0.1 dB provides precision performance solutions to design engineers, system integrators and OEM's.
- Four-pole Butterworth or Bessel transfer functions with a broad range of corner frequencies are offered to meet a wide range of applications.
- High channel count density without sacrificing performance maximizes chassis utilization.

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2. Specifications

(@ 25°C and Rated Power Input)

Analog Input	
1. Impedance	1 MΩ//22pF
2. Maximum Input	20 V pk-pk, each leg
3. Linear Input Range	±8V pk
4. AC coupling (Optional)	Fixed frequency from 1 kHz
5. CMRR	≥50 dB, DC to 100 kHz ≥40 dB, 100 kHz to 2 MHz
Analog Output	
6. Impedance	1.0Ω, 10Ω max.
7. Offset Voltage	25 mV typ. 50 mV max.
8. Linear Operating Range	±4 V into 500Ω
9. Offset Temp. Coeff.	±(5 + 100/G) μV/°C max. 25 mV/°C referred to input
Frequency Characteristics	
10. Anti-Alias Filtering	Fixed frequency 4-pole low-pass Butterworth or Bessel
11. Cut-off Frequency fc (-3 dB)	>100 kHz to 2.0 MHz
12. Amplitude Match*	±0.2 dB @DC
13. Phase Match*	2.0° max @fc
14. Noise Voltage, RTI	25nV/√Hz @ 1 kHz
15. Distortion (2V pk-pk)	≤-60 dB, 20 Hz to 100 kHz ≤-50 dB, 100 kHz to 2.0 MHz
Gain	
16. Gain programming	0.25X to 64X in factors of 2:1 32 channels programmed over VMEbus with read-back
17. Gain Accuracy	±0.1dB
VMEbus	
18. Interface	A16/D16, D08 (EO), Slave
19. Registers	Three active R/W registers in 64 byte block
Power Supply	
20. From VME Backplane	+5V - 1.0A max. ±12 – 1.25A max.
Environmental	
21.Operating	0°C to +70°C
22. Storage	-25°C to +85°C
23. Humidity	0-95% non-condensing
Mechanical	
24. Card Size	VMEbus 6U single slot 9.17 x 6.3 inches, (233 x 160 mm)
25. No. of Input Channels	32 DC-coupled
26. No. of Output Channels	32 Single Ended, DC-coupled, Two groups of 16
27. Mating Connectors	Input: Male high-density 78-pin D sub, Quantity 1 Output: Female high-density 44-pin D sub, Quantity 2
28. Weight	1 LB., (454 grams)

* Any two channels set to same gain and loading

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3. Description

The VM2.0PAFF is a single width B-size (6U) VME model that consists of a motherboard and up to 32 daughter modules. The motherboard contains the VMEbus interface and input and output connections. Each daughter module is made up of two boards: a high precision programmable gain amplifier board and a 4-pole filter/buffer amplifier combination board.

VME Bus Interface and Input/Output Connections

The VM2.0PAFF appears on the VMEbus as a Revision C.1 compliant A16/D16 slave. The VMEbus backplane offers a software programmable interface to set the gain of each daughter module. Through the interface, a user can also read back individual channel gain settings. This VM2.0PAFF read/write or bi-directional access to the individual amplifier modules is especially useful when building auto-ranging systems and/or fault tolerant systems. Additionally, it is good for diagnosing system failures, for debugging newly developed systems, and for constructing reliable test header files.

The motherboard uses an indexed channel-addressing scheme and transfers gain data to/from the selected channel over a simple serial channel. **Figure 3-1** is a simplified block diagram of the VM2.0PAFF showing one amplifier/filter channel and all of the common functions.

The serial channel incorporates some features that are especially important when providing precision, low noise signal conditioning. When the board is not being accessed (the normal case during a test) the serial channel is entirely static. When the board is accessed to set or read back a channel gain, only the channel being accessed is clocked, so the other channels on the board see no logic transitions that could inject noise or induce DC offsets.

The serial channel is slow compared to VMEbus transfer rates. Rather than hold the VMEbus while gain data is serialized and transferred to the selected channel, the VM2.0PAFF board uses a BUSY flag interlock while data transfer to/from the selected channel is taking place.

The motherboard provides simultaneous access to up to 32 Differential - DC-coupled wideband input signals. It offers up to 32 Single-Ended – DC coupled output channels in four groups of eight. Available options includes AC-coupled input channels.

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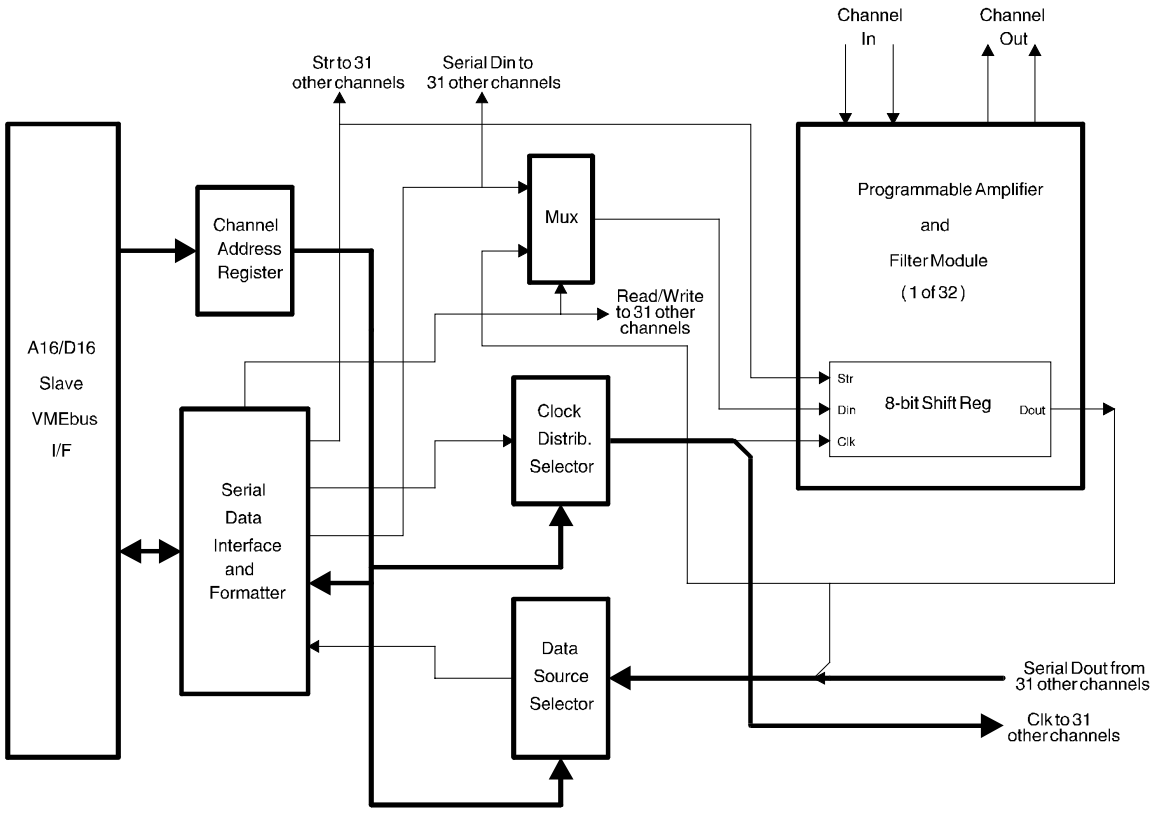

Figure 3-1: VM2.0PAFF Simplified Functional Block Diagram.
One out of 32 possible channels is shown.

Programmable Gain Amplifiers

The programmable gain amplifiers (PGA) are located on daughter modules, see **Figure 3-2**. There is one PGA for each channel, up to a maximum of 32 channels per VM2.0PAFF. The input to the gain amplifier is a precision instrumentation amplifier that provides a high impedance differential input with high common mode rejection capability. The differential inputs for the channel are converted to a single ended signal before being applied to the gain amplifier where the signal is amplified or attenuated by the value programmed by the user. The gain can be selected to vary between x0.25 (-12.04dB) to x64 (+36.12dB) in steps of x2 (6.02dB).

When power is first applied to the board, the gain of each channel is arbitrary. The user must program the board in order to established a given gain value.

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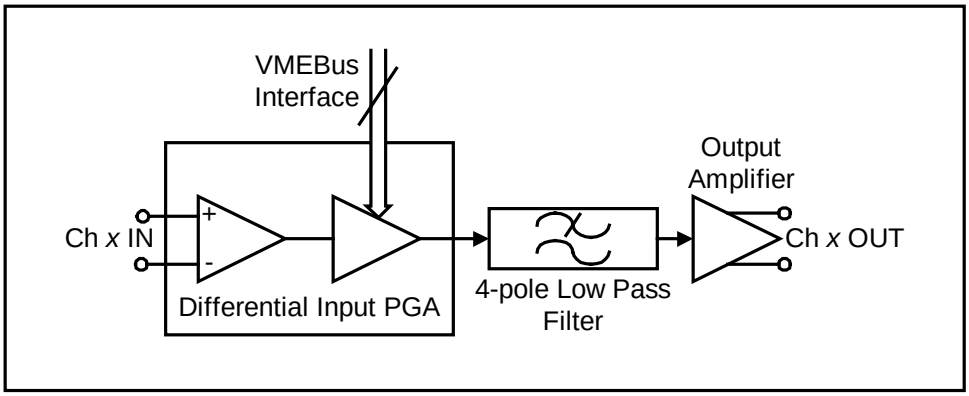
PGA (a)



PGA (b)

Figure 3-2 PGA (a) and PGA (b): A daughter module.
X represents the channel number of 1 up to 32.

Anti-Alias Filters

Each channel provides a fixed frequency 4-pole Bessel or Butterworth linear analog low-pass filter. The corner frequency for each filter is user specified between 100 kHz and 2.0 MHz. There is no bypass mode for the anti-alias filter.

Output Amplifiers

The output of each filter module is applied to the output amplifier. This output stage converts the signal to an output with a low output impedance.

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4. Hardware Preparation

Unpacking and Inspection

Before unpacking the VM2.0PAFF shipping container, carefully inspect the exterior of the package for evidence of damage. After noting areas of possible shipping damage, open and unpack the shipping container, being careful to preserve the container and packing materials in case they are needed later.

CAUTION:
The VM2.0PAFF Board is sensitive to STATIC ELECTRICITY.
Use proper GROUNDING TECHNIQUES
when handling the board.

Carefully remove the VM2.0PAFF board from its anti-static bag and visually inspect for evidence of damage. If the board appears to be damaged in any way, notify the shipping carrier immediately.

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Hardware Configuration

Once the VM2.0PAFF VMEbus board has been removed from its anti-static bag and carefully inspected for damage, you are ready to configure the board's base address for your particular system. Communication to all amplifier/filter modules is done through three registers whose Base Address can be set throughout all of A16 space. A VM2.0PAFF board occupies a 64-byte block in A16 address space and may be configured on any 64-byte boundary. The user will need to set a Base Address that is appropriate for the VME system in which the VM2.0PAFF will be installed. The Base Address is the only hardware configuration on the VM2.0PAFF board. The factory set Base Address is 2000(hex). Before attempting to use the board, the user should set/verify the base address using the address jumper JP1 on the board.

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Use proper GROUNDING TECHNIQUES
when handling the board.

To reconfigure the VM2.0PAFF Base Address, lay the board flat as shown in **Figure 4-1**. The ten-position jumper block shown in **Figure 4-1** is used to set the board's base address in A16 address space. The ten jumper positions correspond to address lines A15 through A06. Jumper position 06 corresponds to address line A06, jumper position 07 corresponds to A07, etc. An installed jumper sets a logic '1' while a missing jumper sets a logic '0'. For example, to set the VM2.0PAFF Base Address to 800(hex), install a jumper on position 11 which corresponds to A11.

After the board's base address has been configured, the VM2.0PAFF is ready for installation in a VME system.

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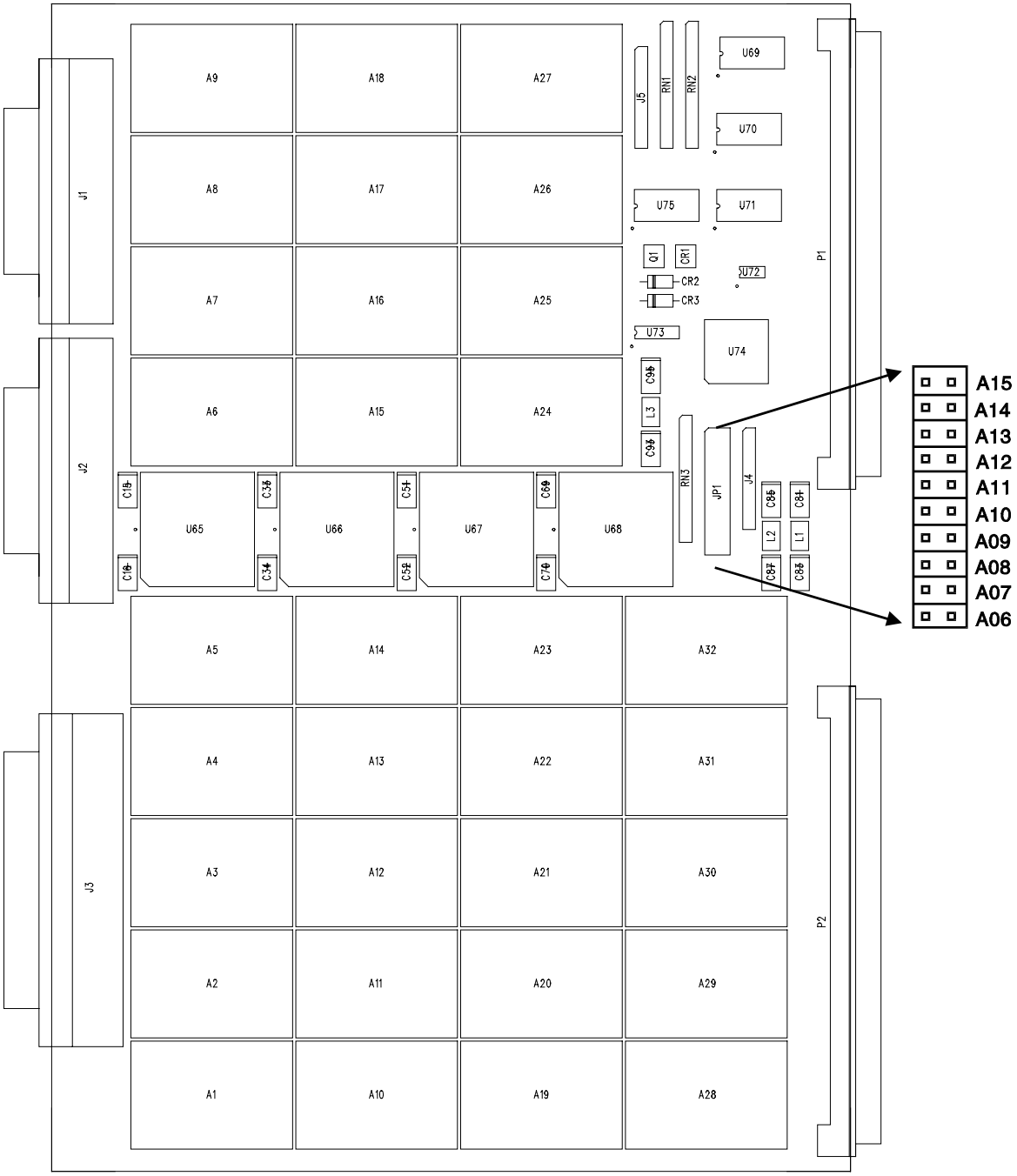

Figure 4-1: VM2.0PAFF Base Address Configuration Jumpers.
An installed jumper sets a logic '1' while a missing jumper sets a logic '0'.

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Board Installation

Frequency Devices' VM2.0PAFF conforms mechanically, in every respect, to the single width VME "B" size (6U) form factor. Installation of a VM2.0PAFF board into a standard VME mainframe can proceed exactly as for any other standard single width "B" size (6U) VME board.

CAUTION:
The VM2.0PAFF Board is sensitive to STATIC ELECTRICITY.
Use proper GROUNDING TECHNIQUES
when handling the board.

The VM2.0PAFF board may be installed in any available mainframe slot except Slot 0 (VMEbus Master). The board does not use VMEbus interrupts or bus-mastering capabilities, but passes all VMEbus daisy chained signals automatically.

The major considerations in locating the VM2.0PAFF board in the mainframe are for EMI and I/O signal cabling. To minimize interference from other boards in the system, it is good practice to keep one or more empty slots between analog signal conditioning boards and high-speed digital boards in the system. When cabling the system, it is desirable to keep the analog signal cabling as short as possible and physically located away from high speed digital cabling and high voltage switching lines.

I/O Connections and the Front Panel

The following information is provided to assist the user/integrator in installing and interconnecting a VM2.0PAFF board into a VME system.

Figure 4-2 shows the layout of the VM2.0PAFF front panel. The following sections provide detailed information about connectors, pinouts, and cabling. There are no front panel indicators or controls on the VM2.0PAFF.

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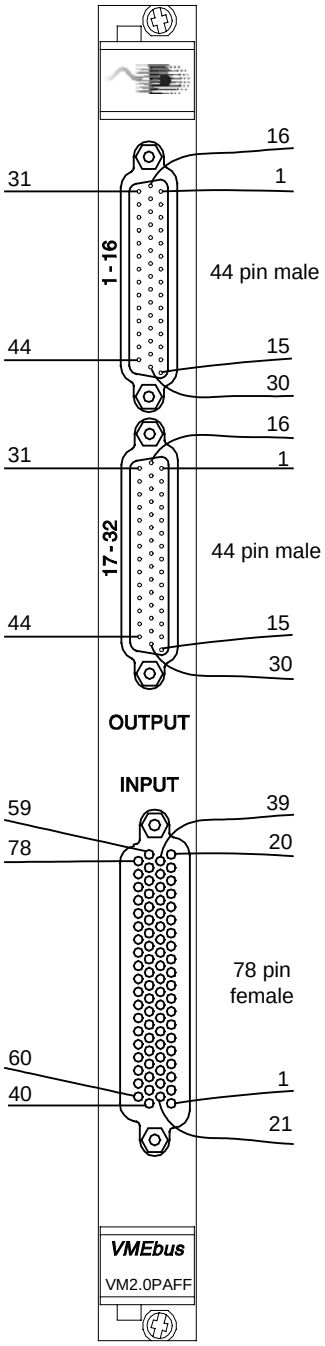

Figure 4-2: VM2.0PAFF Front Panel
The analog input connector is a female 78-pin D-shell connector.
The analog output connectors are two male 44-pin D-shell connectors.

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Connector/Cable Information and I/O Connections

The Analog Input connector is a 78-pin female "D" shell connector located near the bottom of the front panel. Analog Input connections are as follows:

Function	Input Connector (J3) 78 Pin Female D-shell	Function	Input Connector (J3) (Cont'd) 78 Pin Female D-shell
Channel 00 Hi	69	Channel 16 Hi	61
Channel 00 Lo	70	Channel 16 Lo	62
Channel 01 Hi	50	Channel 17 Hi	42
Channel 01 Lo	51	Channel 17 Lo	43
Channel 02 Hi	31	Channel 18 Hi	23
Channel 02 Lo	32	Channel 18 Lo	24
Channel 03 Hi	11	Channel 19 Hi	3
Channel 03 Lo	12	Channel 19 Lo	4
Channel 04 Hi	71	Channel 20 Hi	63
Channel 04 Lo	72	Channel 20 Lo	64
Channel 05 Hi	52	Channel 21 Hi	44
Channel 05 Lo	53	Channel 21 Lo	45
Channel 06 Hi	33	Channel 22 Hi	25
Channel 06 Lo	34	Channel 22 Lo	26
Channel 07 Hi	13	Channel 23 Hi	5
Channel 07 Lo	14	Channel 23 Lo	6
Channel 08 Hi	73	Channel 24 Hi	65
Channel 08 Lo	74	Channel 24 Lo	66
Channel 09 Hi	54	Channel 25 Hi	46
Channel 09 Lo	55	Channel 25 Lo	47
Channel 10 Hi	35	Channel 26 Hi	27
Channel 10 Lo	36	Channel 26 Lo	28
Channel 11 Hi	15	Channel 27 Hi	7
Channel 11 Lo	16	Channel 27 Lo	8
Channel 12 Hi	75	Channel 28 Hi	67
Channel 12 Lo	76	Channel 28 Lo	68
Channel 13Hi	56	Channel 29Hi	48
Channel 13 Lo	57	Channel 29 Lo	49
Channel 14 Hi	37	Channel 30 Hi	29
Channel 14 Lo	38	Channel 30 Lo	30
Channel 15 Hi	17	Channel 31 Hi	9
Channel 15 Lo	18	Channel 31 Lo	10

Table 4-1: Analog Input Connections.

Refer to **Figure 4-2** for connector orientation. The mating connector is a male high-density 78-pin D-sub.

Frequency Devices recommends that input signals be wired using cable consisting of individually shielded twisted pairs of #22 AWG stranded wire.

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The Analog Outputs are carried on two 44-pin male "D" shell connectors located in the center and near the top of the front panel. Analog Output connections are as follows:

Function	Output Connector Channels 00-15 (J1) 44 Pin Male D-shell	Function	Output Connector Channels 16-31 (J2) 44 Pin Male D-shell
Channel 00 Hi	33	Channel 16 Hi	33
Channel 00 Lo	32	Channel 16 Lo	32
Channel 01 Hi	19	Channel 17 Hi	19
Channel 01 Lo	18	Channel 17 Lo	18
Channel 02 Hi	4	Channel 18 Hi	4
Channel 02 Lo	3	Channel 18 Lo	3
Channel 03 Hi	35	Channel 19 Hi	35
Channel 03 Lo	34	Channel 19 Lo	34
Channel 04 Hi	21	Channel 20 Hi	21
Channel 04 Lo	20	Channel 20 Lo	20
Channel 05 Hi	6	Channel 21 Hi	6
Channel 05 Lo	5	Channel 21 Lo	5
Channel 06 Hi	37	Channel 22 Hi	37
Channel 06 Lo	36	Channel 22 Lo	36
Channel 07 Hi	23	Channel 23 Hi	23
Channel 07 Lo	22	Channel 23 Lo	22
Channel 08 Hi	8	Channel 24 Hi	8
Channel 08 Lo	7	Channel 24 Lo	7
Channel 09 Hi	39	Channel 25 Hi	39
Channel 09 Lo	38	Channel 25 Lo	38
Channel 10 Hi	25	Channel 26 Hi	25
Channel 10 Lo	24	Channel 26 Lo	24
Channel 11 Hi	10	Channel 27 Hi	10
Channel 11 Lo	9	Channel 27 Lo	9
Channel 12 Hi	41	Channel 28 Hi	41
Channel 12 Lo	40	Channel 28 Lo	40
Channel 13Hi	27	Channel 29Hi	27
Channel 13 Lo	26	Channel 29 Lo	26
Channel 14 Hi	12	Channel 30 Hi	12
Channel 14 Lo	11	Channel 30 Lo	11
Channel 15 Hi	43	Channel 31 Hi	43
Channel 15 Lo	42	Channel 31 Lo	42

Table 4-2: Analog Output Connections.

Refer to **Figure 4-2** for connector orientation. The mating connectors are female high-density 44-pin D-subs.

Frequency Devices recommends that output signals be wired using cable consisting of individually shielded twisted pairs of #22 AWG stranded wire.

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5. Programming

Register Level Programming

A register-based read/write programming interface makes the VM2.0PAFF family of VMEbus amplifier/filter boards extremely easy to program. All the programmable gain modules on the motherboard may be programmed through three 16-bit registers. These are the Channel Address Register, the Data Register, and the Reset Register. **Figure 5-1** shows the VM2.0PAFF, VMEbus memory map.

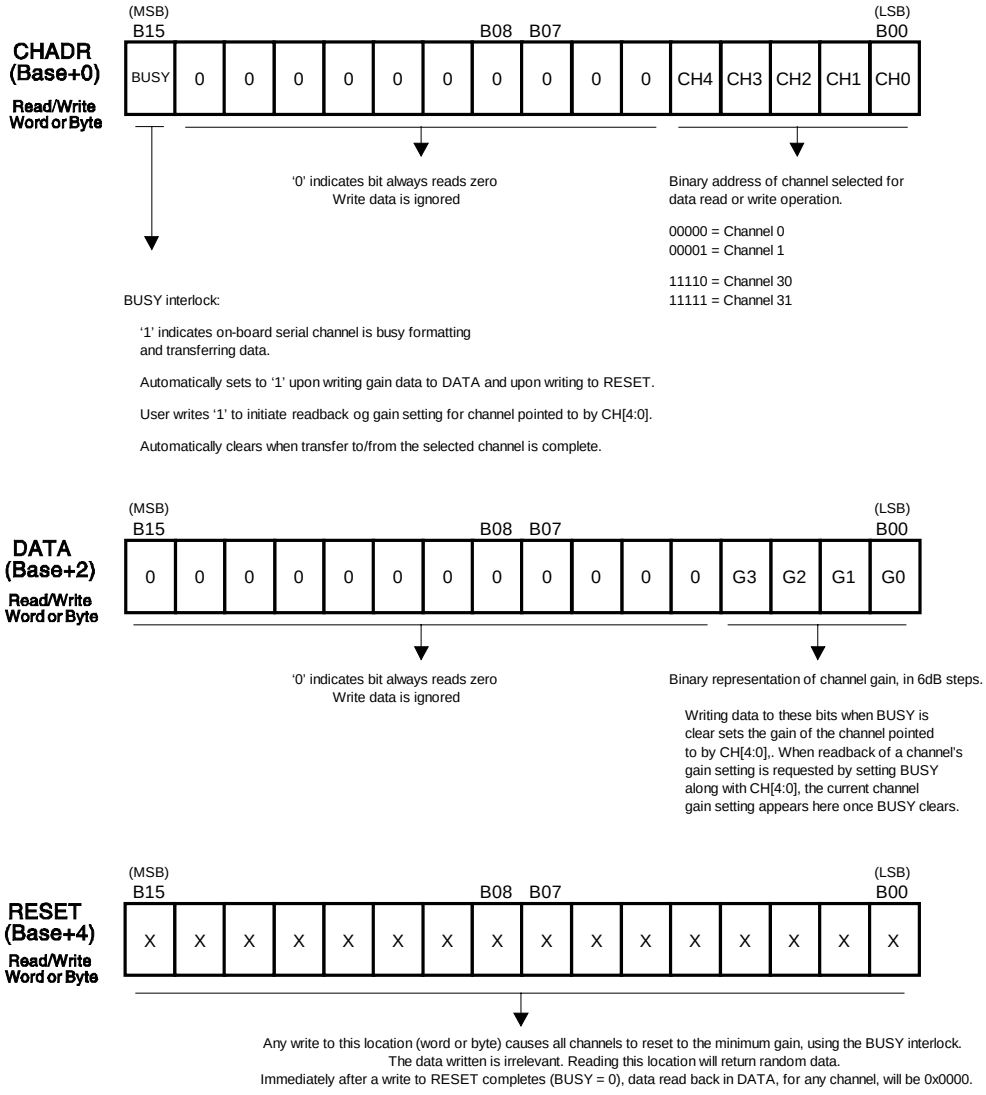

Figure 5-1: VM2.0PAFF VMEbus Memory Map.
The memory map consists of three VMEbus 16-bit registers.

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The Channel Address Register or CHADR (located at Base Address + 0) holds the address of the daughter module being addressed. The first amplifier channel, Channel 0, has an address of (00)x and the last amplifier channel, Channel 31, has an address of (1F)x. The channel addresses occupy the lowest five LSB's of CHADR, that is, from B00 up to B04. One bit of this register is also used as a flag to indicate that the serial interface is busy and new data cannot be accepted until this bit is cleared. This BUSY interlock bit is located at the MSB of CHADR, or B15.

The Data Register or DATA (located at Base Address + 2) holds the binary representation of a specific channel gain. Only the four lowest LSB's of DATA are used. Writing data to these bits when BUSY is clear, sets the gain of the channel pointed to by CHADR. When a readback of a channel's gain setting is requested by setting BUSY, the current channel gain setting appears in DATA once BUSY clears. The lowest gain setting (-12dB) is set by writing a (0)x to DATA and the highest gain setting (+36dB) is set by writing a (8)x to DATA. **Table 5-1** shows DATA gain settings.

Gain Weight (Vo/Vi)	Gain (dB)	Encoded Value (decimal)	Encoded Value (hex)
¼	-12.04	0	0
½	-6.02	1	1
1	0.00	2	2
2	+6.02	3	3
4	+12.04	4	4
8	+18.06	5	5
16	+24.08	6	6
32	+30.10	7	7
64	+36.12	8	8

Table 5-1: DATA register gain settings.

The Reset Register or RESET (located at Base Address + 4) allows the user to set all channels on the board simultaneously to their minimum gain setting. This is useful for system initialization and in auto-ranging applications. Writing anything to RESET transfers all zero data to all of the channels simultaneously. The data written is irrelevant. Readback requests on this location return random data. The reset function uses the BUSY interlock just as a normal write to DATA would.

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Programming Procedure

To write gain data to a channel, the user first reads the CHADR (Base Address + 0) and tests its BUSY bit to see if the serial interface is busy. If BUSY is set, the user can go on to other things and come back to the board later, or the user can poll CHADR, waiting for BUSY to clear. Once BUSY is found clear the user writes the desired channel address to CHADR. The user must also make sure to write '0' to the BUSY bit.

Once the desired channel has been selected, the user then sets that channel's gain by writing the desired gain data to DATA (Base Address + 2). The VM2.0PAFF automatically sets the BUSY bit in the CHADR register to indicate that the serial bus is transferring data. The BUSY bit is automatically cleared once the transfer is complete. The serial channel will be busy for approximately 4 microseconds.

To read a channel's gain setting, the user first tests the BUSY bit to see if the serial interface is busy by reading CHADR's BUSY bit. If BUSY is set, the user can go on to other things and come back to the board later, or the user can poll CHADR, waiting for BUSY to clear. Once BUSY is found clear, the user writes the desired channel address to CHADR, making sure to write a '1' to the BUSY bit. The serial interface accesses gain data from the selected channel and clears the BUSY bit in CHADR when the requested data is available in DATA. The requested data is available in DATA approximately 4 microseconds after writing to CHADR.

Please note, when a flag can be controlled by two or more systems, instructions that generate read/modify/write cycles (or read followed by write cycles) should be avoided while testing the state of the BUSY bit. The safest way to test BUSY is to read CHADR into a local register and then test the state of the BUSY bit in the registered copy.

In addition to VM2.0PAFF register map, **Figure 5-1** also defines the read/write function of each bit. Notice that registers may be accessed as words or as bytes.

Programming Considerations

There are some considerations that the user must take into account for when trying to program the VM2.0PAFF.

- Attempting to access the VM2.0PAFF board in other than A16 address space will cause a bus timeout.
- Attempting long word access or unaligned transfers will cause the board to respond to the bus cycle with a bus error (BERR).
- Changing the channel address while BUSY is set results in erroneous data during a data read operation and will corrupt the settings of two or more channels during a data write operation.
- VM2.0PAFF hardware prevents changing of the channel selection while BUSY.
- Writing to the Data Register or the Reset Register while BUSY is set is inhibited in hardware.

None of these events are flagged by the board, so it is important to use the BUSY interlock before writing to any register.

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- Reading the Data Register while BUSY is set will yield erroneous data but will not impair board operation or contaminate any channel settings. This event is not flagged, so it is important to use the BUSY interlock before reading the Data Register.
- It is not possible to write '0' to the BUSY bit from the VMEbus, so this is not an error. Attempting to write '1' to the BUSY bit when it is already set is also not an error condition and therefore is not flagged.
- Attempting to set a channel's gain beyond the normal gain range will cause the channel to automatically set to its maximum gain. If the channel's gain setting is subsequently read back, the proper code for maximum gain will be returned.

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6. Troubleshooting and Technical Support

If you have difficulty installing the VM2.0PAFF board, or if the board fails to operate properly, contact Frequency Devices for technical assistance. Technical assistance is available weekdays 8:00 AM to 5:00 PM Eastern time at 978-374-0761 or 800-252-7074. Inquiries may also be faxed to 978-521-1839 or emailed to: sales@freqdev.com.

If you need to contact Frequency Devices in writing, our address is:

25 Locust Street
Haverhill, MA 01830
Attn: Customer Service

Please have the following information handy prior to contacting Frequency Devices for assistance:

- Model Number and Serial Number
- Purchase Order Number
- Your "Bill To" and "Ship To" addresses

If Frequency Devices determines the board must be returned to the factory, you will be issued a Return Material Authorization (RMA) number. Use this number on all shipping containers, repair purchase orders, and shipping documents. DO NOT ATTEMPT TO RETURN BOARDS WITHOUT FIRST OBTAINING AN RMA NUMBER.

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7. Warranty Information

Unless otherwise specified in writing by FDI, all FDI products sold hereunder are warranted against defects in workmanship and material under normal use and service for a period of one (1) year from the date of shipment, except that, where applicable liability for defective components purchased by FDI and are resold to the purchaser hereunder shall conform and be limited to the obligations prescribed by the original manufacturer's warranties applicable to such components.

All warranties hereunder are contingent upon proper use in the application for which the product was intended and do not cover products which have been modified or repaired without FDI approval or which have been subjected to neglect, accident, improper installation or application or on which the original identification marks have been removed or altered. These warranties will not apply if adjustment, repair or parts replacement is required because of accident, neglect, misuse, power failure, transportation or other causes other than ordinary use.

FDI's responsibility under the above warranty shall be limited to the repair or replacement, at FDI's option, free of charge to the purchaser, of any component which fails during the one-year period; provided that the purchaser has promptly reported such failure to FDI in writing and FDI has, upon inspection, found such components to be defective. The purchaser must obtain shipping instructions for the return of any item under this warranty provision and compliance with such instructions shall be a condition of this warranty.

EXCEPT FOR EXPRESS WARRANTIES STATED ABOVE, FDI DISCLAIMS ALL WARRANTIES WITH REGARD TO THE PRODUCTS SOLD HEREUNDER, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS.

Limitation of Liability

Expressed warranties stated herein are in lieu of all obligations or liabilities on the part of FDI for damages, including but not limited to consequential damages arising out of or in connection with the use or performance of the product.

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8. Ordering Guide

VM2.0PAFF Ordering Guide

For flexibility in many applications the Frequency Devices VM2.0PAFF, VMEbus Board may be ordered with 8, 16, or 32 amplifier/filter modules. **Figure 4-1** indicates the location of each channel.

Transfer Function
B - Butterworth
L - Bessel

Options
A-AC Coupled Input

VM2.0PAFF-16-PGAB5-750kHz-A

Channels
8, **16** or **32**

-3dB Corner Frequency
e.g. >100kHz to 2.0 MHz

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