ZT 8952
ZT 8953

Integrated Drive Electronics (IDE) Interfaces

Hardware User Manual

ZIATECH CORPORATION

CONTENTS

MANUAL ORGANIZATION

This manual describes the operation and use of the ZT 8952/8953. The term ZT 8952 is used throughout the manual to reference both the ZT 8952 and the ZT 8953, except where otherwise noted. Specific differences between the two are explicitly stated. Refer to Appendix B for specifications.

Chapter 1, "**Introduction**," offers an overview of the ZT 8952. It includes a product definition, a listing of product features, a functional block diagram, and a brief description of each block. This chapter is most interesting to those comparing the features of the ZT 8952 against the needs of a specific application.

Chapter 2, "**Getting Started**," summarizes the information essential to getting your ZT 8952 operational. This includes system requirements and memory and I/O mapping. In many cases, this information is all that is needed to begin using the ZT 8952.

Chapter 3, "**Operational Overview**," presents answers to some frequently asked questions and a detailed description of the ZT 8952 interface to STD 32 bus structures. Other topics discussed include memory, I/O, interrupt structure, and direct memory access.

Chapter 4, "**IDE Interface**," discusses Integrated Drive Electronics (IDE) interface registers.

Chapter 5, "**IDE Command Descriptions**," describes various commands performed via the IDE command block.

Appendix A, "**Jumper Configurations**," describes the jumpers included on the ZT 8952 to allow you to custom-configure your board.

Appendix B, "**Specifications**," contains the electrical, mechanical, and environmental specifications for the ZT 8952.

Appendix C, "**Glossary**," lists the command codes and defines important terms and acronyms used in this manual.

Appendix D, "**Customer Support**," offers a product revision history, technical support information, and instructions for returning the ZT 8952 if service is necessary.

1. INTRODUCTION

This chapter provides a brief introduction to the ZT 8952/8953 IDE Interface and Mounting Board. It includes a product definition, a listing of product features, a functional block diagram, and a description of each block. Unpacking information and installation instructions are in Chapter 2, "Getting Started."

The term ZT 8952 is used throughout this manual to reference both the ZT 8952 and the ZT 8953, except where otherwise noted.

The ZT 8952 is an Integrated Drive Electronics (IDE) interface for the STD 32 buses that support PC-AT technology disk drives. The ZT 8952 also serves as a mechanical mounting board for the drive, allowing for a modular plug-in unit for the STD bus. The ZT 8952 supports 2½ inch disk drives, while the ZT 8953 supports 3½ drives, both mounted directly to the board. The ZT 8952 is also available with no drive mounted (ZT 8952-0) for applications that require remote mounting of the drive. Cables are restricted to 18 inches in length from controller to drive. The ZT 8952 will support up to two drives.

Mechanically, the ZT 8952 is compatible with the STD 32 Bus Specification. The ZT 8952 supports 8 MHz and 5 MHz STD-80 timings, as well as STD 32 transfers. Both 8-bit and 16-bit transfers are supported under STD 32. The ZT 8952 will support up to four Mbytes/second transfer rates on the backplane (one word every four 8-MHz cycles.) The actual transfer rate will vary with the host CPU and drive used.

The PC-AT IDE interface is a 16-bit interface only when transferring data through the 01F0h data register. The ZT 8952 supports full 16-bit transfers for STD 32 processors. For 8-bit processors, the ZT 8952 will byte pack and unpack the 16-bit IDE transfer to provide 8-bit STD bus transfers. All signals are fully buffered between the STD bus and the IDE interface. The IDE interrupt may be jumpered to drive INTRQ*, INTRQ1*, INTRQ2* (CNTRL*), INTRQ3*, IRQx (STD 32), or one of five frontplane interrupts. Some versions of Ziatech's STD DOS require the use of interrupts.

Onboard logic may be disabled for direct access to the IDE drive via the interface cable. This is useful for accessing data from a board that already has an IDE interface (such as the ZT 8910). The ZT 8952 will support an IDE drive of any capacity. The Ziatech BIOS supports all drives sold by Ziatech. Contact Ziatech for BIOS support on drives not supplied by Ziatech.

The ZT 8952 decodes I/O addresses 1F0h-1F7h and 3F6h-3F7h. All 16 bits of I/O address are decoded to avoid contention at alias addresses.

FEATURES

- STD 32 bus compatible
- PC-AT compatible register set
- 4 Mbytes/second backplane transfer rate
- Integrated 2½ inch support (ZT 8952)
- Integrated 3½ inch support (ZT 8953)
- Standalone (non-integrated) support (ZT 8952-0)
- Frontplane interrupt capability
- 16-bit/8-bit dynamic data transfer capability
- Burned in at 55º Celsius and tested
- STD 32 compliance

  I/O Slave: SA16, SA8 - I, IXL, IXP
- Two-year warranty

The figure "Functional Block Diagram" illustrates the functional blocks of the ZT 8952. A description of each block follows.

IDE Hard Disk

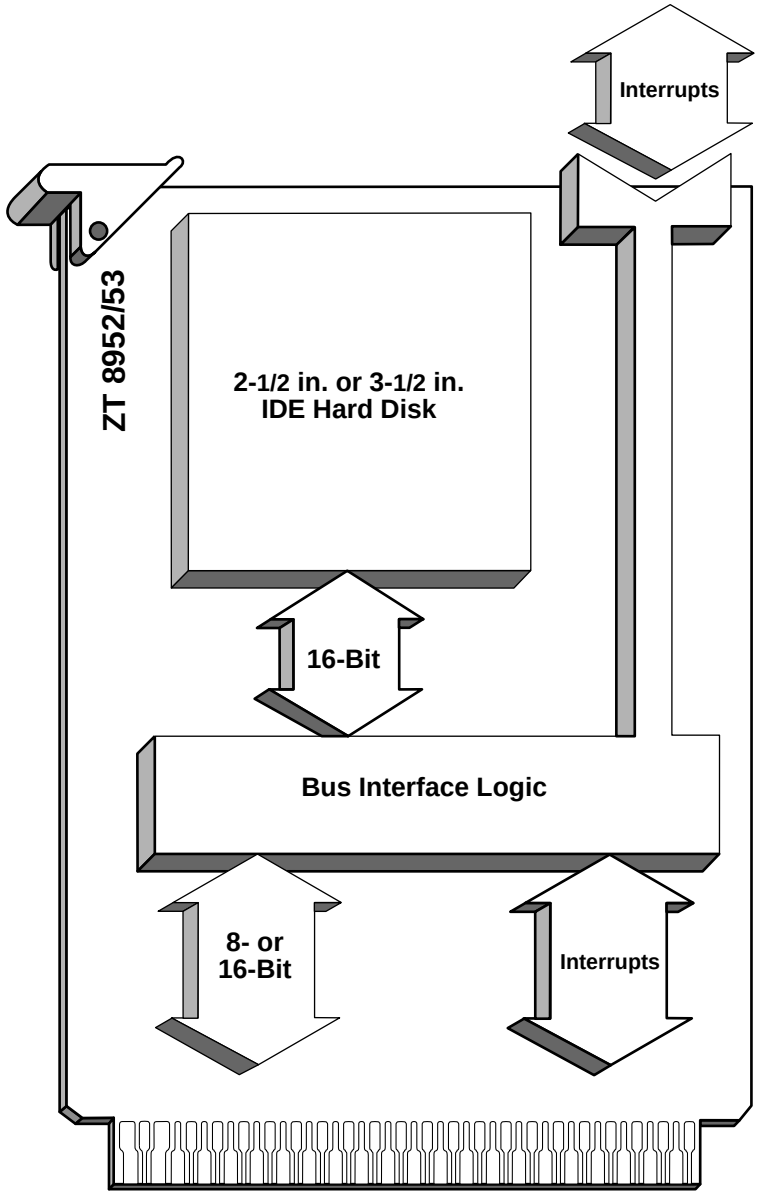
Either a 2½ inch drive (ZT 8952) or a 3½ inch drive may be mounted directly to the interface to provide a compact, modular unit for STD applications. The drive may also be remotely mounted and cabled. The cable length is restricted to 18 inches. The interface is available via a 2 mm right angle female header or a 0.1 inch right angle male header.

Bus Interface Logic

The ZT 8952 supports both 16-bit and 8-bit data transfers on the STD bus by packing and unpacking the 16-bit IDE data on behalf of the IDE drive. For 16-bit STD 32 CPUs the ZT 8952 will provide 16-bit data directly, allowing the maximum transfer rate of 4 Mbytes/second.

Interrupts

The IDE interface normally drives an interrupt to the BIOS for data ready status. This interrupt may be jumpered to either INTRQ*, INTRQ1*, INTRQ2* (CNTRL*), INTRQ3*, or IRQx on the backplane. Alternatively, one of five frontplane interrupts may be selected to provide interrupt support.



Functional Block Diagram

2. GETTING STARTED

This chapter summarizes features of the ZT 8952 and ZT 8953. Since most features of the two boards are identical, the term ZT 8952 is used for simplicity. Where features differ, the specific product number is used. Read this chapter and Chapter 3, "Operational Overview", before you use the board.

UNPACKING

Be sure to check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Ziatech for an insurance settlement. Retain the original shipping carton and packing material for inspection by the carrier. Save the anti-static bag for storing or returning the ZT 8952.

Do not return any product to Ziatech without a Return Material Authorization (RMA) Number. Appendix D, "Customer Support", explains the procedure for obtaining an RMA number from Ziatech.

Caution: Like all equipment utilizing MOS devices, the ZT 8952 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the ZT 8952 to handle the board.

SYSTEM REQUIREMENTS

The ZT 8952 is designed for use in an STD bus application. The board is therefore mechanically and electrically compatible with the STD 32 bus specifications.

Physical Requirements

ZT 8952 requires between one and three slots depending upon the size drive mounted on the board. ZT 8953 requires between two and four slots depending upon the drive used. See Appendix B, "Specifications", for specific drive requirements.

Power Requirements

Power required by the ZT 8952 and ZT 8953 is dependent upon the type of drive interfaced to, since power for the drive is supplied by the controller board.

- The base board without drive requires 320 mA typical, 470 mA maximum at +5 V
- ZT 8952 with drive (for example, ZT 8952-40) requires only +5 V

- ZT 8953 with integrated drive (for example, ZT 8953-50) requires both +5 V and +12 V for the drive

See Appendix B, "Specifications", for specific drive requirements.

Ziatech recommends vertical mounting for applications in which a fan is not used. Horizontal mounting requires a minimum air flow of 30 cubic feet/minute passing over the surface of the board.

INSTALLATION

If the ZT 8952 or ZT 8953 is used as an integrated unit you need only insert it into the card cage. For non-integrated usage the drive needs to be mounted and a cable run between the ZT 8952-0 and the drive. Be sure that the interfacing cable is no longer than 18 inches.

The ZT 8952 is supported by Ziatech BIOS version 3.2 or greater on CPU boards that do not have an onboard IDE interface (for example, ZT 8910).

The ZT 8952 includes several jumper options that tailor the operation of the board to specific application requirements. The following jumper configurations are suggested. These configurations will vary depending upon the application.

16-Bit Vs. 8-Bit STD 32 Transfers

Jumper W2 controls whether or not the board looks at BHE* on the backplane. This jumper must be installed for BHE* to be decoded and 16-bit transfers to take place in STD 32 backplanes with 16-bit processors (SA16). In an 8-bit backplane W2 should be removed because STD-80 CPUs drive BHE* (MEMEX) in non-standard fashion. W2 must be installed for SA16 CPU boards (for example, ZT 8902 or ZT 8911).

Disabling the ZT 8952 Controller

You can disable the logic on the ZT 8952 by removing W9. This procedure may be useful for diagnostic/debugging purposes.

Interrupt Selections

Jumpers W3-W7 and W11-W15 select which, if any, interrupt the IDE interface can drive to the STD bus. W3-W7 select one of five frontplane interrupts, while W11-W15 select the backplane interrupt to be driven. The ZT 8902, ZT 8911, and all STD 32 STAR SYSTEMS require W15 to be installed.

IDE Diagnostic

Some IDE drives feature an internal diagnostic for use when two drives are daisy chained. Both drives execute this diagnostic. The slave drive then indicates to the master a successful completion of the diagnostic.

Jumper W8 lets you drive the signal low for any master that needs this default. No drive currently shipped by Ziatech requires installation of this jumper.

Jumper Requirements—16-Bit Transfers

Installed: W1, W2, W5, W9, W10A

Not installed: W3, W4, W6, W7, W8, W10B, W11, W12, W13, W14, W15

This configuration selects 16-bit transfers and does not drive any backplane interrupt. W5 is loaded to select FP5*, but some versions of STD DOS will use alternative selections. If you need an interrupt, remove the jumper from W5 and use it to select the desired interrupt. The ZT 8902, ZT 8911, and all STAR SYSTEMS require W15 to be installed.

Jumper Requirements—8-Bit Transfers

Installed: W1, W5, W9, W10A

Not installed: W2, W3, W4, W6, W7, W8, W10B, W11, W12, W13, W14, W15

This configuration does not allow the ZT 8952 to respond to BHE*. Use this configuration when installing this board in non-STD 32 card cages. Some CPU cards drive BHE* (STD-80 MEMEX) in non-standard ways and will cause the board to misalign data. For this reason we recommend that W2 be removed in 8-bit CPU systems or in STD-80 backplanes.

STD 32 Compliance

STD 32 peripherals are required to meet certain compliance standards. This allows the system integrators to match capabilities among different manufacturers' boards.

The ZT 8952 has the following STD 32 compliance:

I/O Slave: SA16, SA8 - I, IXL, IXP

Definitions:

- SA16: STD-80 style 16-bit transfers
- SA8: STD-80 style 8-bit transfers
- I: Drives INTRQ*, INTRQ1*, INTRQ2* (CNTRL*), INTRQ3*
- IXL: Drives IRQx active low
- IXP: Drives IRQx with positive active edge

STD 32 peripheral boards are available from a variety of manufacturers.

3. OPERATIONAL OVERVIEW

This chapter presents an operational overview of the hardware for ZT 8952. The board's functions are described in detail, and answers are provided for some commonly asked questions.

Other topics discussed in this chapter include:

- Using the ZT 8952 in an STD DOS application
- Using the ZT 8952 in 8-bit and 16-bit mode
- How the ZT 8952 I/O is mapped into the STD I/O space
- Drive interfacing

FREQUENTLY ASKED QUESTIONS

Is ZT 8952 compatible with STD 32?

Yes. ZT 8952 meets timing requirements for STD 32 bus structures. STD 32 is a superset of STD-80.

What is the IDE Interface?

IDE stands for Integrated Drive Electronics. IDE applies to PC-AT style controllers and to any other drive using front end logic to manage the physical media. This logic improves performance by relieving an external controller's need to manage the physical media. While the AT style IDE drive is the most popular interface, other drives are available for other standards. "IDE drive", as used in this context, is an AT style IDE drive.

The IDE interface is a 16-bit interface for the IBM AT. How does ZT 8952 allow operation within the STD bus and with 8-bit CPUs?

ZT 8952 uses control logic to convert from the STD bus to the IDE interface. Byte packing and unpacking is done for the IDE interface during transfers to and from the STD bus. The first byte in 8-bit CPU data writes is buffered, then written to the drive when the second (odd) byte is transferred. The logic latches the odd byte of the 16-bit read, while returning the even byte. The latched data is returned on the next read to the odd byte location.

Does the ZT 8952 support full 16-bit transfers?

Yes. When used in an STD 32 backplane with a 16-bit CPU board such as the ZT 8901, ZT 8952 performs 16-bit transfers during the data transfer phase of a disk read or write. 16-bit transfers allow backplane transfers of up to 4 Mbytes/second. Only 8-bit transfers are performed within older STD-80 series backplanes, or with 8-bit processors.

Can I use ZT 8952 with a CPU such as ZT 8910, which has a built in IDE controller?

Yes. You can use ZT 8952 for hard disk service if it is possible to disable the IDE controller on board the CPU (as with ZT 8910). Most of these CPUs need IRQ14 asserted by the off-board IDE controller. IRQ14 must then be routed to the appropriate address so that the CPU card can service the interrupt. This is not supported by STD DOS. Contact Ziatech for configuring the ZT 8952 in this manner.

What types of IDE drives can the ZT 8952 interface to?

The ZT 8952 has two connector locations for interfacing. The first, J1, is a 0.1 inch center, right angle header that is used to cable to 3½ inch drives via a standard 0.050 inch ribbon cable. This is the type of cable found inside the typical PC-AT clone. The second connector location, J2, allows for either a female, right angle, 2 mm connector for direct drive mounting or a header style 2 mm cable used to cable to a remote drive via a 1 mm ribbon cable 2½ inch drives use the 2 mm connector. The connector used depends upon the connector type used by the drive.

Ziatech BIOS versions greater than 4.0 support a configurable drive parameter option (called USER). This option allows the BIOS to immediately support new drives by entering the exact number of cylinders, heads, and sectors.

Do I need to low-level format the IDE drive?

No, this is not recommended. The IDE concept isolates the user from the drive interface. Manufacturers may occasionally take advantage of this to squeeze higher capacity out of the drive. This is often done by varying the rotational speed of the drive for different tracks; more data can be packed in outer tracks by slowing the disk down for outside tracks. If a low-level format is issued the drive will typically zero the data and return a completed status rather than actually put down new format data. Most manufacturers do not recommend that their drive be low-level formatted.

How does the IDE drive differ from what I have in my PC-AT at home?

From a software standpoint the IDE drive behaves in identical fashion. The same tools used to set up a "normal" AT hard disk are used for the ZT 8952-IDE combination. FDISK is used to partition the drive. DOS FORMAT is used to format and enter the system information into the hard disk. Do not confuse the DOS FORMAT utility with the

low-level formatting provided by the manufacturer. DOS FORMAT verifies sectors, writes out directory information, and the like. See the preceding question above.

How do I select which drive in a two-drive system is Drive C: or Drive D:?

FDISK is used to partition each drive. In a two-drive system, the primary DOS partition on Drive 0 will be designated drive C:. The primary partition on Drive 1 will be designated drive D:. Drive letters are then first sequentially allocated to the remaining logical drives in the logical partition of Drive 0. The remaining logical drives on Drive 1 are then assigned sequential drive letters. For example, consider a two-drive system composed of four logical drives on each physical drive. A total of eight logical drives are distributed as follows.

Drive C:	Fixed Disk 0	Primary Partition
Drive D:	Fixed Disk 1	Primary Partition
Drive E:	Fixed Disk 0	Extended Partition
Drive F:	Fixed Disk 0	Extended Partition
Drive G:	Fixed Disk 0	Extended Partition
Drive H:	Fixed Disk 1	Extended Partition
Drive I:	Fixed Disk 1	Extended Partition
Drive J:	Fixed Disk 1	Extended Partition

Drive C: is assigned to the primary partition in a single drive system. The FDISK process determines partition size, maximum being 33 Mbytes for DOS version 3.3 and below. Newer DOS versions allow larger partitions.

What are the shock and vibration specifications for IDE drives?

Because shock and vibration specifications often differ between models and between manufacturers, presenting a generic specification for all IDE drives would be misleading. In general, 2½ inch drives fare better than do their 3½ inch counterparts, mainly because of their smaller mass and more compact design. Please call Ziatech if you need specifications for a particular drive.

Should I FDISK and FORMAT the disk when I receive the ZT 8952 as an integrated unit?

All drives are already FDISKed and FORMATted when you receive them. If bought as a system component the drive has been tested at the system level. The size of the partitions on larger drives, however, may not be tailored to your particular needs.

Ziatech recommends that you FDISK and FORMAT the disk in order to avoid any ambiguity with this issue.

How do I install a second drive to the system?

For ZT 8952-X users (for example, ZT 8952-40) it is not possible to install a second drive because the system lacks a cable mechanism.

For ZT 8953-X users (for example, ZT 8953-50) a number of modifications are needed. A new power cable must be extended to the second drive. Jumpers on the existing drive must be changed from default for setup as master, and on the new drive for setup as slave. These jumpers differ depending on the drive manufacturer. We recommend that you contact Ziatech for drive-specific configurations for a two-drive system.

In general, a higher capacity drive is more cost effective than two drives in a master/slave arrangement. A single drive will generally require less power and have a better Mean Time Between Failure.

The ZT 8952 does not work with my old revision (prior to Rev. A.2) ZT 8950 Floppy Disk Controller. Why?

Since the ZT 8952 and ZT 8950 share I/O register 3F7h, the ZT 8950 was revised to A.2 to allow correct operation with the ZT 8952. Be sure your ZT 8950 is Revision A.2 or greater.

I recently received revision 0.2 boards with a new jumper that was not present on revision 0 or 0.1 boards. What is W15 for?

W15 adds the capability to drive INTRQ3* on the STD 32 backplane. Your ZT 8902 or ZT 8911 processor board uses INTRQ3* by default for the hard disk interrupt.

STD BUS COMPATIBILITY

The ZT 8952 is compatible with Version 1.2 of the *STD 32 Bus Specification*, a superset of the STD-80 Series Bus Specification.

CPU AND STD BUS INTERFACE

The ZT 8952 interfaces two standards, the IDE interface and the STD bus. In addition to signal reformatting, ZT 8952 also performs byte packing and unpacking for 8-bit CPUs when transferring to and from the 16-bit only IDE interface. A state machine handles this transfer in dynamic fashion. In 16-bit STD 32 card cages ZT 8952 will perform 16-bit data transfers directly to and from the IDE drive and the STD 32 bus. 16-bit transfers allow a maximum data transfer rate of 4 Mbytes/second, assuming four clocks per transfer, or 3.2 Mbytes/second with five clocks per transfer.

Data Transfers

The ZT 8952 performs both 8-bit and 16-bit transfers as defined by the host processor. All transfers are eight bits except to I/O address 1F0h, which causes the ZT 8952 to drive the signal IO16* low. This informs the CPU that a 16-bit transfer is desired. If the CPU is a 16-bit processor such as the ZT 8901, and the system is an STD 32 system, the processor will drive BHE* low. This indicates to ZT 8952 that a high data byte is being transferred during this cycle.

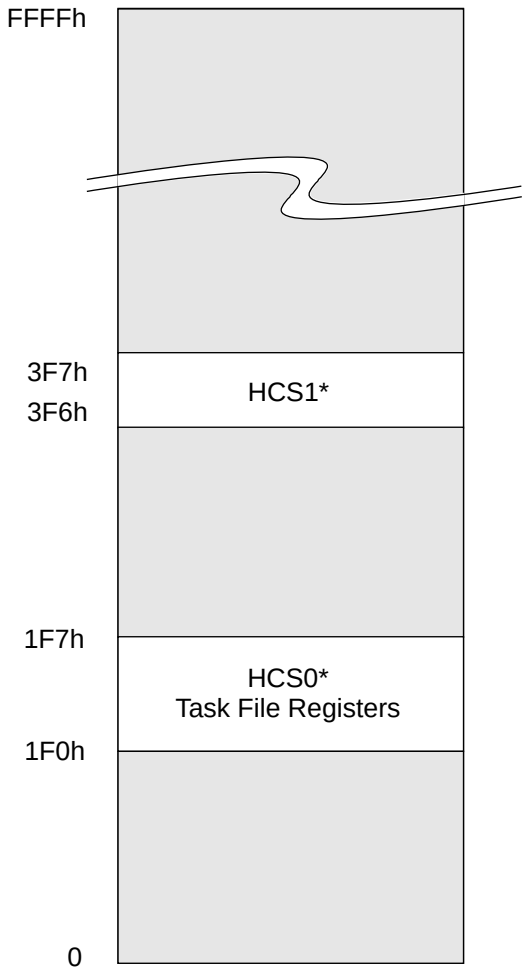
For 8-bit processors or for 16-bit processors used in older 8-bit backplanes it is recommended that W2 be removed so that BHE* is not used. BHE* was formerly a STD-80 signal called MEMEX that was not clearly defined. Some processors either drive this signal low or allow it to be driven via a parallel port bit. Since ZT 8952 interprets this signal for data size, an 8-bit transfer would be misinterpreted as a 16-bit transfer should BHE* be driven low. W2 should be installed when the ZT 8952 is used in an STD 32 backplane with a 16-bit processor. W2 may be left installed when used with an 8-bit processor that always drives BHE* (the old MEMEX signal) high.

MEMORY

The ZT 8952 does not occupy any part of the memory map.

I/O

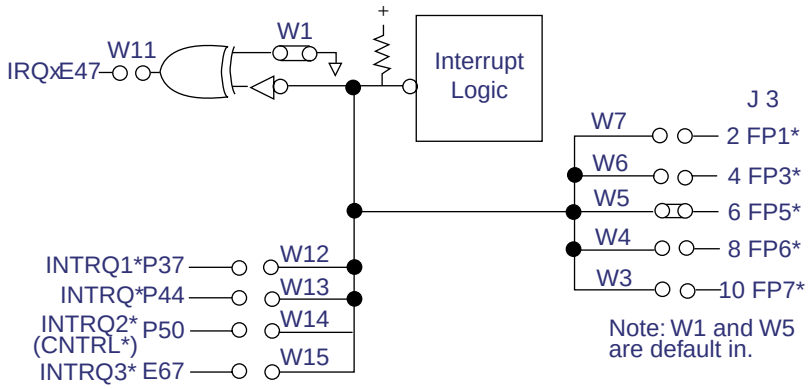
The ZT 8952 decodes two address ranges within the I/O map. The primary address range used is 1F0h-1F7h and the secondary is 3F6h-3F7h. Note that use with the ZT 8950 Floppy Disk Controller requires that the ZT 8950 be Revision A.2 or greater. This is because both the ZT 8952/8953 and the ZT 8950 share register 3F7h.



I/O Map

INTERRUPTS

ZT 8952 can drive one of four backplane interrupts or one of five frontplane interrupts with the IDE interrupt. Any systems shipped that require interrupt usage will contain the appropriate interrupt jumper loaded by the system integrator. The "Interrupt Structure" figure below illustrates the possible interrupt selections. ZT 8902 and ZT 8911 systems should have W15 installed.



Interrupt Structure

DIRECT MEMORY ACCESS (DMA)

The ZT 8952 and IDE interface do not require Direct Memory Access (DMA) services from any host.

IDE REGISTERS

The IDE Interface is composed of 10 register locations. Eight of these are decoded at 1F0h-1F7h, with the remaining two at 3F6h and 3F7h. The "I/O Register Addresses and Functions" table below defines all of the register addresses and functions for these I/O locations.

I/O Register Addresses and Functions

I/O PORT	I/O READ	I/O WRITE
ADDRESS	FUNCTION	FUNCTION
1F0h†	Data Register	Data Register
1F1h	Error Register	Write Precompensation Reg.
1F2h	Sector Count	Sector Count
1F3h	Sector Number	Sector Number
1F4h	Cylinder Low	Cylinder Low
1F5h	Cylinder High	Cylinder High
1F6h	SDH Register	SDH Register
1F7h	Status Register	Command Register
3F6h	Alt. Status Reg.	Digital Output Register
3F7‡	Drive Address Reg.	Not Used

These registers are described in greater detail in Chapter 4, "IDE Interface."

† 16-bit transfer

‡ 3F7h is shared with the floppy disk interface

4. IDE INTERFACE

The Integrated Drive Electronics (IDE) Interface is composed of 10 register locations in the I/O map. This chapter describes the common registers used by all manufacturers.

Many manufacturers have added superset commands for such things as diagnostic utilities and power down modes for low power applications. Consult Ziatech for specific drive commands or features.

IDE INTERFACE REGISTERS

Data Register

(1F0h, Read/Write - 8 or 16 bits)

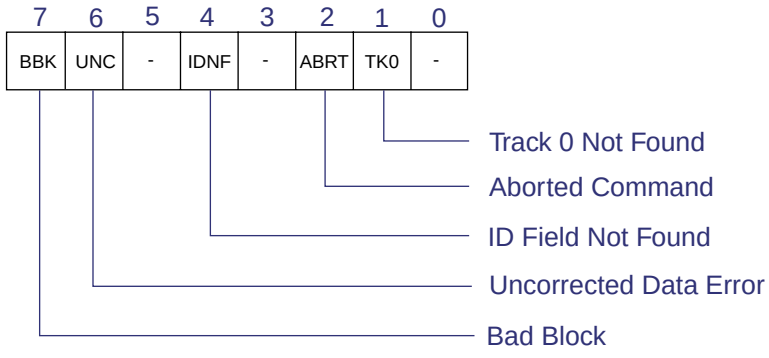
All data transferred between the hard disk and the host CPU passes through the data register. The host CPU passes sector table information during execution of the FORMAT command. ZT 8952's control circuitry dynamically packs and unpacks 16-bit data for 8-bit processors. In 16-bit systems, full 16-bit transfers are performed.

Transfers of ECC bytes are 8-bit transfers during the execution of the Read/Write Long command.

Error Register

(1F1h, Read - 8 bits)

The error register contains status information about the last command executed by the drive. The contents of this register are valid only when the error bit (ER) is set in the status register, except after power-on or after the completion of an internal diagnostic. Error bits are defined in the "Error Register" figure following.



Error Register

BBK—Bad Block

Indicates a bad block mark was detected in the sector's ID field.

UNC—Uncorrectable Data Error

Indicates an uncorrectable data error has been encountered.

IDNF—ID Field Not Found

Indicates the requested sector's ID field was not found.

ABRT—Aborted Command

Indicates the requested command has been aborted due to a drive status error such as Not Ready or Write Fault, or because the command code was invalid.

TK0—Track 0 Not Found

Indicates track 0 was not found during a recalibrate command.

Write Precompensation Register

(1F1h, Write - 8 bits)

This register, originally used for write precompensation, is typically not used. Most IDE drives do not require write precompensation. Some drives define an alternate usage for this register.

Sector Count Register

(1F2h, Read/Write - 8 bits)

The sector count register defines the number of sectors of data to be transferred across the host bus for a subsequent command. For a value of zero written, a count of 256 is used. This count is decremented after each sector is transferred, the register retaining the number of sectors left to transfer. If the command's execution is not successful the register contains the number of sectors that must be transferred to complete the original request. Some drives also define superset commands that use this register.

Sector Number Register

(1F3h, Read/Write - 8 bits)

This register contains the starting sector number for any disk access. The sector number is a value between 1 and the maximum number of sectors per track. At the completion of each sector, and at the end of the command, this register is updated to reflect the last sector read correctly, or the sector on which the error occurred. During multiple sector transfers this register is updated to point to the next sector to be read/written if the previous sector's operation was successful.

Cylinder Low Register

(1F4h, Read/Write - 8 bits)

The cylinder low register contains the low order 8 bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register when the command is executed, to reflect the current cylinder number. The high order 8 bits are handled by the cylinder high register described next.

Cylinder High Register

(1F5h, Read/Write - 8 bits)

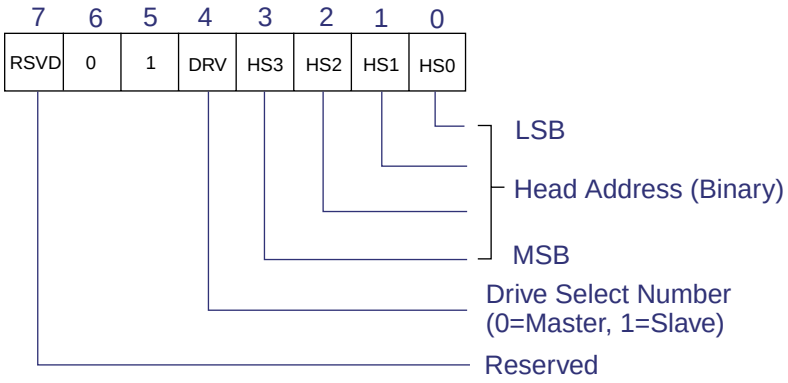
The cylinder high register contains the high order 8 bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register when the command is executed, to reflect the current cylinder number. The low order 8 bits are handled by the Cylinder Low Register described above.

Drive/Head Register

(1F6h, Read/Write - 8 bits)

The drive/head register, also called the SDH register, contains the drive ID number and its head numbers. The host defines the contents of the drive/head register by executing the Initialize Drive Parameters command. At the completion of each sector and at the end of the command this register is updated to reflect the currently selected head.

Register bits are defined in the following figure "SDH Register".



SDH Register

DRV—Drive Select Number

Indicates which drive is currently selected. The primary (master) drive is indicated by logical 0. The secondary (slave) drive in a two-drive system is indicated by logical 1.

HS3—Most Significant Head Address Bit

HS2—

HS1—

HS0—Least Significant Head Address Bit

Status Register

(1F7h, Read - 8 bits)

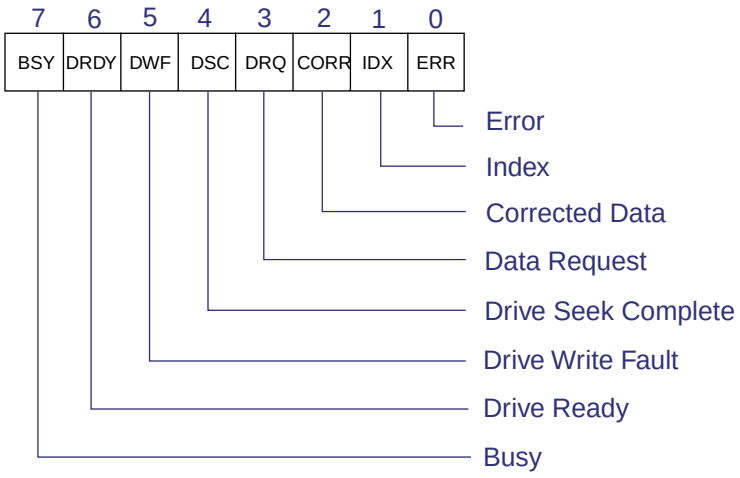
This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the BSY bit is active no other bits are valid. When the BSY bit is not set (logical 0) the remaining bits in the status register are valid.

When an interrupt is pending the drive considers that the host has acknowledged the interrupt when it reads the status register. The bits in this register are defined in the following figure, "Status Register".

BSY—Busy

The BSY bit is active whenever the drive accesses the IDE registers. This locks out the host from accessing the registers. This bit is activated under the following conditions:

- After a hard reset (as opposed to CNTRL-ALT-DEL), or at the activation of the software reset through the digital output register.
- After the host writes to the command register with a read, read long, read buffer, seek recall, initialize drive parameters, verify, identify, or diagnostic command.
- After the transfer of 512 bytes of data during the execution of a write, format track, or write buffer command, or when 512 bytes of data and four ECC bytes have been transferred during the execution of a write long command. When BSY is active (logical 1), any host read of the command block register will return the status register. The host may not write any command blocks when BSY is active.



Status Register

DRDY—Drive Ready

DRDY indicates that the drive is ready to accept a command. When an error occurs this bit remains unchanged until the host reads the status register, then again indicates that the drive is ready. At power-on this bit should be cleared until the drive is up to speed and ready to accept a command.

DWF—Drive Write Fault

When an error occurs this bit remains unchanged until the status register is read, then again indicates the current write fault status.

DSC—Drive Seek Complete

This bit is set after the completion of a seek and when the head has settled over a track. When an error occurs this bit remains unchanged until the host reads the status register, at which time it will again indicate the current seek complete status.

DRQ—Data Request

This bit indicates that the drive is ready to transfer a word or byte of data from the host to the data port.

CORR—Corrected Data

This bit is set when the drive encounters and corrects a data error. This condition does not terminate a multisector read operation.

IDX—Index

This bit is set when the drive detects the index mark during each revolution of the disk.

ERR—Error

This bit indicates that the previous command ended in an error. The error register and other status register bits contain further information as to its cause.

Command Register

(1F7h, Write - 8 bits)

The host CPU sends commands to the drive via an 8-bit code written to the command register. Some drives have additional commands that are a superset of the original AT command set. Consult the drive manufacturer's manual for additional information. The

command is executed as soon as received from the host. Each command may need additional programming of the sector count, sector number, cylinder, and/or drive/head register(s). Command codes and parameters are shown in the following Table, "Command Codes and Parameters".

See Chapter 5, "IDE Command Descriptions," for further details.

Command Codes and Parameters

COMMAND		PARAMETERS				
NAME	CODE	SC	SN	CY	DH	
EXECUTIVE DRIVE DIAGNOSTIC	90h				D*	CORE COMMANDS FOR ALL DRIVES
FORMAT TRACK	50h	Y		Y	Y	
IDENTIFY DRIVE	ECh			D		
INITIALIZE DRIVE PARAMETERS	91h	Y			Y	
READ BUFFER	E4h				D	
READ MULTIPLE	C4h	Y	Y	Y	Y	
READ SECTORS, with retry	20h	Y	Y	Y	Y	
READ SECTORS, no retry	21h	Y	Y	Y	Y	
READ LONG, with retry	22h	Y	Y	Y	Y	
READ LONG, no retry	23h	Y	Y	Y	Y	
READ VERIFY SECTORS, with retry	40h	Y	Y	Y	Y	
READ VERIFY SECTORS, no retry3	41h	Y	Y	Y	Y	
RECALIBRATE	1Xh				D	
SEEK	7Xh			Y	Y	
SET MULTIPLE MODE	C6h	Y			D	
WRITE BUFFER	E8h				D	
WRITE MULTIPLE	C5h	Y	Y	Y	Y	
WRITE SECTORS, with retry	30h	Y	Y	Y	Y	
WRITE SECTORS, no retry	31h	Y	Y	Y	Y	
WRITE LONG, with retry	32h	Y	Y	Y	Y	
WRITE LONG, no retry	33h	Y	Y	Y	Y	
READ DEFECT LIST - Quantum	F0h	Y	Y	Y	Y	QUANTUM SPECIFIC
READ CONFIGURATION- Quantum	F0h	Y	Y	Y	Y	
SET CONFIGURATION- Quantum	F0h	Y	Y	Y	Y	
SET BUFFER MODE-Conner	EFh	N	N	N	D	CONNER SPECIFIC
TRANSLATE COMMAND- Conner	F1h	N	Y	Y	D	
POWER COMMANDS - Conner	Exh	Y	N	N	D	
PHYSICAL SEEK - Conner	F2h	N	N	Y	Y	
DEFECT LIST - Conner	F5h	N	N	N	D	
ENABLE INDEX - Conner	F6h	N	N	N	D	

Key: SC = Sector Count Register CY = Cylinder Register
SN = Sector Number Register DH = Drive/Head Register

Y indicates that the register contains a valid parameter for this command; for the Drive/Head Register, that the drive uses both the drive and head parameters.

D indicates that only the drive parameter is valid, not the head parameter.

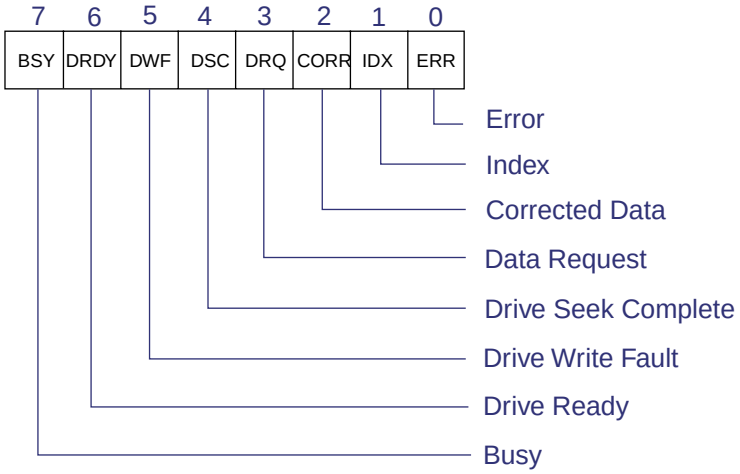
D* indicates that the host addresses the parameter to Drive 0, but both drives execute the command.

Where a parameter is blank, the command does not require the contents of the register.

Alternate Status Register

(3F6h, Read - 8 bits)

The alternate status register contains the same information as does the status register at 1F7h. The only difference is that reading this register does not clear the interrupt, which implies interrupt acknowledgment of the interrupt source. All bit definitions are the same. See the following figure, "Alternate Status Register".

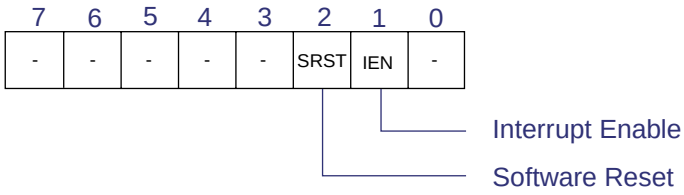


Alternate Status Register

Digital Output Register

(3F6h, Write - 8 bits)

This register contains two control bits as shown in the following figure, "Digital Output Register".



Digital Output Register

IEN—Interrupt Enable

This bit enables the interrupt from the disk drive when set to a logical 0. Setting this bit to a logical 1 will three-state the interrupt.

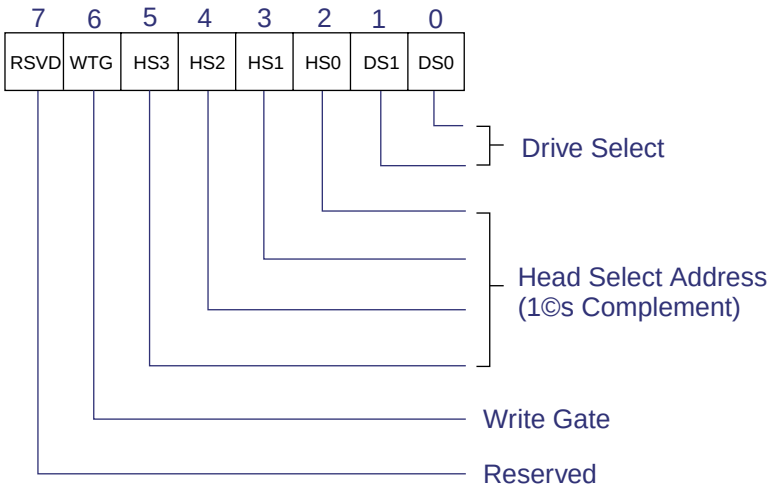
SRST—Software Reset

This bit, when set, will hold the drive in reset until cleared. If two drives are daisy chained, both will be reset simultaneously.

Drive Address Register

(3F7h, Read - 8 bits)

This register loops back the drive select and head select addresses of the currently selected drive. The bits in this register are shown in the following figure, "Drive Address Register".



Drive Address Register

RSVD—Reserved

This bit is reserved for floppy disk drive subsystem usage. In the original AT implementation the hard disk and floppy disk systems shared this register location. The ZT 8952 does not drive this bit on the STD bus in order to avoid contention should a floppy disk controller be in the system.

WTG—Write Gate

This bit is set when a write to the hard disk is in process.

HS3 - HS0—Head Select Address

These bits represent the 1's complement of the binary coded address of the currently selected head. For example, head 3 (0011) selected is represented by 1100, which is the 1's complement of 3 in binary.

DS1 - DS0—Drive Select

These bits represent the drive currently selected. A logical 0 indicates the respective drive is selected. For example, if drive 0 is selected, then DS0 will be logical 0 (active) and DS1 will be logical 1 (inactive).

5. IDE COMMAND DESCRIPTIONS

This chapter describes various commands that can be performed via the IDE command block. These commands are performed by writing to register 1F7h. The core commands common to all drives are presented here. Contact Ziatech for drive-specific support.

CORE COMMANDS

All commands are decoded from the command register. The host computer programs the host interface to perform commands. The interface returns status to the host at command completion. When two drives are daisy chained on the interface, commands are written in parallel to both drives. Only the selected drive executes the command, except for the diagnostic command. In that case, both drives execute the command and the slave drive reports its status to the master via the PDIG signal.

Drives are selected by the DRV bit in the drive/head register and designated as either a master or a slave by a jumper on the drive. When the DRV bit is reset, the master drive is selected. When the DRV bit is set, the slave drive is selected. When drives are daisy chained, one must be jumpered as the master and one as the slave. When a single drive is attached to the interface, it must be jumpered as the master.

To issue a command, load the pertinent registers in the command block, activate the interrupt enable bit (IEN in the digital output register), and then write the command code to the command register. Execution begins as soon as the command register is written.

Recalibrate (1xh)

This command moves the read/write heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY and executes a seek to cylinder 0. The drive then waits for the seek to complete before updating status, resetting BSY, and generating an interrupt. If the drive cannot reach cylinder 0, the error bit is set in the status register and the track 0 bit is set in the error register. An aborted command response is given if the drive is not spinning or is not on track. Upon successful completion of the command, the command block registers are as follows:

Error Register	00
Sector Count	Unchanged
Sector Number	Unchanged
Cylinder Low	00
Cylinder High	00
SDH	Unchanged

Read Sector(s) (2xh)

This command reads from 1 to 256 sectors as specified in the command block, beginning at the specified sector (sector count equal to zero requests 256 sectors).

When the command register is written, the drive sets the BSY bit and begins execution of the command. An aborted command is set if bits 2 and 3 are not equal to zero. An ID Not Found error is returned if incorrect command block parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive searches for the appropriate ID field. If the ID is read correctly, the data field is read into the sector buffer, error bits are set if an error was encountered, the DRQ bit is set, and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector.

Upon command completion, the command block registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command. Multiple sector reads set DRQ and generate an interrupt when the sector buffer is filled at the completion of each sector, and the drive is ready for the data to be read by the host. DRQ is reset and BSY is set immediately when the host empties the sector buffer.

If an error occurs during a multiple sector read, the read terminates at the sector where the error occurs. The command block registers contain the cylinder, head, and sector number of the sector where the error occurs. The host then reads the command block to determine what error has occurred, and on which sector. The flawed data, whether a correctable or non-correctable error, is loaded into the sector buffer. The read does not terminate if the error is correctable. If no error is detected, the cylinder, head, and sector registers are updated to point to the next sequential sector.

A read long may be executed by setting the long bit in command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine if there has been any type of data error. Data bytes are 16-bit transfers and ECC bytes are 8-bit transfers.

Write Sector(s) (3xh)

This command writes from 1 to 256 sectors as specified in the command block, beginning at the specified sector (a sector count equal to zero requests 256 sectors).

When the command register is written, the drive waits for the host to fill the sector buffer with data to be written. No interrupt is generated to start the first buffer fill operation. Once the buffer is full, the drive sets BSY and begins command execution.

If bits 2 and 3 are on, the command terminates with Aborted Command. An ID Not Found error is returned if incorrect command block parameters are passed.

If the drive is not on the desired track, an implied seek is performed. Once on the desired track, the drive searches for the appropriate ID field. If the ID is read correctly, data loaded in the buffer, followed by the ECC bytes, is written to the sector's data field.

Upon command completion, the command block registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

Multiple sector writes set DRQ and generate an interrupt each time the buffer is ready to be filled. DRQ is reset and BSY is set immediately when the host fills the sector buffer.

If an error occurs during a multiple sector write, the write will terminate at the sector where the error occurs. The command block indicates the error's sector location. The host then reads the command block to determine what error has occurred, and on which sector. If no error is detected, the cylinder, head, and sector registers are updated to point to the next sequential sector.

A write long is executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer. The drive itself will not generate the ECC bytes for the write long command. Data byte transfers are 16 bits. ECC bytes are 8-bit transfers.

Verify Sectors (4xh)

This command works the same as the read sectors command except that no data is transferred. Up to 256 sectors are read into the sector buffer, and ECC bytes verified, beginning at the location specified by the command block.

When each sector is verified the command block is updated, but no data request or interrupt is set to indicate that the sector has been verified. When all sectors are verified, an interrupt is generated to indicate that all sectors have been transferred. A value of 00 in the sector count register indicates that 256 sectors are to be verified. Read look-aheads are enabled for this command.

Format Track (50h)

The format command's purpose is to provide a means by which defective sectors may be either marked bad or reassigned. This command has been used on other drives to perform the low level formatting job of placing the header and creating data fields for all tracks on the drive. You do not need to execute a format command prior to operating the drive because all required low level formatting for this hard sectored drive is done during factory certification.

IDE drives support the format command only to allow any sectors that become defective to be handled as required by different operating systems. The format command operates on one logical track at a time. All sectors on that track are filled with zeros.

Seek (7xh)

This command initiates a seek and selects the head specified in the command block. The drive need not be formatted for a seek command to execute properly.

When the command is issued, the drive sets BSY in the status register, initiates the seek, resets BSY, and generates an interrupt. Only the cylinder register is valid for this command. The drive does not wait for the seek to complete before returning the interrupt. Seek complete is set upon completion of the command. If a new command is issued to a drive while a seek is being executed, the drive will wait, with BSY active, for the seek to complete before executing the new command.

No checks are made on the validity of the sector number in the command block. The error bit in the status register and the ID Not Found bit in the error register of the command block is set if an illegal cylinder number is passed.

Execute Drive Diagnostic (90h)

This command performs internal diagnostic tests implemented by the drive. The diagnostic tests are executed only upon receipt of this command.

The drive sets BSY immediately upon receipt of the command. If the drive is a master it performs the diagnostic tests and saves the results. The drive then checks for the presence of a slave drive and waits for up to five seconds for the slave to complete its diagnostics. The slave asserts PDIAG when its diagnostics are successfully completed.

If the slave does not successfully complete its diagnostics the error register is set. The master drive resets BSY and generates an interrupt. The value in the error register should be viewed as a unique 8-bit code and not as a single-bit flag. The interface registers, except for the error register, are set to initial values. The following table, "Error Register Codes", defines the codes in the error register.

Error Register Codes

Error Code	Description
5l 01	no error detected
03	sector buffer error
8x	slave drive failed

Note: If the slave drive fails diagnostics, the master drive will "OR" 80h with its own status and load that code into the error register. If the slave drive passes diagnostics or there is no slave drive connected, the master drive will set bit 7 of the error register in the command block to 0.

Initialize Drive Parameters (91h)

This command enables the host to set the head switch and cylinder increment points for multiple sector operations. The drive activates translate mode only if the sector count register contains the value 17 at the issuance of this command.

In the translate mode the logical head, sector numbers, and cylinder number in the command block are translated to their native physical values as part of the command's execution. The sector, head, and cylinder values in the command block are not checked for validity by this command. If they are invalid no error is reported until an illegal access is made by some other command.

Read Multiple Command (C4h)

The read multiple command is identical to the read sectors operation except that several sectors are transferred to the host as a block without intervening interrupts, and DRQ qualification of the transfer is required only at the start of the block count on each sector. Long transfers are not permitted. The block count, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command, which must be executed prior to the read multiple command. When the read multiple command is issued the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) modulo (block count)

If the read multiple command is attempted before the set multiple mode command has been executed or when read multiple commands are disabled, the read multiple operation is rejected with an aborted command error.

Disk errors encountered during read multiple commands are reported at the beginning of the block or partial block transfer, but DRQ is set and the transfer takes place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks are transferred only if the error is a correctable data error. All other errors cause the command to stop after transfer of the block containing the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

Read look-aheads are not active for this command.

Write Multiple Command (C5h)

The write multiple command performs similarly to the write sectors command except that the controller sets BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid. Several sectors are transferred to the host as a block without intervening interrupts, and DRQ qualification of the

transfer is required only at the start of the block instead of on each sector. There is no interrupt request prior to the first block transfer.

The block count, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command, which must be executed prior to the write multiple command. When the write multiple command is issued, the sector count register contains the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) modulo (block count)

If the write multiple command is attempted before the set multiple mode command has been executed or when write multiple commands are disabled, the write multiple operation is rejected with an aborted command error.

All disk errors encountered during write multiple commands are reported after the attempted disk write of the block or partial block is transferred. The write operation ends with the sector in error, even if in mid-block. In the event of an error, subsequent blocks are not transferred. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

Set Multiple Code (C6h)

This command enables the controller to perform read and write multiple operations and establishes the block count for these commands. Prior to command issuance, the sector count register should be loaded with the number of sectors per block. Block sizes supported are 1, 2, 4, 8, and 16.

Upon receipt of the command, the controller sets BSY and looks at the sector count register contents. If the register contents are valid and supported block count is supplied, that value is loaded for all subsequent read and write multiple commands and execution of these commands is enabled. Any unsupported block count in the register will result in an aborted command error and read and write multiple commands being disabled. If the sector count register contains 0 when the command is issued, read and write multiple commands are disabled.

Read Buffer (E4h)

The read buffer command allows the host to read the current contents of the drive's sector buffer. Only the command register is valid for this command. When this command is issued the drive will set BSY, set up the sector buffer for a read operation, set DRQ, reset BSY, and generate an interrupt. The host may then read up to 512 bytes of data from the buffer.

Write Buffer (E8h)

The write buffer command allows the host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the command register is valid for this command. When this command is issued the drive will set BSY, set up the sector buffer for a write operation, set DRQ, reset BSY, and generate an interrupt. The host may then write up to 512 bytes of data to the buffer.

Identify Drive (ECh)

The identify command allows the host to receive parameter information from the drive. When the command is issued the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The host may then read the information out of the sector buffer.

The parameter words in the buffer are arranged as follows:

- All reserved bits or words should be zeros
- All numbers are given in hexadecimal format, right justified
- All reserved words are zero

Word Parameters

Word 00	Drive dependent
Word 01	Number of fixed cylinders
Word 02	Number of removable cylinders
Word 03	Number of heads
Word 04	Number of unformatted bytes/physical track
Word 05	Number of unformatted bytes/sector
Word 06	Number of physical sectors/track
Word 07	Vendor unique
Word 08	Vendor unique
Word 09	Vendor unique
Word 10-19	Serial number
Word 20	Buffer type
Word 21	Buffer size in 512 byte increments
Word 22	Number of ECC bytes passed on read/write long commands
Word 23-26	Controller firmware revision
Word 27-46	Model number
Word 47	Reserved

OPERATIONS DESCRIPTION

The following pages describe operations that span several of the commands covered in the preceding section.

Reset

A reset condition will set the drive busy, allowing the drive to perform the proper initialization required for normal operation. A reset condition can be generated in four ways. There are two hardware resets, one from the host and one from the drive power sense circuitry. These are set high when the system and the drive, respectively, acknowledge good power. The other two resets are software generated. The host can write to the digital output register and set the reset bit. The host software reset condition will persist until the reset bit is written to a zero. The drive microprocessor can set reset through a write to a register. The drive processor reset is valid for one cycle and like all other resets is ORed together to generate the signals that initialize the hardware.

Once the reset has been removed and the drive has been re-enabled, with BSY still active, the drive will perform any necessary hardware initialization, clear any previously programmed drive parameters, revert to the defaults, load the command block registers with their initial values, and reset BSY. No interrupt is generated when initialization is complete.

Initial values for the command block registers areas are as follows:

Error Register	01h
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Drive/Head Register	00h

BSY Operation

The latch holding BSY is set in a number of ways. A reset condition as described above is one way. Another method occurs when the host issues a command. For a read type command, the register is clocked BSY on the host write of the command register. The disk controller and microprocessor prepare the data to return and set the drive not busy to allow the host access to the data requested.

When a write type command is issued, the IO16 Enable and Data Request are set. After the data to be written is put into the RAM buffer the BSY flip-flop is set. This can be done only when the buffer is full in write mode and it is not the last transfer. Write type commands include Write Sector(s), Format, and Write Sector Buffer.

A drive can respond properly to a command only when the drive microprocessor is active. When BSY is active the drive has read and write access to the command block registers. The host, however, can read only the status register and alternate status register. Any attempted host read of a command block register while BSY is active results therefore in a read of the status register instead. The BSY latch can be cleared only by the drive microprocessor, which can set or reset the BSY flip-flop. When BSY is inactive the host has read and write access to all command block registers.

Data Retry Algorithm

When an ECC error is detected in the data field during a read operation, the retry algorithm shown in the following table "Data Retry Algorithm" is used.

Step 1	read retry
Step 2	read retry
Step 3	read retry
Step 4	apply ECC to Step 3
Step 5	read retry with +65 micro inch offset
Step 6	apply ECC to Step 5
Step 7	read retry
Step 8	apply ECC to Step 7
Step 9	read retry with -65 micro inch offset
Step 10	apply ECC to Step 9
Step 11	read retry
Step 12	read retry
Step 13	read retry
Step 14	read retry
Step 15	read retry
Step 16	read retry

In the event of a hard error steps 1-16 are repeated eight times for a total of 128 retries. Allowing 17 ms for each read retry and 75 ms for each ECC correction, the total time is 4.0 seconds (17 ms * 12 * 8 + 75 ms * 4 * 8 = 4032 ms) to return a non-recoverable

error condition to the host. With the exception of disabling retries (retry count = 0), the retry count of 128 is currently not changeable.

When the read/write heads are switched or a seek is completed the drive will attempt an offtrack read when less than 200 µinches from the center of the track. If this attempt is successful 17 ms of latency is saved and seek performance of the drive will exceed the specification. When this attempt is not successful the drive will read the sector on the next pass as in a normal read operation (100 µinches) and the seek specification is met.

Header Retry Algorithm

When an ECC error is detected while reading the header field, 20 read retries are attempted before a header error is returned to the host. If a header is successfully read before the 20 retries are completed, the header retry counter is reset and the data field is processed. For a hard error in the data field the total amount of time for 20 retries is 0.34 seconds (17 ms * 20 = 340 ms). Header retries cannot be disabled from the interface, nor can the header retry count be changed.

ERROR REPORTING

In general, errors are detected in the following fashion by the drive microprocessor. At the start of execution of a command the command register is checked for conditions that would lead to an aborted command. The operation is then attempted. Any subsequent error terminates the command at the point of discovery. Errors valid for each command are summarized in the "Error Reporting Matrix" table following. Any subsequent error terminates the command at the point of discovery.

The following abbreviations are used in the matrix, where V means the error type is valid for this command:

BBK	bad block detected
UNC	non-correctable data error
IDNF	requested ID not found
ABRT	aborted command error
TKO	track 0 not found error
DRDY	disk drive not ready detected
DWF	disk drive write fault detected
DSC	disk drive seek complete not detected
CORR	corrected data error
ERR	error bit in the status register

Error Reporting Matrix

	BBK	UNC	IDNF	ABRT	TKO	DRDY	DWF	DSC	CORR	ERR
Recalibrate				V	V	V	V	V		V
Read Sector	V	V	V	V		V	V	V	V	V
Read Long	V		V	V		V	V	V		V
Write Sector	V		V	V		V	V	V		V
Write Long	V		V	V		V	V	V		V
Read Verify	V	V	V	V		V	V	V	V	V
Format Track			V	V		V	V	V		V
Seek			V	V		V	V	V		V
Execute Drive										
Diagnostics				V						V
Initiator Drive										
Parameters				V						
Read Multiple	V	V	V	V		V	V	V	V	V
Write Multiple	V		V	V		V	V	V		V
Set Multiple				V						V
Read Buffer				V						V
Write Buffer				V						V
Identify Drive				V						V
Cache On/Off				V						V

The following errors are valid upon issuing an invalid command code:

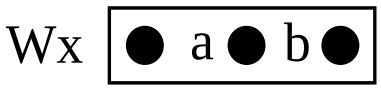
Invalid Command Error Codes

	BBK	UNC	IDNF	ABRT	TKO	DRDY	DWF	DSC	CORR	ERR
Invalid Command Code					V					V

A. JUMPER CONFIGURATIONS

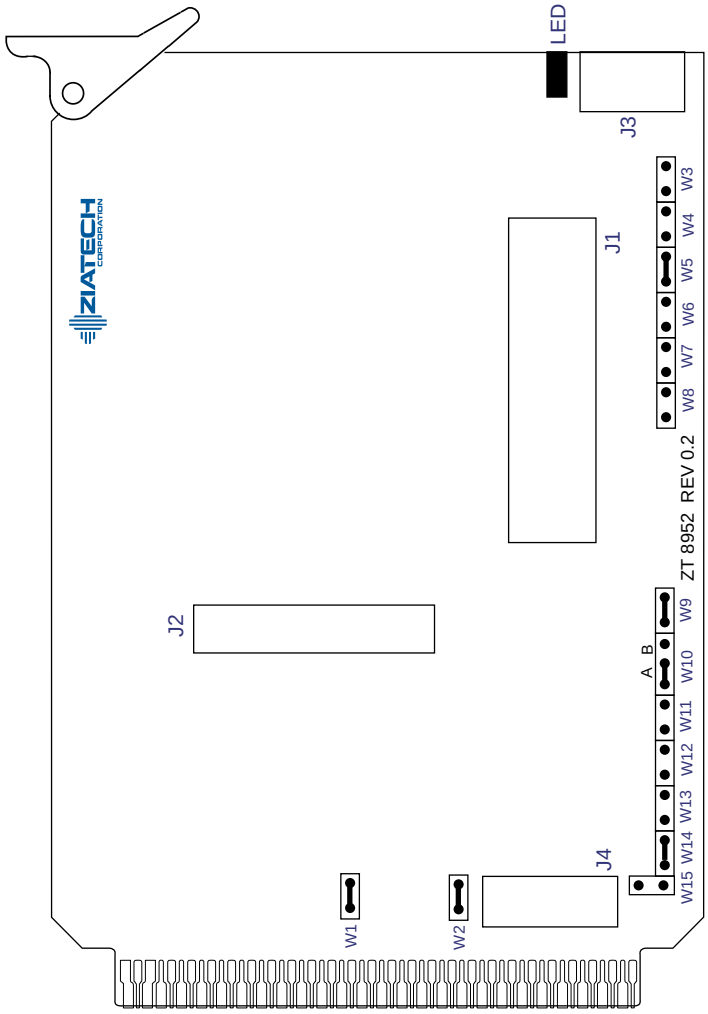
JUMPER OPTIONS

The ZT 8952 includes several jumper options that tailor the board's operation to the requirements of specific applications. Jumpers having only two jumper posts are labeled Wx, where x defines the jumper number. Jumpers having three jumper posts are labeled Wx "a" and "b." These jumpers have two possible selections, where "a" is one selection and "b" is another. See the below figure, "Triple Post Jumpers".



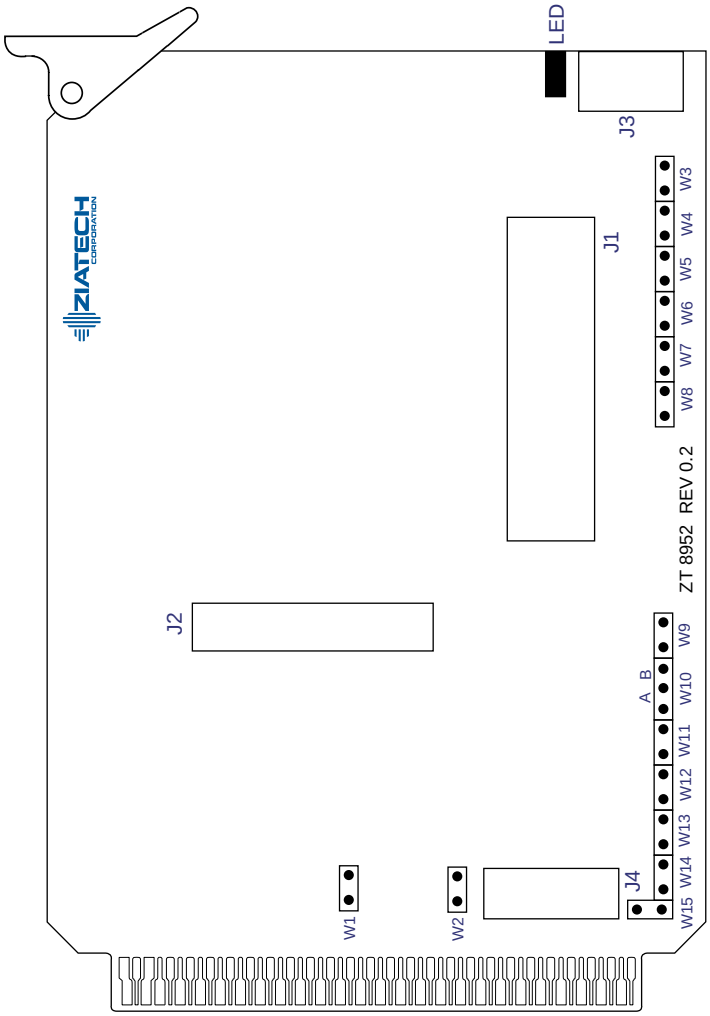
Triple Post Jumpers

Default jumper configurations for the ZT 8952 board are illustrated in the figure below, "Default Jumper Locations". The following figure, "Customer Jumper Locations", is used to document customer-specific configurations.



Note: W2 in for 16-bit transfers only.

Default Jumper Locations



Customer Jumper Locations

The table below, "Jumper Cross Reference", divides the jumpers into functional groups and lists page numbers where a description of the jumpers can be found. These descriptions are presented in numerical order following the table. Standard default jumper settings are indicated in the table by a dagger (†).

Jumper Cross Reference

FUNCTION	JUMPER #
8-bit/16-bit Transfer Mode	W2
Backplane Interrupt Selection	W11-W15
Disable/Enable Controller Logic	W9
Frontplane Interrupt Selection	W3-W7
IDE Diagnostic	W8
IDE Interrupt Mode	W10A, W10B
IRQx Polarity Selection	W1

JUMPER DESCRIPTIONS

W1

Selects the polarity of the Slot Specific Interrupt. Installed, IRQx is driven low during an active interrupt. Not installed, IRQx is driven high. Polarity selection is important for STD 32 permanent master interrupt processing. STD 32 allows for both. Factory default is installed.

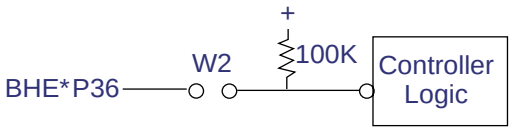
W1	FUNCTION
†IN	IRQx driven low during active interrupt
OUT	IRQx driven high during active interrupt

† Factory default configuration

W2

Selects whether the control logic uses BHE*. Installed, BHE* selects the high byte of a 16-bit transfer to or from register 1F0h. See below figure "8-Bit/16-Bit Transfer Jumper". Factory default is installed. Install W2 in systems with ZT 8911, ZT 8902, ZT 8901, and STD 32 CPUs performing 16-bit transfers.

W2	FUNCTION
†IN	BHE* enabled
OUT	BHE* ignored



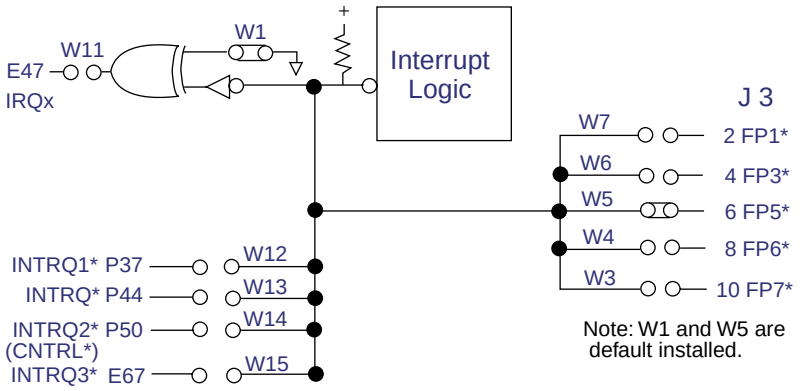
8-Bit/16-Bit Transfer Jumper

† Factory Default Configuration

W3-W7

Selects which frontplane interrupt to drive. The BIOS does not use interrupts for hard disk transfers. See the figure "Interrupt Structure" below for details. Factory default is W5 installed.

JUMPER IN	FUNCTION
W3	FP7* enabled
W4	FP6* enabled
†W5	FP5* enabled
W6	FP3* enabled
W7	FP1* enabled



Interrupt Structure

† Factory Default Configuration

W11-W15

Selects which backplane interrupt to drive the IDE interrupt status. The default is to drive no backplane interrupt. Factory Default is none installed.

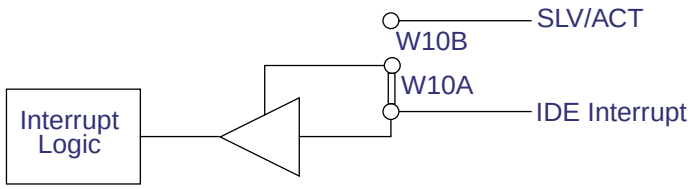
JUMPER IN	FUNCTION
W11	IRQx enabled (STD 32 slot-specific interrupt)
W12	INTRQ1* enabled
W13	INTRQ* enabled
W14	INTRQ2* enabled
W15	INTRQ3* enabled (STD 32 only)

Note: W15 is available on revisions 0.2 or greater. ZT 8911 or ZT 8902 CPU systems should have W15 installed.

W10A, W10B

Selects interpretation mode for IDE interrupts. W10A enables and drives the interrupt active. W10B drives the interrupt active but does not enable (gate it) on the backplane unless the SLV/ACT signal is driven high by the IDE interface. This maintains compatibility with some PC/AT Conner Peripheral IDE interface cards. See the following figure "IDE Interrupt Interpretation" for details. Factory default is W10A installed.

JUMPER IN	FUNCTION
†W10A	Enables, drives active IDE interrupts
W10B	Drives active IDE interrupts enables when SLV/ACT is driven high



IDE Interrupt Interpretation

† Factory default configuration

W8

Drives PDIAG low on the IDE interface. Some drives require this at all times. No drives currently shipped by Ziatech require installation of this jumper. Factory default is not installed.

W8	FUNCTION
IN	PDIAG low (logical 0)
†OUT	PDIAG high (logical 1)

W9

Enables or disables control logic. Removing this jumper lets a drive be powered by the ZT 8952 but controlled via an external IDE interface. Removing the jumper does not let the board drive the backplane with data during backplane reads to I/O space normally decoded by the ZT 8952. This jumper is normally left in. Factory default is installed.

W9	FUNCTION
†IN	Enables control logic
OUT	Disables control logic

† Factory default configuration

B. SPECIFICATIONS

This appendix provides specifications for ZT 8952 and ZT 8953 integrated drive units. The ZT 8952-0 (non-integrated controller) is also represented. The electrical and environmental specifications of the integrated drives are greatly affected by requirements of the drive itself. This is seen when the base ZT 8952-0 is compared to integrated versions.

All data is current and will be updated when appropriate. Contact Ziatech for further details on individual drives.

The term "typical" when used with current requirements for integrated drives means the sum of base controller typical (ZT 8952-0) plus the Random Read/Write current requirements. "Maximum" means the sum of the maximum controller current plus the spin-up current.

STD-80 Compatibility

The ZT 8952 is designed for use in an STD 32 backplane environment. While designed to be backward compatible with STD-80 systems, the ZT 8952 is not guaranteed to work in all system topologies.

Requirements

Current, environmental, and mechanical specifications are presented in the table below.

Current, Environmental, and Mechanical Requirements

	PRODUCT	CURRENT REQUIREMENTS AT +5V TYP. (mA) (R/W)	+5V MAX. (mA) (Spinup)	+12V TYP. (mA) (R/W)	+12V MAX. (mA) (Spinup)	AVG. SEEK (ms)	ENVIRONMENTAL REQUIREMENTS STORAGE TEMPERATURE (°C)	OPERATING TEMPERATURE (°C)	% HUMIDITY (NONCONDENSING AT 40°C)	MAXIMUM OPERATING ALTITUDE (FEET)	MAXIMUM STORAGE ALTITUDE (FEET)	MTBF (K HOURS)	MECHANICAL SPECIFICATIONS CARDCAGE SLOTS REQUIRED	BOARD WEIGHT (LBS)	BOARD HEIGHT (INCHES)	VIBRATION (G) Non Op.	VIBRATION (G) Op.	SHOCK (G) Non Op.	SHOCK (G) Op.
2 1/2" DRIVES	ZT 8952-0	320	470	-	-	-	-40 to +85	0 to +65	5 to 95	-	-	-	1	0.2	.35	-	-	-	-
	ZT 8952-40†	880	1580	-	-	15	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	100	2	0.7	.75	5	0.5	100	10
	ZT 8952-80†	880	1580	-	-	16	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	100	2	0.7	.75	5	0.5	100	10
	ZT 8952-85	710	1250	-	-	15	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	100	1	0.4	0.5	5	0.5	125	20
	ZT 8952-120	770	1580	-	-	16	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	150	2	0.7	.75	5	0.5	100	10
3 1/2" DRIVES	ZT 8953-50†	630	780	410	1000	19	-40 to +65	+4 to +50	8 to 85	+10,000	+40,000	60	3	1.3	1.4	2	1	60	6
	ZT 8953-80	710	730	140	1100	17	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	150	3	1.5	1.4	5	0.5	100	10
	ZT 8953-120	600	850	200	1100	19	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	150	3	1.5	1.4	4	0.5	75	5
	ZT 8953-170	710	730	140	1100	17	-40 to +60	+5 to +55	8 to 80	+10,000	+40,000	150	3	1.5	1.4	5	0.5	100	10

† Obsolete. Data provided for reference.

STD Bus Loading Characteristics

Unit load is a convenient method of specifying input and output drive capability for STD bus cards. In STD bus systems one unit load is equal to one LSTTL load as follows:

- Maximum high level input current: 20 mA
- Maximum low level input current: -400 mA

The STD bus unit load reflects input current requirements at worst case conditions over recommended supply voltage and ambient temperature ranges. An output rate of 60 unit loads can drive 60 STD bus cards that have an input rate of one unit load.

The "STD Bus Signal Loading, P Connector" table below shows STD-80 signals for P Connectors. The "STD Bus Signal Loading, E Connector" table shows signals used in STD 32 systems. These signals are referred to as E signals.

STD Bus Signal Loading, P Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
RSVD	0		E2	E1			GND
XA23	0		E4	E3		0	XA19
XA22	0		E6	E5		0	XA18
XA21	0		E8	E7		0	XA17
XA20	0		E10	E9		0	XA16
RSVD	0		E12	E11		0	NOWS*
+5 VDC			E14	E13			+5 VDC
DREQX*			E16	E15		0	DAKx*
GND			E18	E17			GND
D31	0		E20	E19		0	D27
D30	0		E22	E21		0	D26
D29	0		E24	E23		0	D25
D28	0		E26	E25		0	D24
GND			E28	E27		0	D23
D15	2	58	E30	E29		0	D22
D14	2	58	E32	E31		0	D21
D13	2	58	E34	E33		0	D20
D12	2	58	E36	E35			GND
D11	2	58	E38	E37		0	D19
D10	2	58	E40	E39		0	D18
D9	2	58	E42	E41		0	D17
D8	2	58	E44	E43		0	D16
MASTER16*			E46	E45			GND
AENx*	0		E48	E47	60	0	IRQx
BE3*	0		E50	E49		0	BE1*
BE2*	0		E52	E51		0	BE0*
GND			E54	E53		0	MEM16*
W-R	0		E56	E55		0	M-IO
DMAIOR*	0		E58	E57		0	DMAIOW*
EX8*	0		E60	E59	60	0	IO16*
START*	0		E62	E61		0	CMD*
EX32*	0		E64	E63		0	EX16*
T-C	0		E66	E65		0	EXRDY
+5 VDC			E68	E67		0	LOCK*
MREQx*			E70	E69		0	MAKx*
MSBURST*			E72	E71		0	SLBURST*
XA31*	0		E74	E73		0	XA27*
XA30*	0		E76	E75		0	XA26*
XA29*	0		E78	E77		0	XA25*
XA28*	0		E80	E79		0	XA24*

Notes:

REQ indicates required connection

[1] High order address bits multiplexed over databus D0-D7

[2] PCI is connected directly to PCO

STD Bus Signal Loading, E Connector

PIN (CIRCUIT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC							PIN (COMPONENT SIDE) / OUTPUT DRIVE / INPUT LOAD / MNEMONIC
LOCK*	0		E2	E1			GND
XA23	0		E4	E3		0	XA19
XA22	0		E6	E5		0	XA18
XA21	0		E8	E7		0	XA17
XA20	0		E10	E9		0	XA16
RSVD	0		E12	E11		0	NOWS*
+5 VDC			E14	E13			+5 VDC
DREQX*			E16	E15		0	DAKx*
GND			E18	E17			GND
D31	0		E20	E19		0	D27
D30	0		E22	E21		0	D26
D29	0		E24	E23		0	D25
D28	0		E26	E25		0	D24
GND			E28	E27		0	D23
D15	2	58	E30	E29		0	D22
D14	2	58	E32	E31		0	D21
D13	2	58	E34	E33		0	D20
D12	2	58	E36	E35			GND
D11	2	58	E38	E37		0	D19
D10	2	58	E40	E39		0	D18
D9	2	58	E42	E41		0	D17
D8	2	58	E44	E43		0	D16
MASTER16*			E46	E45			GND
AENx*	0		E48	E47	60	0	IRQx
BE3*	0		E50	E49		0	BE1*
BE2*	0		E52	E51		0	BE0*
GND			E54	E53		0	MEM16*
W-R	0		E56	E55		0	M-IO
DMAIOR*	0		E58	E57		0	DMAIOW*
EX8*	0		E60	E59	60	0	IO16*
START*	0		E62	E61		0	CMD*
EX32*	0		E64	E63		0	EX16*
T-C	0		E66	E65		0	EXRDY
+5 VDC			E68	E67	60	0	INTRQ3*
MREQx*			E70	E69		0	MAKx*
MSBURST*			E72	E71		0	SLBURST*
XA31*	0		E74	E73		0	XA27*
XA30*	0		E76	E75		0	XA26*
XA29*	0		E78	E77		0	XA25*
XA28*	0		E80	E79		0	XA24*

Notes:

REQ indicates required connection

[1] High order address bits multiplexed over databus D0-D7

[2] PCI is connected directly to PCO

MECHANICAL

Card Dimensions and Weight

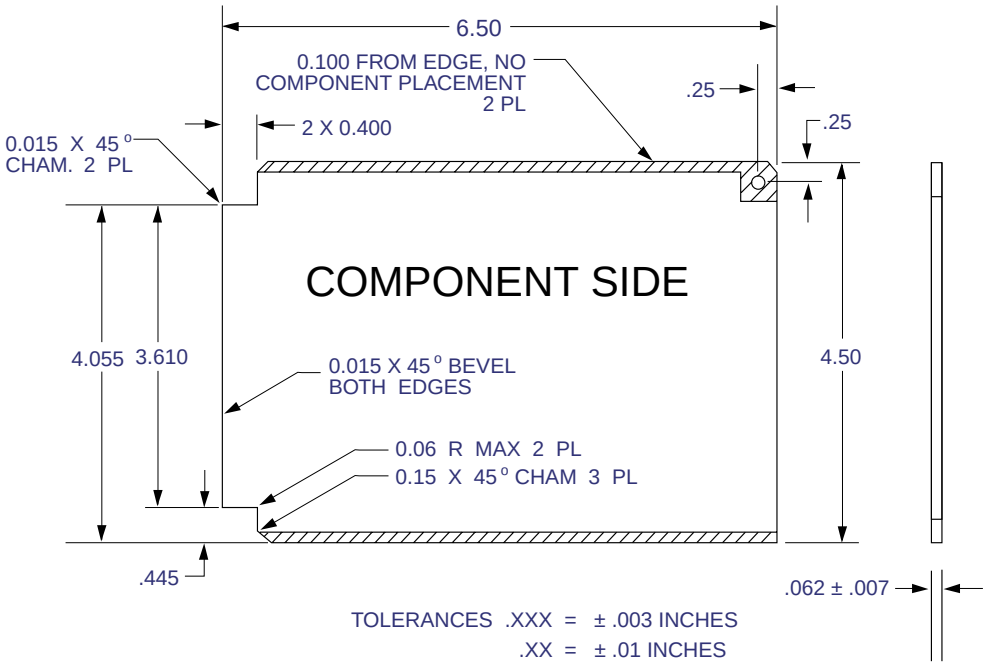
ZT 8952 meets the STD 32 bus specification for all mechanical parameters. In a card cage with 0.625 inch spacing the ZT 8952 requires one card slot as a stand-alone card. As an integrated hard disk controller it requires up to 4 slots. Configurations and card slot requirements are shown in "Current, Environmental, and Mechanical Requirements" table.

Board Length .....6.5000 ± .010

Board Width .....4.500 ± 0.010

Board Thickness .....0.062 ± 0.008

Board dimensions are shown in figure "Board Dimensions" below.



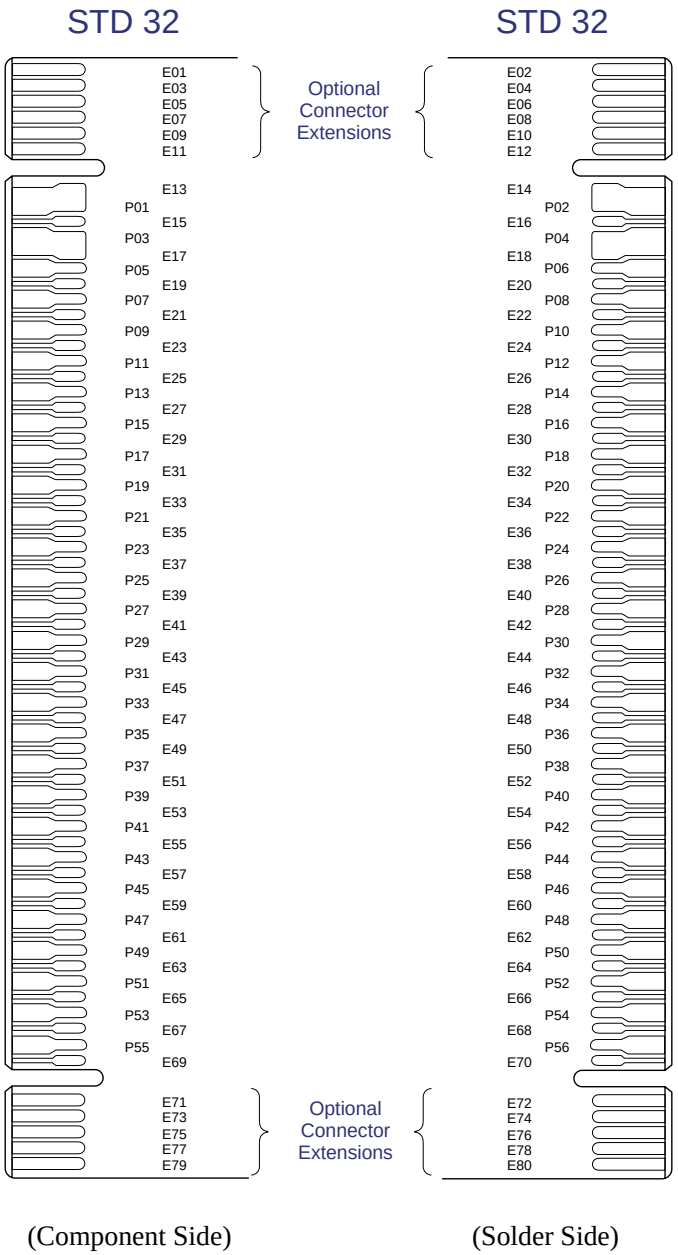
Board Dimensions

Connectors

The ZT 8952 includes four connectors plus the backplane interface connector. The backplane interface is compatible with the STD 32 specification.

Backplane Interface - STD 32 Connector

The backplane interface comprises two sets of finger patterns interlaced so that the ZT 8952 interfaces to both STD-80 and STD 32 buses. The "P" fingers are the original STD-80 signals. The additional STD 32 signals are designated "E" fingers and interlace with the "P" fingers to create the STD 32 interface. This unique patented feature allows backward compatibility when ZT 8952 is inserted in STD-80 backplanes and also allows insertion of older STD-80 boards in STD 32 backplanes. Pin-to-pin spacing on the STD 32 connector is 0.0625 inches.



STD 32 P/E Connector Pinout

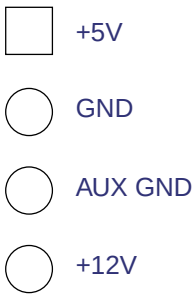
Frontplane Connectors

J1: 3½ inch IDE Drive Interface. J1 is a right angle 0.1 inch dual row interface for connecting to 3½ inch IDE drives using CBA-90096. A total of 40 signals on this connector are replicated on J2. The table "J1 and J2 Pin Assignments" indicates the signal definition for both J1 and J2. Remotely mounted drives use this connector for interfacing. No power is supplied via this connector.

J2: 2½ inch IDE Drive Interface. This 2 mm connector location can be loaded with either a 2 mm header style connector for ribbon cable interfacing or a right angle receptacle for direct mounting of the hard disk to the ZT 8952. J2 is composed of 44 signals, four being added to power the 2½ inch disk drive directly. The 40 signals remaining are in common with those of J1, and comprise the control interface for the IDE interface. The table "J1 and J2 Pin Assignments" shows the signal definition for both J1 and J2.

J3: Frontplane Interrupt Interface. J3 is a 10-pin male transition connector with 0.1 inch pin-to-pin spacing. J3 provides a mechanism for driving the IDE interrupt to the host processor when no backplane interrupts are available for this service. Pin assignments are given in the following table "Frontplane Interrupt Connector". The mating connector is a T&B Ansley #622-1030 or equivalent.

J4: 3½ inch Hard Disk Power Connector. This interface location provides power to integrated 3½ inch drives when the board is shipped as a ZT 8953-XXX. The figure below "J4 3½-Inch Drive Power Connector" illustrates the pinout for this location.



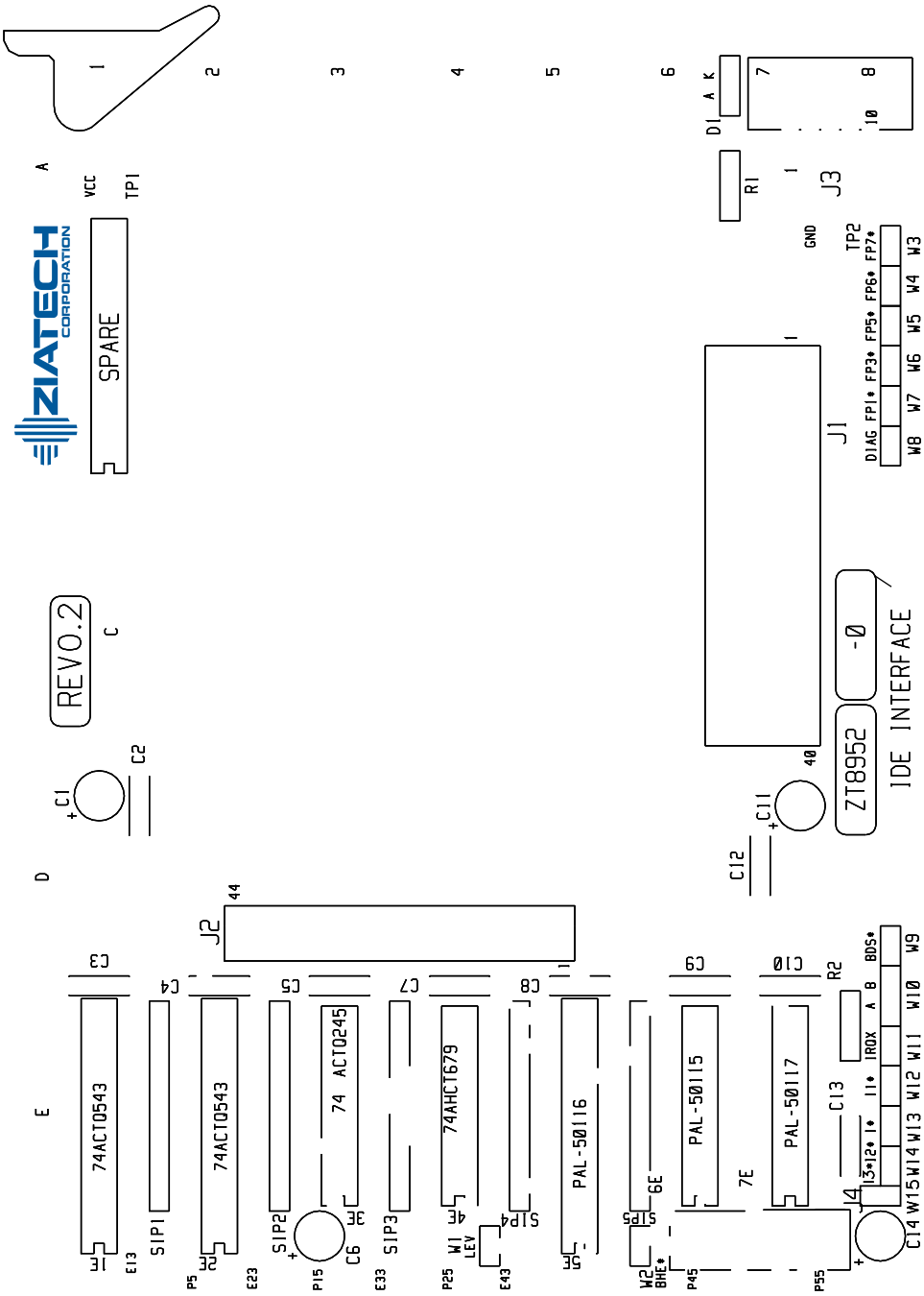
J4 3½-Inch Drive Power Connector Pinout

J1 and J2 Pin Assignments

Pin Number	Signal	Pin Number	Signal	
01	-Host Reset	02	GND	J1 & J2
03	+Host Data 7	04	+Host Data 8	
05	+Host Data 6	06	+Host Data 9	
07	+Host Data 5	08	+Host Data 10	
09	+Host Data 4	10	+Host Data 11	
11	+Host Data 3	12	+Host Data 12	
13	+Host Data 2	14	+Host Data 13	
15	+Host Data 1	16	+Host Data 14	
17	+Host Data 0	18	+Host Data 15	
19	GND	20	Key	
21	Reserved	22	GND	
23	-Host IOW	24	GND	
25	-Host IOR	26	GND	
27	Reserved	28	+Host ALE	
29	Reserved	30	GND	
31	+Host IRQ14	32	+Host IO16	
33	+Host ADDR 1	34	-Host PDIAG	
35	+Host ADDR 0	36	+Host ADDR 2	
37	-Host CSO	38	-Host CS1	
39	-Host SLV/ACT	40	GND	
41	VCC	42	VCC	J2 Only
48	GND	44	Reserved	

Frontplane Interrupt Connector

Pin	Signal	Description
2	FP1*	Frontplane Interrupt 1
4	FP3*	Frontplane Interrupt 3
6	FP5*	Frontplane Interrupt 5
8	FP6*	Frontplane Interrupt 6
10	FP7*	Frontplane Interrupt 7



Assembly Diagram

C. GLOSSARY

This appendix lists the command codes and defines important terms and acronyms used in this manual.

COMMAND CODES

Command Codes and Parameters

COMMAND		PARAMETERS				
NAME	CODE	SC	SN	CY	DH	
EXECUTIVE DRIVE DIAGNOSTIC	90h				D*	CORE COMMANDS FOR ALL DRIVES
FORMAT TRACK	50h	Y		Y	Y	
IDENTIFY DRIVE	ECh			D		
INITIALIZE DRIVE PARAMETERS	91h	Y			Y	
READ BUFFER	E4h				D	
READ MULTIPLE	C4h	Y	Y	Y	Y	
READ SECTORS, with retry	20h	Y	Y	Y	Y	
READ SECTORS, no retry	21h	Y	Y	Y	Y	
READ LONG, with retry	22h	Y	Y	Y	Y	
READ LONG, no retry	23h	Y	Y	Y	Y	
READ VERIFY SECTORS, with retry	40h	Y	Y	Y	Y	
READ VERIFY SECTORS, no retry3	41h	Y	Y	Y	Y	
RECALIBRATE	1Xh				D	
SEEK	7Xh			Y	Y	
SET MULTIPLE MODE	C6h	Y			D	
WRITE BUFFER	E8h				D	
WRITE MULTIPLE	C5h	Y	Y	Y	Y	
WRITE SECTORS, with retry	30h	Y	Y	Y	Y	
WRITE SECTORS, no retry	31h	Y	Y	Y	Y	
WRITE LONG, with retry	32h	Y	Y	Y	Y	
WRITE LONG, no retry	33h	Y	Y	Y	Y	
READ DEFECT LIST - Quantum	F0h	Y	Y	Y	Y	QUANTUM SPECIFIC
READ CONFIGURATION- Quantum	F0h	Y	Y	Y	Y	
SET CONFIGURATION- Quantum	F0h	Y	Y	Y	Y	
SET BUFFER MODE-Conner	EFh	N	N	N	D	CONNER SPECIFIC
TRANSLATE COMMAND- Conner	F1h	N	Y	Y	D	
POWER COMMANDS - Conner	Exh	Y	N	N	D	
PHYSICAL SEEK - Conner	F2h	N	N	Y	Y	
DEFECT LIST - Conner	F5h	N	N	N	D	
ENABLE INDEX - Conner	F6h	N	N	N	D	

Key: SC = Sector Count Register CY = Cylinder Register
SN = Sector Number Register DH = Drive/Head Register

Y indicates that the register contains a valid parameter for this command; for the Drive/Head Register, that the drive uses both the drive and head parameters.

D indicates that only the drive parameter is valid, not the head parameter.

D* indicates that the host addresses the parameter to Drive 0, but both drives execute the command.

Where a parameter is blank, the command does not require the contents of the register.

TERMINOLOGY

backplane	Refers to the STD bus.
BHE*	A former STD-80 signal called MEMEX. See *MEMEX*.
BIOS	Basic Input Output System. This code typically provides low level basic I/O services.
CNTRL*	Control. An auxiliary timing signal or an interrupt signal on the STD bus.
CPU	Central Processing Unit.
DMA	Direct Memory Access. Can access memory directly without CPU requirements. Use for faster data transfer rate when processing of I/O data on a byte-by-byte basis is not required.
FIFO	First In First Out. Register cue that sequences accesses in the same order as programmed.
frontplane	User accessible symbols not routed through the STD bus. Also refers to the front of a card where the I/O connectors reside. The connectors are typically latching and may be used for chaining interrupts from one card to another.
IDE	Integrated Drive Electronics (IDE) refers to a disk drive that has the control logic embedded on the drive itself. There are many types of IDE drives. The generally accepted reference is to a PC-AT compatible controller that is embedded. The ZT 8952 uses a PC-AT IDE type disk drive.
INTRQ*	Interrupt request. Processor card input signals that conditionally interrupt the program when enabled by a specific program instruction.
IRQx	Slot-specific interrupt request used within STD 32 systems.
IXL	Slot-specific interrupt support, low-level asserted.
IXP	Slot-specific interrupt support, positive edge-triggered.
Mbps	Megabits per second. Used to define floppy disk serial transfer rates between the drive and the controller.
MEMEX	Memory Expansion. Output to STD bus used to expand memory access capability.
RAM	Random Access Memory.

register	A memory location for operating parameters.
SA8	STD-80 8-bit transfer capability. SA8 is used within STD 32 to define transfer types.
SA16	16-bit transfer using STD-80 control signals. Used to define STD 32 transfer type.
STD bus	The collection of signals defined on P connector to support 8-bit transfers between masters and slaves.
STD 32 bus	The extension to the STD bus to support 8-bit, 16-bit, and 32-bit transfers, backplane DMA, bus arbitration, and slot-specific configuration.
STD-80bus	STD bus signals that are compatible with Intel 80XX series microprocessors.

D. CUSTOMER SUPPORT

This appendix offers technical and sales assistance information for this product, warranty information, and necessary information for the return of a Ziatech product.

TECHNICAL/SALES ASSISTANCE

If you have a technical question, please call Ziatech's Customer Support Service at the number below, or e-mail our technical support team at tech_support@ziatech.com. Ziatech also maintains an FTP site located at ftp://ziatech.com/Tech_support.

If you have a sales question, please contact your local Ziatech Sales Representative or the Regional Sales Office for your area. Address, telephone and FAX numbers, and additional information are available at Ziatech's website, located at http://www.ziatech.com.

Corporate Headquarters

1050 Southwood Drive

San Luis Obispo, CA 93401 USA

Tel (805) 541-0488

FAX (805) 541-5088

RELIABILITY

Ziatech takes extra care in the design of the product in order to ensure reliability. The product was designed in top-down fashion, using the latest in hardware and software design techniques, so that unwanted side effects and unclean interactions between parts of the system are eliminated. Each product has an identification number. Ziatech maintains a lifetime data base on each board and the components used. Any negative trends in reliability are spotted and Ziatech's suppliers are informed and/or changed.

RETURNING FOR SERVICE

Before returning any of Ziatech's products, you must phone Ziatech at (805) 541-0488 and obtain a Return Material Authorization (RMA) number. Please supply the following information to Ziatech in order to receive an RMA number:

- Your company name and address for invoice
- Your shipping address and phone number
- The product I.D. number
- The name of a technically qualified individual at your company familiar with the mode of failure

Once you have an RMA number, follow these steps to return your product to Ziatech:

1. Contact Ziatech for pricing if the warranty expired.

2. Supply a purchase order number for invoicing the repair if the warranty expired.

3. Pack the board in **anti-static** material and ship in a sturdy cardboard box with enough packing material to adequately cushion it.

Note: Any product returned to Ziatech improperly packed will immediately void the warranty for that particular product!

4. Mark the RMA number clearly on the outside of the box.

ZIATECH WARRANTY

Warranty information for Ziatech products is available at Ziatech's website, located at http://www.ziatech.com.

TRADEMARKS

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