125 Series
Wi125

CONNOR
WINFIELD

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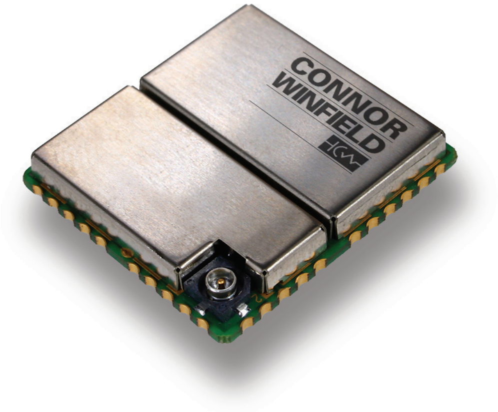
DATA SHEET



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Revision History of Version 1.0

Revision	Date	Released By	Note
00	07/20/09	Keith Loiselle	New Release of Wi125 Data Sheet
01	04/13/10	Dave Jahr	Update to 1PPS (timing) Accuracy Specification
02	06/16/10	Dave Jahr	125 Series Revised

Table 1 Revision History

Other Documentation

The following additional documentation may be of use in understanding this document.

Document	By	Note
Wi125 User Manual	Connor-Winfield	
Wi125 Dev Kit User Manual	Connor-Winfield	

Table 2 Additional Documentation List

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1 INTRODUCTION

The 125 Series Wi125 is a small OEM surface mount GPS module specifically designed for use in synchronization and timing in WiMax applications. This compact module has an on-board programmable NCO oscillator that outputs a synthesized frequency up to 30 MHz that is steered by a GPS receiver. The self-survey mode of operation allows the receiver to enter a position hold mode allowing accurate timing to be continued with only one satellite being tracked.

Additionally, the 125 Series Wi125 has phase alignment of 1 PPS/10 MHz with a very stable holdover. The 1 PPS/10 MHz outputs maintain phase alignment with holdover being base only on the local oscillator, dismissing spurious GPS measurements during reacquisition. When the receiver regains GPS lock after a period of holdover, the 1PPS and 10 MHz outputs maintain phase alignment and are offset in frequency at the maximum rate of 100 ppb until the 1 PPS aligns with that of the GPS solution. This slow recovery from holdover allows for uninterrupted operation of the WiMax base station.

The Wi125 has a highly accurate output frequency, which can achieve full PRC MTIE performance. Additionally it can track satellites and provide GPS synchronization in weak signal areas including indoor applications, reducing the need for high antenna placement.

The Wi125 is an exceptionally small surface mount package with a highly integrated architecture that requires a minimum of external components allowing easy integration into host systems.

Key information includes:

- System Block Diagram
- Maximum Ratings
- Physical Characteristics
    - Wi125 Dimensions, castellation information
    - Solder Pad and placement information
- Signal Descriptions
- Special Features
- Application Information
    - Power supply modes
    - RF connections
    - Grounding
    - Battery Back-up
    - Over Voltage and Reverse Polarity
    - LED’s

Features

- 1PPS/ 10 MHz Phase alignment
- Stable Holdover
- Holdover Recovery
- 1 PPS & NCO Frequency Output
- GPS/UTC time/scale synchronization to 25 ns RMS
- Stable proven design with long term availability and multi-year support
- 12 channel hardware correlator processor design
- OEM SM footprint 25 x 27 mm
- Automatic entry into holdover
- Loss-of-lock and entry-into-holdover indication

The specifications in the following sections refer to the standard software builds of the Wi125 . The performance and specification of the Wi125 can be modified with the use of customized software builds.

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2 SPECIFICATION [1]

2.1 Performance

Physical	Module dimensions	25mm (D) x 27mm (W) x 4.2mm (H)
	Supply voltages	3V3 (Digital I/O), 3V3 (RF), 1V8 (Core option), 3V (Standby Battery)
	Operating Temp	-30°C to +85°C
	Storage Temp	-40°C to +85°C [2]
	Humidity	5% to 95% non-condensing
	Max Velocity / Altitude	515ms^{-1} / 18,000m
	Max Acceleration / Jerk	4g / 1gs^{-1} (sustained for less than 5 seconds)
Sensitivity	Acquisition w/network assist	-185dBW
	Tracking	-186dBW
	Acquisition Stand Alone	-173dBW
Acquisition Time	Hot Start with network assist	Outdoor: <2s Indoor (-178dBW): <5s
	Stand Alone (Outdoor)	Cold: <45s Warm: <38s Hot: <5s Reacquisition: <0.5s (90% confidence)
Accuracy	Position: Outdoor / Indoor	<5m rms / <50m rms
	Velocity	<0.05ms^{-1}
	Latency	<200ms
	Raw Measurement Accuracy	Pseudorange <0.3m rms, Carrier phase <5mm rms
	Tracking	Code and carrier coherent
Power	1 fix per second	0.6W typically
	Coma Mode Current (RF3V3+DIG 3V3)	10mA
	Standby Current (VBATT)	1.5μA
Interfaces	Serial	3 UART ports, CMOS levels
	Multi-function I/O	1PPS and Frequency Output available on GPIO [0] Event Counter/Timer Input Up to 4 x GPIO (multi-function) 2 x LED Status Drive I^2C, External Clock (on special build)
	Protocols	Network Assist, NMEA 0183, Proprietary ASCII and binary message formats
	1pps Timing Output	10nS rms accuracy, <5nS resolution User selectable pulse width
	Event Input	30nS rms accuracy, <10nS resolution
	Frequency Output (GPIO [0])	10 Hz to 30 MHz (Wi125)
	Receiver Type	12 parallel channel x 32 taps up to 32 point FFT. Channels, taps and FFT can be switched off to minimize power or simulate simpler designs.
General	Processor	ARM 966E-S on a 0.18μ process at up to 120 MHz.

Note: 1. The features listed above may require specific software builds and may not all be available in the initial release.
2. Please contact factory for other temperature options.

Table 3 Wi125 Specification

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2 SPECIFICATION continued

2.2 Recommended Ratings

Symbol	Parameter	Min	Max	Units
RF_3V3	RF Supply Voltage	+3.0	+3.6	Volts
DIG_3V3	Digital Supply Voltage	+3.0	+3.6	Volts
DIG_1V8	Digital Supply Voltage	+1.65	+1.95	Volts
VBATT	Battery Backup Voltage	+2.7	+3.5	Volts
ANT_SUPPLY	Antenna Supply Voltage	+3.0	+12	Volts

Table 4 Recommended Maximum Ratings

2.3 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
RF_3V3	RF Supply Voltage	-0.3	+6.5	Volts
DIG_1V8	Digital Supply Voltage	-0.3	+2.0	Volts
DIG_3V3	Digital Supply Voltage	-0.3	+3.7	Volts
VBATT	Battery Backup Voltage	-0.5	+7.0	Volts
ANT_SUPPLY	Antenna Supply Voltage	-15	+15	Volts
DIG_SIG_IN	Any Digital Input Signal	-0.3	+5.5	Volts
RF_IN	RF Input	-15	+15	Volts
TSTORE	Storage temperature	-40	+85	°C
IOUT	Digital Signal Output Current	-6	+6	mA

Table 5 Absolute Maximum Ratings

2.4 Block Diagram

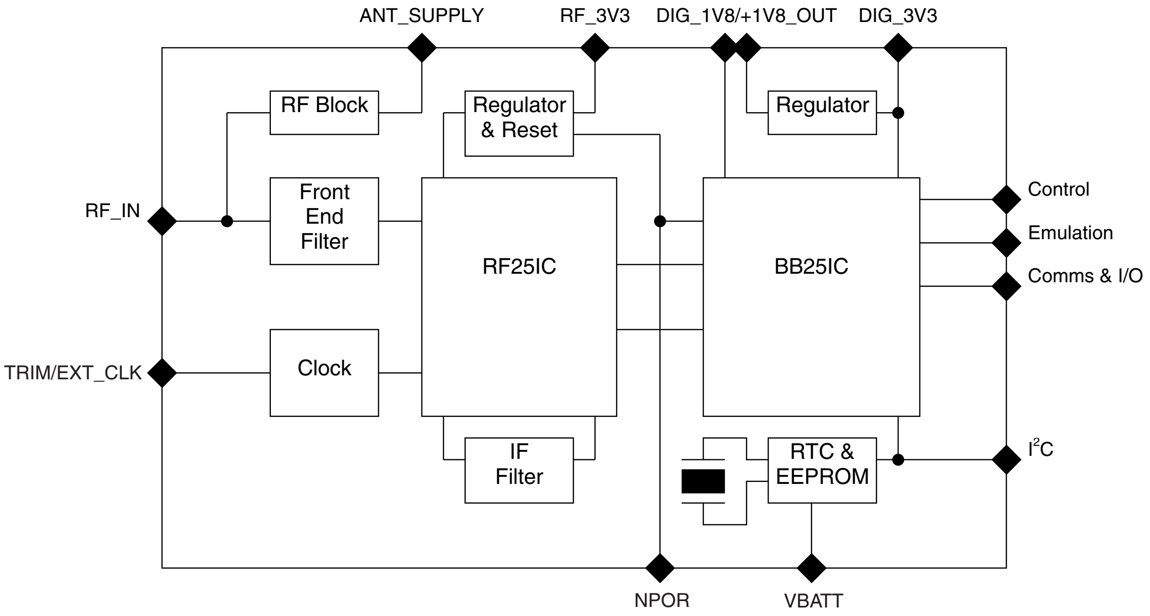

Figure 1 Wi125 Block Diagram

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3 PHYSICAL CHARACTERISTICS

The 125 Series Wi125 is a multi-chip module (MCM) built on an FR4 fiberglass PCB. All digital and power connections to the Wi125 are via castellations on the 25 x 27 mm PCB. The RF connection is via castellations or an RF connector. The general arrangement of the Wi125 is shown in the diagram below. Dimensions are in mm (inches/1000).

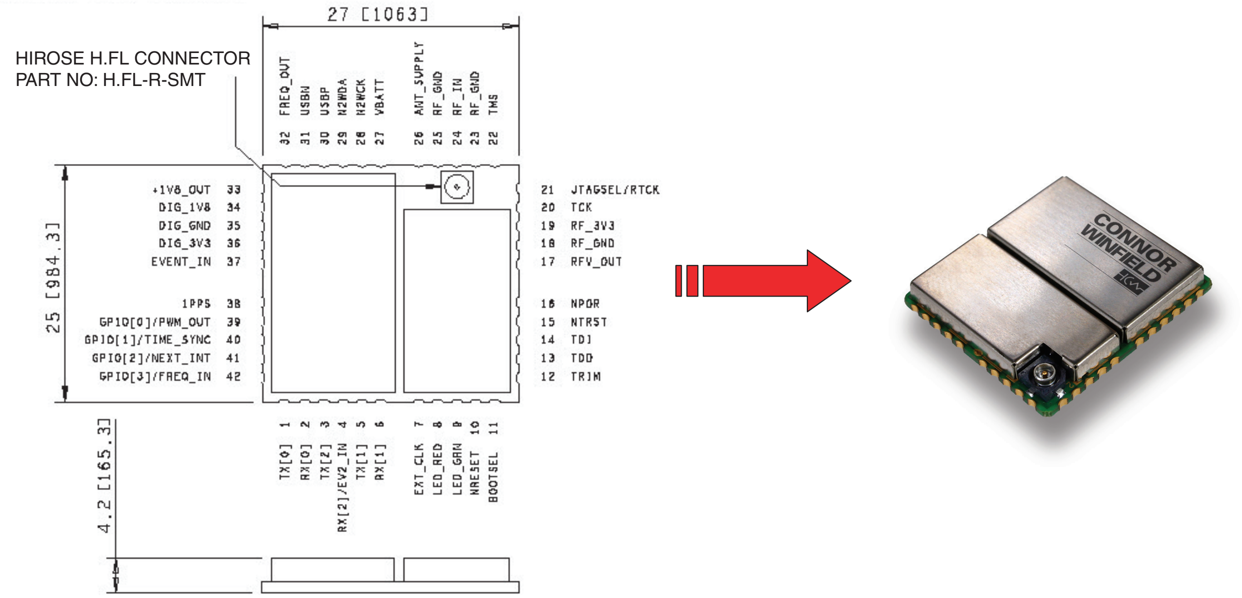

Figure 2 Wi125 Form and Size

3.1 Physical Interface Details

The interface to the Wi125 is via 1mm castellations on a 2mm pitch. There are 42 connections in all. There is also an RF connector for connecting to the GPS antenna. The details of the interface connections are given below.

Pin	Function	Pin	Function	Pin	Function
1	TX[0]	15	NTRST	29	N2WDA
2	RX[0]	16	NPOR	30	USBP
3	TX[2]	17	RFV_OUT	31	USBN
4	RX[2]/EV2_IN	18	RF_GND	32	FREQ_OUT [3]
5	TX[1]	19	RF_3V3	33	+1V8_OUT
6	RX[1]	20	TCK	34	DIG_1V8
7	EXT_CLK	21	JTAGSEL/RTCK	35	DIG_GND
8	LED_RED	22	TMS	36	DIG_3V3
9	LED_GRN	23	RF_GND	37	EVENT_IN
10	NRESET	24	RF_IN	38	1PPS
11	BOOTSEL	25	RF_GND	39	GPIO[0]/PWM_OUT
12	TRIM	26	ANT_SUPPLY	40	GPIO[1]/TIME_SYNC
13	TDO	27	VBATT	41	GPIO[2]/NEXT_INT
14	TDI	28	N2WCK	42	GPIO[3]/FREQ_IN

Note: 3. Frequency Output is available on pin 32 (FREQ_OUT) with custom software only.

Table 6 Wi125 Signal List

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3 PHYSICAL CHARACTERISTICS continued

3.2 Wi125 Dimensions

The figure below provides the dimensions of the positioning of the Wi125 castellations. Dimensions are in mm (inches/1000).

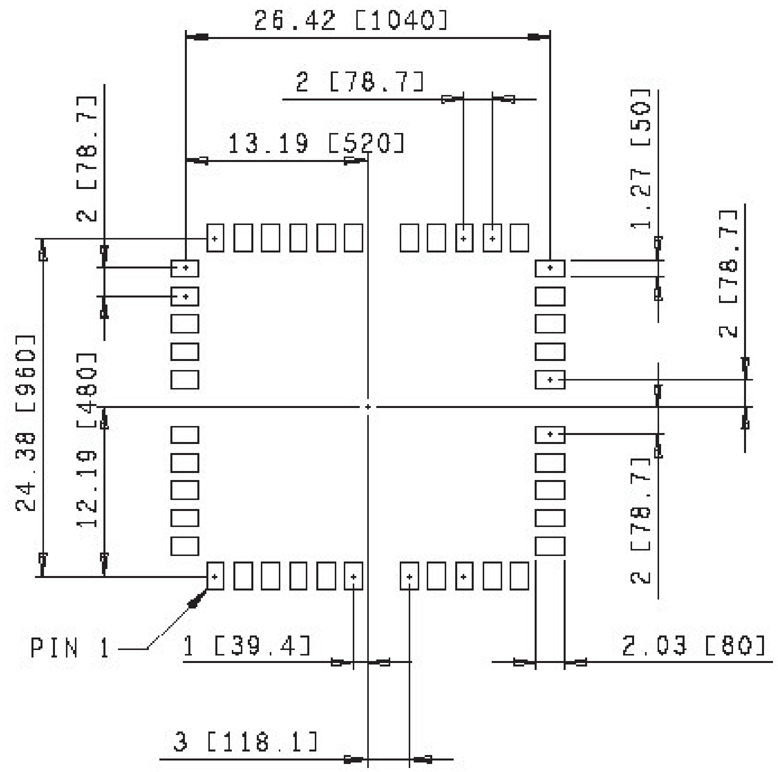

Figure 3 Wi125 Dimensions

3.3 Solder Pad Size and Placement

It is recommended that the footprint of the solder pad under each castellation be 2mm x 1mm, centered on the nominal centre point of the radius of the castellation. The castellations are gold plated and so are lead free. Note that if the RF_IN connector is being used, there should not be a pad or solder resist under the RF_IN castellation. If the RF_IN castellation is to be used, the pad should be shortened by 0.5mm underneath the Wi125 and standard RF design practices must be observed. The diagram below shows the placement of the pads under the castellations.

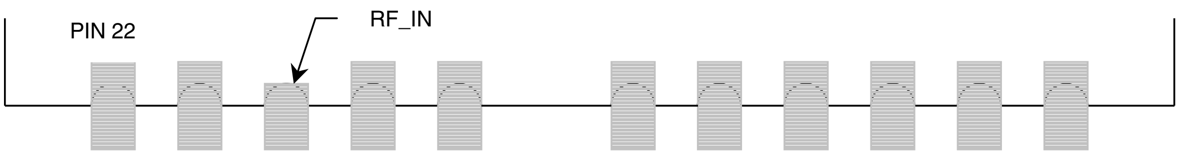

Figure 4 Solder Pad Size and Placement

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4 SIGNAL DESCRIPTION

The signals on the Wi125 are described in the table below.

4.1 Power Signals

RF_3V3	Type: Power	Direction: Input	Pin: 19
	The RF Supply Input. This 3.3V ± 10% input supplies the 2.9V LDO regulator in the RF section of the Wi125 . It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to RF_GND.		
RF_GND	Type: Power	Direction: Input/Output	Pins: 18, 23, 25
	The RF Input Ground. This is the return path for the RF_3V3 supply and the ground for the antenna feed. The RF_GND must be tied to the DIG_GND externally to the Wi125 .		
RFV_OUT	Type: Power	Direction: Output	Pin: 17
	The output from the LDO regulator that is powered by the RF_3V3 signal. This supplies the power to the RF subsystem of the Wi125 . This may also be used to power external RF components but care must be taken not to inject noise onto this signal. No more than an additional 30mA may be taken from this signal by external circuitry.		
ANT_SUPPLY	Type: Power	Direction: Input	Pin: 26
	The Antenna Supply Voltage. This may be used to supply power to the RF_IN signal, for use by an active antenna. The maximum voltage should not exceed ±15V and the current should be limited to 50mA.		
DIG_3V3	Type: Power	Direction: Input	Pin: 36
	The Digital Supply Input. This 3.3V ± 10% input supplies the I/O ring of the BB25IC chip and the LDO regulator in the digital section of the Wi125 . It is important that this supply is well filtered with no more that 50mV peak to peak noise with respect to DIG_GND.		
DIG_1V8	Type: Power	Direction: Input	Pin: 34
	The 1.8V ± 5% digital core supply for the BB25IC. This is normally connected directly to the +1V8_OUT signal. However, if an external 1.8V ± 5% is available, a lower overall system power consumption may be achieved by using an external supply.		
+1V8_OUT	Type: Power	Direction: Output	Pin: 33
	The 1.8V output from the LDO regulator that is powered by the DIG_3V3 signal. Normally, this is connected to the DIG_1V8 signal. This may also be used to power external logic but care must be taken not to inject noise onto this signal. No more than an additional 50mA may be taken from this signal by external logic.		
DIG_GND	Type: Power	Direction: Input/Output	Pin: 35
	The Digital Ground. This is the return path for the DIG_3V3 supply and the ground reference for all the digital I/O. The DIG_GND must be tied to the RF_GND externally to the Wi125 .		

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4 SIGNAL DESCRIPTION continued

4.1 Power Signals cont'd

VBATT	Type: Power	Direction: Input/Output	Pin: 27

The Battery Backup Supply. The Wi125 has an on board Real Time Clock (RTC). This is powered from the VBATT signal. A supply of typically 3v (greater than 2.5V and less than DIG_3V3) should be applied to this signal. This signal can be left floating if not required. The input has a blocking diode and so rechargeable batteries will need an external charging circuit. Typically, a 1K resister in series with this signal and the external battery will provide an easy method of measuring the current consumption from VBATT during test.

4.2 RF Signals

RF_IN	Type: RF	Direction: Input	Pin: 24

The RF Input Signal. This attaches to the GPS antenna. Standard RF design rules must be used when tracking to this signal. This signal has an RF blocked connection to the ANT_SUPPLY signal. This is the same signal presented on the RF connector on the Wi125 . Only one antenna connection should be made. If the RF connector is to be used, then there should be no connection, even an unconnected pad, to this castellation.

TRIM	Type: RF	Direction: Input	Pin: 12

This signal trims the output frequency of the VCTCXO. This signal is normally left open. When floating, this signal is biased to the control voltage of the VCTCXO. Any noise injected into this signal will severely compromise the performance of the Wi125 . This signal should only be used in conjunction with specific application notes.

EXT_CLK	Type: RF	Direction: Input	Pin: 7

This input is the external clock input. This signal is to be used only in special builds of the Wi125 that are not fitted with an internal VCTCXO. For the normal build, containing the VCTCXO, do not connect this input. The external clock is a 9 MHz to 26 MHz clipped sinewave input with an amplitude between 1V and 3V peak to peak. The return path for this signal is RF_GND.

4.3 Emulation/Test Signals

TDI	Type: Test	Direction: Input	Pin: 14

The Test Data In Signal. This is the standard JTAG test data input. The signal return path is DIG_GND.

TDO	Type: Test	Direction: Output	Pin: 13

The Test Data Out Signal. This is the standard JTAG test data output. The signal return path is DIG_GND.

TCK	Type: Test	Direction: Input	Pin: 20

The Test Clock Signal. This is the standard JTAG test clock input. The signal return path is DIG_GND.

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4 SIGNAL DESCRIPTION continued

4.3 Power Signals cont'd

TMS Type: Test Direction: Input Pin: 22

The Test Mode Select Signal. This is the standard JTAG test mode input. The signal return path is DIG_GND.

JTAGSEL/RTCK Type: Test Direction: Input/Output Pin: 21

This is a Dual Function Signal. When the NPOR signal is asserted (low), this signal is an input and selects the function of the JTAG interface. When high, JTAG emulation into the embedded ARM9 processor is selected. When low, the BB25IC chip boundary scan mode is selected. The value on this signal is latched when NPOR de-asserts (goes high). When NPOR is de-asserted (high) and the JTAG emulation mode has been latched, this signal provides the return clock to the ARM Multi-ICE. Because the ARM9 functions off a single clock domain, the TCK has to be internally synchronized in the ARM9. This can cause a variable length delay in the validity of the TDO signal. The RTCK is a synchronized version of the TCK signal. The Multi-ICE uses the RTCK output signal to indicate when the TDO signal is valid. The signal return path is DIG_GND.

NTRST Type: Test Direction: Input Pin: 15

The Test Reset Signal. This is the active low JTAG test reset signal. The signal return path is DIG_GND.

4.4 Control Signals

NPOR Type: Control Direction: Input/Output Pin: 16

The Power On Reset Signal. This active low, open collector signal is the master reset for the Wi125 . The Wi125 can be held in reset by asserting this signal. The signal can be used to reset external circuitry, but care must be taken to ensure no DC current is drawn from this signal as the internal pull-up resistor value is 100K.

NRESET Type: Control Direction: Input/Output Pin: 10

The System Reset Signal. This active low, open collector signal is generated by the BB25IC chip in response to the assertion of the NPOR. It may also be driven to reset the ARM9 processor in the BB25IC without completely re-initializing the chip.

BOOTSEL Type: Control Direction: Input Pin: 11

The Boot Select Signal. The BB25IC has four boot up modes, but only two are supported by the Wi125 . This signal is sampled when the NPOR is de-asserted. If the BOOTSEL signal is high or left floating, then the Wi125 boots from its on-chip FLASH memory. If the BOOTSEL signal is pulled low, the Wi125 boots from its on-chip ROM.

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4.5 I/O Signals

TX[0]	Type: I/O	Direction: Output	Pin: 1	The Transmit Signal for UART 0. This is a standard UART output signal. The signal return path is DIG_GND.
TX[1]	Type: I/O	Direction: Output	Pin: 5	The Transmit Signal for UART 1. This is a standard UART output signal. The signal return path is DIG_GND.
TX[2]	Type: I/O	Direction: Output	Pin: 3	The Transmit Signal for UART 2. This is a standard UART output signal. The signal return path is DIG_GND.
RX[0]	Type: I/O	Direction: Input	Pin: 2	The Receive Signal for UART 0. This is a standard UART input signal. The signal return path is DIG_GND.
RX[1]	Type: I/O	Direction: Input	Pin: 6	The Receive Signal for UART 1. This is a standard UART input signal. The signal return path is DIG_GND.
RX[2]/EV2_IN	Type: I/O	Direction: Input	Pin: 4	This is a Dual Mode Signal. Normally, this is the receive signal for UART 2, a standard UART receive signal. Under software control, it can also be used as general purpose I/O or to detect events. It can be used to detect the timing of the leading edge of the start bit of the incoming data stream. The signal return path is DIG_GND.
FREQ_OUT	Type: I/O	Direction: Input/Output	Pin: 32	Optional Frequency Output Signal. This is NOT the same signal as pin 39. This signal is turned off by default. This is a complex signal which under software can provide any of either an NCO generated output frequency, a PWM signal, a GPS aligned EPOCH pulse or general purpose I/O signal. The signal return path is DIG_GND.
1PPS	Type: I/O	Direction: Input/Output	Pin: 38	The 1 Pulse Per Second Signal. This is normally a 1 pulse aligned with GPS time, but can under software control also provide general purpose I/O or an additional event input. The pulse width of the 1PPS is software selectable with a default of 100μs. The signal return path is DIG_GND.
EVENT_IN	Type: I/O	Direction: Input/Output	Pin: 37	The Event Input Signal with internal connection to Pin 39 (GPIO[1] / Time Sync) allows phase measurement of the Frequency Output. The signal return path is DIG_GND.

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4.5 I/O Signals cont'd

N2WCK Type: I/O Direction: Input/Output Pin: 28

The NavSync 2 Wire Clock Signal. This is the open collector I2C compatible Clock Signal for the 2 wire serial interface. The signal return path is DIG_GND.

N2WDA Type: I/O Direction: Input/Output Pin: 29

The NavSync 2 Wire Data Signal. This is the open collector I2C compatible Data Signal for the 2 wire serial interface. The signal return path is DIG_GND.

USBP [4] Type: I/O Direction: Input/Output Pin: 30

The positive USB Signal. The signal return path is DIG_GND.

USBN [4] Type: I/O Direction: Input/Output Pin: 31

The negative USB Signal. The signal return path is DIG_GND.

LED_RED Type: I/O Direction: Output Pin: 8

This is a Dual Function Signal. Normally this signal is used to drive a red LED. Standard software builds use this signal to indicate GPS status. In special software builds, this signal can be used as GPIO. This signal has a 3.3V CMOS drive. A series limiting resistor is required to limit output current to ±5mA. The signal return path is DIG_GND.

LED_GRN Type: I/O Direction: Output Pin: 9

This is a Dual Function Signal. Normally this signal is used to drive a green LED. Standard software builds use this signal to indicate GPS status. In special software builds, this signal can be used as GPIO. This signal has a 3.3V CMOS drive. A series limiting resistor is required to limit output current to ±5mA. The signal return path is DIG_GND.

GPIO[0]/PWM Type: I/O Direction: Input/Output Pin: 39

Normally the GPIO[0]/PWM output provides a Frequency Output that defaults to 10 MHz, and is user configurable from 10 Hz to 30 MHz signal. The output is enabled on power-up and is steered by the GPS solution. Custom software versions can also configure this pin for general I/O, PWM or EPOCH output. The signal return path is DIG_GND.

GPIO[1]/TIME_SYNC Type: I/ODirection: Input/Output Pin: 40

The GPIO[1]/TIME_SYNC pin provides a synchronization pulse generated by the onboard RTC. Custom software versions can also configure this pin for general purpose I/O, or an additional PPS output. The signal return path is DIG_GND.

Note: 4. USB is not supported in the current software build.

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4 SIGNAL DESCRIPTION continued

4.5 I/O Signals cont'd

GPIO[2]/NEXT_INT Type: I/O Direction: Input/Output Pin: 41

The GPIO[2]/NEXT_INT output provides an active high status indicator for the Frequency Output available on pin 39 (GPIO[0]/PWM). Custom software versions can also configure this pin for general purpose I/O. The signal return path is DIG_GND.

GPIO[3]/FREQ_IN Type: I/O Direction: Input/Output Pin: 42

The GPIO[3]/FREQ_IN output provides an active high status 3D fix indicator. This indicator can also be used to determine the validity of the pin 38 (1PPS) output. The signal return path is DIG_GND.

5 SPECIAL FEATURES

While most of the features on the Wi125 are just a subset of the capabilities of the Wi125 and so are described in the Wi125 Data Sheet and the Wi125 User Manual, there are some additional features specific to the Wi125 that require explanation.

5.1 User Commands

The Wi125 can accept a number of specific user commands for setting receiver parameters such as UART baud rate and NMEA message subset, output frequency, etc. Many of these parameters are stored in Non-Volatile Memory (NVM) so that the settings are retained when the receiver loses power. The available commands are defined in detail in the Wi125 User Manual.

5.2 Self Survey

To optimize timing performance, the Wi125 performs a 10-minute survey each time the receiver is powered up and after obtaining a GPS fix. When the survey is complete, the receiver automatically enters fixed timing mode. For applications with specific timing performance requirements, it may be necessary to allow the survey to complete before using the 1PPS and frequency outputs. The status of the survey can be determined by querying the receiver dynamics setting as described in the Wi125 User Manual.

5.3 Wi125 Embedded Identification

The hardware version number is hard coded onto the Wi125; firmware also contains a version number allowing for easy identification of the hardware and software version in embedded applications.

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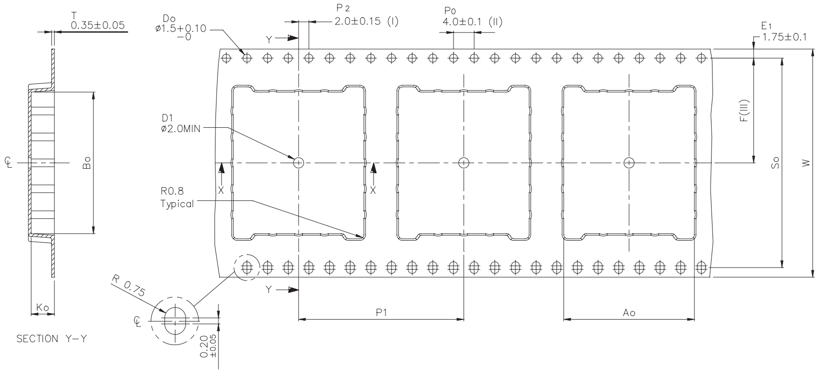
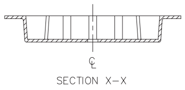
6 TAPE AND REEL SPECIFICATIONS



Ao	25.30 +/− 0.1
Bo	27.30 +/− 0.1
Ko	4.50 +/− 0.1
F	20.20 +/− 0.15
P1	32.00 +/− 0.1
So	40.40 +/− 0.1
W	44.00 +/− 0.3

General Tolerance ±0.2
Drawing not to Scale



(I) Measured from center line of sprocket hole to center line of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from center line of sprocket hole to center line of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

Figure 5 Tape and Reel

7 SOLDER PROFILE

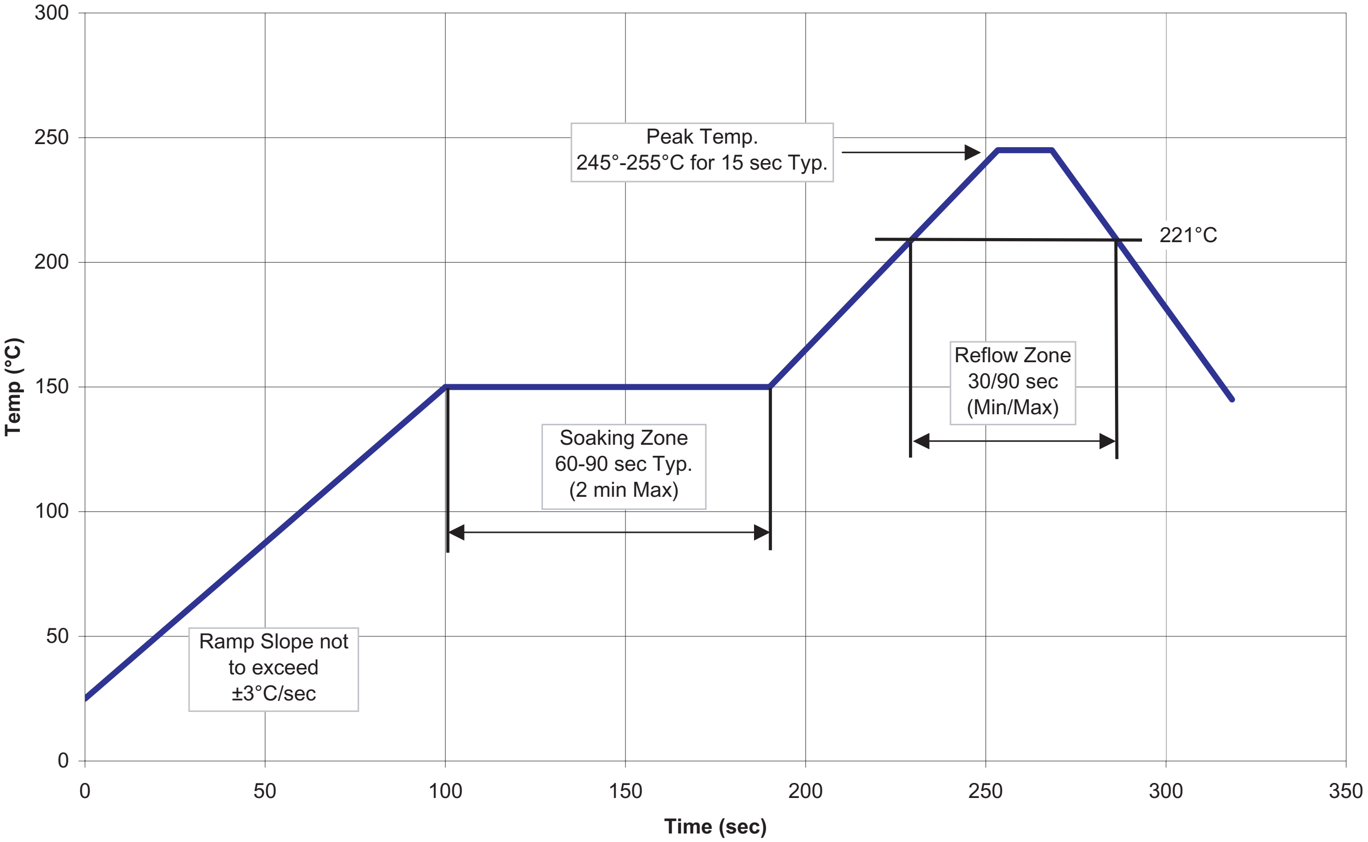


Figure 6 Solder Profile

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8 APPLICATION HINTS

The following are a list of application hints that may help in implementing system based on the Wi125 .

8.1 Power Supply

The power supply requirements of the Wi125 can all be provided from a single 3.3V supply. To simplify system integration on-board regulators provide the correct voltage levels for the RF and oscillator (2.9V or 3.0V) and low voltage digital core (1.8V). In power sensitive applications it is recommended that the DIG_1V8 supply is provided from a high efficiency external 1.8V source e.g. switch mode power supply, rather than the on-board linear regulator.

If the source impedance of the power supply to the Wi125 is high due to long tracks, filtering or other causes, local decoupling of the supply signals may be necessary. Care should be taken to ensure that the maximum supply ripple at the pins of the Wi125 is 50mV peak to peak.

8.2 RF Connection

The RF connection to the Wi125 can be done in two ways. The preferred method is to use standard microstrip design techniques to track from the antenna element to the RF_IN castellation. This also allows the systems integrator the option of designing in external connectors suitable for the application. The user can easily fit an externally mounted MCX, SMA or similar connector, provided it is placed adjacent to the RF_IN castellation. If the tracking guidelines given below are followed, the impedance match will be acceptable. The diagram below shows how this could be achieved. In this diagram, the centre via of the RF connector is presumed to be plated through with a minimal pad top and bottom. The PCB material is assumed to be 1.6mm thick FR4 with a dielectric constant of 4.3. Two situations are considered; one with no ground plane and one with a ground plane on the bottom of the board, underneath the RF connector. In both cases there is no inner layer tracking under the RF connector.

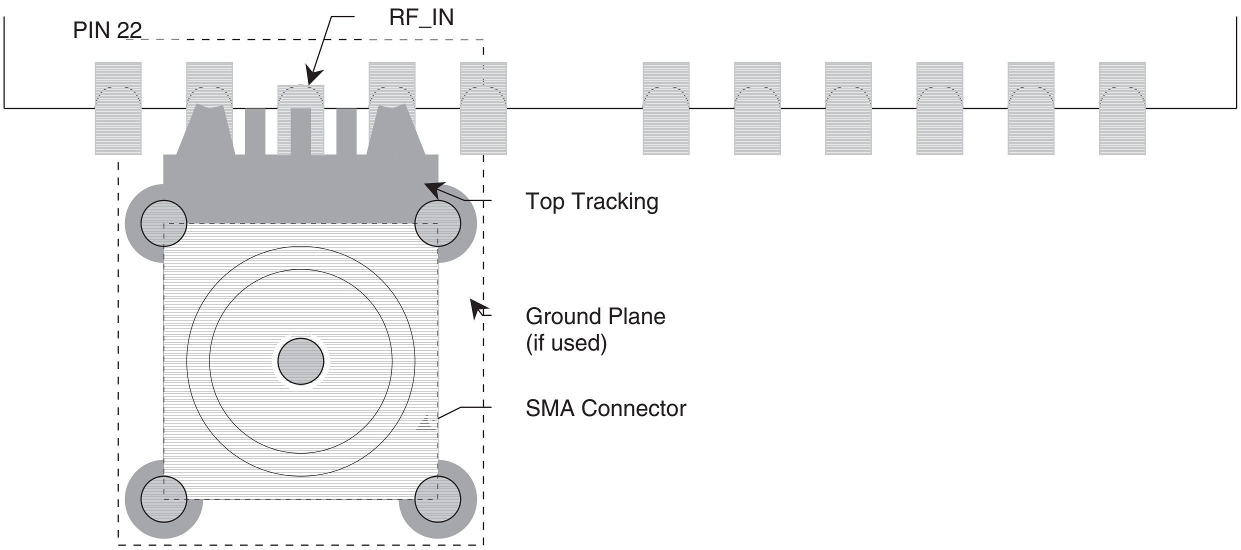

Figure 7 RF Tracking Example

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8 APPLICATION HINTS continued

The widths of the RF_IN track and the associated gaps are given in the table below.

Scenario	**Track Width** (1/1000 Inch)	**Gap Width** (1/1000 Inch)
Without ground plane	37	6
	56	8
With ground plane	32	6
	43	8

Table 7 RF Track & Gap Widths

Alternatively, the user can attach the antenna to the Hirose H.FL-R-SMT using a flying lead fitted with a suitable plug.

8.3 Grounding

In connecting the Wi125 into a host system, good grounding practices should be observed. Specifically, ground currents from the rest of the system hosting the Wi125 should not pass through the ground connections to the Wi125 . This is most easily ensured by using a single point attachment for the ground. There must also be a good connection between the RF_GND and the DIG_GND signals. While there is not a specific need to put a ground plane under the Wi125 , high energy signals should not be tracked under the Wi125 . It is however recommended that a ground plane be used under the Wi125 . In this case, the following would be an example of the pattern that may be used

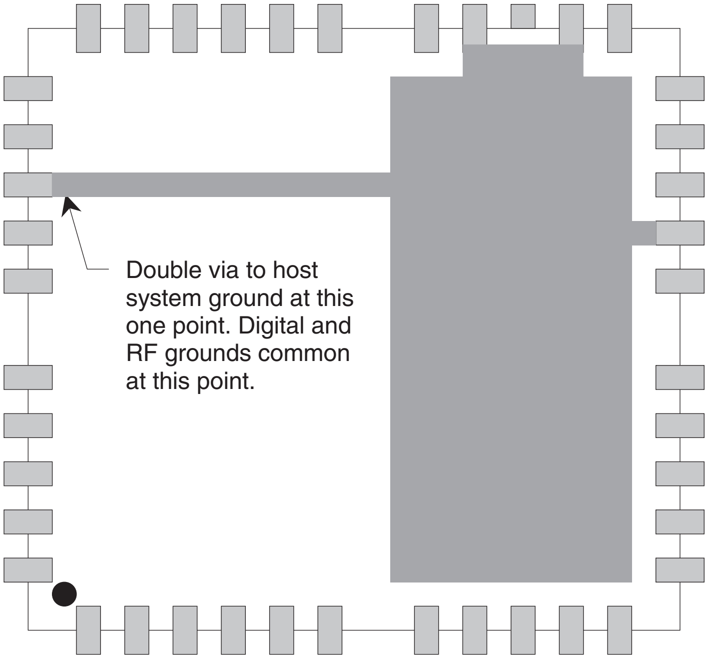

Figure 8 Grounding the Wi125 with a Ground Plane

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8 APPLICATION HINTS continued

8.4 Battery Backup

The Wi125 has an on-board real time clock (RTC). This is used to store date and time information while the Wi125 is powered down. Having a valid date and time speeds the Time To First Fix (TTFF), allowing the Wi125 to meet its quoted TTFF specification. The Wi125 relies on an external power source to power the RTC (VBATT) when the DIG_3V3 is not present. If the user application does not require the warm or hot fix performance, or the required information is provided by network assistance, there is no need to provide the VBATT signal. The VBATT signal must be greater than 2.6V and less than DIG_3V3 + 0.6V. Typically, a 3V lithium primary cell or a high capacity "supercap" will be used. The Wi125 has an internal blocking diode, so if a "supercap" or rechargeable battery is used, an external charging circuit will be required.

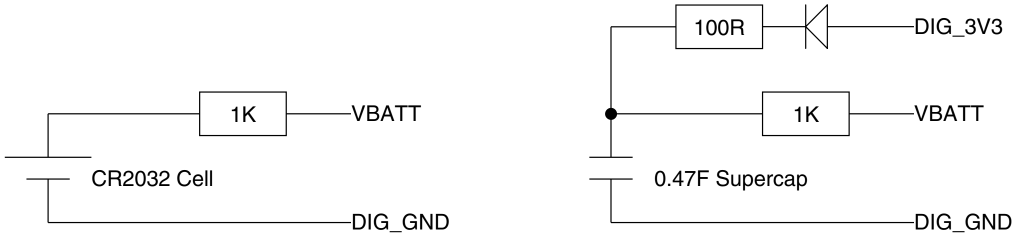

Figure 7 Typical VBATT Supplies

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125 Series
Wi125 Series

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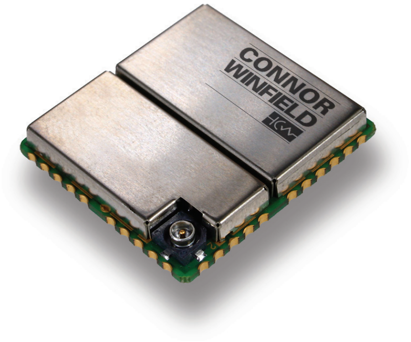

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