USER MANUAL

	Class: VME		Function: Optical to RF (DIGITAL)	
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RF_RX_D v2.0

Optical to RF Digital VMEbus Interface Card Hardware user manual

Summary:

This document describes the functionality of the RF_Rx_Digital card (the hardware is detailed, and the VME mapping is described)

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Table of Contents

1. Introduction 3

2. RF_RX_D Hardware 4

Power description 4

Optical Interface 4

2.2.1. Photodiodes Modules: 5

2.2.1.1. Photodiode selection (Depending of the signal to transmit) 7

2.2.1.2. Photodiode configuration (Threshold and Selection) 7

2.2.1.3. Signal Detection Circuit 9

2.2.2. Photodiodes Modules – Post processing Logic 9

2.2.2.1. Frequency divider: 10

2.2.2.2. Output Format Selection 10

2.3. VMEbus interface 11

2.3.1. Addr module sellection 12

2.3.2. Software: Vme addres map 13

2.3.3. Registers Description 14

2.3.3.1. ReceiverModID 14

2.3.1.1. STATUS 14

2.3.3.2. VRef Registers (Only for TRR or equivalent photodiodes) 15

2.3.3.3. Frequency Counters 19

2.3.3.4. Board Identification 20

2.3.1.2. Ident Code 20

2.3.1.3. Card ID 20

2.3.1.4. Board ID 20

2.3.1.5. Firmware Version 21

2.4. Calibration procedures (Trr or similar photodiode) 22

2.4.1. Manual Calibration (Fix Vref Values) 22

2.4.2. Through VME Knowing the Signals and Photodiodes used 25

2.4.3. Through VME Unknowing the Signals and Photodiodes 25

2.5. Board configuration- Jumpers and switch 28

2.6. Fibre / cable connections 28

2.7. Front-panel LEDs 29

2.8. References or more information 29

3. TTC common software 30

3.3. Introduction 30

3.3.1. H/W Environment 30

3.3.2. S/W Environment 30

3.4. Test programs 30

3.5. The user library 30

1. INTRODUCTION

The RF_RX_D (Optical to RF VMEbus card) is an interface VME card developed as receiver of RF_TX_D VMEbus Interface card.

This document contains a hardware description of the board and all the accessible registers of the RF_RX_D card as well as a description of the generic S/W that has been developed for this card. At the end of this document, some basic examples of configuration procedures are proposed.

2. RF_RX_D HARDWARE

POWER DESCRIPTION

This board requires a VME crate with the standard VME64 power supply, with +12, -12, and +5 Volts available. The nominal consumption for these power lines is the following:

Voltage	Current (A)	Fuse Current
5V	2A	3A
+12V	150mA	0.5A
-12V	16mA	0.1A

Table 2.1: Power consumption

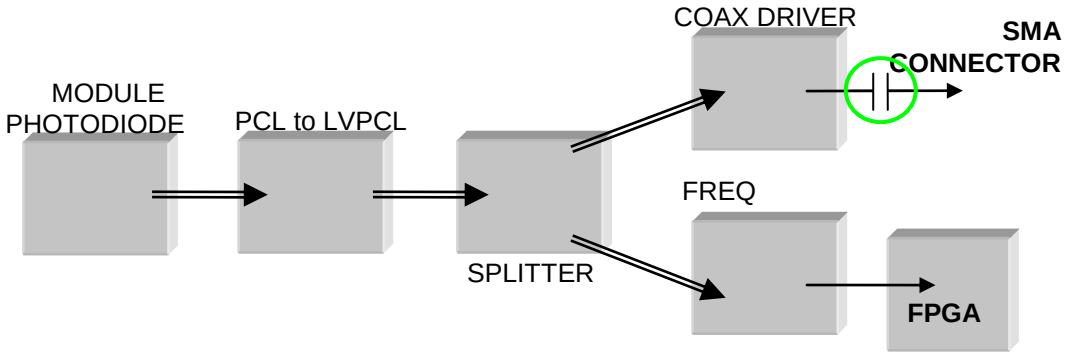
In order to check the power supplied to the board, three LEDs have been installed to indicate the presence of +12V, -12V and +3.3V* (generated from +5V, indicating with this light both voltages).

*If this LED is not lighting, proceed checking the +5V fuse state.

OPTICAL INTERFACE

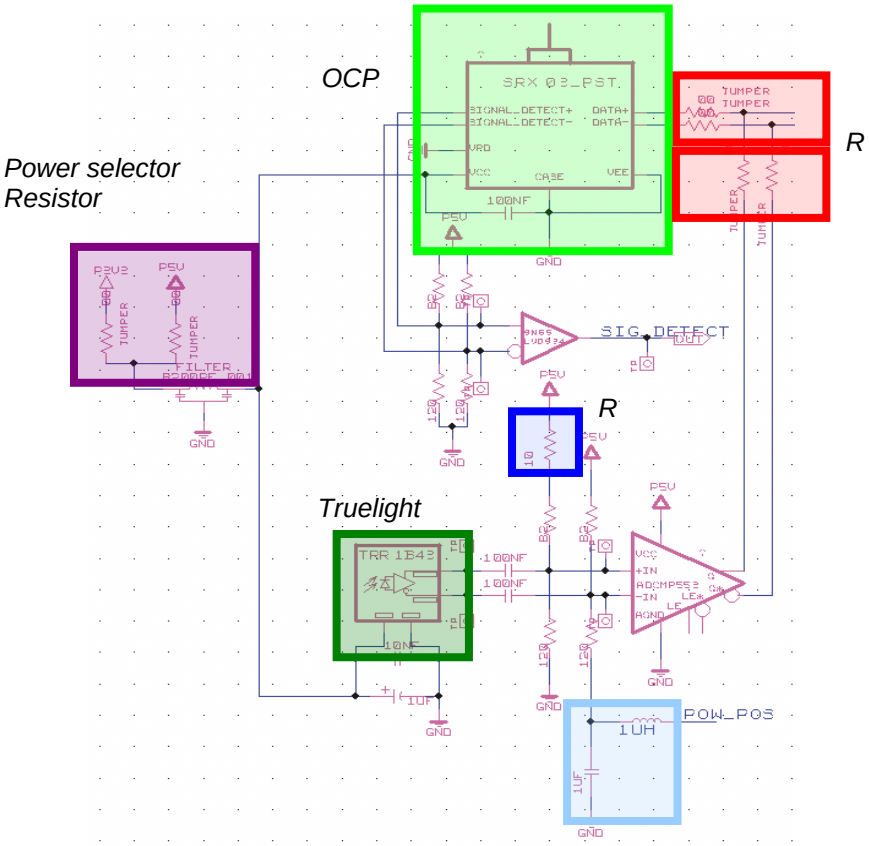
The optical interface is composed of three equal channels based on two parallel circuits using two different photodiodes, one being mounted at a time.

Both photodiodes have differential output and are connected to a group of ECL gates that will clean and prepare the signal to be amplified by a coaxial driver and processed with a FPGA.

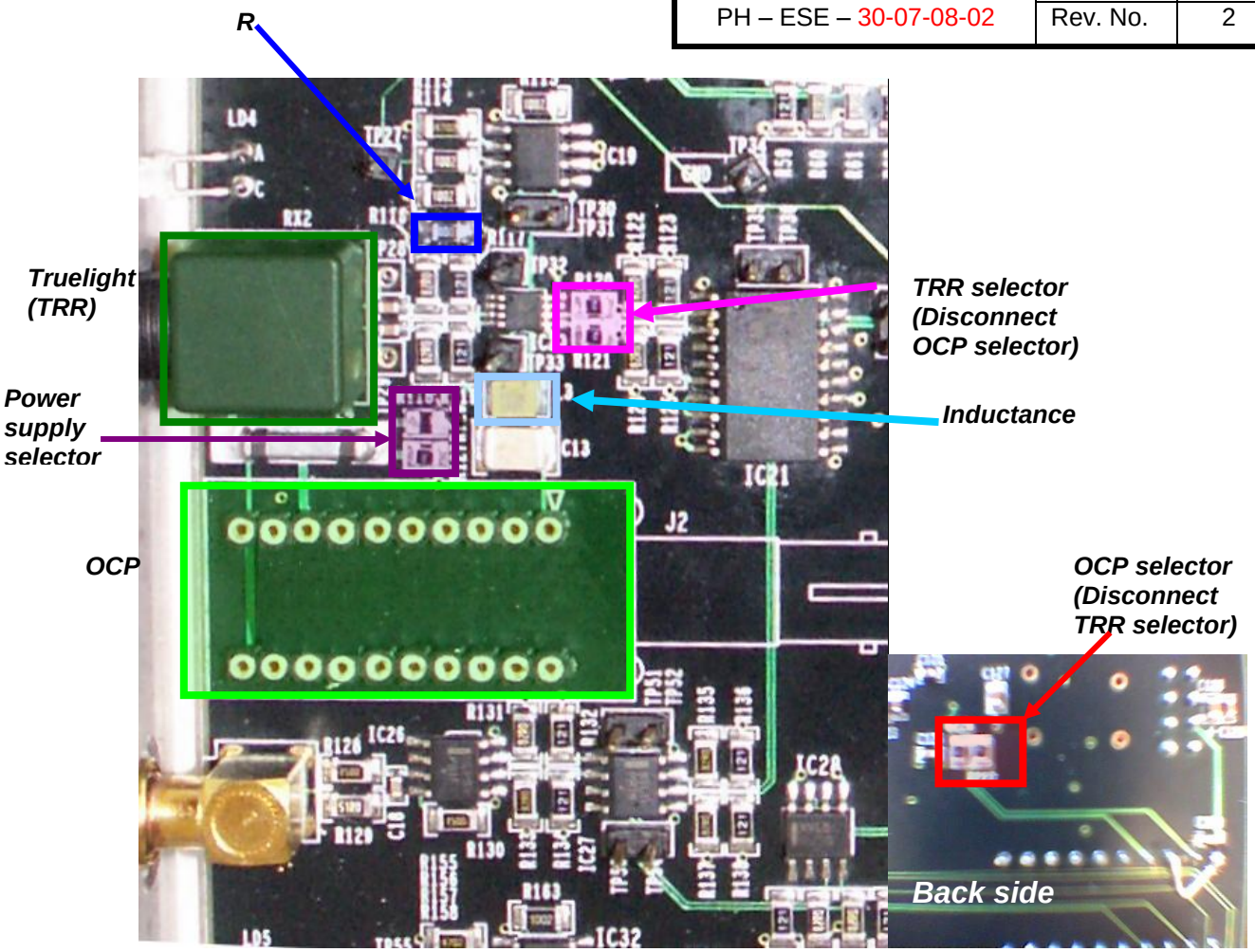


Picture 2.2: Optical Interface Diagram

2.2.1. PHOTODIODES MODULES:



Picture 2.2.1.a: Photodiodes Module in EDA 1382



Picture 2.2.1.b: important points in the board EDA 1382

Block	Signal	Vref Value
Light Green	OCP Place/ socket	Supported: Not adjustable
Dark Green	Truelight Place/ socket	Not supported
VIOLET UP RES.	3.3 Volts supply	Only one connected
VIOLET DOWN RES	5 Volts supply	Only one connected
PINK RESISTORS	Truelight signal selected	when 0R0 res. Are placed
RED RESISTORS (back side)	OCP signal selected	when 0R0 res. Are placed
BLUE RESISTORS	Resistor unbalancing the Thevenin Network manually	when R /= 0R0 res.
BLUE INDUCTANCE	FPGA Control Thevenin	when placed (1uH)

Table 2.2.1: Block description

2.2.1.1. PHOTODIODE SELECTION (DEPENDING OF THE SIGNAL TO TRANSMIT)

To the table below summarizes a review coming from the "Laser and Photodiodes Evaluation" that shows the bandwidth and signal types that each Photodiode can receive. For more information and characteristics, check the evaluation document or datasheets.

Photodiode	Bandwidth	Signal Example	Supported	Threshold / Thevenin adjustable
OCP SRX 03	Time of bit (Tb) < 10us to 2ns Freq: ~100 KHz to ~250 MHz	10MHz square	YES	NO
OCP SRX 03	Tb >10us Freq > 300Mhz	10KHz square 5ns width 11Khz (pulse)	NO	NO
OCP SRX 24	Tb < 10us to 1ns Freq: ~100 KHz to ~500 MHz	10MHz square 400MHz square	YES	NO
OCP SRX 24	Tb > 10us	10KHz square 5ns width 11Khz (pulse)	NO	NO
Truelight	50KHz to 400Mhz	10MHz square 400MHz square	YES	YES
Truelight	Tb(high) < 16us	Positive pulses (maximum 16us width)	YES	YES

Table 2.2.1.1: Signals supported by each photodiode.

2.2.1.2. PHOTODIODE CONFIGURATION (THRESHOLD AND SELECTION)

The table below shows a brief summary of the necessary adjusts that need to be done in each channel to select the photodiode that is going to be used.

Photodiode	Mode: Manual(HW) / FPGA(SW)	Components to replace
OCP	NOT THRESHOLD ADJUSTABLE	OCP CONNECTED (GREEN LIGHT) DARK BLUE (DB) : don't care LIGHT BLUE (LB) : don't care PINK RESISTORS (PR): disconnected RED RESISTORS (RR): connected VIOLET RES. (VR): just 0R0 in bottom(5V)
Truelight	MANUAL THRESHOLD ADJUSTABLE	TRUELIGHT CONN. (GREEN DARK) DARK BLUE (DB) : 10ohms resistor LIGHT BLUE (LB) : disconnected PINK RESISTORS (PR): connected RED RESISTORS (RR): disconnected VIOLET RES. (VR): just 0R0 in bottom(5V)
Truelight	THRESHOLD ADJUSTABLE by FPGA	DARK BLUE (DB) : 0ohms resistor LIGHT BLUE (LB) : connected 1uH PINK RESISTORS (PR): connected RED RESISTORS (RR): disconnected VIOLET RES. (VR): just 0R0 in bottom(5V)

Table 2.2.1.2: photodiode selection table

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In case **that another photodiode** is going to be used, it has to be connected on:

- OCP place if the Output format is pure PECL for all the bandwidth
- TRUELIGHT place if the Output is differential NO PECL, with AGC in the last stage of the preamplifier or with and internal AC coupled in the output.

In both cases the voltage must be selected between 3.3V and 5V with the Violet Resistors

****

*In FPGA mode VME FPGA who unbalances the Thevenin network. For this, it is necessary write in the Vref Register a value different from 0. This makes it possible to unbalance the network from ~0 to ~750mv.

2.2.1.3. SIGNAL DETECTION CIRCUIT

The signal Detection circuit works ONLY with the OCP SRX photodiode. This circuit will translate the signal detection state from the OCP to the Front panel.

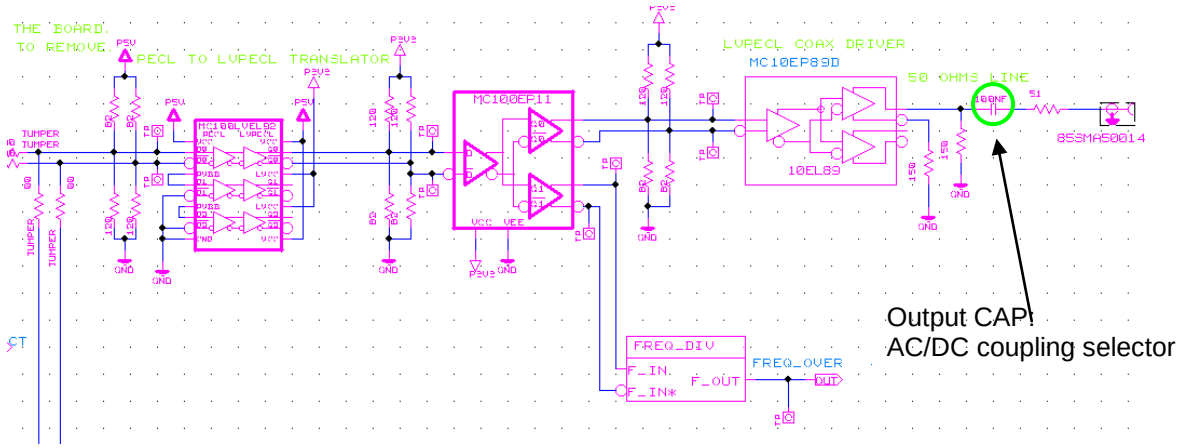
A LED on the FP indicates the presence of optical power in each channel through a GREEN light or the absence with a RED light.

In a future Firmware version signal detection for Truelight Photodiodes, based on the frequency of the received signal, will be added. Meanwhile, the Frequency detectors registers can be used to know the signal presence

2.2.2. PHOTODIODES MODULES – POST PROCESSING LOGIC

The post-processing logic is based on a few ECL gates that will increase the signal power in order to drive the signal through long cables. The user will be able to choose the output format between AC coupled 50 Ω or DC coupled LVPCL.

Another function of the Post Processing circuit is to split the signal and apply a frequency divider with the objective to be able to monitor the frequency with the FPGA through the VME interface.



Picture 2.2.2: Photodiodes Post-Processing Logic

2.2.2.1. FREQUENCY DIVIDER:

The Frequency Divider is composed of 5 Flip-Flops (FF) that divide the frequency by 16.

2.2.2.2. OUTPUT FORMAT SELECTION

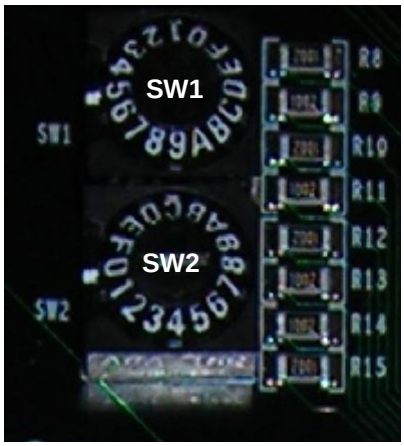
In order to select the format of the output (50Ω AC coupled ~800Vpp) or DC coupled LVPECL, you must place in the output of the system a capacitor of 100 nf (AC) or a 0Ω RESISTOR for DC coupling.

2.3. VMEBUS INTERFACE

The VMEbus interface of the RF_RX_D cards is implemented in its FPGA and based on a VHDL Module developed by the AB/RF group. This Module has been developed especially for VME64 but adapted for using some functionality of VME64X (like automatic addressing).

The firmware installed has been configured to work in the addressing mode of: A24/D16 and works as a memory decoder, where all the memory space is available.

The access modes (dictated by address modifier) are only available for 0x39 and 0x3D, where the there is no distinction between privilege user and normal user



Picture 2.3: Module address selector

Two switches are used for address definition:

SW1: only the smallest bit is used.

If bit0 is set to 0 (SW1= 0x0, 0x2, 0x4, 0x6…), the SW2 defines the address.

if bit 0 is set to 1 (SW1= 0x1, 0x3, 0x5 …), the address is set by the geographical position of the module in the crate.

2.3.1. ADDR MODULE SELLECTION

Rotary Switch 1 (bit0)	Rotary Switch 2	Module address (MA)
1	M	Automatic GEO Address [A23…A20] <= GEOGA(3 : 0)
0	M	0xM Manual Address [A23…A20] <= M

**Requires VME64X crate*

Table 2.3.1: Address and ADDR Mode selection

In others words, the bottom rotary switch (sw1) controls the addressing mode with the lower two bits, which switches to automatic mode if the bit(0) or bit(1) = 1.

Examples:

Rotary Switch 1	Rotary Switch 2	Module MODO / ADDRESS / SPACE
0x1	5	Manual address Module address: 0x50 0000
0x0	X	Geographical address Module address: Depends on the slot into which the card is plugged
0x3	4	Manual address Module address: 0x40 0000

Table2.3.1.b: Examples of Module Addr

2.3.2. SOFTWARE: VME ADDRES MAP

Offset	Size (bytes)	Function	Mode	Remarks
0xN00000	2	Unused		
0xN00002	2	VMEIRQStatID	Read / Write	
0xN00004	2	VMEIRQLevel	Read / Write	
0xN00006	2	Status	Read Only	
0xN00008	2	Ident Code	Read Only	0x001A
0xN0000A	4	Unused		
0xN00010	2	ReceiverModID	Read Only	Note (1)
0xN00012	2	CH1_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00014	2	CH2_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00016	2	CH3_OUTPUT_REF_SIGNAL	Read / Write	TRR module only, Def. Val. 0xA0
0xN00018	4	CH1_FREQ	Read Only	Freq Ch1 (0..31), Note (2)
0xN0001C	4	CH2_FREQ	Read Only	Freq Ch2 (0..31), Note (2)
0xN00020	4	CH3_FREQ	Read Only	Freq Ch3 (0..31), Note (2)
0xN00024	2	CARD ID	Read Only	0x1382
0xN00026	2	unused		
0xN0003A	2	BOARD ID	Read Only	0x016C
0xN0003C	180	Unused		Unused
0xN000F0	4	FirmwareVer	Read Only	Firmware version
0xN000F4		Unused		
0xN50000	64 kbyte	CTRV VME Slot 1		Reserved
0xN60000	64 kbyte	CTRV VME Slot 2		Reserved
0xN70000	64 kbyte	CTRV VME Slot 3		Reserved
>0xN80000		Unused		Unused

2.3.3. REGISTERS DESCRIPTION

2.3.3.1. RECEIVERMODID

Bits 0-5 of the Receiver Module Ident code word are used to identify the installed Receiver modules (between OCP SRX03 or SRX24, and TRR)

ReceiverModID		0xN00006
bit	**Function**	**Remarks**
0-1	Ch1	See below
2-3	Ch2	See below
4-5	Ch3	See below
6-15	Unused	

The two-bit code has the following meaning:
00 = No module installed
01 = OCP SRX03
10 = OCP SRX24
11 = TRR, Truelight Module

2.3.1.1. STATUS

Name	Offset	Size	Access	Default Values
STATUS	0x006	8 bits	R/W	0xA0

Bits	Function	Remarks
STATUS	0x006	8 bits
15-3	Unused	
2	PrstCh3	1 = CH3 present*
1	PrstCh2	1 = CH2 present*
0	PrstCh1	1 = CH1 present*

The channel is declared as being present if the measured frequency (see CHX_FREQ registers) matches with the following table:

	frequency
OCP	8.99 MHz up to 402.28 MHz
TRR	1.6 kHz up to 50.01 MHz

OCP :SRX03 & OCP SRX24

TRR : Truelight Module

2.3.3.2. VREF REGISTERS (ONLY FOR TRR OR EQUIVALENT PHOTODIODES)

These registers only work with the photodiodes plugged in the Truelight socket. They set up the value of the comparator threshold installed at the input of each channel. For a balanced signal (typically a clock), the value must be as low as possible, but has to be above the noise threshold.

Name	Offset	Size	Access	Default Values
CH1_OUTPUT_REF_SIGNAL	0x0012	8 bits	R/W	0xA0
CH2_OUTPUT_REF_SIGNAL	0x0014	8 bits	R/W	0xA0
CH3_OUTPUT_REF_SIGNAL	0x0016	8 bits	R/W	0xA0

For a balanced signal (typically a clock), the value must be as low as possible, but has to be above the noise threshold. That is why the appropriated value for clock signals is between 0x05 and 0x09 at -12dB.

For a unbalanced signal (typically a pulse (Revolution Frequency, injection pulse)), the value must be more than the amplitude of the pulse at the output of the optical receiver, but not too high. That is why the appropriated value for pulse signals is between 0x70 and 0xA0 at -12dB.

Note: be careful, if the VREF value is 0x0 (see below), the module is measuring the frequency of the noise…And it is possible that the measured frequency of the picked up noise recognised as a good one. So never put less than 0x5 on the VREF registers

Here are some details about these registers:

CHX_REF are a group of register that control the previously mentioned Thevenin Network in the 3 channels. The values of these registers will be sent to the DAC to modify the network.

The modification is linear and follows the equation:

$$Vdiff = V^{+} - V^{-} = 120 \bullet \frac{Voff(202 + R) - Vcc \bullet R}{(202) \bullet (202 + R)}$$

$$Voff(mV) = DACvalue * 4.7mV$$

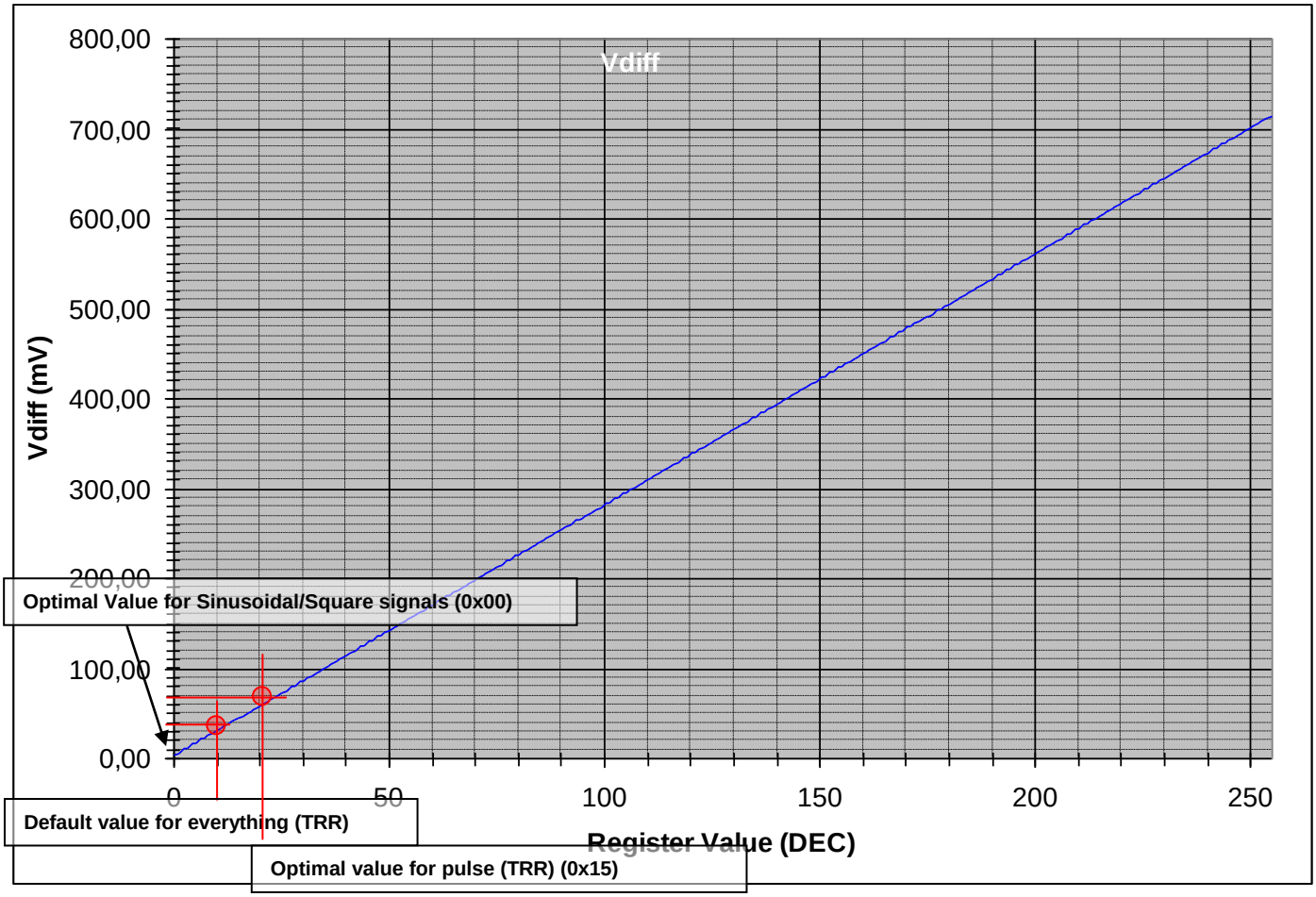
Where:

Vdiff is the differential voltage between the differential lines

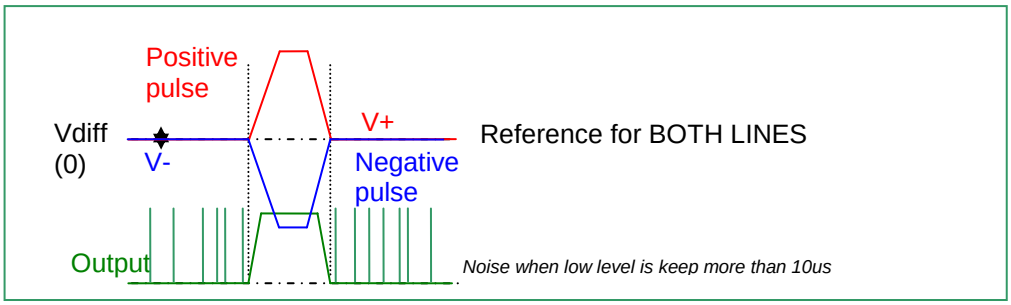
Voff is the DAC voltage value

R is the Manual Thevenin modifier

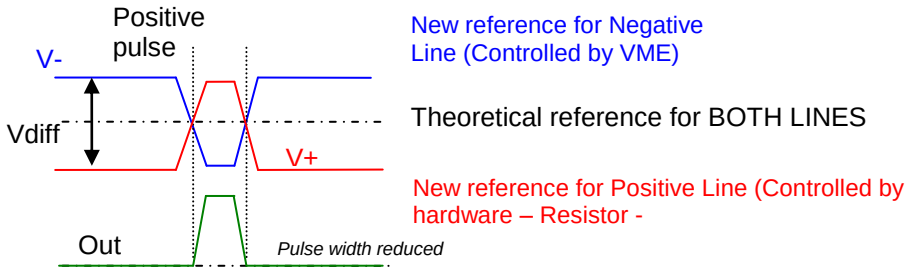
Supposing a R=0 we can obtain this graph where is possible to select graphically the value for the register (the value is in Decimal, do not forget to change to hexadecimal)



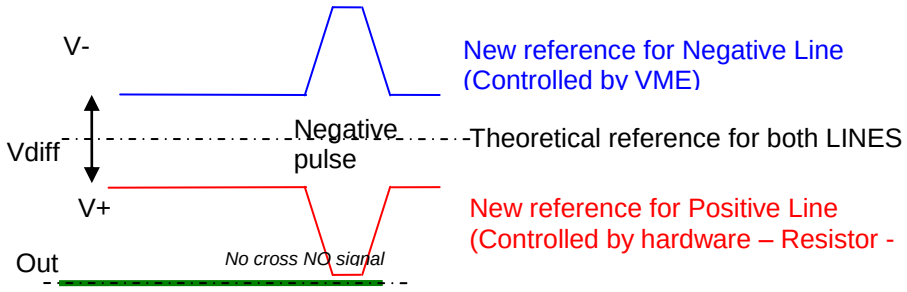
Picture 2.3.3.3a : Vdiff variation with Vref_register



Picture 2.3.3.3b: Positive pulse in balanced Thevenin network



Picture 2.3.3.3c: Positive pulse in an Unbalanced Thevenin network



Picture 2.3.3.3d: Negative pulse in an Unbalanced Thevenin network

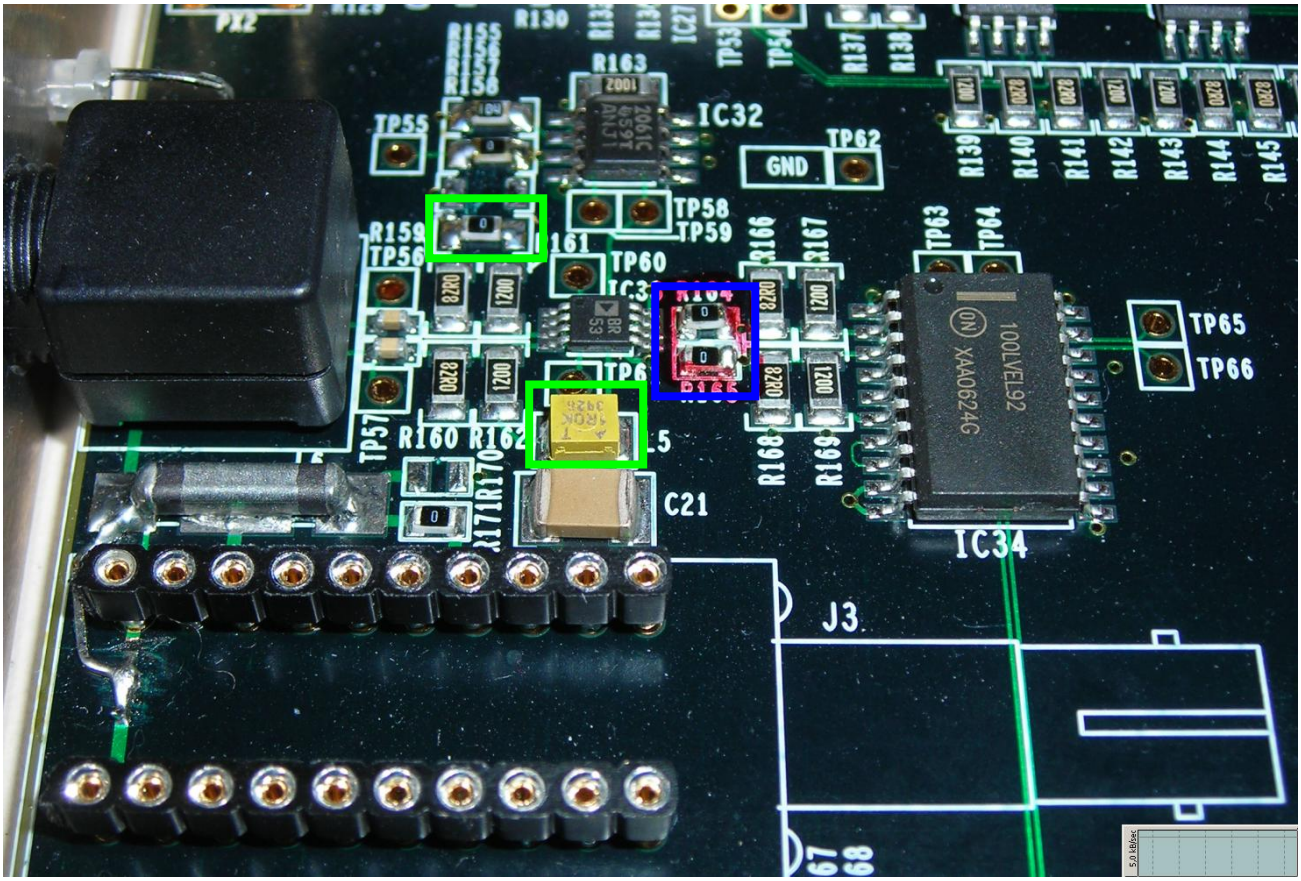
Review:

When the network is balanced, the user must avoid keeping a level for more than 10us.

When the network is UNBALANCED, the network will force zero detection when there is no signal, negative or zero signal. When a positive level is received, the output will change to positive following the received signal for a maximum of 10us will received.

Examples of Outputs with unbalanced network:

Input	Output	notes
Low level 50 seconds	Low level 50 seconds	
Low (50s) high(5us) low (50s)	Low (50s) high(5us) low (50s)	
Low (50s) high(50us) low (50s)	Low (50s) high(~10us) low (50s+ 40us)	AGC actuation, setting up the level received to 0



Picture 2.3.3.3e: Truelight Selection – Vref controlled by FPGA/VME (0R0) + Inductance

2.3.3.3. FREQUENCY COUNTERS

CH1

Name	Offset	Size	Access
CH1_FREQ_LOW	0x0018	16 bits	R
CH1_FREQ_HIGH	0x001A	16 bits	R

CH2

Name	Offset	Size	Access
CH2_FREQ_LOW	0x001C	16 bits	R
CH2_FREQ_HIGH	0x001E	16 bits	R

CH3

Name	Offset	Size	Access
CH3_FREQ_LOW	0x0020	16 bits	R
CH3_FREQ_HIGH	0x0022	16 bits	R

The full 32 bits frequency register must be read in a special order, which is from LSW to MSW.

If not, the 32 bits register won't be updated the right way.

These registers are generated by internal counters that count the number of rising clocks between rising edges in the received signals.

In order to measure higher frequencies than the clock frequency, a frequency divider has been installed on the board (4 hardware Flips-Flops = > 1/16) and inside the FPGA (software divider 1/22)

Every counter has a size of 32 bits that is divided in two registers of 16bits that must be read separately due to the fact that the board has only A24/D16 access.

In order to calculate the frequency, the equation is:

$$Freq = \frac{80 \bullet 16 \bullet 22}{FreqLow + FreqHigh \bullet 65536^{*}}$$

* This multiplication must be done in LONG UNSIGNED INT or FLOAT

Examples:

Frequency Original (MHz)	ValueReg1	Value Reg2	Frequency Measured (MHz)
10	0x0000	0x0B00	10
40.078	0x0000	0x02BF	40.0568
	0x0000	0x02BE	40.113
400.78	0x0000	0x0047	396.619
	0x0000	0x0046	402.285
Pulse 1MHz	0x0000	0x6e00	1MHz
Pulse 11.245KHz	0x0026	0x361A	11.245027KHz
No signal	0xFFFF	0xFFFF	6Hz

Table 2.3.3.4 : Typical examples of values of the frequency counter

2.3.3.4. BOARD IDENTIFICATION

2.3.1.2. IDENT CODE

Ident Code			0xN0008
Bit	Function	default	access
0-15	Ident Code	0x1A	R

2.3.1.3. CARD ID

CARD ID			0xN00024
Bit	Function	default	access
0-15	CARD ID	0x1382	R

This register contains the EDA number of the board (EDA-001382)

2.3.1.4. BOARD ID

BOARD ID			0xN0003A
Bit	Function		access
0-15	BOARD id	0x016C	R

This register contains the VME64x board ID of the RF-RX (CERN centrally defined) and is set to the value 364 (0x16C). See http://ess.web.cern.ch/ESS/boardIDistribution/PHP/ for details

2.3.1.5. FIRMWARE VERSION

Firmware version			0xN0003A
Bit	Function		access
0-31	Firmware version		R

2.4. CALIBRATION PROCEDURES (TRR OR SIMILAR PHOTODIODE)

The calibration procedure will apply only to the channels where a TRUELIGHT or equivalent photodiode is installed.

The OCP photodiodes DO NOT REQUIRE ANY CALIBRATION. Only be selected (see section 2.2.1.1)

The calibration procedure can be done manually or trough VME, dividing this last option in two different scenarios.

Knowing the frequency and type of the signal received

Unknowing the frequency and type of the signal received

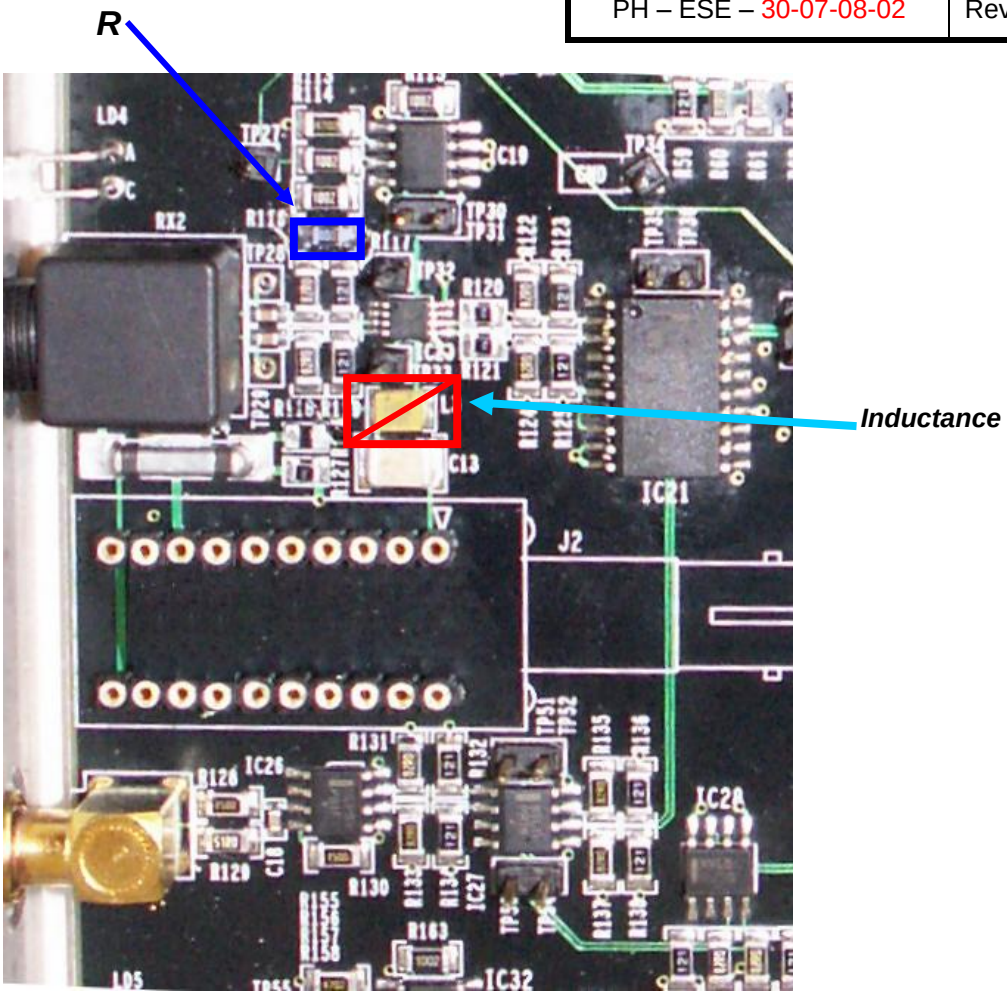
In order to read and modify the board's registers the program rfrxscope * has been developed. It helps the user accessing the board registers in an interactive way.

* rfrxscope has been written by Markus Joos.

2.4.1. MANUAL CALIBRATION (FIX VREF VALUES)

This configuration will be applied when a VME controller is not present or block the references to avoid third part modifications or intromission.

The manual modification is done by modifying the Resistors R and disconnecting/de-soldering the inductance (more information about full Truelight Set UP in section 2.2.1)



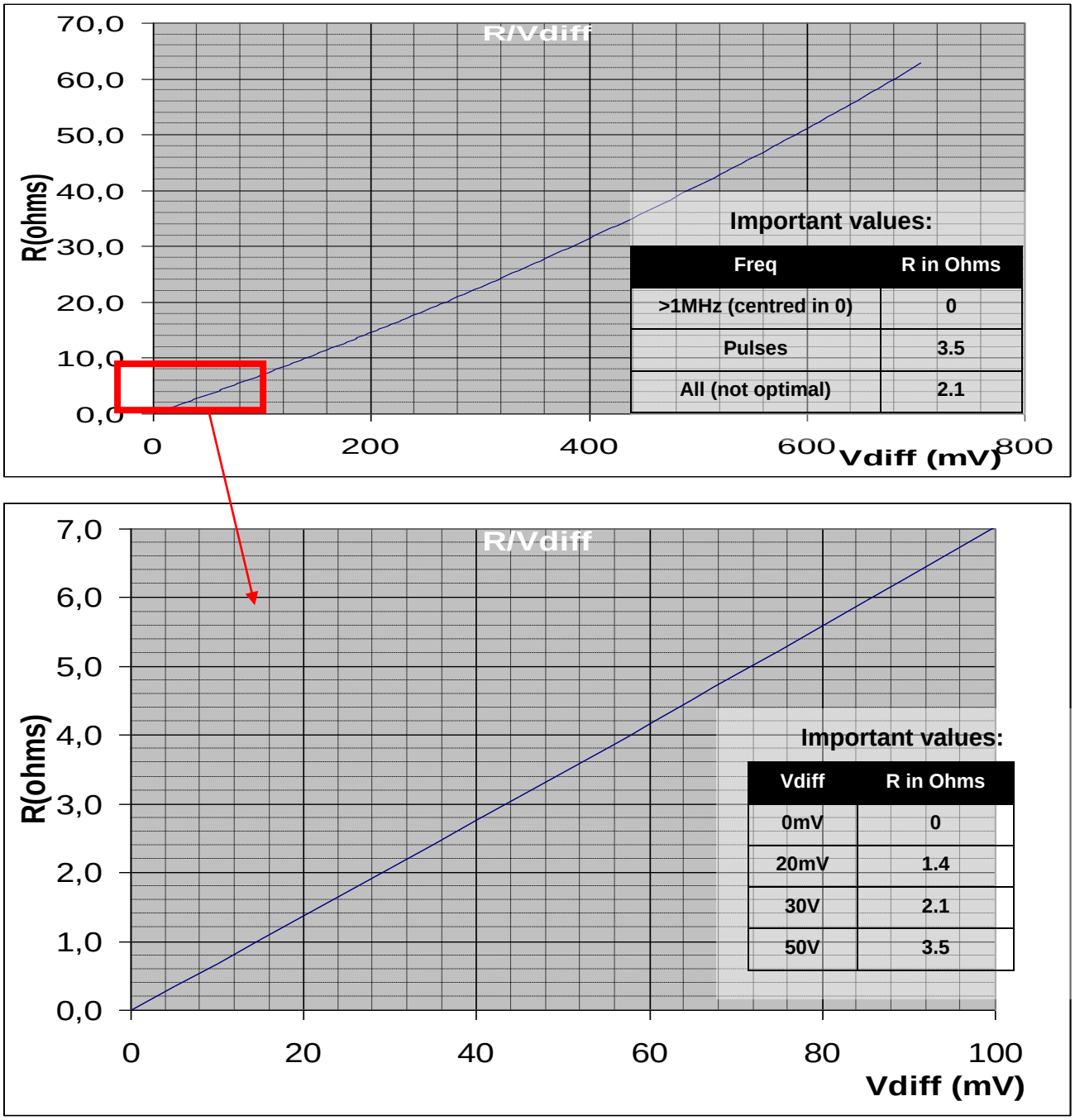
Picture 2.4.1a: Manual Calibration set UP

In order to calculate the R convenient the user must follow the equation:

$$Vdiff = V^{+} - V^{-} = 120 \bullet \frac{Vcc \bullet R}{(202) \bullet (202 + R)}$$

$$R = \frac{202 \bullet Vdiff}{Vcc \bullet 0.594 - Vdiff}$$

Or the next Graphs:



Pictures 2.4.1b: Calibration Graphs

2.4.2. THROUGH VME KNOWING THE SIGNALS AND PHOTODIODES USED.

The calibration can be done with monitor software like rfrxscope (By Markus Joos) or with readRXD monitor (Tcl application that run over Markus Joos Vme_Drivers).

If the user is close to the board and knows the type of receivers that are mounted and which signal type they are receiving.

Then, apply these rules

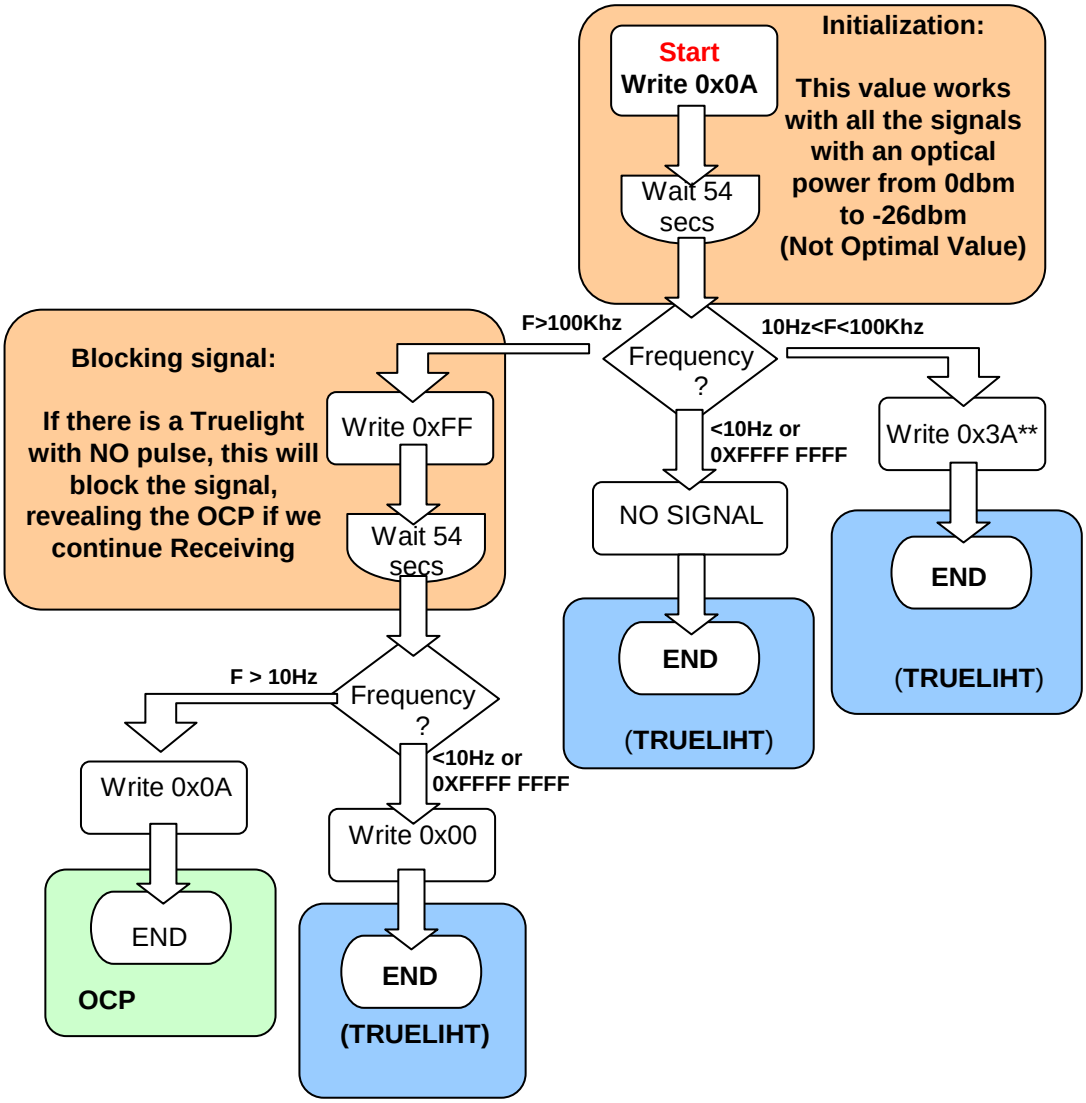
Photodiode	Signal	Vref Value
OCP SRX 03	1Mhz to 100Mhz clocks	No adjustment required
OCP SRX 03	400Mhz or Pulses clocks	Don't care – Not supported
OCP SRX 24	1Mhz to 500Mhz clocks	No adjustment required
OCP SRX 24	Pulses	Don't care – Not supported
Truelight	0.5Mhz to 400Mhz clocks	Required: 0x09
Truelight	Pulses	Required: 0xa0
Truelight	*Any (not optimal)*	*Required: 0xa0*

Table 2.4.2: Manual Calibration Values

2.4.3. THROUGH VME UNKNOWING THE SIGNALS AND PHOTODIODES

This will be the procedure (algorithm) to apply when the user doesn't know what types or receivers are installed in the board and which types of signals are received.

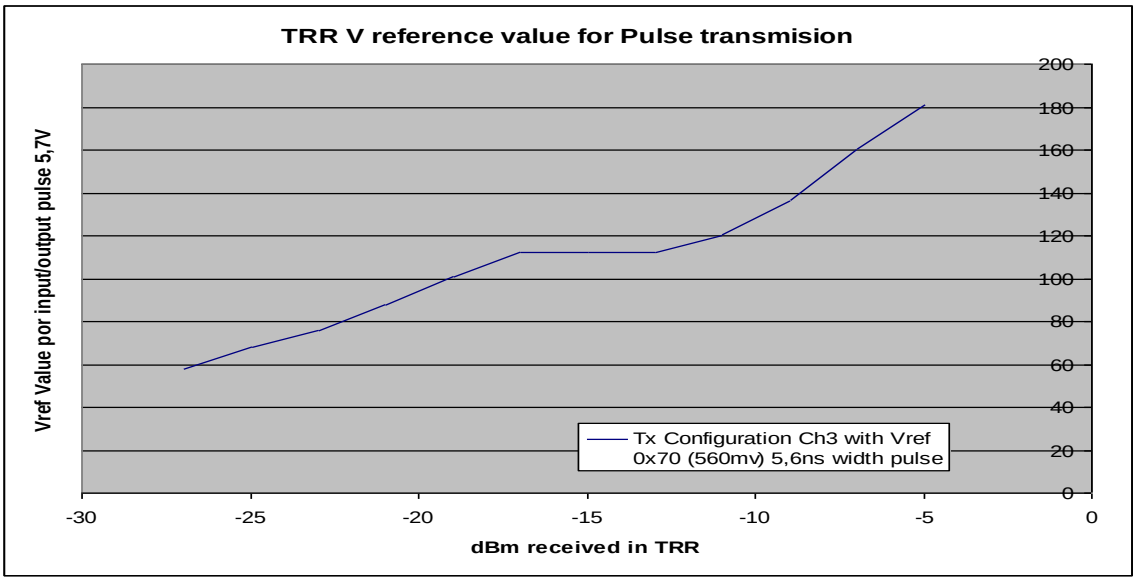
Like in the same procedure, VME access software will be required in order to read and modify the desired registers.

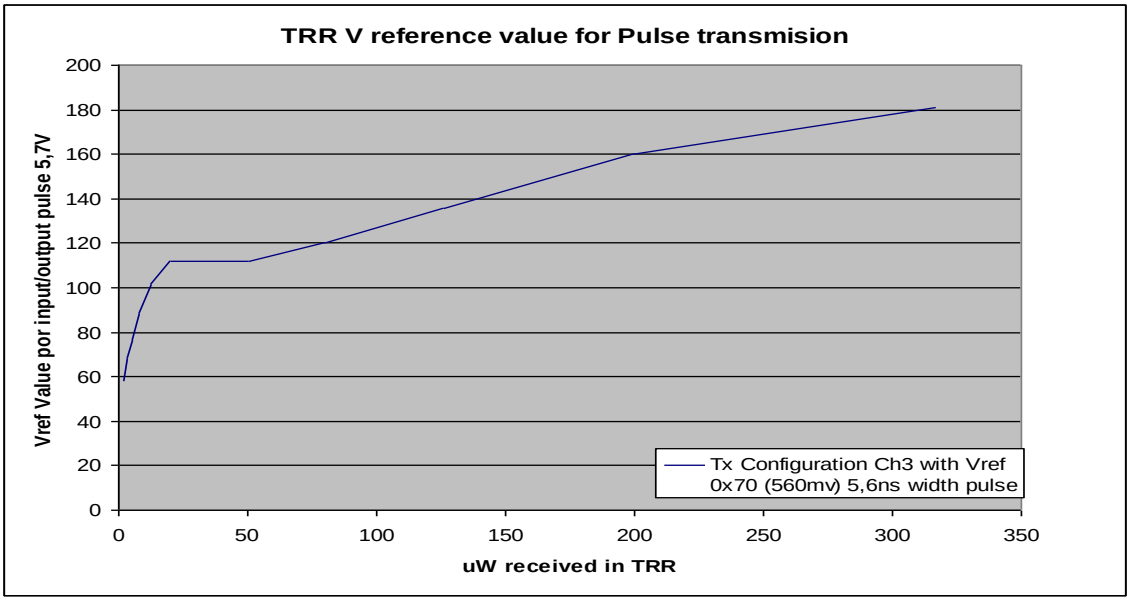


Picture 2.4.3: Remote Calibration Procedure

** This value is the minimum value to accept the pulse in good conditions and correspond to the worst scenario possible (signal reception at -27dBm). More values can be found in the next tables and graphs

Power Received in dBm (5.6ns width)	Pw (uW)	Value Hex for obtain a output Pulse widh of 5,6ns	Value Dec
-5	316	0xB5	181
-7	199	0XA0	160
-9	125	0X88	136
-11	79	0X78	120
-13	50	0X70	112
-15	31	0X70	112
-17	19	0X70	112
-19	12	0X65	101
-21	7	0X58	88
-23	5	0X4C	76
-25	3	0X44	68
-27	1	0X3A	58





2.5. BOARD CONFIGURATION- JUMPERS AND SWITCH

Element	Description
LSB rotary switch	See 2.3.1 section
MSB rotary switch	See 2.3.1 section
Reset(Front Panel) button	Generate a Soft reset of the FPGA when is pressed
ST5	Always OFF
ST4	Always ON
TP25	Frequency selector0 for the JTAG
TP26	Frequency selector1 for the JTAG
ST3	If ST3 is ON -> the FPGA will be reprogrammed when the VME crate reset will be activated (triggered by a VMEbus SYSRESET)

Table 2.5: Jumpers and Switch descriptions

2.6. FIBRE / CABLE CONNECTIONS

Connector name	To be connected to	Format
CH1 IN Optical Link	RF Digital TX	Optical (Digital or Analog)
CH1 RF Out	50omhs LOAD	LVPECL 50ohms AC/DC coupled
CH2 IN Optical Link	RF Digital TX	Optical (Digital or Analog)
CH2 RF Out	50ohms LOAD	LVPECL 50ohms AC/DC coupled
CH3 IN Optical Link	RF Digital TX	Optical (Digital or Analog)
CH3 RF Out	50ohms LOAD	LVPECL 50ohms AC/DC coupled
J5	JTAG	JTAG MODE (FPGA)
J6	JTAG	BIT BLASTER MODE (EEPROM)

Table 2.6: Connectors and Descriptions

2.7. FRONT-PANEL LEDS

LED	Description
VME COMM	Indicates if the last VME cycle was successful or wrong
ERROR LED	Indicates an VME bus error (wrong register access)
CH1 LED (SD CH1)	Indicates Optical signal when is receiving >-30dbm
CH2 LED (SD CH2)	Indicates Optical signal when is receiving >-30dbm
CH3 LED (SD CH3)	Indicates Optical signal when is receiving >-30dbm

Table 2.7: Front Panel LEDS

2.8. REFERENCES OR MORE INFORMATION

Lasers and Photodiodes evaluation (by Angel Monera)

EDA documents (https://edms.cern.ch/nav/eda-01382)

RF_RX_D TCL console Manual

RF_TX_D User Manual

3. TTC COMMON SOFTWARE

3.3. INTRODUCTION

3.3.1. H/W ENVIRONMENT

3.3.2. S/W ENVIRONMENT

3.4. TEST PROGRAMS

3.5. THE USER LIBRARY