DSP2

User's Manual

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http://www.ro.feri.uni-mb.si/Welcome.html-l2

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Firmware version:	V0.80	(April 17, 2000)
PCB version:	V1.00	(Februar 12, 2000)
Bios version:	V1.10	(Mai 12, 2000)
Terminal version:	V1.1a	(Jan 23, 2000)

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1. DSP board overview

The DSP-2 board is a high performance, floating point digital signal processor (DSP) based inverter controller designed primarily to control a three-phase AC motor. The board is based on Texas Instruments TMS320C32 DSP and Field Programmable Gate Array (FPGA) XCS40-4PQ240C member of Xilinx Spartan Family.

- DSP TMS320C32-60MHz
  - DSP serial interface
  - Two timer general purpose io pins
  - DSP MPSD interface for XDS510 emulator
- FLASH 256K x 8 - 70ns
- SRAM 128K x 32 0WS
- 4 channel simultaneous 12bit A/D with serial output
  - Conversion and transfer to register in FPGA 2,6µs for all four channels
  - One channel has unipolar input range 0 to 4.095V or 0 to 40,95mA with 100OHM shunt resistor (udc)
  - Two have bipolar input range –2.096 to 4.094V or -40,96mA to 40.94mA with 100OHM shunt resistor
  - One channel has input multiplexer to select one of eight voltage input signals
  - First order input RC filters (time constant 33µs for i1 and i3 and 100µs for udc)
- Two channel 12bit D/A converter with serial input and unipolar output 0 to 4V
- RS232 full duplex interface with fixed Baud Rate (38400kBd 8bits ,1stop ,No parity)
- RS485 interface (not implemented in this firmware version (April 17, 2000)
- RS422 receiver for incremental encoder
- Three logic inputs and one output – all optically isolated (12V passive)
- Bridge protection circuit
  - Interlock between bottom and top IGBT activation and dead time
  - Minimum pulse width, minimum pause width
  - In the presence of fault signal the bridge is shut down unconditionally
- Three phase synchronous pulse width modulator
  - Twelve bit up/down counter for triangle generation
  - Symmetrical output pulses
  - 66.6ns time resolution
  - can generate interrupt pulses ones or twice in one modulator period
- Incremental encoder speed measurement with improved MT method
  - 66.6ns time resolution
  - Position register contain position increment during sampling period
  - Time register contain relative time (in one modulator period) of last position change
  - Booth registers are saved on interrupt and are available until next interrupt
- Stand alone operation. Program is preloaded in FLASH.
- Operation with personal computer
  - Code Composer software development environment
  - Standard RS232 serial interface (38400Bd) and Terminal software
  - MPSD interface for XDS510 emulator
  - Multipoint communications RS485 and CAN (not implemented yet)
- Board dimensions 161 x 130 mm

2. Simplified Function Diagram

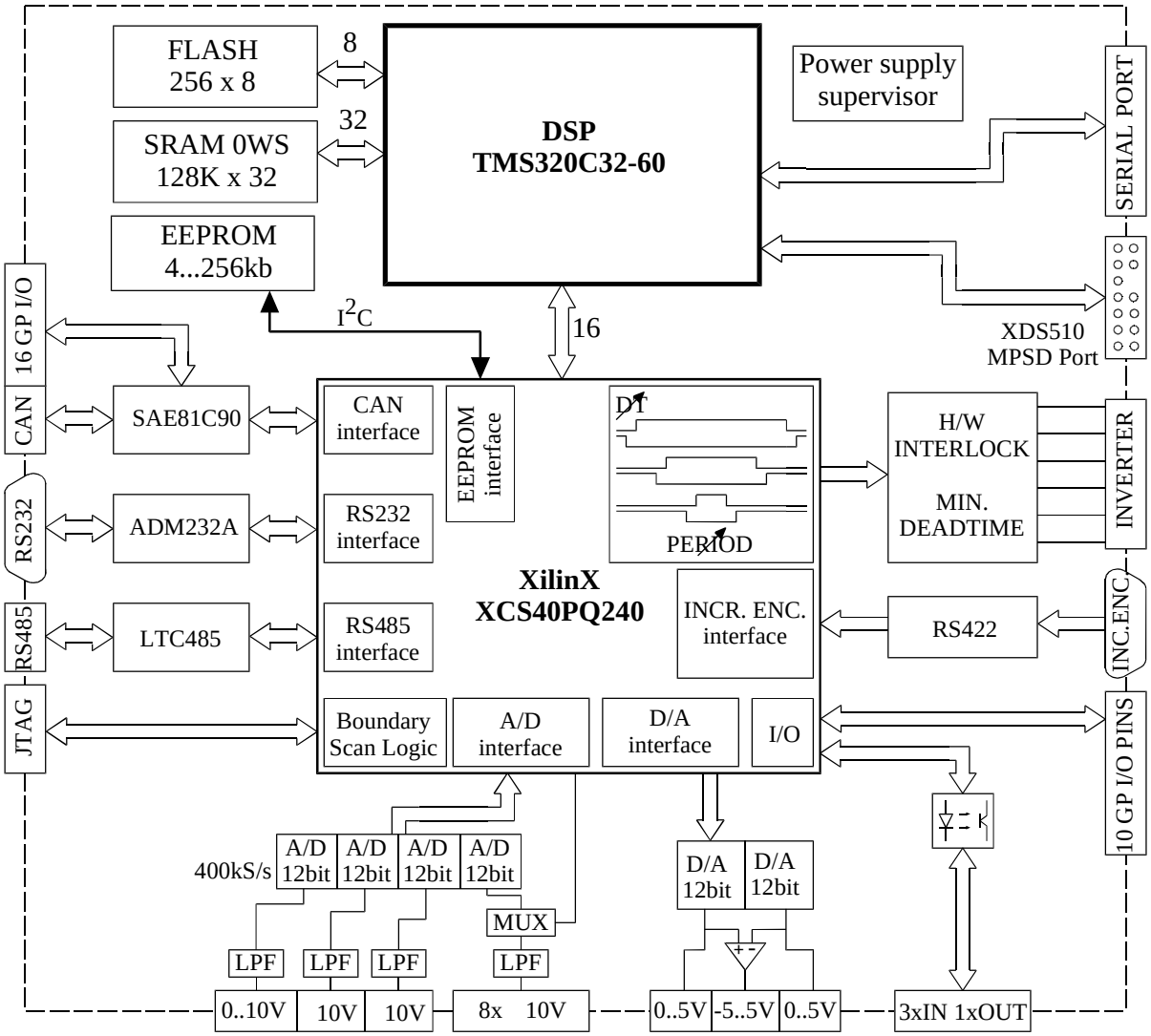


Figure 1: DSP2 Function Diagram

3. DSP2 Memory Map

Table 1: DSP2 Memory Map

0x810000 … 0x82FFFF	FLASH	128K*8 bits
0x880000 … 0x89FFFF	RAM	128K*32bits
0x900000 … 0x900FFF	FPGA	*16bits

4. Interrupts

External interrupts are controlled by firmware in FPGA. In this version (April 17, 2000) only one interrupt (INT0) are generated by three phase pulse width modulator. Interrupt can be generated once or twice in one modulator period. Interrupt INT1 is used for boot mode select.

5. FPGA Registers Reference

Table 2: FPGA Register Map

Address	WRITE	READ
0x900000	DA0	DA_STAT
0x900001	DA1	AD0 (udc)
0x900002	ADCRTL	AD1 (i1)
0x900003	TX0	AD2 (i3)
0x900004	CTRL	AD3 (mux)
0x900005	W_MOD_PER	RX0
0x900006	W_MOD_T1	RS_STAT
0x900007	W_MOD_T2	R_INC_POS
0x900008	W_MOD_T3	R_INC_TIME
0x900009	W_MOD_TM	R_CAN_STAT
0x90000A	W_CAN_CTRL	Reserved
0x90000B	Reserved	Reserved
0x90000C	Reserved	Reserved
0x90000D	Reserved	Reserved
0x90000E	W_I2C	R_I2C
0x90000F	W_FLASH	R_MOD_STAT
0x900800 … 0x9008ff	W_CAN	R_CAN

5.1 AD Unit

Figure 2: Analog Input Configuration

Note: -Analogue VCC is separated
-Internal voltage reference is used
-Vss pin is connected to –5V for bipolar operation i1,i3!
-Leading bits for udc are zero except MSB (bit 15) which is 1 during A/D conversion (unsigned extension to 16 bits)
-For currents measurement (i1 and i3) leading bits (bit 15, 14, 13 and 12) are equal to bit 11 (signed extension to 16 bit)
-User must extend read value to 32 bits depend on data type

5.1.1 AD Operation

AD conversion is started by interrupt request. After approximately 2.5 microseconds simultaneous conversion of all four channels is finished. You have time to next interrupt to read converted data.
Fourth channel (AD3) is connected to multiplexer which choose one of eight analogue inputs. Decision is made with register ADCTRL and bits 0 to 2.

Note: In current version of FPGA firmware (April, 17 2000) A/D conversion is started when write to ADCTRL register appear.

Register ADCTRL (address 0x900002 - WRITE)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	NC	NC	NC	NC
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
NC	NC	NC	NC	NC	AD_MUX2	AD_MUX1	AD_MUX0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Table 3: AD3 Input selection table

ADCTRL	AD_MUX2	AD_MUX1	AD_MUX0	Analog
0x0000	0	0	0	CH0
0x0001	0	0	1	CH1
0x0002	0	1	0	CH2
0x0003	0	1	1	CH3
0x0004	1	0	0	CH4
0x0005	1	0	1	CH5
0x0006	1	1	0	CH6
0x0007	1	1	1	CH7

Note: -Use 0 for all unused bits for future FPGA configurations compatibility.
-NC means not care (for this firmware)

Register AD0 (address 0x900001 - READ)

15	14	13	12	11	10	9	8
AD_BUSY	0	0	0	B11	B10	B9	B8
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

AD_BUSY: A/D converter status:
1 = conversion is in progress (You must wait until bit is set 0!)
0 = conversion finished

Note: Same busy bit (AD0.AD_BUSY) is used for all four analogue converters because the conversion is simultaneous.

B0 – B15: 16-bit unsigned data udc. IF AD_BUSY is 0!

Registers AD1 (address 0x900002), AD2 (address 0x900003), AD3 (address 0x900004)

15	14	13	12	11	10	9	8
B11	B11	B11	B11	B11	B10	B9	B8
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

AD1, AD2 and AD3 are data registers that contain AD conversion results. Bit 11 is a sign bit and is extended to bits 12 thru 15 to form 2nd complement.

Note: Same busy bit (AD0 – BUSY) is used for all four analog converters because the conversion is simultaneous.

B0 – B15: 16-bit unsigned data udc. IF AD_BUSY is 0!

Registers AD1 (address 0x900002), AD2 (address 0x900003), AD3 (address 0x900004)

15	14	13	12	11	10	9	8
B11	B11	B11	B11	B11	B10	B9	B8
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

AD1, AD2 and AD3 are data registers that contain AD conversion results. Bit 11 is a sign bit and is extended to bits 12 thru 15 to form 2nd complement.

Note: Same busy bit (AD0 – BUSY) is used for all four analog converters because the conversion is simultaneous.

5.2 I²C EEPROM

Register W_I2C (address 0x90000E)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	NC	NC	NC	NC
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
NC	NC	NC	NC	NC	NC	SDA	SCL
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Bit 0: connected to SCL line

Bit 1:
0 SDA pin is in THREE STATE (external pull-up resistor apply high logic level)
1 SDA shorted to ground low logic level
Note: NC means not care (for this firmware)
For future compatibility write always write 0 to NC bits

Register R_I2C (address 0x90000E)

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
1	1	1	1	1	1	SDA	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

Bit 1: connected to SDA line

Note: Use only level of Bit 1 (SDA) for future compatibility.

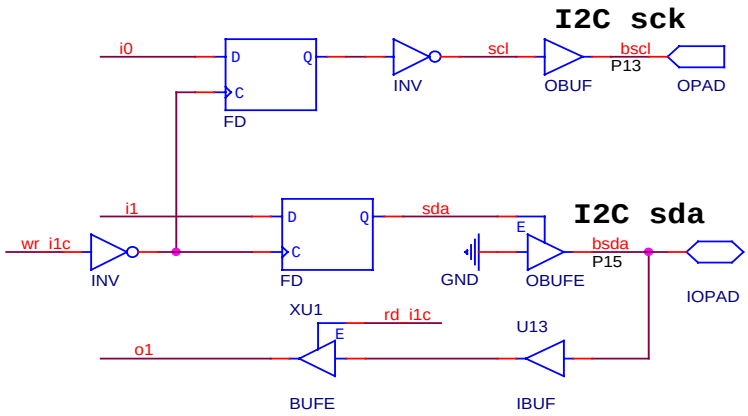


Figure 3: I2C Implementation Detail

Because pin compatibility of serial I2C EEPROMs any type of memory in 8 pin SO package can be used (for example M24C01, M24C02, M24C04, M24C08, M24C16, M24C32, M24C64, M24C128, M24C256 or M24512 – ST Microelectronics) On DSP2 M24C04 is implemented (512 bytes x 8 bits).

Write Control (WC)
This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control (WC) is driven High. (Jumper J7 is not inserted) When Write Control (WC) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

5.3 Asynchronous Serial Communications Interface

Receiver Status Register RS_STAT (address 0x900006)

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
TRF	RRF	OV	FE	1	1	SDA	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

FE: framing error (invalid stop bit)
OV: overflow (previous byte is not read while new received)
RRF: receive register full (unread byte is in receive register)
All three bits are cleared when receive register is read
TRF: transmit register full

Serial Control Register CRTL (address 0x900004)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	NC	NC	NC	NC
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
SRG7	SRG6	SRG5	SRG4	SRG3	SRG2	SRG1	SRG0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

SRG7…0: SELECT Baud Rate
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

Figure 4: Asynchronous Serial Communications Baud Rate Select

SRG	BaudRate1	BaudRate2	Error[%]

SRG	BaudRate1	BaudRate2	Error[%]
195	9600	9615.38	0.16
98	19200	19132.65	0.35
49	38400	38265.31	0.35
33	57600	56818.18	1.36
16	115200	117187.50	-1.73
8	230400	234375.00	-1.73
4	460800	468750.00	-1.73

Note: This feature is not implemented in firmware version April 17, 2000 in FPGA.

Serial Receive Register RX0 (address 0x900005)

15	14	13	12	11	10	9	8
1	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

B7 ... 0: received byte

Serial Transmit Register TX0 (address 0x900003)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	NC	NC	NC	NC
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B7…0: byte to transmit

Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

Receive and transmit registers are double buffered. This mean that another character can be received while previous one is in the receive register. You must read previous character just before next one is complete received. Same thing is with transmit register. When the output shift register is empty then serial transmit register is empty for new character in less than 1 / (**16** * BAUD RATE). Transmission time for one character is 10 / BAUD RATE.

5.4 Three Phase Pulse Width Modulator

Modulator Period Register W_MOD_PER (address 0x900005)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B11…0: modulator period
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

PERIOD register: Half period of PWM is equal PERIOD + 1, while whole period is 2(PERIOD+1). Values for this register must be between 2 and 2000. Unit for period is 1 / 60MHz * 4 = 66.6ns*

Modulator Dead Time Set Register W_MOD_TM (address 0x900009)

15	14	13	12	11	10	9	8
NC	NC	NC	I_EN	OM	RELAY	BOFF	BON
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B7…0: modulator period
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

TM register:
B7 ... 0: dead time between top and bottom switch in bridge (another hardware protection implemented in GAL circuit limit dead time to about 3.5micro second minimum - RC time constant). TM is used because RC constant is not enough accurate - approximately 10%. Unit is 50ns. Value must be between 0 and 255.
Same register contain logic output bits:
B_ON: bridge on
B_OFF: bridge off
RELAY: relay (for by-pass charge resistor for DC link)
OM: -0 single interrupt request in one period of PWM
-1 interrupt request in each half-period of PWM
I_EN: PWM interrupt enable

Important:
Between bridge on and hardware flip-flop RC differentiator is used to prevent override of bridge error or bridge off signal. Bridge on signal MUST be low few tens of microseconds before go to high to switch flip-flop ON.

Modulator Phase 1 Pulse Width Register W_MOD_T1 (address 0x900006)

Modulator Phase 2 Pulse Width Register W_MOD_T2 (address 0x900007)

Modulator Phase 3 Pulse Width Register W_MOD_T3 (address 0x900008)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B11…0: modulator phase 1, 2 and 3 pulse width
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

With register W_MOD_T1 output pulse width for first phase is set. Unit is 66.6ns. Value is between 0 and 2000. When output is 1 TOP IGBT is active, when output is 0 active is bottom one. When transition of signal appear then immediately active IGBT is inactivated and then, after dead time, another one is activated.

Modulator Status Register W_MOD_STAT (address 0x90000F)

15	14	13	12	11	10	9	8
B_EN	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

Status of bridge:
B_EN: bridge enable

With bridge on and bridge off you can toggle hardware flip-flop. Bridge enable show the state of this flip-flop. State of the flip-flop can also be changed with error signal from IGBT Bridge to zero. Error signal in Mini SKiiP bridge includes: over current, earth connection (sum of phase currents must be zero), over heat...

5.5 FLASH PROM Interface

Flash PROM Register W_FLASH (address 0x90000F)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
NC	NC	NC	NC	XX1	XX6	A17_F	A16_F
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Logical outputs:
A16_F: A16 FLASH
A17_F: A17 FLASH
These two bits are for change page in FLASH. Because only 8 bit data width FLASH is only used for boot-loader program. After download FLASH is disabled. In future user program can be downloaded from FLASH.
XX6: test pin xx6
XX1: test pin xx1
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)
For XX6 and XX1 see section FPGA extension pins.

5.6 Analog Output Unit

Analog Output 0 Register DA0 (address 0x900000)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B11… B0: 12 bit unsigned value (0 = 0V, 4095=4.095V)
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

Analog Output 1 Register DA1 (address 0x900001)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

B11… B0: 12 bit unsigned value (0 = 0V, 4095=4.095V)
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)

Analog Output Status Register DASTAT (address 0x900000)

15	14	13	12	11	10	9	8
DA_BUSY	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

DA_BUSY: 1-interface busy

When data is writen to second D/A register serial transmit to D/A converter is started and bit 15 in DASTAT is set to 1. This bit is cleared to zero when both channels are transmitted and interface is ready for new data. When bit 15 in DASTAT is set, writing to any of DA0 or DA1 is prohibited and can cause transmit of void data to DA converter!

5.7 Incremental Encoder Interface

Incremental Encoder Position Read Register R_INC_POS (address 0x900007)

15	14	13	12	11	10	9	8
B11	B11	B11	B11	B11	B10	B9	B8
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

On each interrupt value from position counter is transferred to this register and COUTER IS CLEARED. Position must be externally accumulated. Value is 16 bit long in 2'nd

complement notation. And must be extended to 32 bits with sign and added to software position value. Maximal number of pulses between two interrupts must be less than 2048 pulses. Input signal are sampled 15 million times every second so maximal input frequency must be under 3.75MHz.
In this version of FPGA firmware counter has eleven data bits and sign.

Incremental Encoder Time Read Register R_INC_TIME (address 0x900008)

15	14	13	12	11	10	9	8
STATUS	0	0	0	B11	B10	B9	B8
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
R/-	R/-	R/-	R/-	R/-	R/-	R/-	R/-

STATUS: 1: data are invalid
0: data are valid
B11…B0: time between previous interrupt pulse and last pulse from incremental encoder

This register is used with improved MT method for speed measurement. Most significant bit is set when no pulses are received (in last period) from incremental encoder. In this case the other bits are not valid. If position was changed, this register contains the time between previous interrupt pulse and last pulse from incremental encoder. Units are same as units for PWM (66.6ns). This additional register improves speed measurement particularly for low speed range.

5.8 Extension IO pins on FPGA

Flash PROM Register W_FLASH (address 0x90000F)

15	14	13	12	11	10	9	8
NC	NC	NC	NC	B11	B10	B9	B8
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W
7	6	5	4	3	2	1	0
NC	NC	NC	NC	**XX1**	**XX6**	A17_F	A16_F
-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Logical outputs:
A16_F: A16 FLASH
A17_F: A17 FLASH
XX6: test pin xx6

XX1: test pin xx1
Note: Use 0 for all unused bits for future FPGA configurations compatibility.
NC means not care (for this firmware)
For A16_F and A17_F see section FLASH PROM Interface.

Figure 5: Connector with Test Pins on DSP2 Board Detail

Also the other XX pins are connected to FPGA but firmware version April 17, 2000 in FPGA supports only XX4 with ~1.19 Hz output signal. We use signals XX1 and XX6 for detection of execution times for different parts of software. We connect two led diodes between XX6 (pin 9) and GND (pin 7) and XX4 (pin 5) and GND. XX1 is used to connect oscilloscope.

5.9 CAN Interface

Write CAN Register W_CAN (address 0x900800F)

Read CAN Register R_CAN (address 0x900800F)

CAN Control Register W_CAN CTRL (address 0x9000A)

CAN Status Register W_CAN STAT (address 0x900009)

Firmware for CAN is implemented but is not tested yet.

We use SIEMENS CAN controller with multiplexed data and address bus.

Write is made immediately to registers in FPGA and then transferred to controller. Before next operation you must check busy bit, and in case if bit is set wait.

Read is different because with fist write you set address and after operation is complete you can read requested data in status register.

6. Connectors and Jumpers Locations

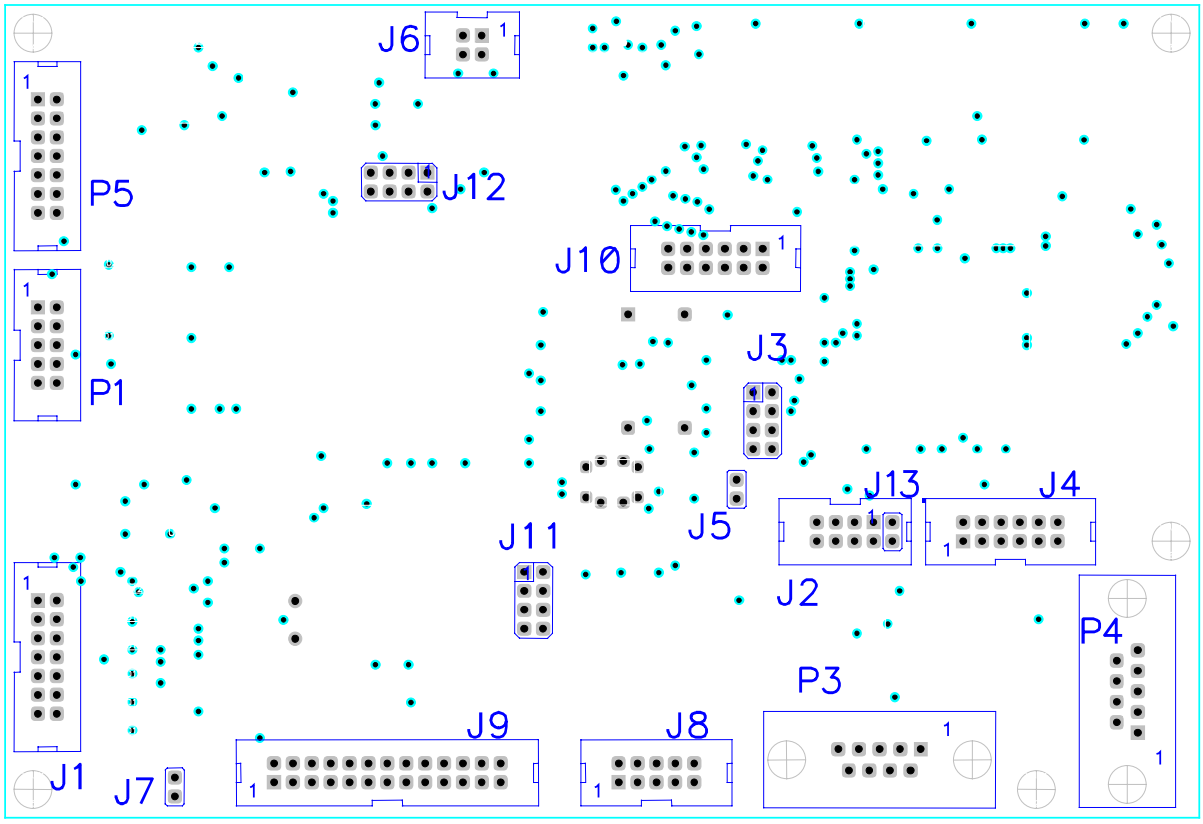


Figure 6: Connectors and Jumpers Locations

6.1 P1 – IGBT Bridge Analogue inputs

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	5	AGND	9	I3
2	V++	6	CH1	10	UDC
3	AGND	7	I1		
4	CH0	8	-		

6.2 P3 Serial communication (RS232)

Pin	Signal	Pin	Signal	Pin	Signal
1	-	4	RX (SEC)*	7	CTS
2	TX	5	GND	8	RTS
3	RX	6	TX (SEC)*	9	-

* SEC can be used in future FPGA configurations for second serial interface on the same connector. For this you must have “Y” cable to split signals.

6.3 P4 Incremental encoder input

Pin	Signal	Pin	Signal	Pin	Signal
1	/a	4	GND	7	+5V

Pin	Signal	Pin	Signal	Pin	Signal
2	GND	5	Ri	8	b
3	/b	6	a	9	/ri

All input signals are RS422 compatible (Complementary signals with TTL levels).
5V power supply can provide maximum 100mA output current.

6.4 P5 IGBT Bridge – digital I/O

Pin	Signal	Pin	Signal	Pin	Signal
1	Vpf	6	TOP3	11	VCC
2	TOP1	7	GND	12	BOT3
3	RELAY	8	BOT1	13	VCC
4	TOP2	9	GND	14	ERROR
5	GND	10	BOT2		

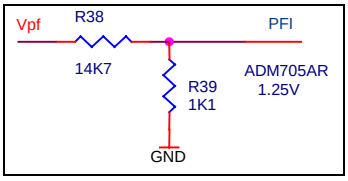


Figure 7: Power Fail Input Detail

If level on Vpf input is under 18V PFO is activated. On PCB this signal is connected to /INT3 input line of DSP. But because at reset of DSP this line is used to choose boot sequence, voltages on Vpf under 18V can start wrong start up sequence. So PFO is disconnected from /IRQ3 and left open. In future this output will be connected to free pin of FPGA and with firmware in it indirectly again connected to /IRQ3. Generally this is used to detect power fail few milliseconds before controller go in reset state and safely stop application. R38 and R39 are placed near P1 connector (bridge analogue inputs) and are shown on PCB picture for fast analogue inputs.

TOP1, TOP2, TOP3, BOT1, BOT2 and BOT3 are signals for 6 IGBT-s in bridge. Active is high output (5V) level.
RELAY output signal (active high level) is used to shortcut charge resistor in DC bus
ERROR is an input signal (active low level) to detect errors in IGBT bridge drive
VCC and GND is 5V supply for this card

6.5 J1 Analogue outputs, analogue inputs

Pin	Signal	Pin	Signal	Pin	Signal
1	V--	6	OUT0	11	CH_6
2	AVSS	7	CH_2	12	CH_7
3	AGND	8	CH_3	13	AGND
4	AOUT	9	CH_4	14	AVCC
5	OUT1	10	CH_5		

V-- is power supply for op amp to generate Aout=OUT0-OUT1 (-15V)
OUT0, OUT1 12 bit analogue outputs (0 … 4.095V)
AVSS power supply for bipolar analogue inputs (-5V)

AVCC power supply for analogue inputs (+5V)
AGND analogue ground
CH_2, 3, … 7 slow bipolar analogue inputs (input RC filter 1.1KOHM, 100nF)

6.6 J2 DSP serial communication

Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	4	CLKX0	7	CLKR0
2	FSX0	5	FSR0	8	GND
3	DX0	6	DR0		

See TMS320C32 data sheet. VCC and GND is supply voltage from card (100mA max).

6.7 J3 Jumpers for DSP Boot mode select

Pin	Signal	Pin	Signal	Pin	Signal
1	/INT0	4	GND	7	/INT3
2	GND	5	/INT2	8	GND
3	/INT1	6	GND		

Normally jumper between pin 3 and pin 4 must be placed. This causes DSP to boot from FLASH memory and starts monitor program in it.

6.6 J4 MPSD – emulator interface

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	5	NO PIN!	9	GND
2	H3	6	VCC	10	EMU0
3	GND	7	GND	11	GND
4	EMU3	8	EMU2	12	EMU1

This connector is provided for C3x emulator head. Emulator use simplified JTAG interface.

6.8 J5 DSP Watch dog enable

Pin	Signal	Pin	Signal
1	WDI (ADM705)	2	XF1 (DSP)

Watchdog input on ADM705 request state change on WDI input at least every 1.6-second. If this is not ensured reset signal for DSP is generated. If jumper is not inserted this function did not work. Current boot loader Version: x.xx written in FLASH did not support this function. Jumper mustn’t be inserted! XF1 is user programmable i/o pin of DSP.

6.9 J6 Serial interface RS485

Pin	Signal	Pin	Signal
1	VCC	3	/A
2	A	4	GND

Connector J6 provides standard RS485 serial interface with 5V power supply. Firmware in FPGA (April, 17 2000) did not support this feature.

6.10 J7 EEPROM write enable

Pin	Signal	Pin	Signal
1	WE (EEPROM)	2	GND

If jumper is not inserted upper half (Microchip) or entire (ST) EEPROM memory is write protected.

6.11 J8 optically isolated (three inputs and one output)

Pin	Signal	Pin	Signal	Pin	Signal
1	IN1+	5	IN3+	9	OUT+
2	IN1-	6	IN3-	10	OUT-
3	IN2+	7	-		
4	IN2-	8	-		

Those optic isolated signals are passive. All Inputs request 12V. Output current must be under 100mA.

6.12 J9 CAN interface (before and after line driver), 16 I/O user defined pins

Pin	Signal	Pin	Signal	Pin	Signal
1	P16	10	VCC	19	P20
2	P17	11	CRX1	20	P21
3	P14	12	GND	21	P22
4	P15	13	CANH	22	P23
5	P12	14	CANL	23	P24
6	P13	15	GND	24	P25
7	P10	16	GND	25	P26
8	P11	17	CRX0	26	P27
9	VCC	18	CTX0		

CAN controller is connected directly to this connector and through CAN transceiver. Part of CAN controller is also 16 IO pins that are directly connected.

6.13 J10 FPGA extension pins

Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	5	XX4 (P92)	9	XX6 (P94)
2	XX1 (P86-FPGA)	6	XX5 (P89)	10	XX9 (P95)
3	XX2 (P88)	7	GND	11	XX10 (P97)
4	XX3 (P87)	8	XX7 (P93)	12	XX8 (P95)

All pins can be freely configurable by FPGA firmware.

FPGA Firmware version (April, 17 2000) supports only ~1.19 Hz output signal on XX4 and signals XX1 and XX6 as test pins (see Flash PROM Register - W_FLASH). For example we can use one test pin for detection of execution times for different parts of software.

6.14 J11 FPGA JTAG interface

Pin	Signal	Pin	Signal	Pin	Signal
1	TMS	4	VCC	7	RST
2	TDO	5	TDI	8	GND
3	TCK	6	-		

This interface is provided for FPGA firmware development and is not needed in regular operation of the DSP2 board. FPGA is initialised by DSP.

6.15 J12 FPGA external programming interface

Pin	Signal	Pin	Signal	Pin	Signal
1	VCC	4	Dout	7	CCLK
2	VCC	5	GND	8	Din
3	PGM	6	GND		

See J11 explanation.

6.16 J13 two DSP timer outputs

Pin	Signal	Pin	Signal
1	TCLK0	2	TCLK1

The ’C3x has two 32-bit general-purpose timer modules. Each timer has an I/O pin that you can be used as an input clock to the timer, as an output clock signal, or as a general-purpose I/O pin. See DSP data sheet.

6.17 Power supply

For board operation folowing power supply voltages must be connected:

Table 4: DSP2 Power supply connections

Name	Connector	Pin
V--	J1	1
AVSS	J1	2
AGND	J1	3
AGND	J1	13
AVCC	J1	14
GND	P1	1
V++	P1	2
AGND	P1	3

Name	Connector	Pin
AGND	P1	5
Vpf	P5	1
GND	P5	5
GND	P5	6
GND	P5	9
VCC	P5	11
VCC	P5	13

Table 5: Power supply signals explanation

Name	Voltage	Current	Explanations
Vpf	>+18V	3mA	Power fail detect
VCC	+5V	1,5A	Logic power supply
GND	0V	-	Logic ground
V++	+15V	25mA	Pos. supply voltage for op-amp
AVCC	+5V	150mA	Pos. analog supply voltage
AGND	0V	-	Analog ground
AVSS	-5V	25mA	Neg. Analog supply voltage
V--	-15V	25mA	Neg. supply voltage for op-amp

Warning! Analog (AGND) and digital ground (GND) MUST be connected together!

7. Fast analog inputs modifications

Table 6: Normal (current) fast analogue input configuration

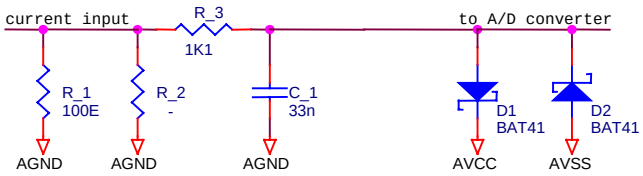
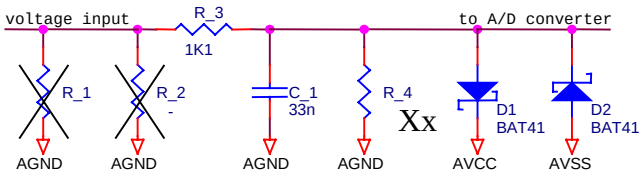
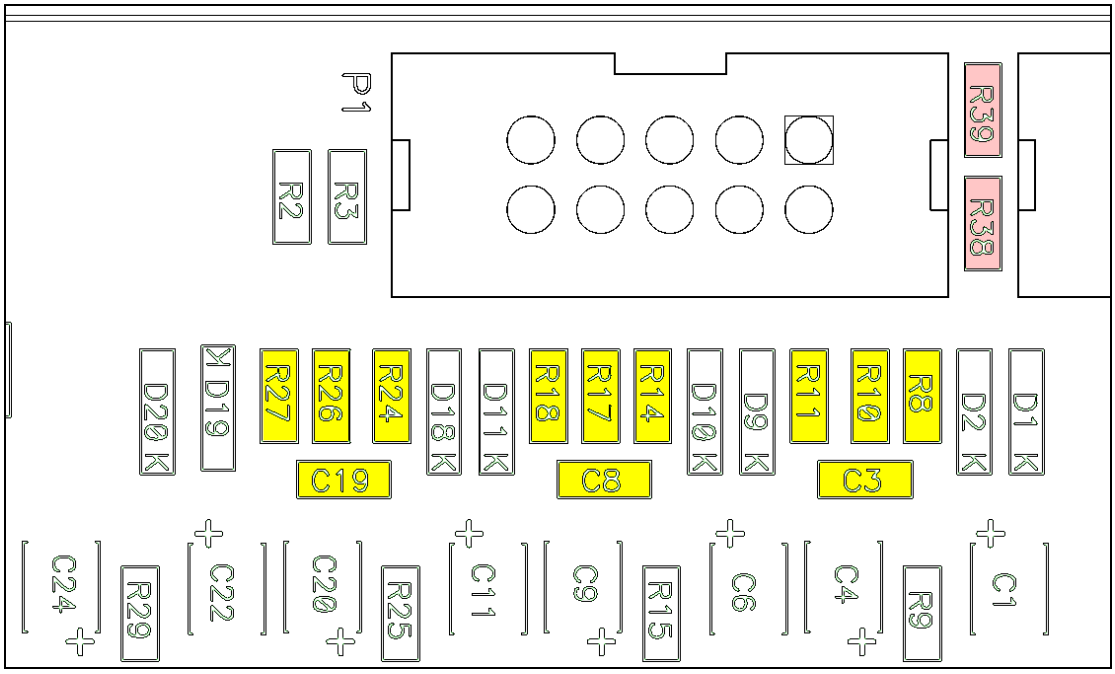
	I1 (T=36us)	I3 (T=36us)	UDC (T=110us)
 Picture shows fast analogue input schematic.			
R_1	R10 100E	R17 100E	R26 100E
R_2	R11 -	R18 -	R27 -
R_3	R8 1K1	R14 1K1	R24 1K1
R_4	-	-	-
C_1	C3 33nF	C8 33nF	C19 100nF
D2 connected to	AVSS	AVSS	AGND
AD converter input range	-4.096 to 4.094V	-4.096 to 4.094V	0 to 4.095V
Current input range	-40.96 to +40.94mA	-40.96 to +40.94mA	0 to +40.95mA

Table 7: Modified fast analogue input configuration for use with MiniSKiiP IGBT module

	I1 (T=36us)	I3 (T=36us)	UDC (T=110us)
 Picture shows fast analogue input schematic.			
R_1	R10 -	R17 -	R26 -
R_2	R11 -	R18 -	R27 -
R_3	R8 1K1	R14 1K1	R24 1K1
R_4	- xx	- xx	- xx
C_1	C3 33nF	C8 33nF	C19 100nF
D2 connected to	AVSS	AVSS	AGND
AD converter input range	-4.096 to 4.094V	-4.096 to 4.094V	0 to 4.095V
Input voltage	-10 to +10V	-10 to +10V	0 to +10V



The DSP2 board was designed with terminal resistors (R_1 and R_2) on channels i1, i3, udc for current input signals.

Since MiniSKiiP IGBT bridge provides voltage signals for i1, i3 and udc, terminal resistors are not inserted. Resistors R_3 and R_4 are building a voltage divider for 10V input signal. R_4 doesn't have its own mounting place on PCB and must be placed on the back of C_1.