Application Report
SPMA051–April 2013

System Design Guidelines for Tiva™ C Series Microcontrollers

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ABSTRACT

Tiva™ C Series TM4C microcontrollers are highly-integrated system-on-chip (SOC) devices with extensive interface and processing capabilities. Consequently, there are many factors to consider when creating a schematic and designing a circuit board. By following the recommendations in this design guide, you will increase your confidence that the board will work the first time it is powered it up.

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1 Introduction

The General Design Information section of this guide contains design information that applies to most designs (Section 3). Topics include important factors in the schematic design and layout of power supplies, oscillators, and debug accessibility. The Feature-Specific Design Information section describes specific peripherals and their unique considerations, allowing you to select the information that is relevant to your design (Section 4).

To further assist you with the design process, Texas Instruments provides a wide range of additional design resources, including application reports and reference designs. These designs and documents are an important reference. See the System Design Examples (Section 5) for links to these resources.

2 Using This Guide

The information in this design guide is intended to be general enough to cover a wide range of designs by describing solutions for typical situations. However, because every system is different, it is inevitable that there will be conflicting requirements and potential trade-offs. This is especially true in designs that include high-performance analog circuits, radio frequencies, high voltages, or high currents. If your design includes these features, then special considerations (beyond the scope of this application report) may be necessary.

Where possible, the distinction is made between *preferred practice* and *acceptable practice*. This distinction addresses the reality that constraints such as size, cost, and layout restrictions might not always allow for best-practice design.

When considering which practices to apply to a design, one of the most important factors is the I/O switching rate and current. If there is only low-speed, low-current switching on the Tiva C Series peripheral pins, then acceptable-practice rules are likely sufficient. If high-speed switching is present, particularly with simultaneous transitions, then best-practice rules are recommended.

NOTE: Some of the information in this guide comes directly from the individual Tiva C Series microcontroller data sheets. The microcontroller data sheets are the defining documents for device usage and may contain specific requirements that are not covered in this design guide. You should always use the most current version of the data sheet and also check the most recent errata documents for the part number you have selected. Visit www.ti.com/tiva-c to sign up for e-mail alerts specific to a Tiva C Series part number.

This document defines system design guidelines for Tiva C Series microcontrollers with part numbers starting with TM4C123.

3 General Design Information

This section contains design information that applies to most Tiva C Series microcontrollers including:

- Power
- Reset
- Oscillators
- JTAG Interface
- System
- All External Signals

3.1 Power

This section describes design considerations related to the microcontroller power supply.

3.1.1 Microcontroller Power Supply

Description	Classification	Applies to...	For more information, see...
Tiva C Series microcontroller power supply requirements	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

Tiva C Series microcontrollers require only a single +3.3-V power supply. Other supply rails are generated internally by on-chip, low drop-out (LDO) regulators. The most visible internal supply rail is the core voltage (V_{DDC}) because it has dedicated power pins for filter and decoupling capacitors.

During normal microcontroller operation, the power-supply rail must remain within the electrical limits listed in the microcontroller data sheet [V_{DD} (min) and V_{DD} (max)]. For optimal performance of the on-chip analog modules, the supply rail should be well regulated and have minimal ripple. Electrical noise sources such as motor drivers, relays, and other power-switching circuits should each have a separate supply rail, especially if analog-to-digital converter (ADC) performance is a factor.

The microcontroller has both analog and digital power-on reset (POR) circuits that release once the V_{DD} and V_{DDA} power-supply rails reach the POR threshold. The brown-out reset (BOR) circuit is a more precise supply rail monitor and is normally used to hold the microcontroller in reset if the supply rail drops out of operating range. The default BOR action is to generate a system reset.

External supervisors may also be used to assert the external reset signal RSTn under power-on, brown-out, or watchdog expiration conditions.

3.1.2 LDO Filter Capacitor

Description	Classification	Applies to...	For more information, see...
Information on selecting the right capacitor for the on-chip LDO voltage regulator	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

All Tiva C Series microcontrollers have an on-chip voltage regulator to provide power to the core. The voltage regulator requires a filter capacitor to operate properly (see the C_{LDO} parameter in the corresponding microcontroller data sheet for acceptable capacitor values).

The recommended V_{DDC} capacitor solution consists of two or more 10%-tolerance ceramic chip capacitors totalling 3.3 µF to 3.4 µF (that is, one each of 3.3-µF and 0.1-µF capacitors). Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

3.1.3 Decoupling Capacitors

Description	Classification	Applies to...	For more information, see...
Information on selecting the right power-rail decoupling capacitors	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

Ideally, Tiva C Series microcontrollers should have one decoupling capacitor in close proximity to each power-supply pin. Decoupling capacitors are typically 0.01 µF or 0.1 µF in value and should be accompanied by a bulk capacitor near the microcontroller. The combined V_{DD} and V_{DDA} bulk capacitance of the microcontroller is typically between 2 µF and 22 µF, with values on the upper end of that range providing measurable ripple reduction in some applications, especially if the circuit board does not have solid power and ground planes. Bulk capacitance is particularly important if the microcontroller is connected to high-speed interfaces or needs to source significant GPIO current (that is, greater than 4 mA) on more than a few pins.

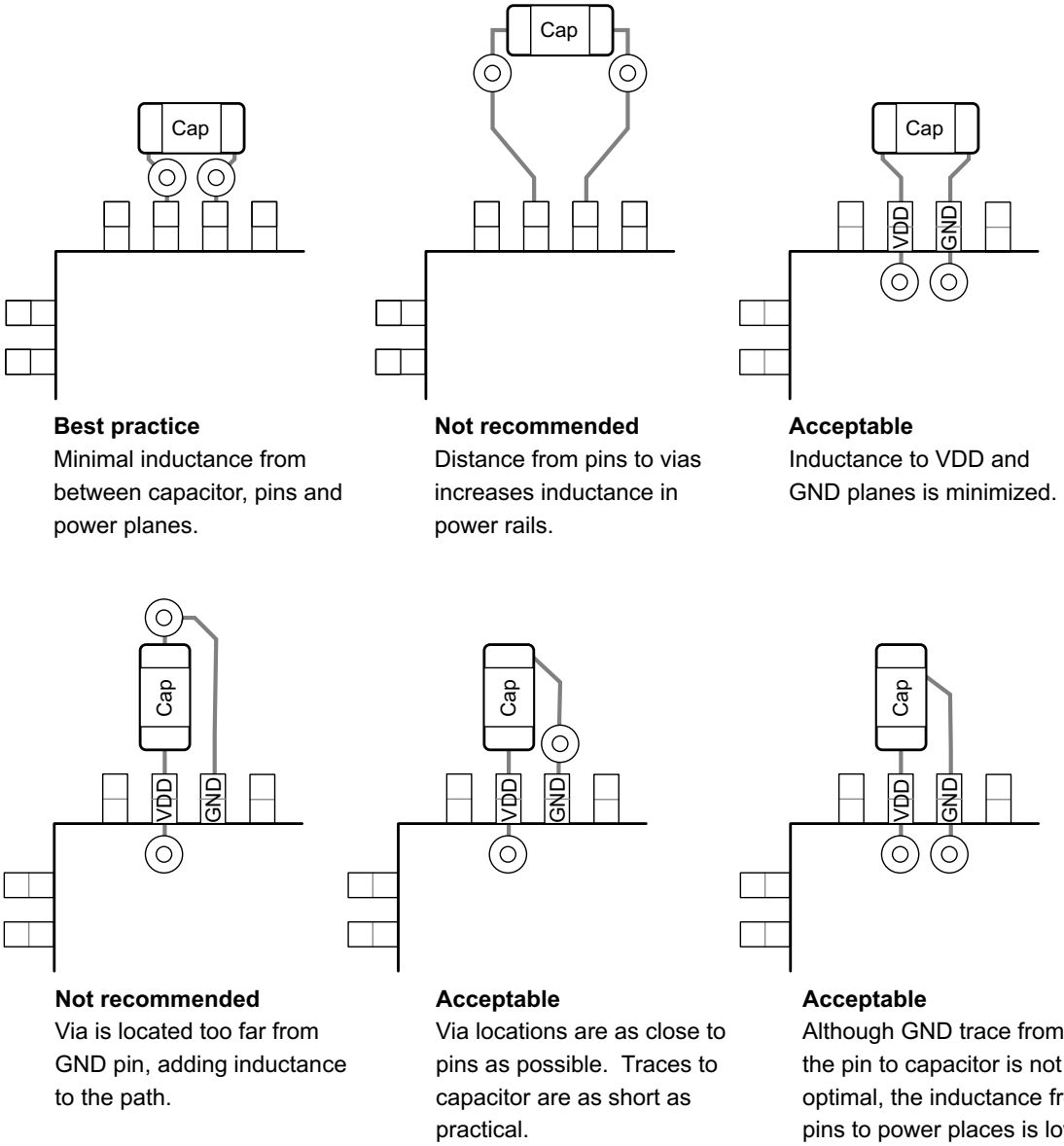
For optimal performance, locate one decoupling capacitor adjacent to each Power and Ground pin pair. At a minimum, there should be one decoupling capacitor on each side of the microcontroller package. V_{DDC} pins should always have an adjacent decoupling capacitor.

Decoupling capacitors should be 10 V to 25 V, X5R/X7R ceramic chip types. Z5U dielectric capacitors are not recommended due to wide tolerance over temperature.

The capacitance of most ceramic capacitors decreases with increasing voltage. Avoid using capacitors at close to their rated voltage unless reduced capacitance is acceptable. X7R capacitors may lose 15%-20% of their capacitance at rated voltage while Y5V capacitors may drop 75%-80%. [(Cain, Jeffrey, Comparison of Multilayer Ceramic and Tantalum Capacitors, AVX Technical Bulletin.)]

Description	Classification	Applies to...	For more information, see...
Optimal layout practices when placing and routing power vias and decoupling capacitors	Layout recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

Figure 1 show different options for routing PCB traces between the Tiva C Series microcontroller power pins and a decoupling capacitor.



Best practice
Minimal inductance from between capacitor, pins and power planes.

Not recommended
Distance from pins to vias increases inductance in power rails.

Acceptable
Inductance to VDD and GND planes is minimized.

Not recommended
Via is located too far from GND pin, adding inductance to the path.

Acceptable
Via locations are as close to pins as possible. Traces to capacitor are as short as practical.

Acceptable
Although GND trace from the pin to capacitor is not optimal, the inductance from pins to power places is low.

Figure 1. PCB Routing Options

3.1.4 Splitting Power Rails and Grounds

Description	Classification	Applies to...	For more information, see...
Factors to consider when deciding how to connect V_{DD}, V_{DDA}, GND, and GNDA pins	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

Tiva C Series microcontrollers are designed to operate with V_{DD} and V_{DDA} pins connected directly to the same +3.3-V power source. Some applications may justify separation of V_{DDA} from V_{DD} to allow insertion of a filter to improve analog performance. Before deciding to split these power rails, the power architecture of the device should be reviewed to determine which on-chip modules are powered by each supply. The device data sheet contains a drawing that shows power distribution.

The use of split V_{DD} and V_{DDA} rails on Tiva C Series microcontrollers offers additional advantages compared to LM3S devices. First, V_{DDA} can be selected as a reference source for the ADC. Additionally, the 12-bit ADC achieves optimal performance when powered with a separate V_{DDA} power rail.

Filter options include filter capacitors in conjunction with either a low-value resistor or inductor/ferrite bead to form a low-pass filter.

If the V_{DD} and V_{DDA} pins are split, the designer must ensure that power is applied and removed at the same time throughout the entire circuit.

The GND and GNDA pins should always be connected together—preferably to a solid ground plane or copper pour.

3.2 Reset

This section describes design considerations related to reset.

3.2.1 External Reset Pin Circuits

Description	Classification	Applies to...	For more information, see...
Guidelines for determining the optimal connection to the $\overline{RST}$ pin	Schematic and PCB layout recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

A special external reset circuit is not normally required. Tiva C Series microcontrollers have an on-chip Power-On-Reset (POR) circuit with a delay to handle power-up conditions.

$\overline{RST}$ can be connected to +3.3 V. For flexibility and noise-immunity, a resistor (1 kΩ) to +3.3 V and a capacitor (0.1 µF) to GND are recommended. The latter also allows the signal to be driven from the JTAG debug connector.

Because the $\overline{RST}$ signal routes to the core as well as most on-chip peripherals, it is important to protect the $\overline{RST}$ signal from noise. This protection is particularly important in applications which involve power switching where fast transitions can couple into the reset line. The reset PCB trace should be less than 2 in (5.08 cm) and routed away from noisy signals. Do not run the reset trace close to the edge of the board or parallel to other traces with fast transients.

The capacitor should be located as close to the pin as possible.

If the $\overline{RST}$ signal source is another board, it is recommended to add a buffer IC on the Tiva C Series board to filter the signal.

A simple push-switch can be used to provide a manual reset. To avoid ringing on the $\overline{RST}$ signal caused by switch bounce and stray inductance, add a low-value resistor (100 Ω) in series with the switch.

Reset circuit options are shown in the respective microcontroller data sheets.

3.3 Oscillators

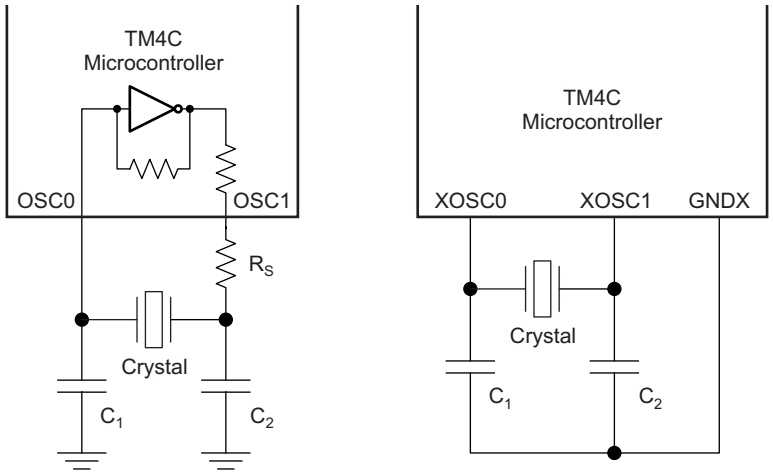
This section describes design considerations related to the microcontroller oscillators.

3.3.1 Crystal Oscillator Circuit Components

Description	Classification	Applies to...	For more information, see...
Select criteria for the oscillator circuit components	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

All Tiva C Series microcontrollers have a main oscillator circuit to provide a clock source for the device. Some parts also have similar clock circuits for the Ethernet PHY or the Hibernation module.

The on-chip, parallel-resonant oscillator circuit requires an external crystal (see Figure 2) and two load capacitors to complete the circuit.



(a) Main Oscillator Circuit TM4C Devices

(b) Hibernate Module Oscillator Circuit TM4C Devices

Figure 2. Comparing Oscillator Circuits in Tiva C Series Devices

Capacitors C_1 and C_2 must be sized correctly for reliable and accurate oscillator operation. Crystal manufacturers specify a load capacitance (C_L) which should be used in the following formula to calculate the optimal values of C_1 and C_2.

$$C_L = (C_1 * C_2) / (C_1 + C_2) + C_S$$

C_S is the stray capacitance in the oscillator circuit. Stray capacitance is a function of trace lengths, PCB construction, and microcontroller pin design. For a typical design, C_S should be approximately 2 pF to 4 pF. Because C_1 and C_2 are normally of equal value, the calculation for a typical circuit simplifies slightly to:

$$C_1 \text{ and } C_2 = (C_L - 3 \text{ pF}) * 2$$

Capacitors with an NP0/C0G dielectric are recommended and are almost ubiquitous for small-value ceramic capacitors.

For TM4C devices, it is particularly important to correctly match the crystal to the oscillator. The capacitors must be the correct value and a series resistor (R_S) may be required to avoid exceeding the maximum driver power of the crystal. The Tiva C Series device data sheets show a selection of suitable crystals as well as optimal capacitor and resistor values.

3.3.2 Crystal Oscillator Circuit Layout

Description	Classification	Applies to...	For more information, see...
PCB layout guidelines for the Tiva C Series oscillator circuits	PCB layout recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

The key layout objectives should be to minimize both the loop area of the oscillator signals and the overall trace length. A poor oscillator layout can result in unreliable or inaccurate oscillator operation and can also be a noise source. Ideal trace length is less than 0.25 in or 6 mm. Do not exceed 0.5 in or 12 mm.

Figure 3 shows a preferred layout for a small surface-mount crystal. The GND side of each capacitor routes directly to a via that provides a low-impedance connection to the GND plane.

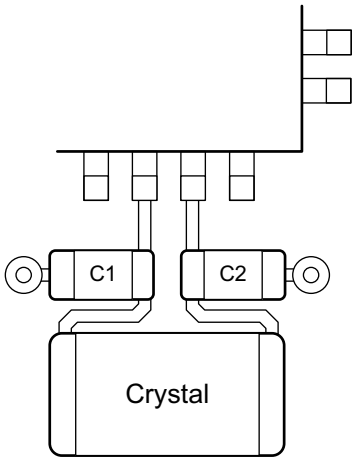


Figure 3. Recommended Layout for Small Surface-Mount Crystal

Some oscillator circuits require a series resistor (to adjust drive); this component should be a small chip resistor located between the crystal and the Tiva C Series device.

3.4 JTAG Interface

This section describes design considerations related to the microcontroller JTAG interface.

3.4.1 Debug and Programming Connector

Description	Classification	Applies to...	For more information, see...
Helpful information on connector and signal options for JTAG/SWD connections	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

When designing a board that uses a Tiva C Series microcontroller, it is preferable to provide connections to all JTAG/SWD signals. In pin-constrained applications, SWD can be used instead of JTAG. SWD only requires two signals (SWCLK and SWDIO), instead of the four signals that JTAG requires, freeing up two additional signals for use as GPIOs. Check that your preferred tool-chain supports SWD before choosing this option. The LM Flash Programmer utility can program devices using SWD.

The most common ARM® debug connector is a 2x10-way, 0.1-in pitch header. Although it is robust, the 0.1-in header is too large for many boards. An alternate connector definition, which is now quite popular, uses a 0.05-in, half-pitch 2x5 connector. The applicable assignments for both connectors are shown in Table 1.

Table 1. Applicable Debug Connector Pin Assignments

JTAG/SWD Signal	ARM 20-pin	ARM 10-pin half-pitch
TCK/SWCLK	9	4
TMS/SWDIO	7	2
TDI	5	8
TDO	13	6
$\overline{\text{RESET}}$	15	10
GND	4, 6, 8, 10, 12, 14, 16, 18, 20	3, 5, 9
TVCC	1	1

Tiva C Series microcontrollers have default internal pull-up resistors on TCK, TMS, TDI, and TDO signals. External pull-up resistors are not required.

3.5 System

This section describes design considerations related to the system including unused pins.

3.5.1 Unused Pins

Description	Classification	Applies to...	For more information, see...
Recommendations for any Tiva C Series microcontroller pins that are not connected	Schematic recommendations	All Tiva C Series microcontrollers	Microcontroller data sheet

The preferred connection for an unused microcontroller pin depends on the pin function. Each Tiva C Series microcontroller data sheet has a table in the **Signals Table** chapter that lists the fixed function pins as well as both the acceptable practice and the preferred practice for reduced power consumption and improved electromagnetic compatibility (EMC) characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the RCGCx register.

3.6 All External Signals

This section describes design considerations related to the microcontroller external signals.

3.6.1 PCB Design Rules: 90° PCB Traces

Description	Classification	Applies to...	For more information, see...
General rules for routing PCB traces on high-speed nets	PCB layout recommendations	All Tiva C Series microcontrollers	• Microcontroller data sheet • Reference design PCB files

For many years, it has been common PCB design practice to avoid 90° corners in PCB traces. In fact, most PCB layout tools have a built-in miter capability to automatically replace 90° angles with two 45° angles.

The reality is that the signal-integrity benefits of avoiding 90° angles are insignificant at the frequencies and edge-rates seen in microcontroller circuits (even up to and past 1 GHz/100 ps). [Johnson, H and Graham, M, High-Speed Digital Design: a Handbook of Black Magic, Prentice Hall: New Jersey, 1993.]

Additionally, one report could find no measurable difference in radiated electromagnetic interference (EMI). [Montrose, Mark I, Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis, undated.]

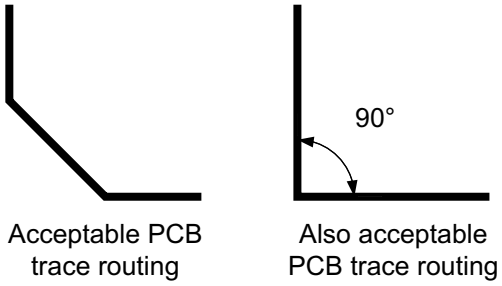


Figure 4. Acceptable PCB Trace Routing

NOTE: Loops in PCB traces are not acceptable, despite the references that indicate that the signal-integrity benefits of avoiding 90° angles is negligible. Loops in traces form antennas and add inductance. The data show that if your layout does have antenna loops, then mitering the angles to 135° is not going to help. Avoid loops in PCB traces.

Despite these conclusions, there are a few simple reasons to continue to avoid 90° angles:

- There is a higher possibility of an acid-trap forming during etching on the inside of the angle (especially in acute angles). An acid trap causes over-etching which can be a yield issue in PCBs with small trace widths.
- Routing at 45° typically reduces overall trace length. This practice frees board area, reduces current loops, and improves both EMC emissions and immunity.
- It looks better. This consideration is an important factor for anyone who appreciates the art of PCB layout.

4 Feature-Specific Design Information

This section contains feature-specific design information and is grouped by function or peripheral:

- USB
- General Guidelines for All High-Speed Interfaces
- ADC

4.1 USB

Description	Classification	Applies to...	For more information, see...
PCB layout guidelines for the Tiva C Series USB signals	PCB layout recommendations	All Tiva C Series microcontrollers with a USB module	• Microcontroller data sheet • Evaluation board schematics • See Section 4.2

Good PCB layout and routing practices are important in ensuring reliable USB signalling. Routing the D+ and D– differential pair is the most important consideration. V_{BUS} and I_D (typically used only in USB OTG and dual-mode applications) signal routing is not critical as these are low-speed signals.

4.1.1 Signal Impedance

The USB D+ and D- signal pair should be routed as a 100-Ω differential pair.

The optimal way to achieve 90-Ω differential impedance is a two-step process. During PCB layout, the designer should use PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance.

NOTE: The PCB fab notes should include annotation that specifies which traces are to be *impedance controlled*.

The second step is performed by the PCB fab house, which adjusts the trace space and width to match their specific materials and process.

Another key benefit of specifying controlled impedance is that the PCB manufacturer assumes on-going responsibility for maintaining the impedance of those traces. This can be a factor when lot-to-lot differences introduce variation.

While specifying controlled-impedance is preferred, it may be acceptable to skip that step if the trace length is less than approximately 2 in (5.08 cm). If good design rules are followed during layout, it should be possible to achieve routing that provides good signal integrity.

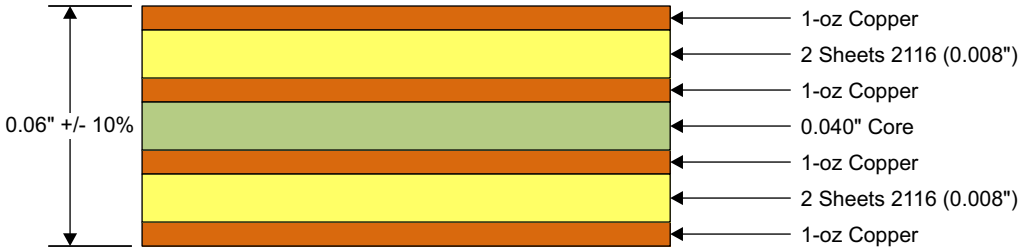
A slight variation of this method, that also avoids the additional cost of controlled-impedance PCBs, is sometimes called *controlled dielectric*. This approach involves the PCB designer using a dielectric specification that is either supplied or agreed to by the board fab house. The material and dielectric constant should be added to the PCB fab notes.

4.1.2 Achieving 90-Ω Impedance

Some PCB design tools have an integrated trace impedance calculator that factors in trace geometry, trace length, board stack-up, and the board material dielectric constant. There are also several free programs that can perform similar calculations. When using these tools, ensure that the differential impedance (impedance between the signals in the pair) is 90 Ω. If a ground plane is present, the single-ended impedance (Z_O) should be 50 Ω.

The typical dielectric constant (E_R) for FR-4 material is approximately 4.6.

A typical configuration for an FR-4, 0.062-in (1.574-mm) circuit board with four layers of 1-oz copper and 1/2-oz plating is shown in Figure 5.



Typical 4 Layer PCB Stack

Figure 5. Typical Four-Layer PCB Stack

For this example, we place a solid ground plane on layer 2. The 1-oz copper plane is 1.4 mils (0.0014 in, or 0.0355 mm) thick. The height of traces above the ground plane is defined by the thickness of the PCB prepreg material—in this case 0.008 in (0.2032 mm) thick. Therefore, total thickness is:

Total thickness = 0.062 in = 4 x 0.0014 in + 0.040 in + 2 x 0.008 in

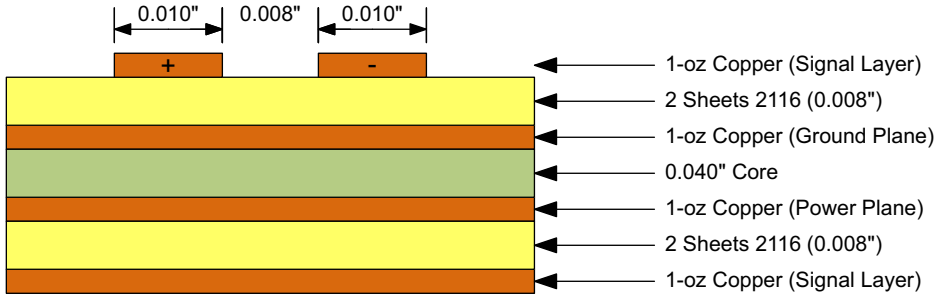
Using the free PCB ToolKit calculator from Saturn PCB Design, Inc., results in the following values for the board stack shown in Figure 6.

Conductor width (W) = 0.010 in (0.254 mm)

Conductor spacing (S) = 0.008 in (0.2032 mm)

$Z_{Differential}$ = 90 Ω

Z_O = 55 Ω



90Ω Microstrip Differential Pair on
a 4-layer 0.06" FR-4 PCB stack

Figure 6. 90-Ω Microstrip Differential Pair on a Four-Layer, 0.06-in FR-4 PCB Stack

The PCB fabricator improves the value and tolerance of these results if the traces are specified as controlled-impedance.

For a two-layer board, the height of the substrate is now the full thickness of the FR-4 PCB material. The height of the substrate means that much wider traces are needed to achieve 90-Ω impedance. The following analysis was performed with HyperLynx because the dimensional aspect ratio is not supported by the free Saturn PCB Design tool.

Conductor width (W) = 0.028 in (0.7112 mm)

Conductor spacing (S) = 0.007 in (0.1778 mm)

$Z_{Differential}$ = 90 Ω

Z_O = 91.5 Ω

4.1.3 Other Design Rules and Considerations

Follow these additional design rules and recommendations for best results:

- Apply the rules for high-speed signal routing listed elsewhere in this application report.
- Maintain symmetry when routing differential pairs. Some PCB layout tools can assist with this kind of routing. Avoid vias if possible. If it is necessary to switch layers, then both signals in the pair should pass through a via at the same distance on the trace.
- Avoid stubs when adding components to D+ and D– signals. Devices such as ESD suppressors should be located directly on the signal trace.
- Route differential signal pairs on the same layer.

4.2 General Guidelines for All High-Speed Interfaces

This section describes design considerations related to the microcontroller Ethernet, USB, EPI, and other high-speed interfaces.

4.2.1 PCB Design Rules: Other Routing Guidelines

Description	Classification	Applies to...	For more information, see...
General rules for routing PCB traces on high-speed nets	PCB layout recommendations	All Tiva C Series microcontrollers with Ethernet, USB, EPI, or other high-speed interface	• Microcontroller data sheet • Reference design PCB files

Avoid discontinuities in ground planes and power planes under high-speed signals as shown in Figure 7. For controlled-impedance interfaces such as Ethernet and USB, discontinuities create impedance changes that impact signal integrity. For all signals, a break in the ground plane removes a direct path for any return current to flow through. This consideration is important even for balanced differential pairs because perfect matching is seldom achievable and ground current is inevitable.

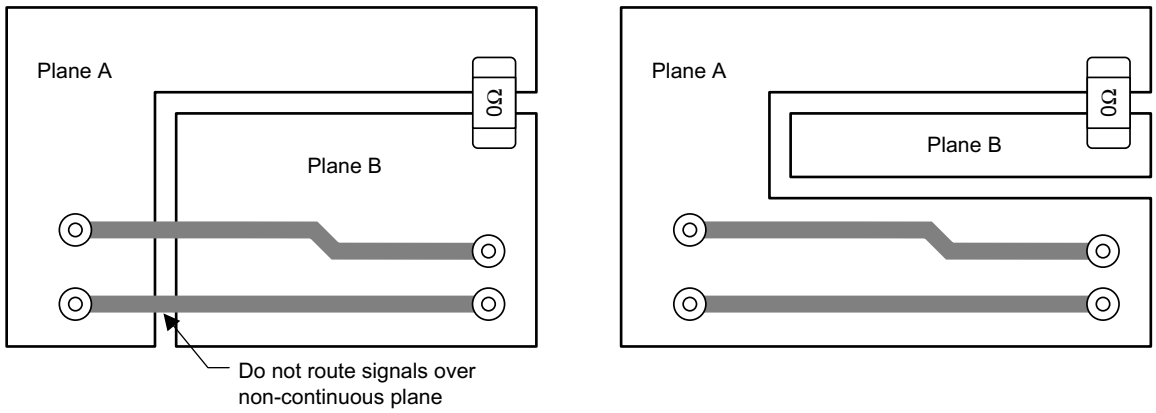


Figure 7. Examples of PCB Trace Layout

Avoid stubs in differential signal pairs where possible (see Figure 8). Where termination or bias resistors are needed, one terminal should be located directly on the trace. Both resistors should be located at the same distance from the source and load.

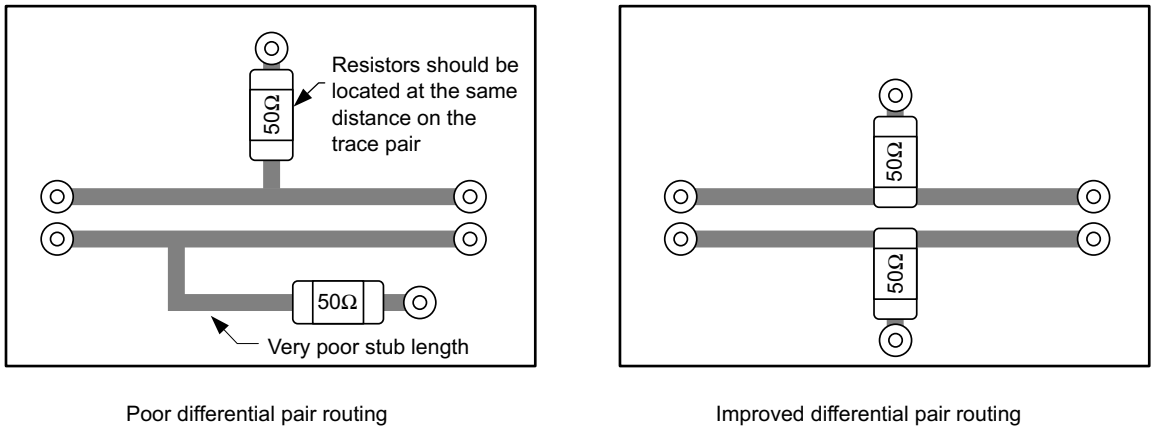


Figure 8. Examples of Differential Pair Layout

Tiva C Series microcontrollers provide programmable drive strength for all digital output pins. To improve the performance of digital signals, set the GPIO drive strength register appropriately. Selecting a lower drive strength can avoid signal integrity issues due to ringing and reflections. If the drive strength is too low, however, timing and rise and fall time requirements may not be satisfied.

4.3 ADC

This section describes design considerations related to the microcontroller ADC module.

4.3.1 ADC Input Schematics

Description	Classification	Applies to...	For more information, see...
How to achieve optimal ADC performance through careful circuit design	Schematic recommendations	All Tiva C Series microcontrollers with ADC	• Microcontroller data sheet • Reference design schematics

In order to achieve the best possible conversion results from an ADC, it is important to start with a good schematic design.

All ADCs require a voltage reference (or occasionally a current reference), whether the voltage reference is provided from an on-chip source or via an external pin. Any deviation in the reference voltage from its ideal level results in additional gain error (or slope error) in the conversion result.

Tiva C Series TM4C microcontrollers offer greater ADC precision and require an external reference voltage. The TM4C circuit should provide a precision voltage source to either the V_{REF+} or V_{DDA} pin. The designer should determine whether the internal reference has sufficient accuracy or if an external reference is needed. If an external reference is used, it should be used with capacitors on both the supply pin and the output pin. See the voltage reference in the corresponding microcontroller data sheet for recommendations on value. Typically, 1 µF or more is recommended.

Optimal ADC accuracy is achieved with a low-impedance source and a large input filter capacitor. As the signal source impedance increases and capacitance decreases, noise on the conversion result increases. Noise sources include coupling from other signals, power supplies, external devices, and from the microcontroller itself. Refer to the respective microcontroller data sheet for source impedance recommendations for TM4C devices.

If resistor dividers are used to scale an input voltage, then best results can be achieved with low-value resistors. The resistor from the ADC input to ground should ideally be less than 1 kΩ. Avoid values higher than 10 kΩ unless a large filter capacitor is present.

Ceramic filter capacitors of 1 µF or more can substantially improve noise performance. The trade-off is a reduction in signal bandwidth (as a function of the source impedance) and phase shifting.

Input protection should also be considered, especially when converting signals from external devices or where transient voltages might be present. The ADC pins on some Tiva C Series devices (in ADC mode) are not 5-V tolerant, but do allow some margin over the +3.0-V span. See the respective microcontroller data sheet for specific information.

Increased source impedance can provide a degree of protection to the ADC. Semiconductor clamping circuits can also be used—typically, zener diodes or clamping diodes to 3 V and GND. When specifying diodes, consider leakage current over temperature (I_R) because this parameter affects overall conversion accuracy.

5 System Design Examples

For example designs using Tiva C Series microcontrollers, see Table 2 for the detailed list of Tiva C Series Reference Design Kits (RDKs), Evaluation Kits (EKs), and Development Kits (DKs).

Schematics are available for all designs. Full PCB design files including Gerber files are available for Tiva C Series reference designs only.

Table 2. Tiva C Series Example Designs

Part Number	Description	Tiva C Series Device	Device Package	Key Features	PCB Layer Count
EK-LM4F232	Evaluation Board	LM4F232H5QD	LQFP144	USB, hibernate, real-time clock	6
EK-TM4C123GXL	LaunchPad Evaluation Board	TM4C123GH6PM	LQFP64	Simple two-layer layout	2

6 Conclusion

Applying good system-design practices from the earliest design stages ensures a successful board bring-up. The design process should include thorough design-reviews using the information in this application report, other embedded system design resources, and reports created by the design team. These efforts will be rewarded with a reliable and properly performing Tiva C Series microcontroller-based design.

The use of the TivaWare™ for C SeriesPeripheral Driver Library also minimizes software changes to the start-up routines that configure the I/O, enabling application code to be moved to the new devices with minimal functional changes.

7 References

The following related documents and software are available on the Tiva C Series web site at www.ti.com/tiva-c:

- Tiva C Series TM4C Microcontroller Data Sheet (individual device documents available through product selection tool).
- TivaWare for C Series Driver Library. Available for download at www.ti.com/tool/sw-tm4c-drl.
- TivaWare for C Series Driver Library User's Manual (literature number SPMU298).

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