TB-FMCL-GLAN-B
Hardware User Manual

Rev.1.02

Revision History

Version	Date	Description	Publisher
Rev.1.00	2012/11/21	Release version	Zhan.z
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Introduction

Thank you for purchasing the **TB-FMCL-GLAN-B** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a board intended for 1000M Ethernet function. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:
All documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Accessories

4 x Short Pin (Hirose HIF3GA-2.54SP)

2. Overview

The board has two Ports of Gigabit Ethernet PHY. The two sets of PHY + RJ45 are compatible with IEEE 802.3 and can work independently. And the board is designed for connection with the platform board with a FPGA Mezzanine Card (FMC) Low-Pin Count connector.

3. Feature

Ethernet PHY	: Marvell's 88E1111-B2-BAB1C000
FMC Connector	: Samtec's ASP-134604-01
RJ45 Connector	: Pulse's JK0-0177NL

4. Block Diagram

This board uses two Ethernet PHY to realize 1000M Ethernet data transmitting and receiving. Two Ethernet PHY can work in GMII mode and RGMII mode.
The FMC-LPC connector is mounted on the solder side of the board.

Figure 4-1 shows the TB-FMCL-GLAN-B board's block diagram.

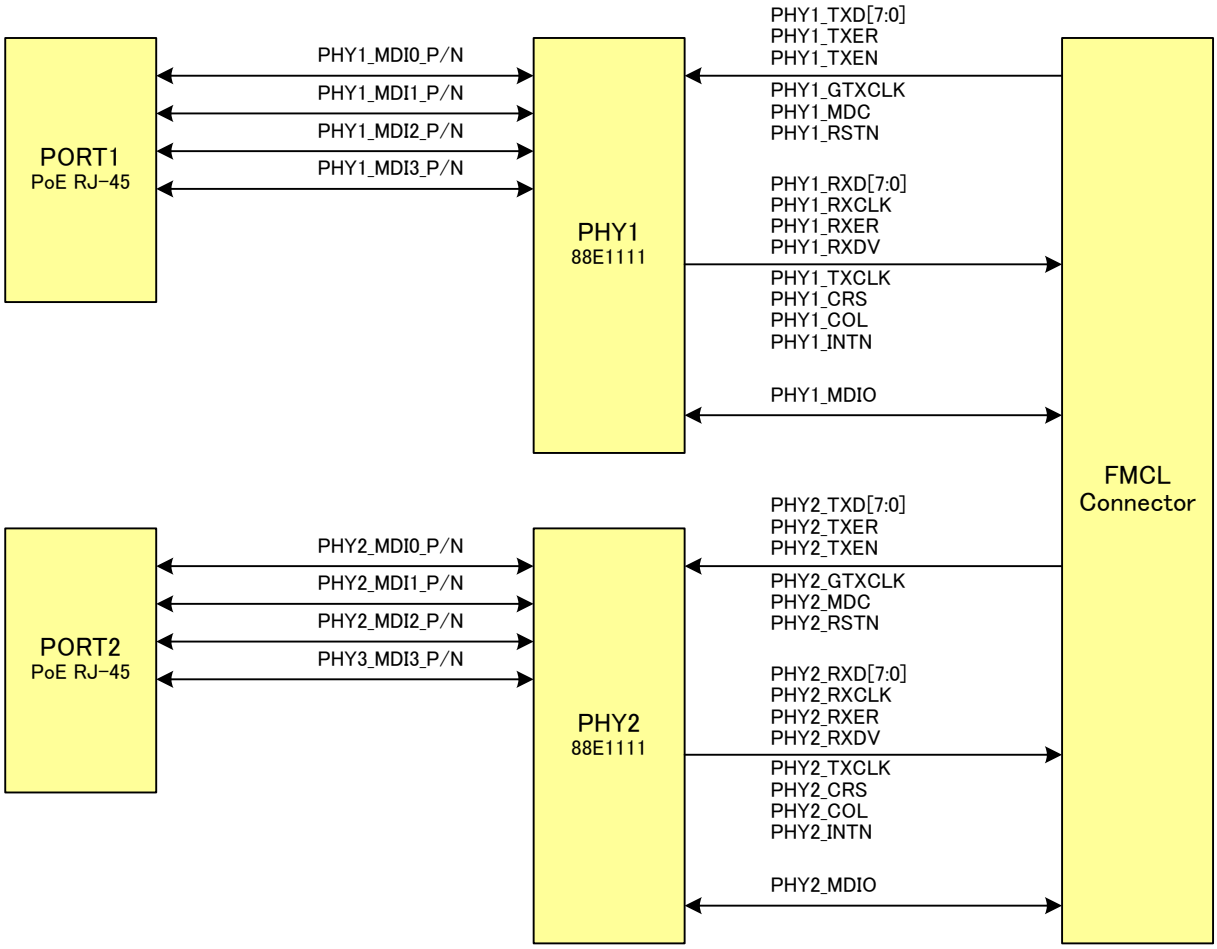


Figure 4-1 Block Diagram

5. External View of the Board

Figure 5-1 and 5-2 shows the external view of the TB-FMCL-GLAN-B board.

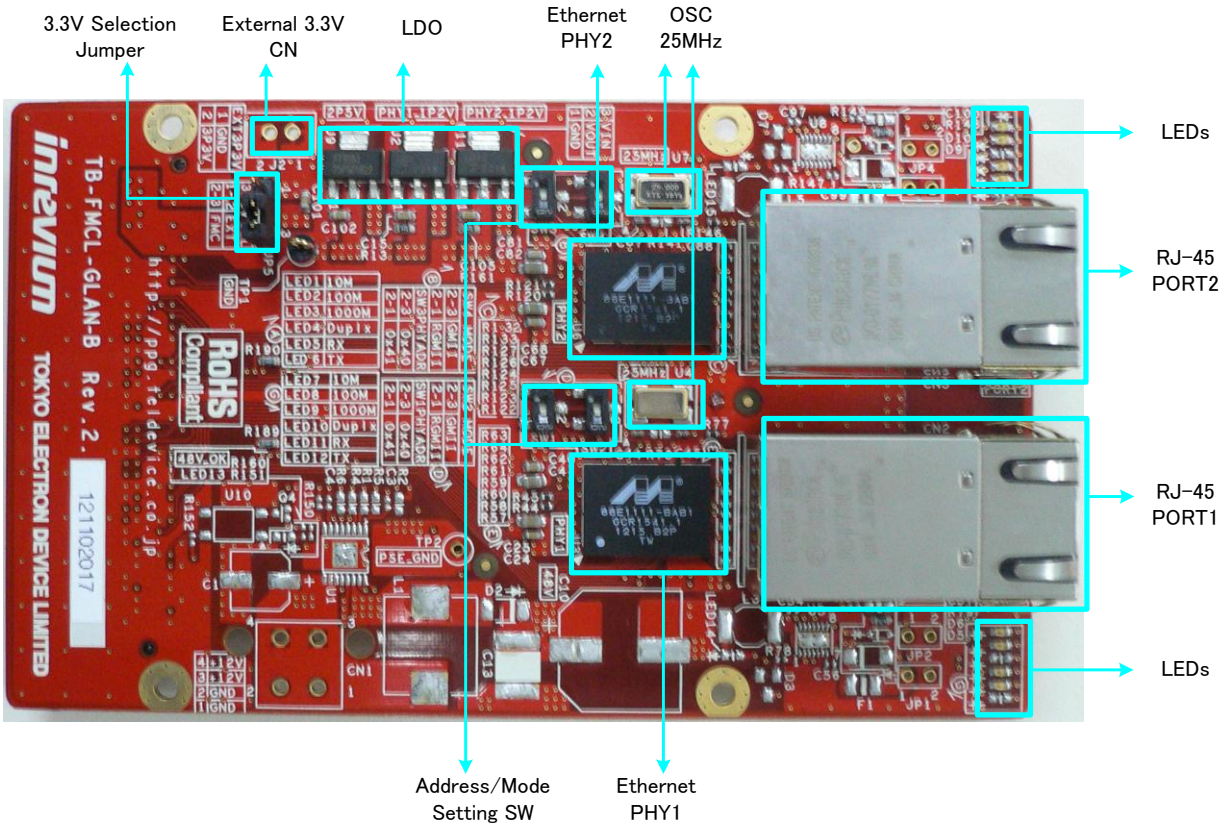


Figure 5-1 Component Side

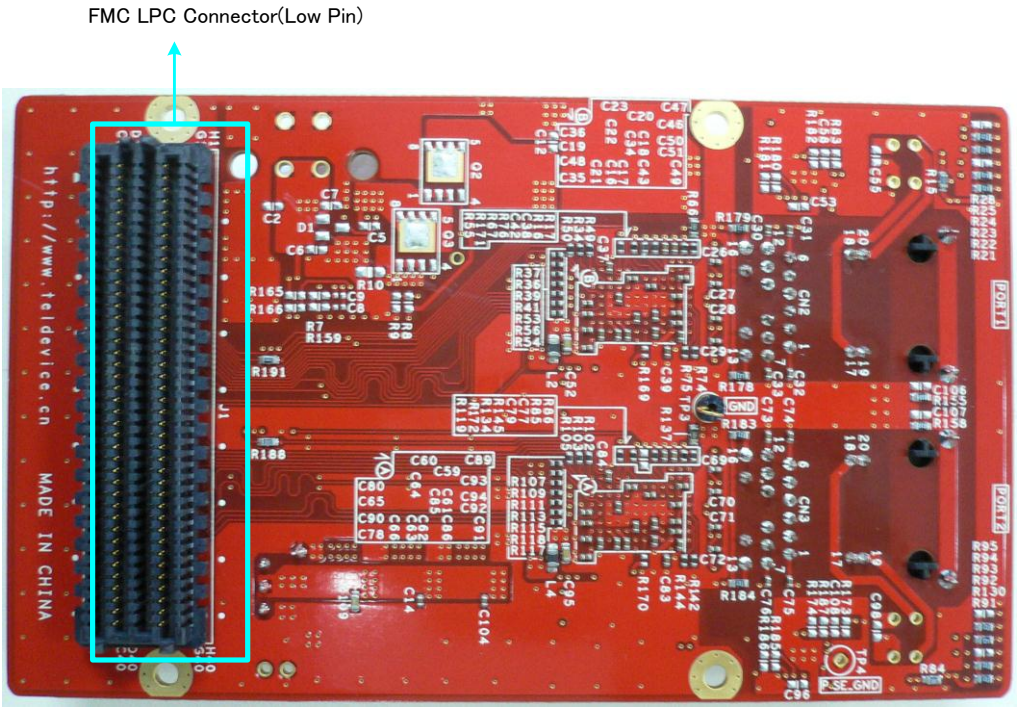


Figure 5-2 Solder Side

6. Board Specifications

Figure 6-1 shows the board specifications.

External Dimensions:	115 mm (W) x 69 mm (H)
Number of Layers:	8 layers
Board Thickness:	1.6 mm
Material:	FR-4
FMC Connector:	Samtec's ASP-134604-01
RJ-45 connector:	Pulse's JK0-0177NL

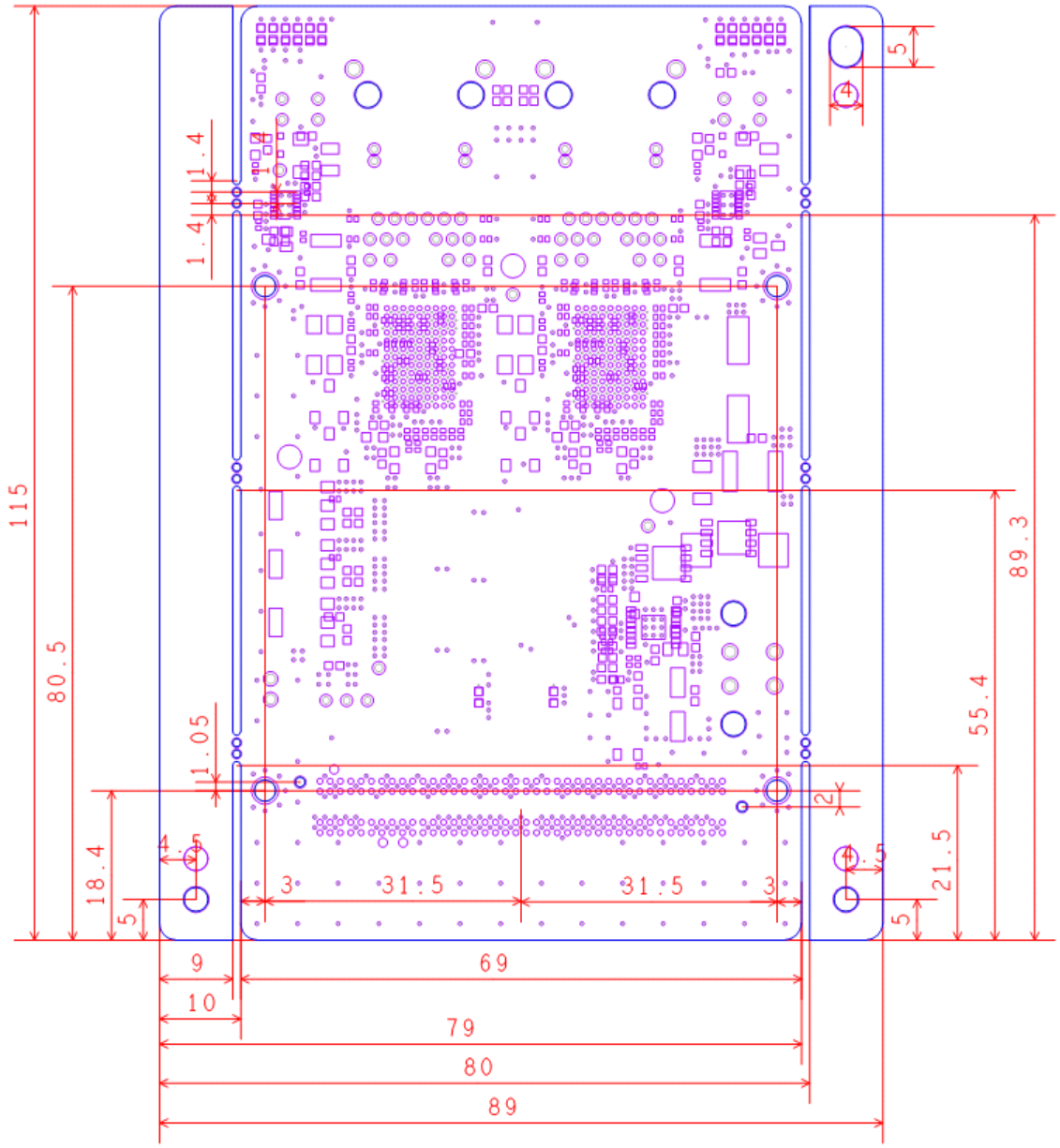


Figure 6-1 Board Dimensions (inclusive of wastable substrate)

7. Description of Components

7.1. Power Supply Structure

Figure 7-1 shows the TB-FMCL-GLAN-B board's power supply structure.

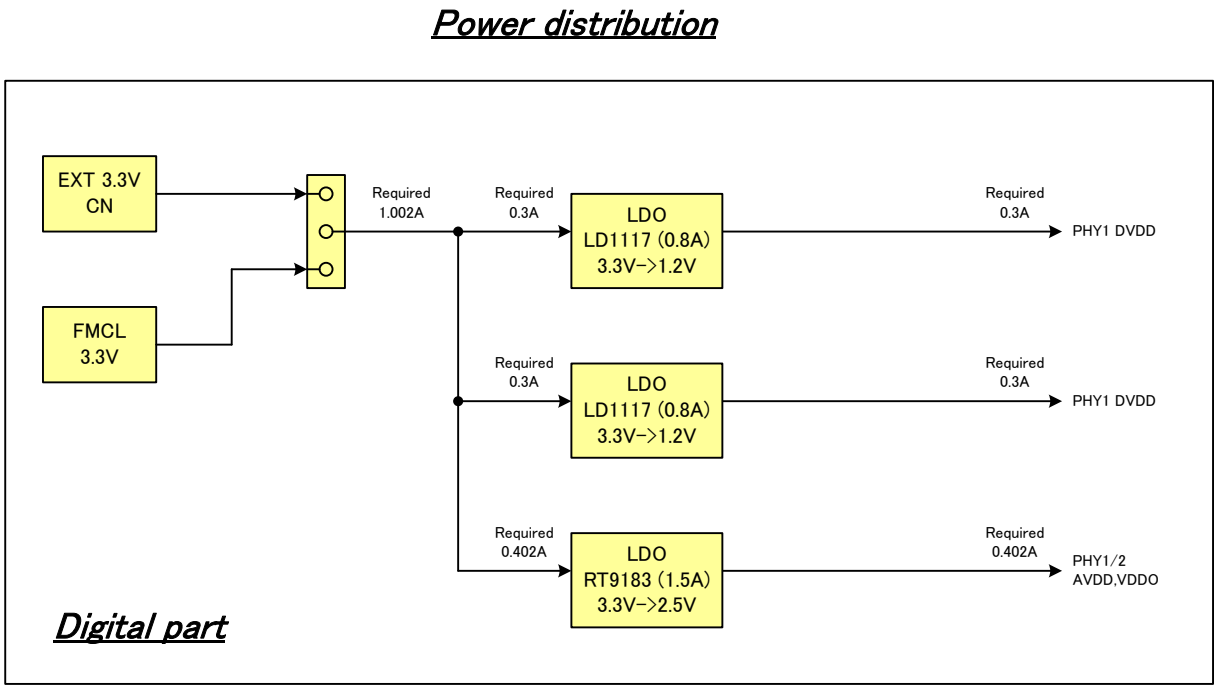


Figure 7-1 Power Supply Structure

7.2. EXT3.3V Connector

There is a 2 pin connector (J2) for external 3.3V power supply. J2 is not mounted. It is an addition for power input when carrier board dose not provide +3.3V via FMC connector.

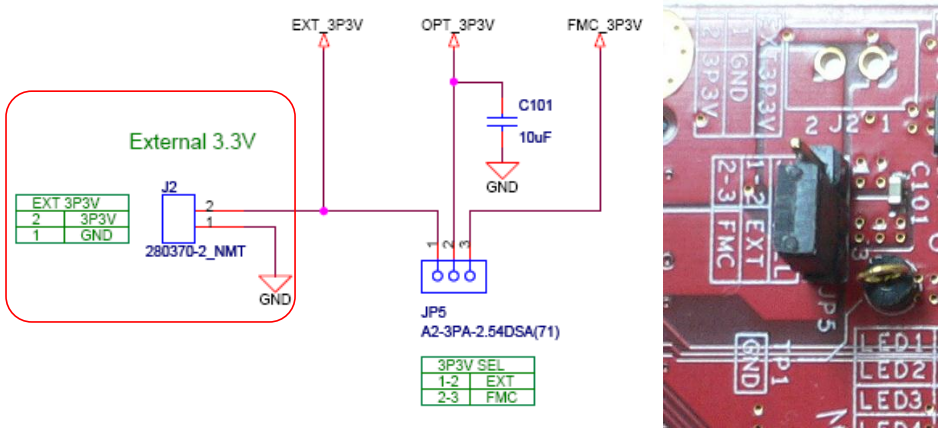


Figure 7-2 EXT3.3V Connector

7.3. 3P3V SEL Jumper

There is a 3 pin Jumper for 3.3V power selection.

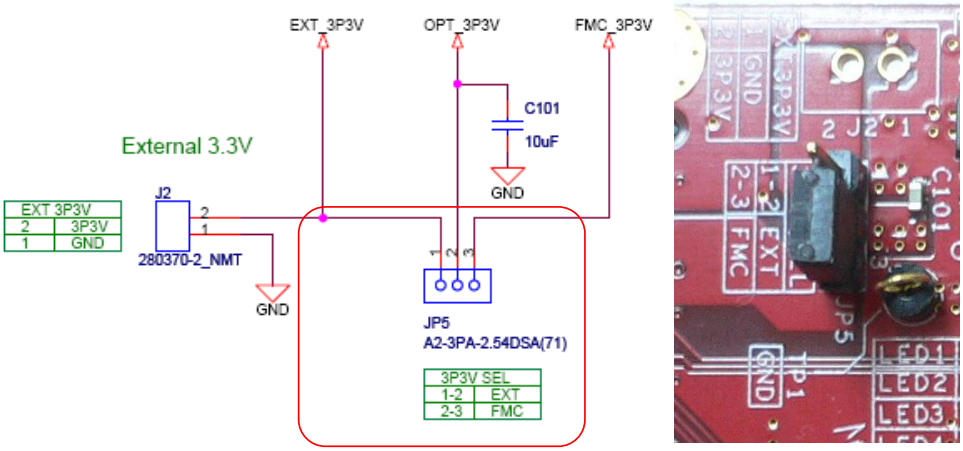


Figure 7-3 3P3V SEL Jumper

7.4. FMC Connector Interface

The board provides Samtec's FMC Low-Pin Count (J1) connector.

Figure 7-2 shows the VITA-57 Low -Pin Count pin list respectively.

Notice: Not all pins of LPC are connected to the Ethernet PHY.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-4 Power Supply Structure

The following table shows the detailed of FMC Low-Pin Count (J1) connector.

Table 7-1 FMC I/F Connector pin assignment table (J1)

Connection	C		D	Connection
GND	GND	1	PG_C2M	-
-	DP0_C2M_P	2	GND	GND
-	DP0_C2M_N	3	GND	GND
GND	GND	4	GBTCLK0_M2C_P	PHY1_CK125_OUT
GND	GND	5	GBTCLK0_M2C_N	-
-	DP0_M2C_P	6	GND	GND
-	DP0_M2C_N	7	GND	GND
GND	GND	8	LA01_P_CC	PHY1_RXCLK_CC
GND	GND	9	LA01_N_CC	-
PHY1_TXD5	LA06_P	10	GND	GND
PHY1_MDIO	LA06_N	11	LA05_P	PHY1_INTN
GND	GND	12	LA05_N	PHY1_MDC
GND	GND	13	GND	GND
PHY1_GTXCLK	LA10_P	14	LA09_P	PHY1_RSTN
PHY1_TXER	LA10_N	15	LA09_N	PHY1_TXD0
GND	GND	16	GND	GND
GND	GND	17	LA13_P	PHY1_TXEN
PHY1_CRS	LA14_P	18	LA13_N	-
PHY1_COL	LA14_N	19	GND	GND
GND	GND	20	LA17_P_CC	PHY2_TXCLK
GND	GND	21	LA17_N_CC	
PHY2_RXCLK_CC	LA18_P_CC	22	GND	GND
PHY2_INTN	LA18_N_CC	23	LA23_P	PHY2_TXD5
GND	GND	24	LA23_N	PHY2_MDIO
GND	GND	25	GND	GND
PHY2_MDC	LA27_P	26	LA26_P	PHY2_RSTN
PHY2_TXER	LA27_N	27	LA26_N	PHY2_TXEN
GND	GND	28	GND	GND
GND	GND	29	TCK	-
-	SCL	30	TDI	-
-	SDA	31	TDO	-
GND	GND	32	※1 3P3VAUX	-
GND	GND	33	TMS	-
-	GA0	34	TRST_L	-
-	12P0V	35	GA1	-
GND	GND	36	3P3V	FMC_3P3V
-	12P0V	37	GND	GND
GND	GND	38	3P3V	FMC_3P3V
FMC_3P3V	3P3V	39	GND	GND
GND	GND	40	3P3V	FMC_3P3V

Connection	G		H	Connection
GND	GND	1	VREF_A_M2C	-
PHY2_RXCLK_GC	CLK1_M2C_P	2	PRSNT_M2C_L	-
-	CLK1_M2C_N	3	GND	GND
GND	GND	4	CLK0_M2C_P	PHY1_RXCLK_GC
GND	GND	5	CLK0_M2C_N	-
PHY1_TXCLK	LA00_P_CC	6	GND	GND
V48V_PGN_25	LA00_N_CC	7	LA02_P	PHY1_RXD0
GND	GND	8	LA02_N	PHY1_RXD1
PHY1_TXD7	LA03_P	9	GND	GND
PHY1_TXD6	LA03_N	10	LA04_P	PHY1_RXD2
GND	GND	11	LA04_N	PHY1_RXD3
PHY1_TXD3	LA08_P	12	GND	GND
PHY1_TXD4	LA08_N	13	LA07_P	PHY1_RXD4
GND	GND	14	LA07_N	PHY1_RXD5
PHY1_TXD1	LA12_P	15	GND	GND
PHY1_TXD2	LA12_N	16	LA11_P	PHY1_RXD6
GND	GND	17	LA11_N	PHY1_RXD7
-	LA16_P	18	GND	GND
-	LA16_N	19	LA15_P	PHY1_RXDV
GND	GND	20	LA15_N	PHY1_RXER
PHY2_TXD7	LA20_P	21	GND	GND
PHY2_TXD6	LA20_N	22	LA19_P	PHY2_RXD0
GND	GND	23	LA19_N	PHY2_RXD1
PHY2_TXD4	LA22_P	24	GND	GND
PHY2_TXD3	LA22_N	25	LA21_P	PHY2_RXD2
GND	GND	26	LA21_N	PHY2_RXD3
PHY2_TXD1	LA25_P	27	GND	GND
PHY2_TXD2	LA25_N	28	LA24_P	PHY2_RXD4
GND	GND	29	LA24_N	PHY2_RXD5
PHY2_TXD0	LA29_P	30	GND	GND
PHY2_CRS	LA29_N	31	LA28_P	PHY2_RXD6
GND	GND	32	LA28_N	PHY2_RXD7
PHY2_COL	LA31_P	33	GND	GND
-	LA31_N	34	LA30_P	PHY2_RXDV
GND	GND	35	LA30_N	PHY2_RXER
PHY2_GTXCLK	LA33_P	36	GND	GND
-	LA33_N	37	LA32_P	-
GND	GND	38	LA32_N	-
-	VADJ	39	GND	GND
GND	GND	40	VADJ	-

7.5. PHY_RXCLK Selection

This board is aimed to TB-6S-LX150T-IMG2 Board for implementation of Ethernet communication

When the FPGA on carrier board is Virtex-6, resistor R189, R188 should be mounted. And resistor R191, R190 should be not mounted.

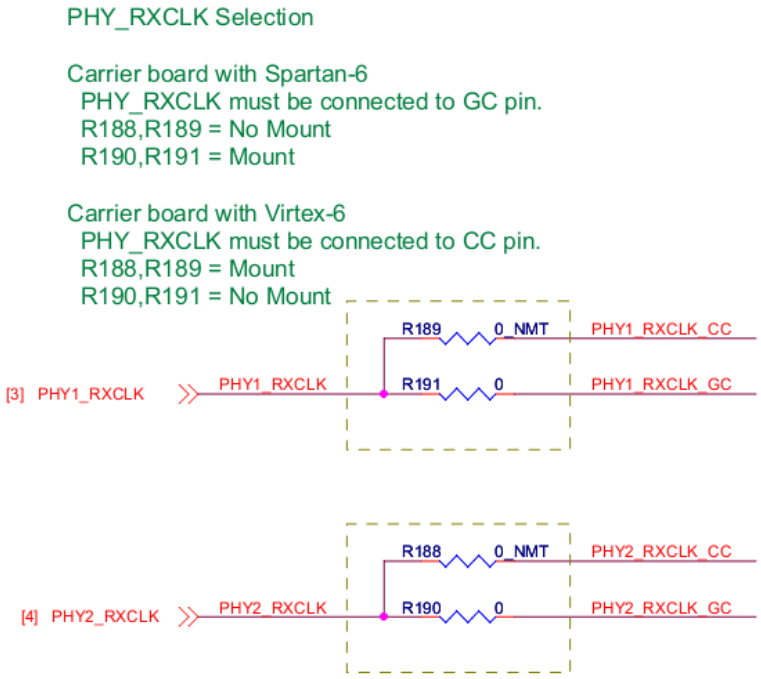


Figure 7-5 PHY_RXCLK Selection

7.6. LED

There are 15 LEDs on the board. These LEDs are used to indicate the statuses of Ethernet PHY.
The function description of LED is in the following table.

Table 7-2 LED Function Table

No.	LED No.	Color	Function	Target IC			Note
				IC No.	Pin No.	Pin Name	
1	LED1	Green	LED for 10BASE-T link or speed.	U6	C8	LED_LINK10	
2	LED2	Green	LED for 100BASE-TX link or speed.	U6	B8	LED_LINK100	
3	LED3	Green	LED for 1000BASE-TX link/speed or link indicator.	U6	A9	LED_LINK1000	Note1
4	LED4	Green	LED for duplex or duplex/collision modes.	U6	E8	LED_DUPLEX	
5	LED5	Green	LED for Receive Activity or Receive Activity/Link modes.	U6	C9	LED_RX	
6	LED6	Green	LED for Transmit Activity or RX/TX Activity/Link modes.	U6	D9	LED_TX	Note1
7	LED7	Green	LED for 10BASE-T link or speed.	U3	C8	LED_LINK10	
8	LED8	Green	LED for 100BASE-TX link or speed.	U3	B8	LED_LINK100	
9	LED9	Green	LED for 1000BASE-TX link/speed or link indicator.	U3	A9	LED_LINK1000	Note1
10	LED10	Green	LED for duplex or duplex/collision modes.	U3	E8	LED_DUPLEX	
11	LED11	Green	LED for Receive Activity or Receive Activity/Link modes.	U3	C9	LED_RX	
12	LED12	Green	LED for Transmit Activity or RX/TX Activity/Link modes.	U3	D9	LED_TX	Note1

Note1:LED3, LED6, LED9, LED12 are not mounted.

RJ-45 connector (Pulse's JK0-0177NL) has internal LEDs.
To indicate the statuses of Ethernet PHY, LEDs are connected to PHY's signal LED_LINK1000 and LED_TX respectively.

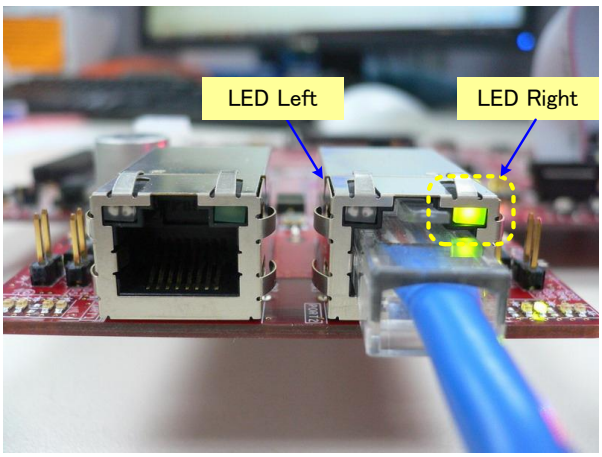


Figure 7-6 RJ-45 internal LED

The function description of RJ-45 internal LED is in the following table.

Table 7-3 RJ-45 internal LED Function Table

No.	LED No.	Color	Function	Target IC		
				IC No.	Pin No.	Pin Name
1	LED Left	Yellow/Green	LED for Transmit Activity or RX/TX Activity/Link modes.	U3/U6	D9	LED_TX
2	LED Right	Green	LED for 1000BASE-TX link/speed or link indicator.	U3/U6	A9	LED_LINK1000

7.7. Jumper

The function description of Jumper is in the following table.

Table 7-4 Jumper Function Table

No.	Jumper No.	Description	Status	Function
1	JP5	3.3V power supply selection	1-2 Short	Use external 3.3V power supply
			2-3 Short	Use FMC connector's 3.3V power supply

7.8. Switch

There are 4 switches on the board. These switches are used for PHY address selection and GMII/RGMII mode selection.

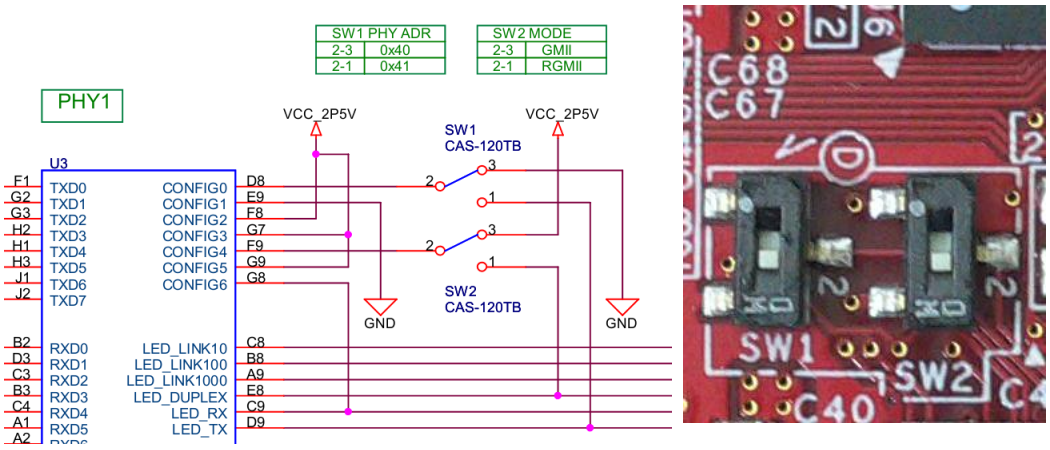


Figure 7-7 Switch

The following table shows the detailed of Switch.

Table 7-5 Switch Function Table

No.	Jumper No.	Description	Status	Function
1	SW1	PHY address selection of Port1	2-3 connect	Port1 PHY address is set to 0x40
			2-1 connect	Port1 PHY address is set to 0x41
2	SW2	MODE selection of Port1	2-3 connect	Port1 MODE is set to GMII
			2-1 connect	Port1 MODE is set to RGMII
3	SW3	PHY address selection of Port2	2-3 connect	Port2 PHY address is set to 0x40
			2-1 connect	Port2 PHY address is set to 0x41
4	SW4	MODE selection of Port2	2-3 connect	Port2 MODE is set to GMII
			2-1 connect	Port2 MODE is set to RGMII

8. Default Switch Settings

The following two tables shows default TB-FMCL-GLAN-B switch settings

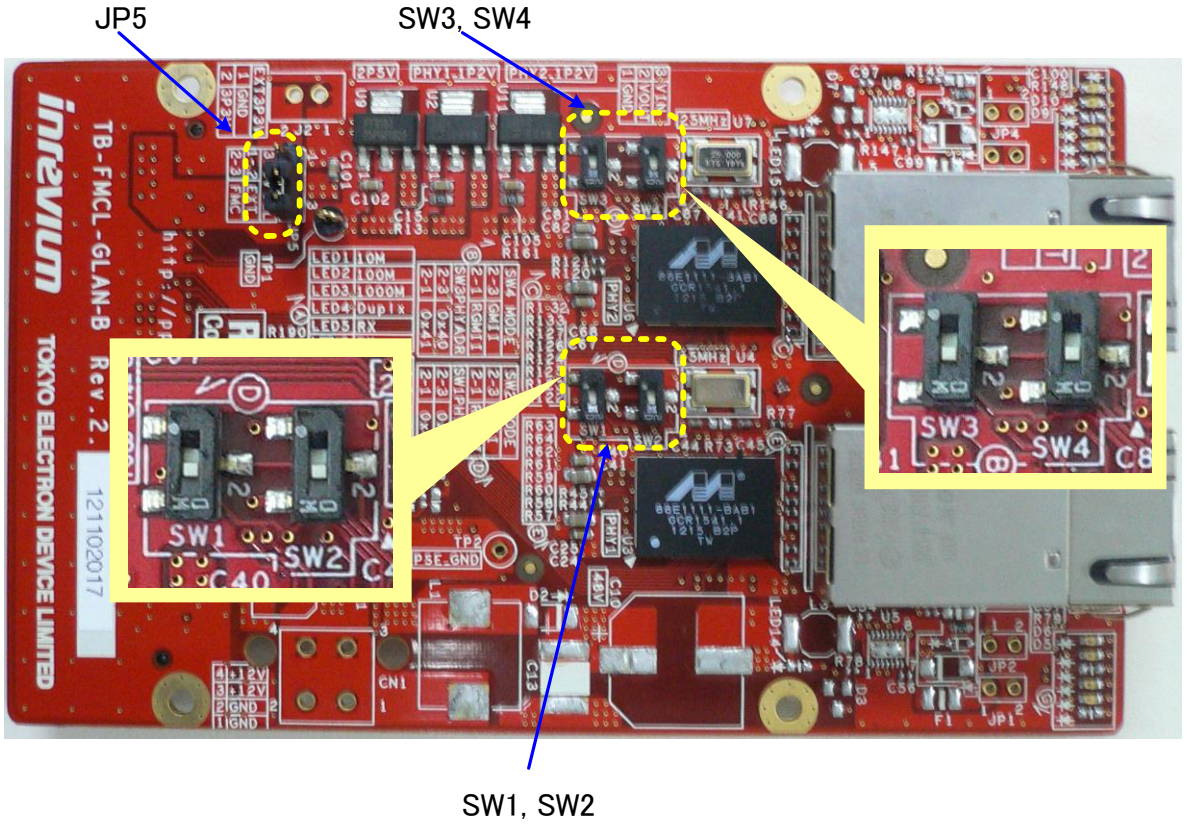


Figure 8-1 Default Jumper Settings (Component Side)

Table 8-1 Default Jumper Settings

No.	Jumper No.	Initial Setting	Function	Note
1	JP5	2-3 Short	Use 3.3V power supply form FMC Connector	

Table 8-2 Default Switch Settings

No.	Jumper No.	Initial Setting	Function	Note
1	SW1	2-3 connect	Port1 PHY address is set to 0x40	
2	SW2	2-3 connect	Port1 MODE is set to GMII	
3	SW3	2-3 connect	Port2 PHY address is set to 0x40	
4	SW4	2-3 connect	Port2 MODE is set to GMII	

9. Appendix

This section describes how to use TB-FMCL-GLAN-B Board with TB-6S-LX150T-IMG2 Board.

9.1. Evaluation environment

Tools: EDK 13.2

OS: Windows 7/64bit

Figure 7-1 shows the evaluation structure.

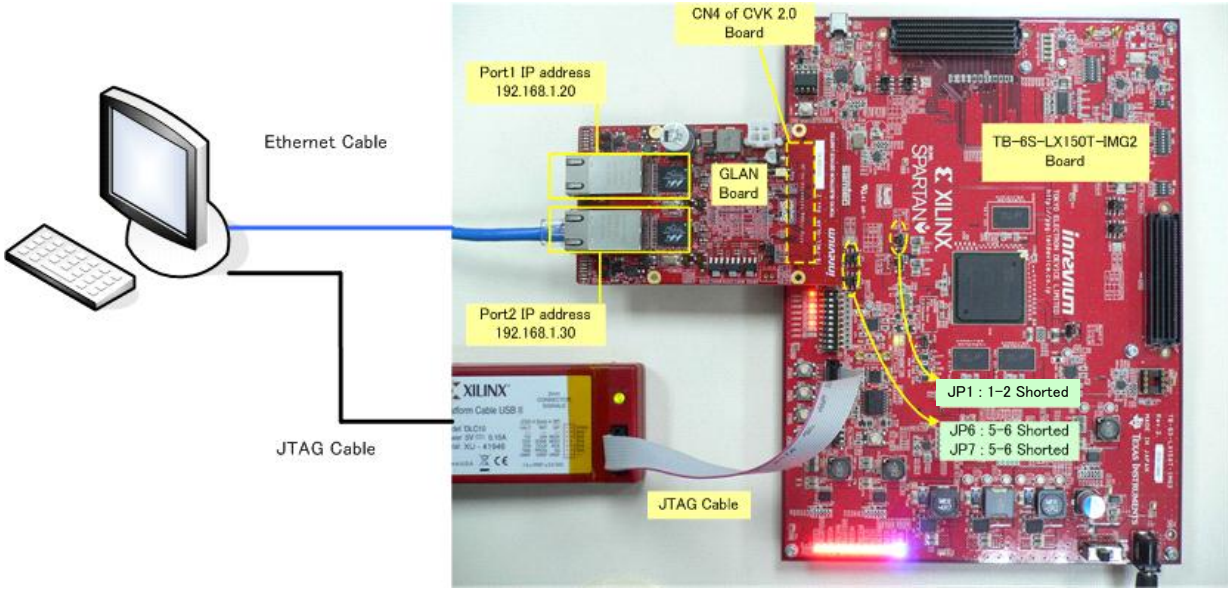
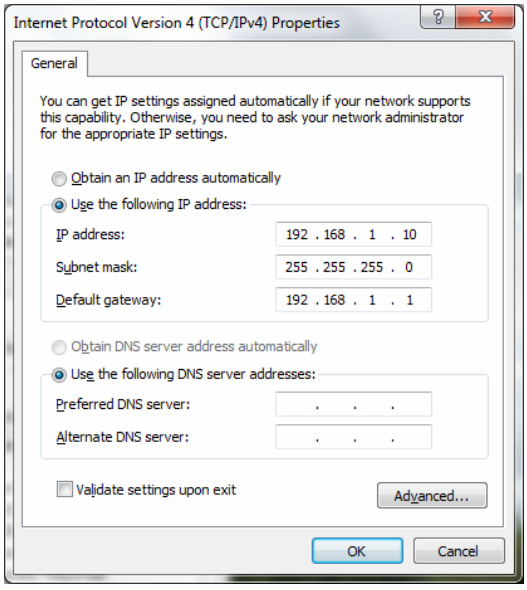


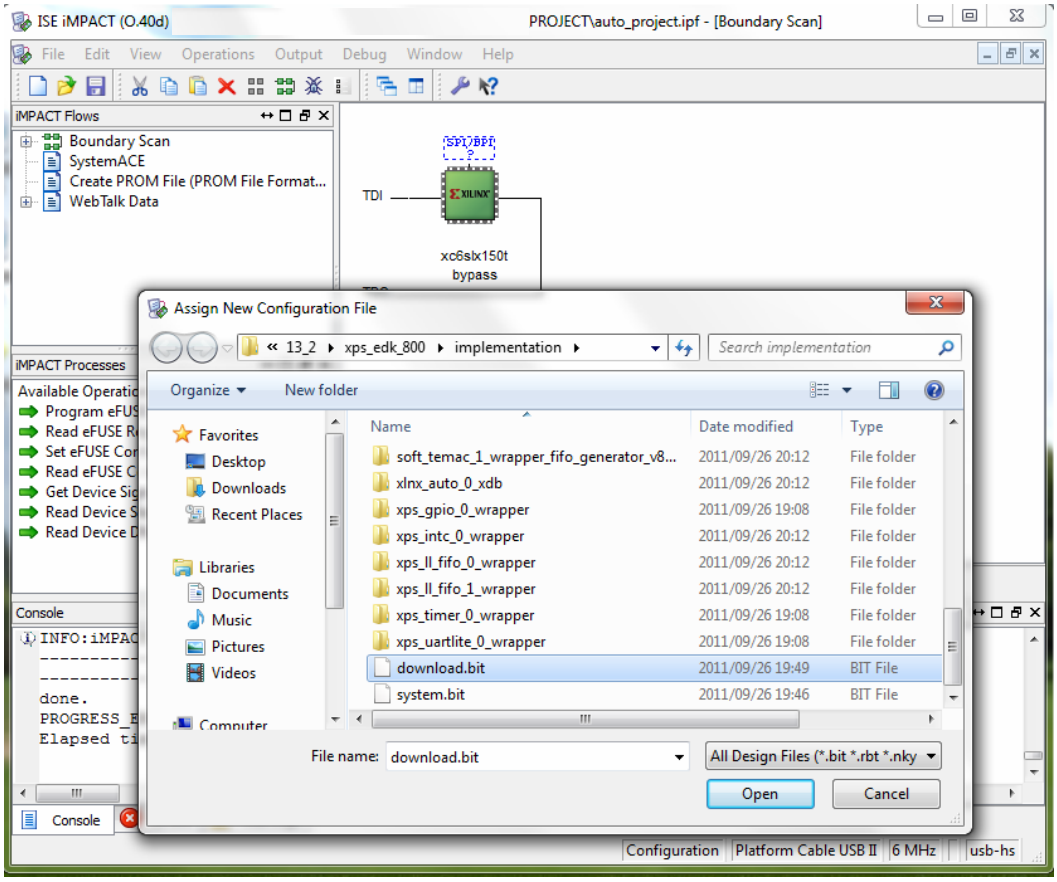
Figure 9-1 evaluation structure

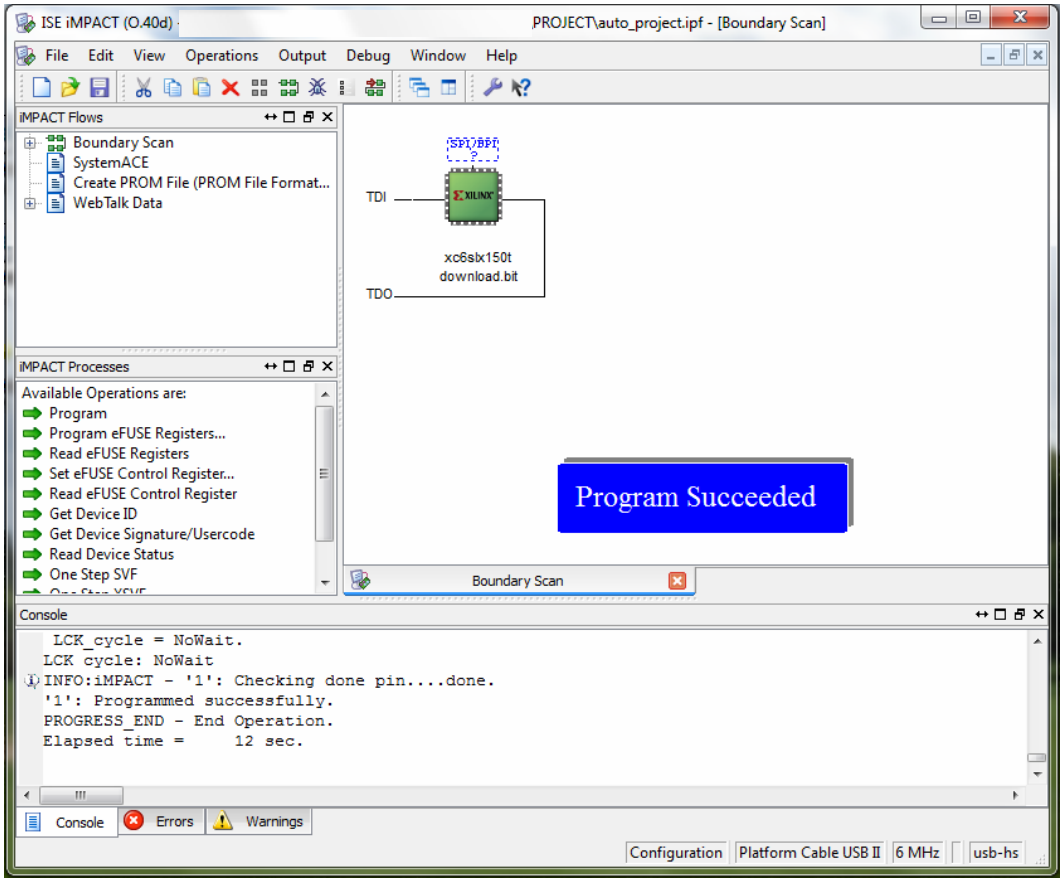
9.2. Ethernet data transmitting and receiving test

- PC IP address setting



➢ Configure FPGA,download bitfile (download.bit)



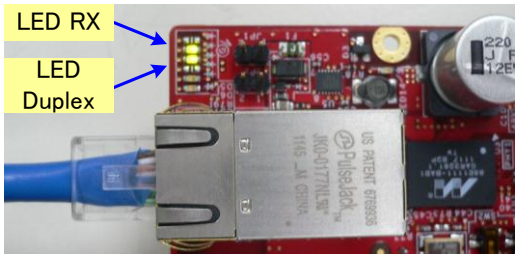


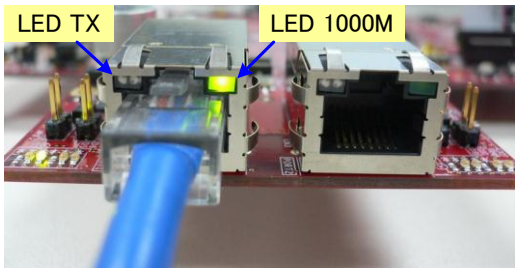
➢ Ping test of Port1

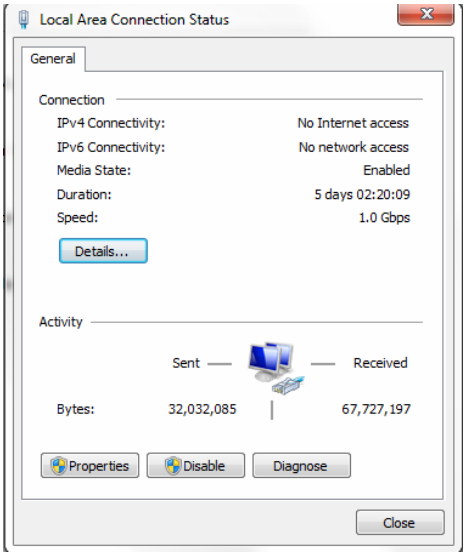
Connect PC to Port1.

LED (1000M) and LED (Duplex) will light on as the following photo.

[1.0Gbps] in the following window indicate current network data rate.

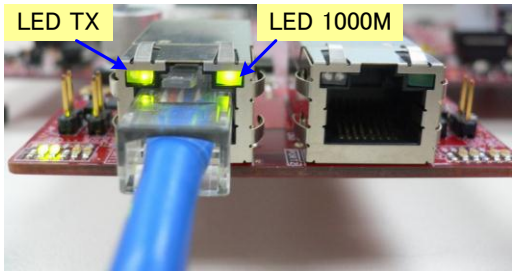


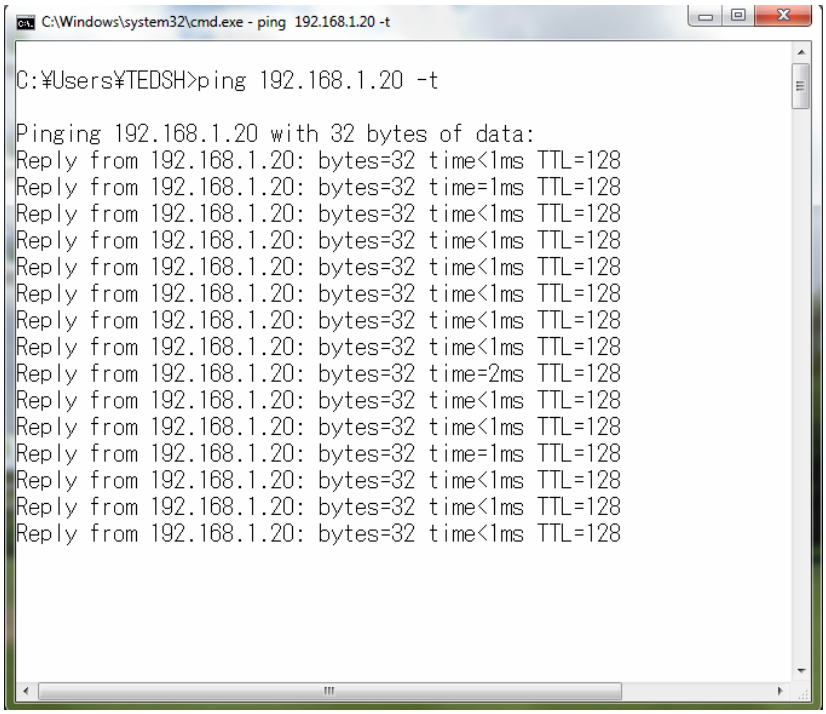




Ping port1 with IP Address 192.168.1.20 and message replies as the following.

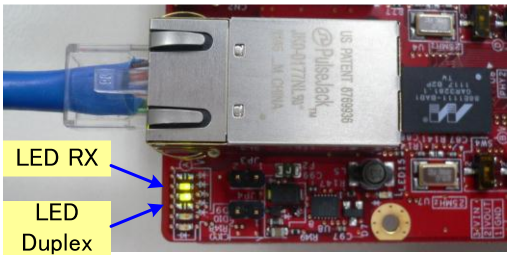
In the test, LED TX will blink.

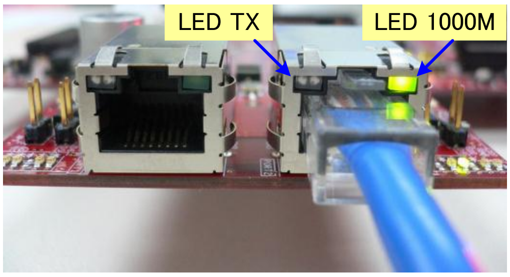


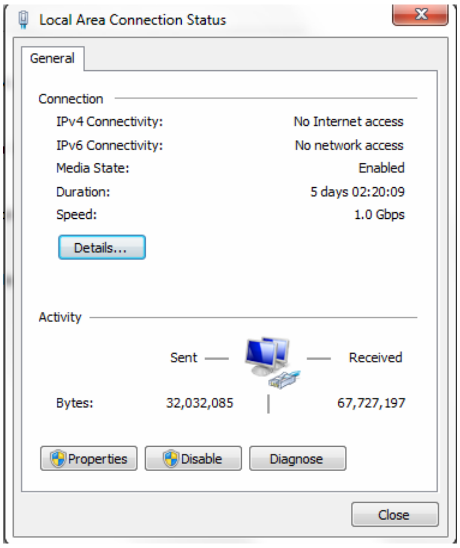


- Ping test of Port2

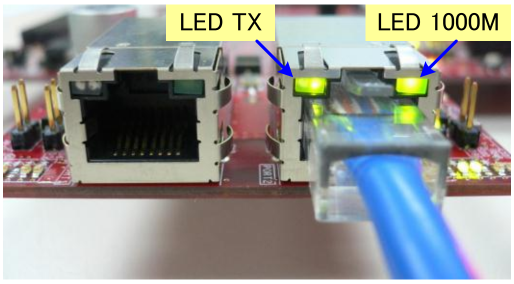
Connect PC to Port2.
LED (1000M) and LED (Duplex) will light on as the following photo.
[1.0Gbps] in the following window indicate current network data rate.

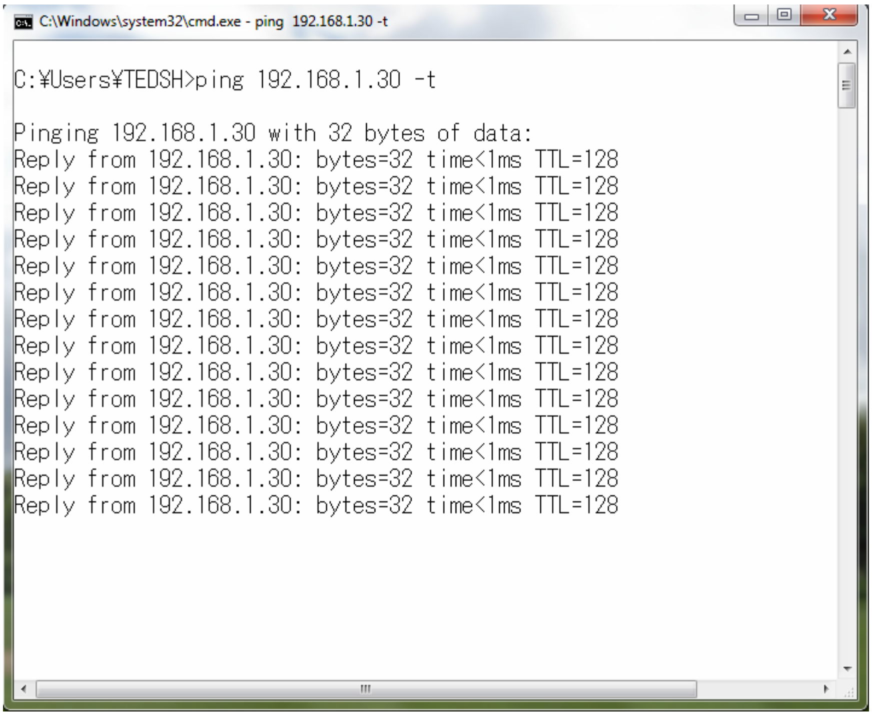






Ping port2 with IP Address 192.168.1.30 and message replies as the following.
In the test, LED TX will blink.






```
C:¥Users¥TEDSH>ping 192.168.1.30 -t

Pinging 192.168.1.30 with 32 bytes of data:
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
Reply from 192.168.1.30: bytes=32 time<1ms TTL=128
```

9.3. About Ethernet PHY's output clock

TB-FMCL-GLAN-B aims for implementation of Ethernet communication on TB-6S-LX150T-IMG2 which will act as a carrier board.
When TB-FMCL-GLAN-B works with other carrier boards, please ensure that Ethernet PHY's output clocks are connected to GC/CC pin of FPGA.

If Ethernet PHY's output clocks are not connected to GC/CC pin of FPGA, there will be Error Message about routing of clock signal in Mapping. Finally, the clock signal inside FPGA can only use local line which lead to in different routing result and unfixed clock delay in every Mapping.
In such case, Ethernet application on TB-FMCL-GLAN-B and carrier board may be unstable.

Please refer to Xilinx's TEMAC User Guide for detailed information about clock's requirements of GMII/RGMII application in Spartan-6 FPGA and Virtex-6 FPGA.

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