Viglen SX140

User Manual

VIG700P

Viglen®

Great
Minds
Think

Viglen®

COMPUTERS ◆ NETWORKS ◆ SOLUTIONS

Viglen EMC and the 'CE' mark

CE Marking

As we begin the 21st century, European standards are being harmonised across borders. If products comply with the same standards in all European countries, product exporting and importing is made simple - paving our way to a common market. If you buy a product with a 'CE' mark on it (shown below), on the box, in the manual, or on the guarantee - it complies with the currently enforced directive(s).

CE

Introduction to EMC

EMC (Electromagnetic Compatibility) is the term used to describe certain issues with RF (Radio Frequency) energy. Electrical items should be designed so they do not interfere with each other through RF emissions. E.g. If you turn on your microwave, your television shouldn't display interference if both items are CE marked to the EMC directive.

If emitted RF energy is not kept low, it can interfere with other electrical circuitry - E.g. Cars Automatic Braking Systems have been known to activate by themselves while in a strong RF field. As this has obvious repercussions ALL electrical products likely to cause RF related problems have to be 'CE' marked from 1st January 1996 onwards.

If a product conforms to the EMC directive, not only should its RF emissions be very low, but its immunity to RF energy (and other types) should be high. The apparatus has to resist many 'real world' phenomena such as static shocks and mains voltage transients.

Viglen's Environment laboratory

To gain a 'CE' mark, the Viglen computer range has had to undergo many difficult tests to ensure it is Electromagnetically Compatible. These are carried out in the in-house 'Environment lab' at Viglen Headquarters. We have made every effort to guarantee that each computer leaving our factory complies fully with the correct standards. To ensure the computer system maintains compliance throughout its functional life, it is essential you follow these guidelines.

Install the system according to Viglen's instructions

If you open up your Viglen System:

Keep internal cabling in place as supplied.
Ensure the lid is tightly secured afterwards
Do not remove drive bay shields unless installing a 'CE' marked peripheral in its place
The clips or 'bumps' around the lips of the case increase conductivity - do not remove or damage.
Do not remove any ferrite rings from the L.E.D cables.
Only use your Viglen computer with 'CE' marked peripherals

This system has been tested in accordance with European standards for use in residential and light industrial areas-this specifies a 10 meter testing radius for emissions and immunity. If you do experience any adverse affects that you think might be related to your computer, try moving it at least 10 meters away from the affected item. If you still experience problems, contact Viglen's Technical Support department who will put you straight through to an EMC engineer - s/he will do everything possible to help. If modifications are made to your Viglen computer system, it might breach EMC regulations. Viglen take no responsibility (with regards to EMC characteristics) of equipment that has been tampered with or modified.

Copyrights and Trademarks

Please note:

The material in this manual is subject to change without notice.

Trademarks

Microsoft, Windows, Windows XP, Windows 2000, Windows NT, Windows 95, MS-DOS and OS/2 are registered trademarks of Microsoft Corporation. i386, i486, Xeon, Pentium, Pentium Pro and MMX are registered trademarks of Intel Corporation. JAC-UP, Contender, Dossier, Vig, Viglen, VigStor and Envy are trademarks of Viglen Limited. Genie and Contender are registered trademarks of Viglen Limited.

Copyright and Patents

Viglen SX140 Server System – User Guide Version 1.0
Printed in the United Kingdom

Liability

No warranty or representation, either expressed or implied, is made with respect to this documentation, its quality, performance, merchantability or fitness for a particular purpose. As a result the documentation is licensed as is, and you, the licensee, are assuming the entire risk as to its quality and performance. The vendor reserves the right to revise this operation manual and all accompanying software and documentation and to make changes in the content without obligation to notify any person or organisation of the revision or change.

In no event will the vendor be liable for direct, indirect, special, incidental or consequential damages arising out of the use or inability to use this product or documentation, even if advised of the possibility of such damages. In particular, the vendor shall not have liability for any hardware, software or data stored or used with the product, including the costs of repairing, replacing or recovering such hardware, software or data.

Contents

1. Overview

This manual describes the Viglen SX140 system. The motherboard is the most important part of your computer. It contains all of the CPU, memory and graphics circuitry that makes the computer work.

Checklist

Please check that the following items have been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

In addition to the motherboard and chassis, various hardware components may have been included with your Viglen SX140 Server, as listed below:

- Intel Xeon Nocona 800 MHz FSB
- Two (2) CPU Passive Heatsinks*
- Six 184-pin DIMM sockets supporting up to 12/24 GB Registered ECC DDR-333/266 (PC2700/PC2100) SDRAM required.
- SCSI Accessories
- One (1) CD-ROM containing drivers and utilities:

- Viglen Server User Guide CD - Release 4.0

The Motherboard Built upon the functionality and the capability of the E7320 (Lindenhurst-VS) chipset, the motherboard provides the performance and feature set required for dual processor-based servers, with configuration options optimized for communications, presentation, storage, computation or database applications. The Intel E7320 (Lindenhurst-VS) chipset consists of the following components: the E7320 (Lindenhurst-VS) Memory Controller Hub (MCH), the I/O Controller Hub (6300ESB ICH), and THE PCI-X Hub (PXH). The E7320 (Lindenhurst-VS) MCH supports single or dual Nocona processors with Front Side Bus speeds of up to 800 MHz. Its memory controller provides direct connection to two channels of registered DDR266, DDR333 with a marched system bus address and data bandwidths of up to 6.4GB/s. The E7320 (Lindenhurst-VS) also supports the new PCI Express high speed serial I/O interface for superior I/O bandwidth. The MCH provides configurable x8 PCI Express interfaces which may alternatively be configured as two independent x4 PCI Express interfaces. These interfaces support connection of the MCH to a variety of other bridges that are compliant with the PCI Express Interface Specification, Rev. 1.0a. The MCH interfaces with the 6300ESB I/O Controller Hub (6300ESB ICH) via Hub Interface. The PCI- Bus provides connection between a PCI Express interface and two independent PCI bus interfaces that can be configured for standard PCI 2.3 protocol, as well as the enhanced high-frequency PCI-X protocol.

The PXH can be configured to support for 32- or 64-bit PCI devices running at 33 MHz, 66 MHz, 100 MHz, and 133 MHz.

This manual contains technical information about the Viglen Motherboard and other hardware components inside your computer. If you are new to computers we recommend that you read the user guide first. If you are an experienced computer user this manual should provide all the information you will need to perform simple upgrades and maintenance.

We hope that this manual is both readable and informative. If you have any comments or suggestions about how we could improve the format then please fill out the form at the back of the manual and send it to us.

Above all we hope that you enjoy using your Viglen SX140 Server.

Motherboard features

CPU

Single or dual Intel® 604-pin 32-bit/Ext. EM64T Nocona TM (upto 3.6GHz) processors at 800 MHz front side bus speed.

Memory

Six 184-pin DIMM sockets supporting up to 12/24 GB Registered ECC DDR-333/266 (PC2700/PC2100) SDRAM required. Note: Interleaved memory; requires memory modules to be installed in pairs.

Chipset

Intel E7320 (Lindenhurst-VS) chipset with support of: MCH, PXH and 6300ESB ICH.

Expansion Slots

One PCI-E slot

Two 64-bit PCI-X slots (One 64-bit PCI-X133 slot, One PCI-X-100 slot).

One 32-bit PCI slot

BIOS

8 Mb AMI® Flash ROM
APM 1.2, DMI 2.1, PCI 2.2, ACPI 2.0, Plug and Play (PnP), SMBIOS 2.3

PC Health Monitoring

Onboard voltage monitors for CPU cores, chipset voltage, Memory voltage, 3.3V, +5V, +12V,-12V, 3.3V standby and 5Vstandby.
CPU/chassis temperature monitors.
Environmental temperature monitor and control via Super Doctor III.
CPU fan auto-off in sleep mode.
CPU slow-down on temperature overheat.
CPU thermal trip support for processor protection, +5V standby alert LED.
Power-up mode control for recovery from AC power loss.
Auto-switching voltage regulator for CPU core.
System overheat LED and control.
Chassis intrusion detection.
System resource alert via Super Doctor III
TM2 Feature.
Fan Control
VRM Protection Feature (88°C, ***98**°C, 108°C) (*Default).

ACPI Features (optional)

Microsoft On Now
Slow blinking LED for suspend state indicator
Main switch override mechanism

Onboard I/O

LSI Logic Single Channel 53C1020 Ultra 320 SCSI
One IPMI 2.0
Two Intel 82541 GI Gigabit Ethernet controllers
2 EIDE Ultra DMA/100 bus master interfaces
1 floppy port interface (up to 2.88 MB)
1 EPP/ECP Parallel Header
PS/2 mouse and PS/2 keyboard ports
Up to 4 USB 2.0 (Universal Serial Bus) (2 ports/2 headers)
2 Intel 6300 ESB Serial ATA
Super I/O

2 Serial port/header

Other

Internal/external modem ring-on

Wake-on-Ring (WOR)

Console redirection

Dimensions

Extended ATX: 12" x 10" (304.8 x 254 mm)

Special Features

BIOS Recovery

The BIOS Recovery function allows you to recover your BIOS image file if the BIOS flashing procedure fails.

Recovery from AC Power Loss

The BIOS provides a setting for you to determine how the system will respond when AC power is lost and then restored to the system. You can choose for the system to remain powered off (in which case you must hit the power switch to turn it back on) or for it to automatically return to a power on state. See the Power Lost Control setting in the Advanced BIOS Setup section (Peripheral Device Configuration) to change this setting. The default setting is Always On.

PC Health Monitoring

This section describes the PC health monitoring features of the VIG700P. Both have an onboard System Hardware Monitor chip that supports PC health monitoring.

Onboard Voltage Monitors for the CPU Cores, Chipset Voltage, +3.3V, +5V, +12V, -12V and +5V Standby

An onboard voltage monitor will scan these voltages continuously. Once a voltage becomes unstable, a warning is given or an error message is sent to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

Fan Status Monitor with Firmware/Software On/Off Control

The PC health monitor can check the RPM status of the cooling fans. The onboard CPU and chassis fans are controlled by the Thermal management via the BIOS.

Environmental Temperature Control

The thermal control sensor monitors the CPU temperature in real time and will turn on the thermal control fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the thermal control fan to prevent any overheat damage to the CPU. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Overheat LED and Control

This feature is available when the user enables the CPU overheat warning function in the BIOS. This allows the user to define an overheat temperature.

Auto-Switching Voltage Regulator for the CPU Core

The auto-switching voltage regulator for the CPU core can support up to 20A current and auto-sense voltage IDs ranging from .8375V to 1.6V. This will allow the regulator to run cooler and thus make the system more stable.

TM2/CPU VRM Overheat

When the CPU reaches 70°C and above (Overheat), the CPU will slow down and CPU Voltage will decrease to reduce CPU power consumption and VRM heat dissipation.

When CPU temperature reaches 78°C (*Default) and above, the system will go into the throttling state. The Overheat LED and Alarm Buzzer will be turned on. The CPU performance will drop 50%. When this happens, you can go to the Health Monitor Setting in the BIOS to reset CPU Overheat Temperature.

VRM Protection

When the CPU VRM temperature reaches the threshold preset by the user in the BIOS, the system will go into the TM2 Mode. The CPU will slow down, the VRM current will drop to prevent the VRM from overheat. (The settings are: 88°C, ***98**°C, 108°C) (*Default)

ACPI Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with Windows 2000, Windows XP and Windows Server 2003.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button to make the system enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. This option can be set in the Power section of the BIOS Setup routine.

External Modem Ring-On

Wake-up events can be triggered by a device such as the external modem ringing when the system is in the SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboards have a 3-pin header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS. Note that Wake-On-LAN can only be used with an ATX 2.01 (or above) compliant power supply.

Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The VIG700P can only accommodate ATX 24-pin power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. You should use one that will supply at least 400W of power and includes the additional +12V, 8-pin power connector – an even higher wattage power supply is recommended for high-load configurations. Also your power supply must supply 1.5A for the Ethernet ports.

NOTE!

An additional 12v power 8-pin power connector (PW2) is required to support Intel Xeon CPUs. Failure to provide this extra power will result in instability of the CPUs after only a few minutes of operation.

It is strongly recommended that you use a high quality power supply that meets ATX power supply Specification 2.02 or above. It must also be SSI compliant. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s. It

also provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP).

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features
auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can flexibly adjust to meet ISA PnP requirements, which support ACPI and APM (Advanced Power Management).

2. SX140 Chassis Specification

The SX140 chassis is designed to be mounted in a 19” rack cabinet. If the server is supplied complete with a pair of industry standard 19” Rails, handles and all of the necessary nuts and bolts.

Physical Specifications

Specifications	
Height	43 mm
Width / Rackmount Height	437 mm
Depth	504 mm
Weight	14.1 kg typical configuration

Chassis Features

The galvanised metal chassis minimises EMI and radio frequency interference (RFI). The removable access cover is attached to the chassis with two thumbscrews and provides easy access to the VIG700P motherboard and power supply.

Feature	Description
Drive Bays	One Slim CD ROM Drive Four SCA 1” Drive Trays One Slim 3.5” Floppy Drive
Baseboard	Viglen VIG700P Server Motherboard
Power supply	420W ATX power supply, with integrated cooling fan.
Expansion slot covers	1 Riser slot for additional card
System cooling Fan	Four (4) 40mm Fans

Chassis Front Controls and Indicators

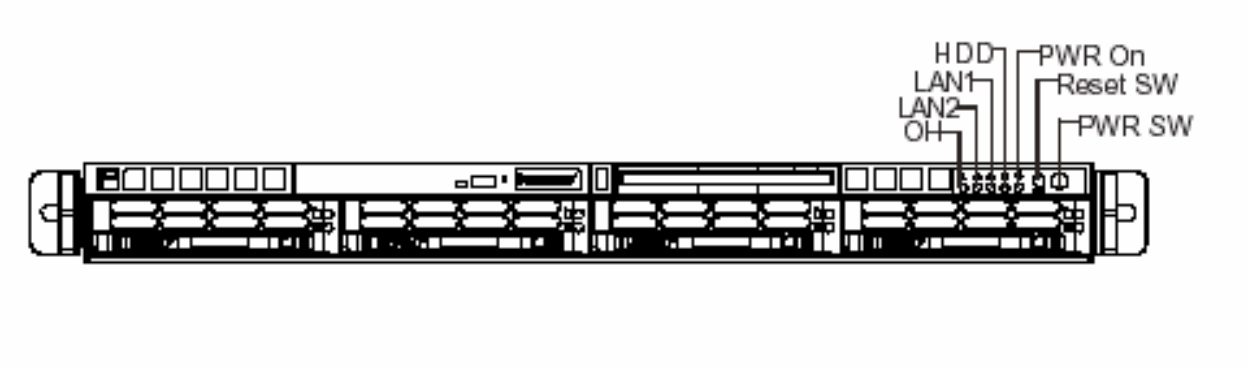


Figure 1: Chassis Front Controls and Indicators

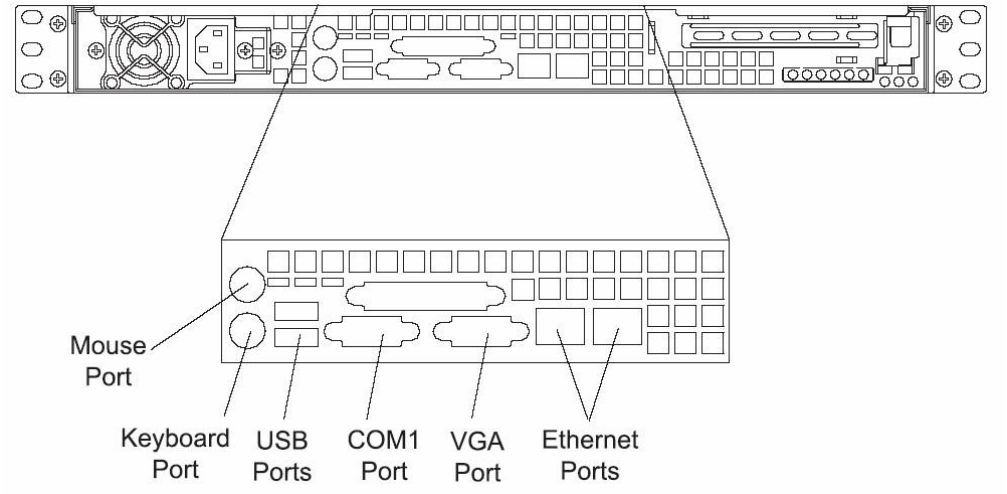


Figure 2: Rear View of Chassis and I/O Ports

Removing the top cover from the Chassis

Before installing any components, replacing chassis fans or accessing the motherboard, you will first need to remove the top cover from the chassis.

1. Press the release tabs to release the top cover from its locking position.
2. Slide the top cover out from the chassis as shown below:
3. You can now lift the side cover up and off the chassis.

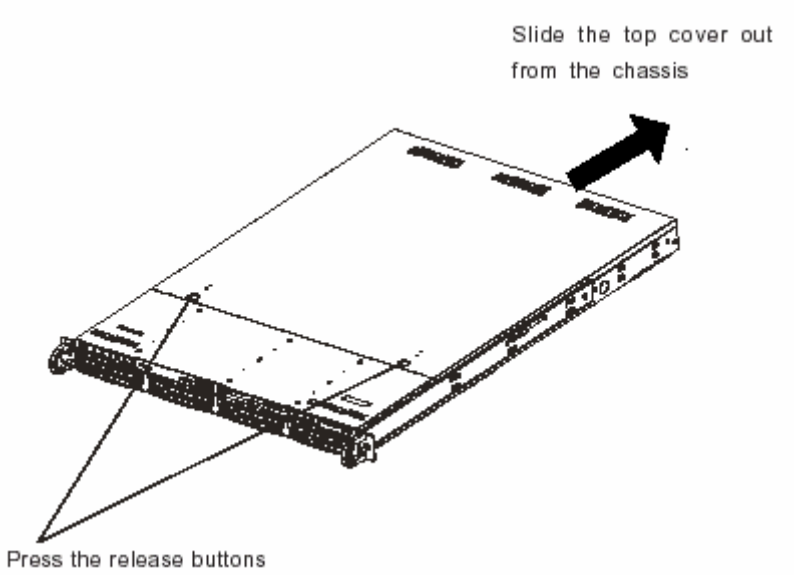


Figure 3: Removing the Top Cover

Accessing the SCA Drive Tray and Installing a Hard Drive

To install the SCA drive into the chassis, you need to first remove the SCA drive try from the chassis so that the SCA drive can be installed in.

1. Press the release tab to release the SCA drive tray from its looking position.
2. Pull the SCA drive tray out from the chassis as shown below:

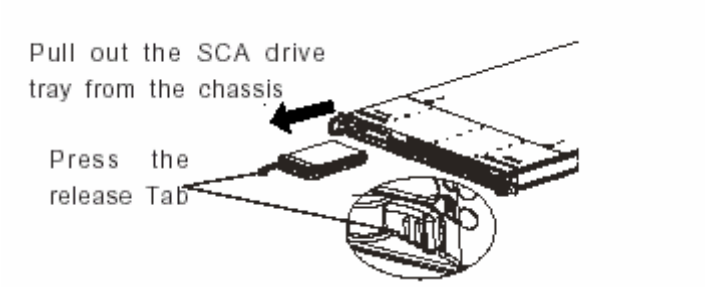


Figure 4: Removing SCA drive tray from the Chassis

3. Remove the two screws that attach to the both sides of the dummy tray, and take out the dummy tray as shown below.

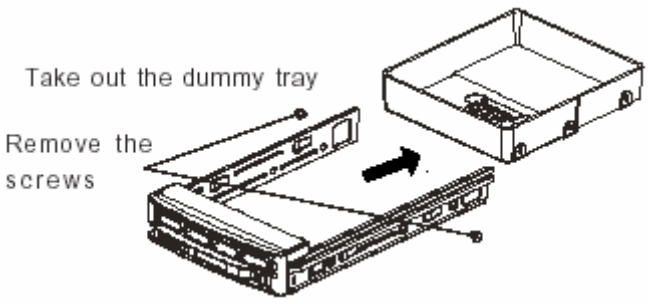


Figure 5: Removing Dummy Tray

4. Slide a hard drive disk (HDD) into the SCA drive tray, and secure the HDD to the tray with three screws on each side of the tray as shown below:

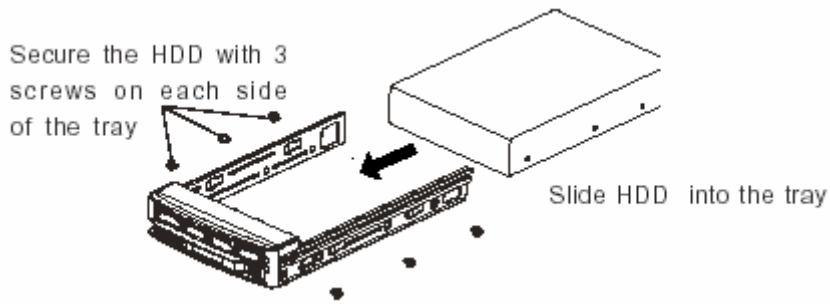


Figure 6: Installing a HDD

5) Once the HDD is securely in placed into the SCA tray, you can install the SCA drive tray back into the chassis.

Rail Installation

Rail Packing includes: One pair of inner slides to be installed on the chassis,
One pair of outer slides to be installed in the rack,
Two pairs of short brackets to be used on the front sides of the outer slides.

(Note: One pair of short brackets include screw thread, and the other pair do not. Use the only pair that will fit into your rack.)

Installing Inner Slides:

1. Locate the right inner slide, (the slide that will be used on the right side of chassis when facing the front panel of the chassis).

2. Align the four (4) square holes on the right inner slide against the hooks on the right side of the chassis as show below on the left.

3. Securely attach the slide to the chassis with two M4 flat head screws and repeat the steps 1-3 to install the left inner slide to the left side of the chassis.

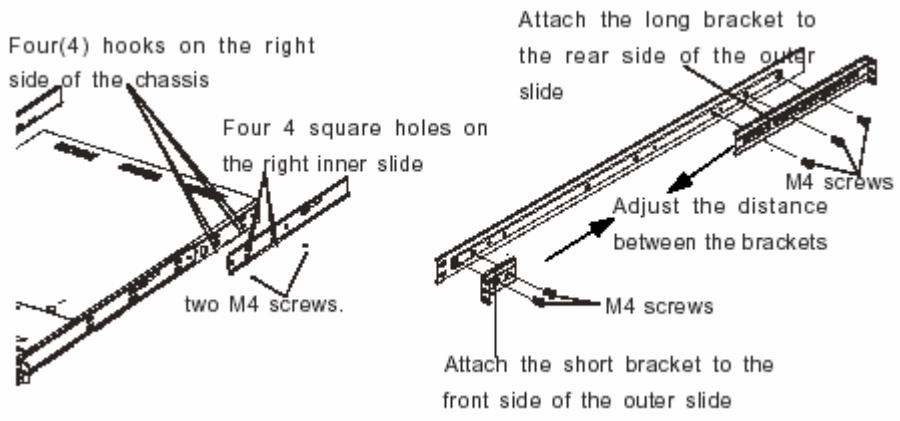


Figure 7: Installing Inner Slides

Installing Outer Slides

1. Measure the distance from the front rail of the rack to the rear rail of the rack.

2. Attach a short bracket to the front side of the right outer slide, and a long bracket to the rear side of the right outer slide as shown above on the right.

3. Adjust the short and long brackets to the proper distance so that the slide can snugly fit into the rack.

4. Secure the short bracket to the front side of the outer slide with two M4 screws and the long bracket to the rear side of the outer slide with threeM4 screws as shown above. Repeat steps 1-4 for the left outer slide.

Installing the Slide Assemblies to the Rack

1. After you have installed the short and long brackets to the outer slides, you are ready to install the whole slide assemblies (outer slides with short and long brackets attached) to the rack. Use M5 screws and washers to secure the slide assemblies into the rack as shown below:

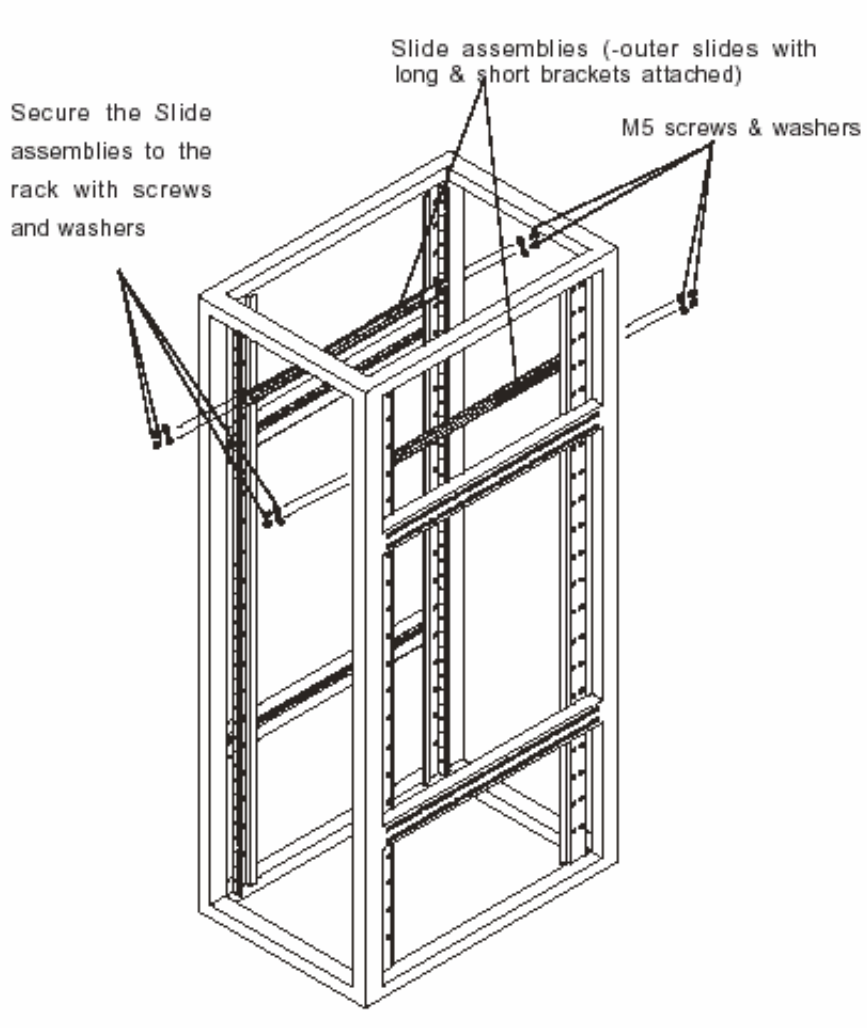
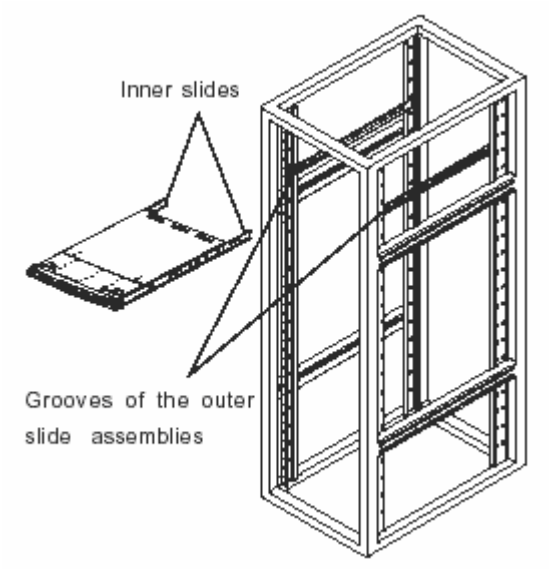


Figure 8: Installing Slide Assemblies to the Rack

Installing the Chassis into the Rack

1. Push the inner slides, which are attached to the chassis, into the grooves of the outer slide assemblies that are installed in the rack as shown below:



2. Push the chassis all the way to the back of the outer slide assemblies as shown below:

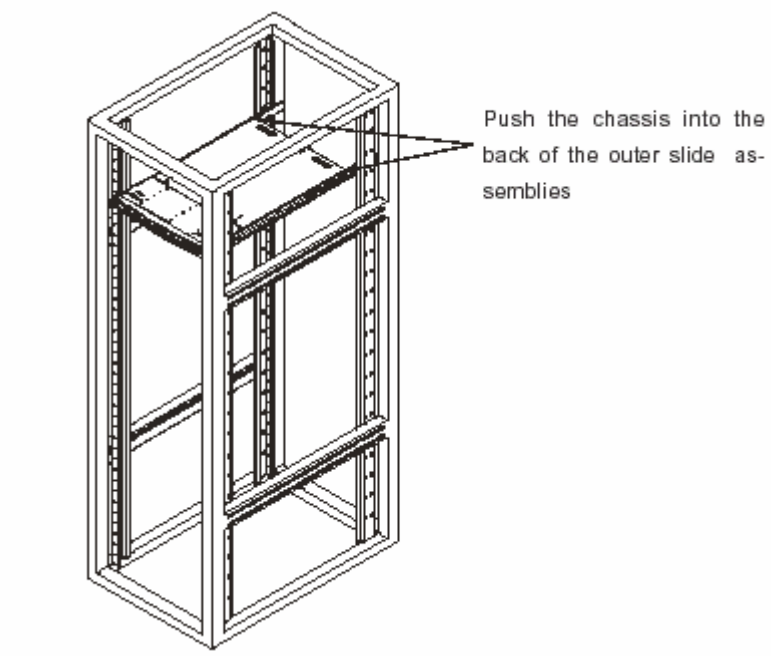


Figure 9: Installing the Server Chassis into the Rack

3. Safety Precautions

Electrical Safety Precautions

- *Basic electrical safety precautions should be followed to protect you from harm and the Viglen SX140 Server from damage:*

- *Be aware of the locations of the power on/off switch on the chassis as well as the room's emergency power-off switch, disconnection switch or electrical outlet. If an electrical accident occurs, you can then quickly remove power from the system.*

- *Do not work alone when working with high voltage components.*

- *Power should always be disconnected from the system when removing or installing main system components, such as the motherboard, memory modules and the CD-ROM and floppy drives. When disconnecting power, you should first power down the system with the operating system and then unplug the power cords of all the power supply units in the system.*

- *When working around exposed electrical circuits, another person who is familiar with the power-off controls should be nearby to switch off the power if necessary.*

- *Use only one hand when working with powered-on electrical equipment. This is to avoid making a complete circuit, which will cause electrical shock. Use extreme caution when using metal tools, which can easily damage any electrical components or circuit boards they come into contact with.*

- *Do not use mats designed to decrease electrostatic discharge as protection from electrical shock. Instead, use rubber mats that have been specifically designed as electrical insulators.*

- *The power supply power cord must include a grounding plug and must be plugged into grounded electrical outlets.*

- *Motherboard Battery: **CAUTION** - There is a danger of explosion if the onboard battery is installed upside down, which will reverse its polarities. On the VIG700P, the positive side should be facing up. This battery must be replaced only with the same or an equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.*

General Safety Precautions

Follow these rules to ensure general safety:

- *Keep the area around the Viglen SX140 Server clean and free of clutter.*
- *The Viglen SX140 Server weighs approximately (14.1 kg) when fully loaded. When lifting the system, two people at either end should lift slowly with their feet spread out to distribute the weight. Always keep your back straight and lift with your legs.*
- *Place the chassis top cover and any system components that have been removed away from the system or on a table so that they won't accidentally be stepped on.*
- *While working on the system, do not wear loose clothing such as neckties and unbuttoned shirt sleeves, which can come into contact with electrical circuits or be pulled into a cooling fan.*
- *Remove any jewelry or metal objects from your body, which are excellent metal conductors that can create short circuits and harm you if they come into contact with printed circuit boards or areas where power is present.*
- *After accessing the inside of the system, close the system back up and secure it to the rack unit with the retention screws after ensuring that all connections have been made.*

ESD Precautions

Electrostatic discharge (ESD) is generated by two objects with different electrical charges coming into contact with each other. An electrical discharge is created to neutralise this difference, which can damage electronic components and printed circuit boards. The following measures are generally sufficient to neutralise this difference before contact is made to protect your equipment from ESD:

- *Use a grounded wrist strap designed to prevent static discharge.*
- *Keep all components and printed circuit boards (PCBs) in their antistatic bags until ready for use.*
- *Touch a grounded metal object before removing the board from the antistatic bag.*
- *Do not let components or PCBs come into contact with your clothing, which may retain a charge even if you are wearing a wrist strap.*
- *Handle a board by its edges only; do not touch its components, peripheral chips, memory modules or contacts.*

- *When handling chips or modules, avoid touching their pins.*

- *Put the motherboard and peripherals back into their antistatic bags when not in use.*

- *For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.*

Operating Precautions

Care must be taken to assure that the chassis cover is in place when the Viglen SX140 is operating to assure proper cooling. Out of warranty damage to the Viglen SX140 system can occur if this practice is not strictly followed.

4. SX140 Server Board Installations

This chapter covers the steps required to install processors and heatsinks to the VIG700P motherboard, connect the data and power cables and install add-on cards. All motherboard jumpers and connections are also described. A layout and quick reference chart are also included in this chapter. ***Remember to close the chassis completely when you have finished working on the motherboard to protect and cool the system sufficiently.***

WARNING & CAUTIONS!

WARNING!

Unplug the system before carrying out the procedures described in this chapter. Failure to disconnect power before you open the system can result in personal injury or equipment damage. Hazardous voltage, current, and energy levels are present in this product. Power switch terminals can have hazardous Voltages present even when the power switch is off.

The procedures assume familiarity with the general terminology associated with personal computers and with the safety practices and regulatory compliance required for using and modifying electronic equipment.
Do not operate the system with the cover removed. Always replace the cover before turning on the system.

As the colours of the wires in the mains lead of this computer may not correspond with the coloured markings identifying the terminals in your plug precede as follows:

*The wire that is coloured green-and-yellow must be connected to the terminal in the plug, which is marked by the letter **E** or coloured green or green-and-yellow.*

*The wire that is coloured blue must be connected to the terminal, which is marked with the letter **N** or coloured black.*

*The wire that is coloured brown must be connected to the terminal, which is marked with the letter **L** or coloured red.*

Handling the VIG700P Motherboard

Static electrical discharge can damage electronic components. To prevent damage to printed circuit boards, it is important to handle them very carefully. Also note that the size and weight of the motherboard can cause it to bend if handled improperly, which may result in damage. To prevent the motherboard from bending, keep one hand under the center of the board to support it when handling. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- *Use a grounded wrist strap designed to prevent static discharge.*
- *Touch a grounded metal object before removing any board from its antistatic bag.*
- *Handle a board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.*
- *When handling chips or modules, avoid touching their pins.*
- *Put the motherboard, add-on cards and peripherals back into their antistatic bags when not in use.*

Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

PGA Processor and heatsink Installation

Warning!

When handling the processor package, avoid placing direct pressure on the label area of the fan. Also, do not place the motherboard on a conductive surface, which can damage the BIOS battery and prevent the system from booting up.

Important!

Always connect the power cord last and always remove it before adding, removing or changing any hardware components. Make sure that you install the processor into the CPU socket ***before*** *you install the heatsink. The VIG700P can support either one or two Intel Xeon 512K L2 cache processors of 3.6+ GHz. If installing one processor only, install it into CPU socket #1.*

Upgrading the CPU

The new Intel Nocona processor uses a new 604-pin core package technology Micro Pin Grid Array, or Micro-PGA. This package utilises a 604-pin zero insertion force socket (PGA-604). Thermal solutions are attached directly to the back of the processor core package with the use of a thermal plate or heat spreader.

When the processor is mounted in the socket 604 connector, it is secured by the ZIF (Zero Insertion Force) socket.

The design of the VIG700P Motherboard makes it a simple job to replace or upgrade the processors. Follow the instructions below for instructions on how to upgrade the processors:

1. Before commencing any work inside your Viglen system please read the warnings and cautions section.

2. Remove the lid from the computer by removing the screws at the rear of the case.

3. Locate the Micro-PGA processors covered with a heat sink.

4. Carefully remove the heat sink by pushing down an out the retention mechanism, to free it from the socket.

5. The CPU is clamped into place using a lever. Gently lift this lever, which is located at the side of the socket 604. This will free the CPU and allow you to lift it clear of the socket. Do not attempt to remove the CPU with the lever in the down position.

6. You can now fit the additional or replacement processor and heatsink into the socket 604 interface.

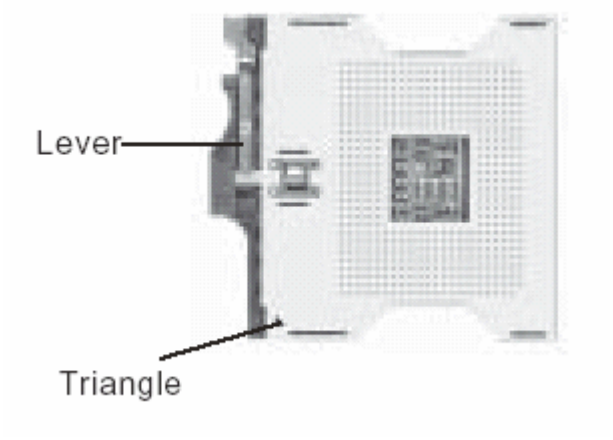


Figure 10: Socket 606 Interface

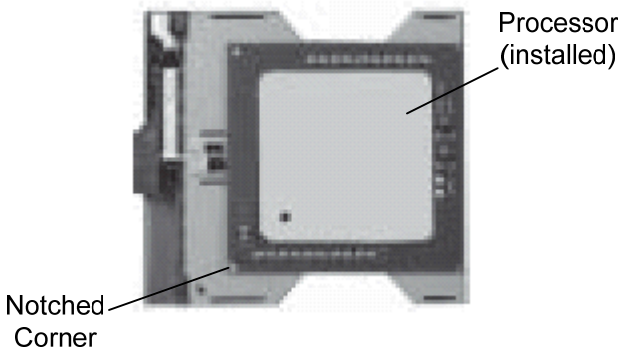


Figure 11: Nocona 604-Pin Processor (Installed)

If the CPU will not easily fit into the socket if you are trying to plug it in the wrong way around.

Warning!

Make sure you lift the lever completely when installing the CPU. If the lever is only partly raised, damage to the socket or CPU may result.

Installing the Heatsinks

Please refer to Figure 12 for heatsink installation. Note that the motherboard shown below is not the Viglen VIG700P; however the heatsink location and installation procedure is identical.

1) Do not apply any thermal grease to the heatsink or the CPU die; the required amount of thermal grease has already been applied.
2) Place the heatsink on top of the CPU so that the four mounting holes are aligned with those on the retention mechanism.
3) Screw in two diagonal screws (i.e. the #1 and #2 screws) until just snug (do not fully tighten the screws to avoid possible damage to the CPU.)
4) Finish the installation by fully tightening all four screws.

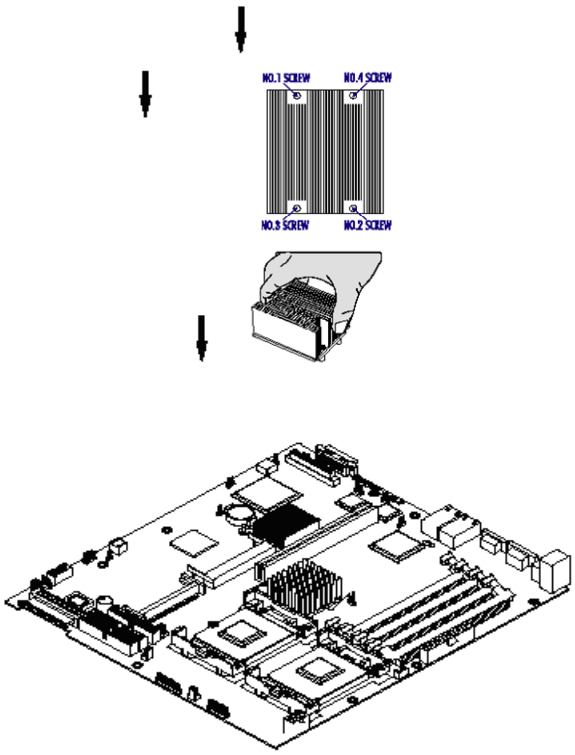


Figure 12: Heatsink Installation

Installing Memory DIMMs

Note!

Please check with your Account Manager or the Viglen web site for recommended memory modules (www.viglen.co.uk).

Caution!

Exercise extreme care when installing or removing DIMM modules to prevent any possible damage. Also note that the SX140 server does support two-way interleaving which means memory must be installed in identical pairs.

DIMM Installation & Removal (See Figure 13 & 14)

1) Insert the desired number of DIMMs into the memory slots, starting with Bank 1.

2) Insert each DIMM module vertically into its slot. Pay attention to the notch along the bottom of the module to prevent inserting the DIMM module incorrectly.

3) Gently press down on the DIMM module until it snaps into place in the slot. Repeat for all modules (see step 1 above).

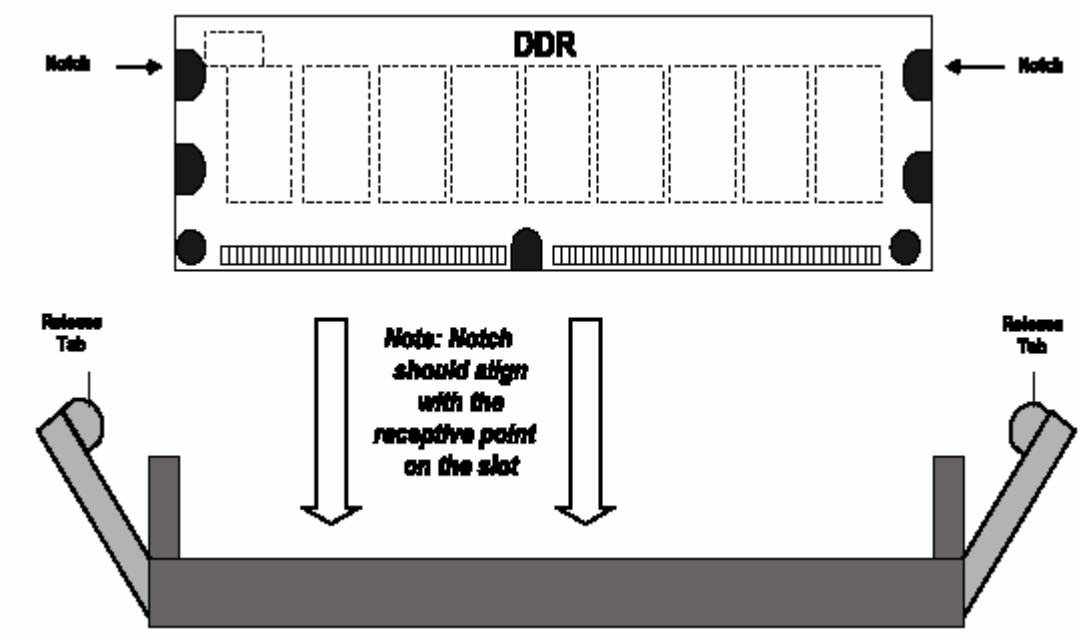


Figure 13: Installing DIMMs

To Install:

Insert module vertically and press down until it snaps into place. Pay attention to the alignment notch at the bottom.

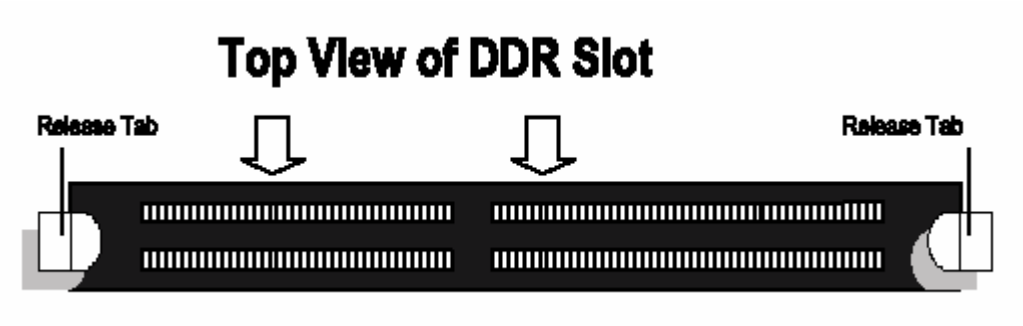


Figure 14: Removing DIMMs

To Remove:

Use your thumbs to gently push near the edge of both ends of the module. This should release it from the slot.

Memory Support

The Viglen SX140 Server only supports up to 12/24 GB of Reg ECC DDR 333/266 (PC2700/PC2400) memory. The VIG700P was designed to support 4 GB modules in each slot, but has only been verified for up to 2 GB modules.

Motherboard Layout

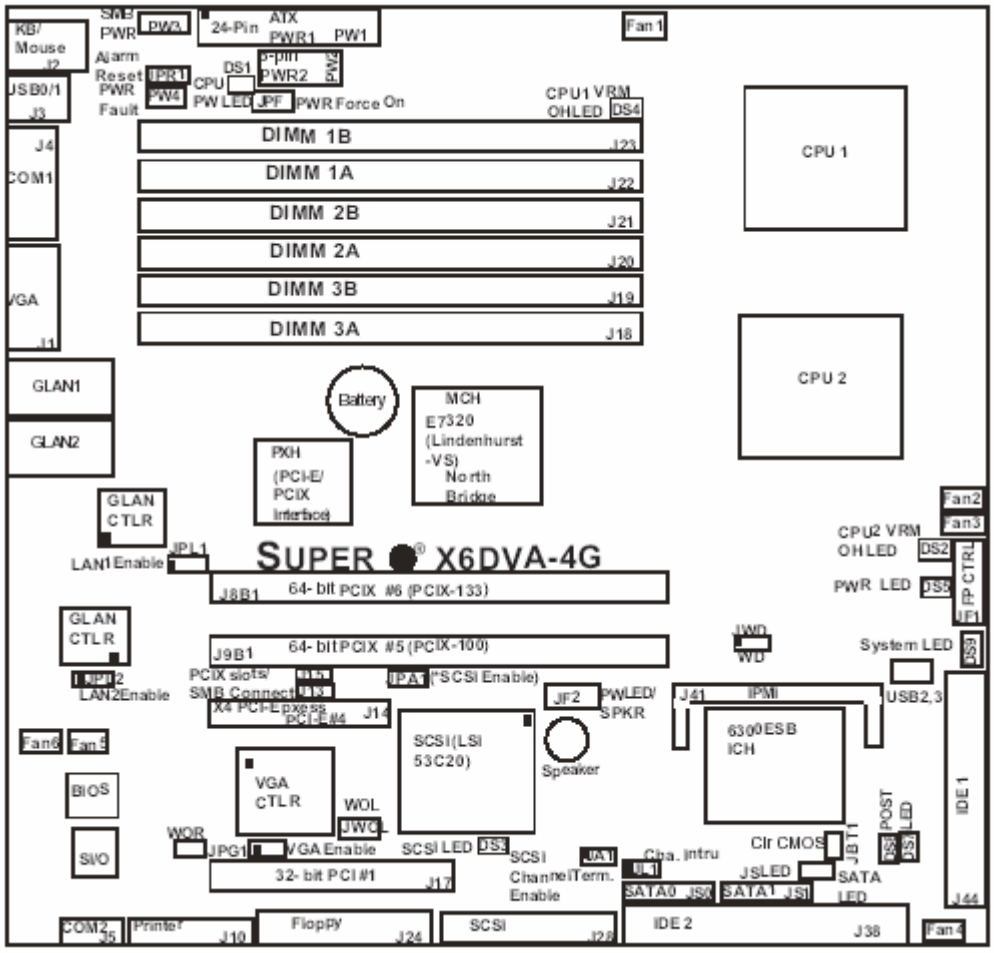


Figure 15: VIG700P Board layout

Jumper	Description	Default Setting
J13/J15	PCI#1/PCI-x#5,#6 to system SMB	On (Connected)
JA1	SCSI Channel Term.	Off (Enable)
JBT1	CMOS Clear	
JPA1	SCSI Controller Enable	Enabled
JPF	Power Force on	Open (Disabled)
JPG1	VGA Enable	Pins 1-2 (Enabled)
JPL1 / JPL2	LAN1/LAN2 Enable/Disable	Pins 1-2 (Enabled)
JPR1	Power Fail Alarm Reset	Open (Disabled)
JWD	Watch Dog Enable	Pins 1-2 (Enabled)

Note!

Jumpers not noted are for test purposes only.

Connector	Description
ATX PWR (PW1)	Primary 24-pin ATX Power Connector
12V PWR (JW2)	12V 8-pin PWR Connector
COM1 (J4)/COM2 (J5)	COM1/COM2 Serial Port Connector/Header
DIMM 1A-3B (J18-J23)	Memory (RAM) Slots (1A, 1B, 2A, 2B, 3A, 3B)
DS1-DS5, DS7-DS8	Onboard LED Indicators DS7/DS8:POST Code LED

DS9	System LED
FAN 1-6	CPU/Chassis Fan Headers
GLAN ½	G-bit Ethernet Ports
IDE1(J44), IDE2(J38)	IDE ½ Hard Disk Drive Connectors
J1	VGA Connector
J2	Keyboard/Mouse
J10	Parallel (Printer) Header
J24	Floppy Disk Drive Connector
J28	SCSI Connector
J41	IPMI Connector
JF1	Front Control Panel Connector
JF2	PWR LED (Pins 1-3), Speaker (Pins 5-7)
JL1	Chassis Intrusion Header
JSLED	Serial ATA LED
PCI#1/PCI-E#4	PCI-#1 32-bit slot / PCI-E#4 x4 PCI-E
PCI#5/PCI#6 (J9B1/J8B1)	64-bit PCI-X 100/PCI-x 133 slot
PW3	Power SMB
PW4	PWR FAIL
SATA 0/1 (JS0/JS1)	Serial ATA0 Header (JS0), Serial ATA1 Header JS1
WOL (JWOL)	Wake-on-LAN Header
WOR (JWOL)	Wake-on-Ring Header
USB 0/1 (J3)	(Back Panel) Universal Serial Bus Ports
USB 2/3	(Front Panel) Universal Serial Bus Headers

Front Control Panel

JF1 contains header pins for various buttons and indicators that are normally located on a control panel at the front of the chassis. Refer to the following section for descriptions and pin definitions.

I/O Port Connectors

The I/O ports are colour coded in conformance with the PC 99 specification. See Figure 16 below for the colours and locations of the various I/O ports.

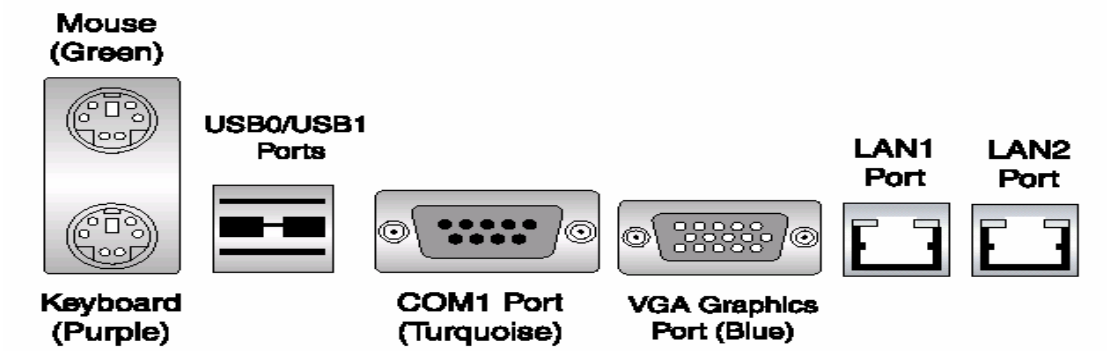


Figure 16: I/O Port Locations and Definitions

Front Control Panel Connector

JF1 contains header pins for various buttons and indicators that are normally located on a control panel at the front of the chassis. These connectors are for use with Viglen SX140 server chassis. See Figure 17 for the descriptions of the various control panel buttons and LED indicators. Refer to the following section for descriptions and pin definitions.

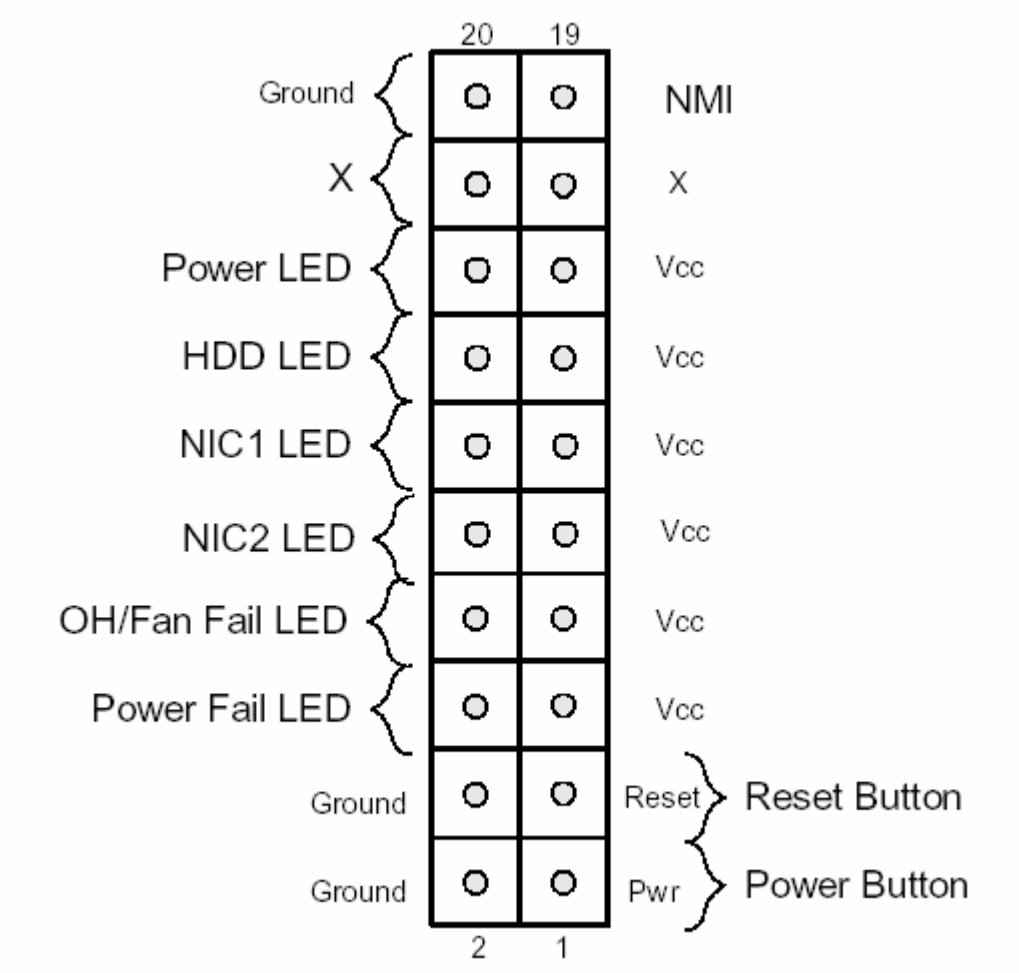


Figure 17: JF1 Header Pins

Connector Definitions

ATX Power Connection

The power supply connector on the VIG700P meets the SSI EPS 12V specification. See the table below for pin definitions.

ATX Power Supply 24-pin Connector Pin Definitions (PW1)

Pin Number	Definition	Pin Number	Definition
13	+3.3V	1	+3.3V
14	-12V	2	+3.3V
15	COM	3	COM
16	PS_ON#	4	+5V
17	COM	5	COM
18	COM	6	+5V
19	COM	7	COM
20	Res(NC)	8	PWR_OK
21	+5V	9	5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	COM	12	+3.3V

Processor Power Connector

In addition to the Primary ATX power connector (above), the 12v 8-pin Processor connector at W2 must also be connected to your power supply. See the table below for pin definitions.

CPU 8-Pin PWR Connector (PW2)

Pins	Definition
1 thru 4	Ground
5 thru 8	+12v

NMI Button

The non-maskable interrupt button header is located on pins 19 and 20 of JF1. Refer to the table below for pin definitions.

NMI Button Pin Definitions (JF1)

Pin Number	Definition
19	Ground
20	Control

Power LED

The Power LED connection is located on pins 15 and 16 of JF1. Refer to the table below for pin definitions.

PWR_LED Pin Definitions (JF1)

Pin Number	Definition
15	Vcc
16	Control

Hard Disk Drive LED

The HDD LED connection is located on pins 13 and 14 of JF1. Attach the hard drive LED cable here to display disk activity (for any hard drives on the system, including SCSI, Serial ATA and IDE). See the table below

HDD LED Pin Definitions (JF1)

Pin Number	Definition
13	Vcc
14	HD Active

NIC2 LED

The NIC (Network Interface Controller) LED connections for the GLAN port1 is located on pins 11 and 12 of JF1, and the GLAN port2 is located on pins 9 and 10 of JF1. Attach the NIC LED cables to display network activity. See the table below,

NIC1 LED Pin Definitions

Pin Number	Definition
11	Vcc
12	GND

NIC2 LED Pin Definitions

Pin Number	Definition
9	Vcc
10	GND

Overheat LED (OH)

Connect an LED to the OH connection on pins 7 and 8 of JF1 to provide advanced warning of chassis overheating. Refer to the table below for pin definitions.

OH/Fan Fail LED Pin Definitions

Pin Number	Definition
7	Vcc
8	GND

Overheat/Fan Fail LED

LED State	Message
Off	Normal
On	Overheat
Blink	Fan Fail

Power Fail Button

The Power Fail Button connection is located on pins 5 and 6 of JF1. Refer to the table below for pin definitions.

Power Fail Button Pin Definitions (JF1)

Pin Number	Definition
5	Vcc
6	GND

Reset Button

The Reset Button connection is located on pins 3 and 4 of JF1. Attach it to the hardware reset switch on the computer case. Refer to the table below for pin definitions.

Reset Pin Definitions (JF1)

Pin Number	Definition
3	Reset
4	Ground

Power Button

The Power Button connection is located on pins 1 and 2 of JF1. Momentarily contacting both pins will power on/off the system. This button can also be configured to function as a suspend button (with a setting in BIOS - see Chapter 6). To turn off the power when set to suspend mode, depress the button for at least 4 seconds. Refer to the table below for pin definitions.

Power Button Connector Pin Definitions (JF1)

Pin Number	Definition
1	PW_ON
2	Ground

Chassis Intrusion

A Chassis Intrusion header is located at JL1. Attach the appropriate cable to inform you of a chassis intrusion.

Chassis Intrusion Pin Definitions

Pin Number	Definition
1	Intrusion Input
2	Ground

Universal Serial Bus (USB0/1)

There are two Universal Serial Bus ports (USB 0/1) located on the I/O panel and additional two USB ports (USB 2/3) next to the IDE1 on the motherboard. These two FP USB ports can be used to provide front side chassis access. See the table below

USB Pin Definition

USB O/1 (Back Panel USB)

Pin#	Definition
1	+5V
2	P0-
3	P0+
4	Ground

USB 2/3 (Front Panel USB)

Pin Number	Definition	Pin Number	Definition
1	+5V	2	+5V
3	PO-	4	PO-
5	PO+	6	PO+
7	Ground	8	Ground
		10	Ground

Serial Ports

There are one Serial Port-COM1 (J4) and one Serial Header-COM2 (J5) on the VIG700P Motherboard. COM2 is located next to the parallel port.

Serial Port Pin Definitions (COM1, COM2)

Pin Number	Definition	Pin Number	Definition
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	Ground
5	Serial Out	10	NC

GLAN 1/2 (Ethernet Ports)

A G-bit Ethernet port (designated JLAN1/JLAN2) is located beside the VGA port on the IO backplane. This port accepts RJF1 type cables.

ATX PS/2 Keyboard and PS/2 mouse Ports

The ATX PS/2 keyboard and PS/2 mouse are located on J2. See the table below for pin definitions.

PS/2 Keyboard and Mouse Port Pin Definitions (J2)

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

FAN Headers

The VIG700P has six fan headers, Fan 1 to Fan 6. These fan headers are 4-pin fans. Pin 1-3 of the fan headers are backward compatible with the traditional 3-pin fans.

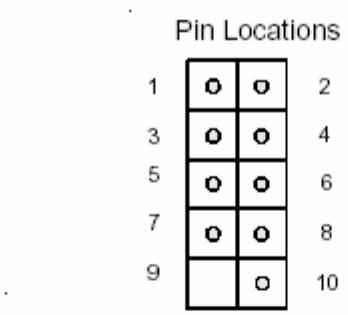
4-pin Fan Header Pin Definitions (CPU and Chassis Fans)

Pin#	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer
4	PWR_Control

Caution: These fan headers use DC power.

Speaker/Power LED/Keylock (JF2)

On the JF2 header, pins 1/3/5/7 are for the Speaker, and Pins 2/4/6 are for the Power LED and pins 8/10 are for the Keylock. Note: The speaker connector pins are for use with an external speaker. If you wish to use the onboard speaker, you should close pins 5-7 with a jumper.



Speaker Connector Pin Definitions (JF2)

Pin Number	Definition
1	Red wire, Speaker data
3	No connection
5	Key
7	Speaker data

PWR LED/Keylock Connector Pin Definitions (JF2)

Pin Number	Definition
2	+Vcc
4	-Vcc
6	-Vcc
8	Keylock
10	Keylock

Wake-On-LAN

The Wake-On-LAN header is designated WOL. See the table below for pin definitions. You must enable the LAN Wake-Up setting in BIOS to use this feature. You must also have a LAN card with a Wake-on-LAN connector and cable.

Wake-On-LAN Pin Definitions (WOL)

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake-up

Overview of Jumper Settings

The system motherboard inside your computer contains headers and jumpers. Different pin and jumper configurations make it possible to change how the computer functions. This section of the manual should give you all the information you will require making any changes.

Changes you can make, in this way, are as follows:

- Reset the CMOS RAM settings to the default values.
- Setting the Front Side Bus Speed
- Enabling or disabling SCSI termination
- Enabling or disabling the onboard Network Connector
- Selecting PCI 64-Bit bus speed

CAUTION!

Never remove jumpers using large pliers as this can damage the pins. The best way to remove a jumper is to use a small pair of tweezers or fine needle-nosed pliers.

Never remove a jumper when the computer is switched on. Always switch the computer off first.

Jumper Explanation

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the motherboard layout pages for jumper locations.

NOTE: *On two pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.*

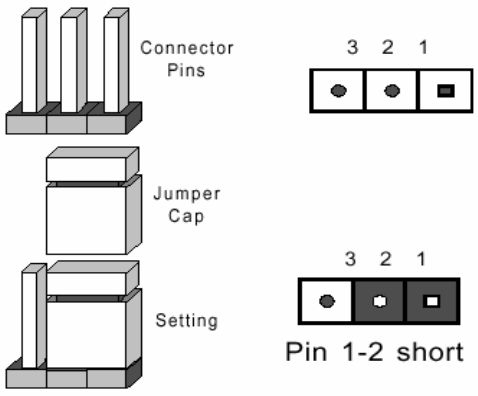


Figure 18: Server Board Jumpers

Clear CMOS

JBT1 is used to clear CMOS. Instead of pins, this "jumper" consists of contact pads to prevent the accidental clearing of CMOS. To clear CMOS, use a metal object such as a small screwdriver to touch both pads at the same time to short the connection. Always remove the AC power cord from the system before clearing CMOS.

NOTE!

For an ATX power supply, you must completely shut down the system, remove the AC power cord and then short JBT1 to clear CMOS. ***Do not use the PW_ON connector to clear CMOS.***

Figure 19: Clear CMOS Jumper

VGA Enable/Disable

JPG1 allows you to enable or disable the VGA port. The default setting is enabled. See the table below for jumper settings.

VGA Enable/Disable Jumper Settings (JPG1)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

Watch Dog Enable/Disable

JWD controls Watch Dog, a system monitor that takes action when a software application freezes the system. Pins 1-2 will have WD reset the system if a program freezes. Pins 2-3 will generate a non-maskable interrupt for the program that has frozen (requires software implementation). Watch Dog must also be enabled in the BIOS.

Watch Dog
Jumper Settings (JWD)

Jumper Position	Definition
Pins 1-2	WD to Reset
Pins 2-3	WD to NMI
Open	Disabled

SMB Data/SMB CLK to PCI

Jumpers J13, J15 allow you to connect or disconnect PCI Slot 1/PCI-X Slot 5/PCI –X Slot6 to the system Management Bus. The default setting is to close pins 1-2 to enable the connection.

PCI/PCIX slots to SMB Connection
Jumper Settings
(J13, J15)

Jumper Position	Definition
Closed	Enabled
Open	Disabled

SCSI Channel Termination Enable/Disable

Jumpers JA1 allows you to enable or disable termination for the SCSI connector. The default setting is **open** to enable (terminate) the SCSI Controller. (*Note: In order for the SCSI drives to function properly, please do not change the default setting set by the manufacturer.)

SCSI Channel Termination Enable/Disable
Jumper Settings
(JA1)

Jumper Position	Definition
Open	Enabled
Closed	Disabled

SCSI Enable/Disable

Jumper JPA1 allows you to enable or disable the SCSI Controller. The default setting is pins 1-2 to enable all four headers.

SCSI Enable/Disable Jumper Settings (JPA1)

Jumper Position	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

Alarm Reset

The system will notify you in the event of a power supply failure. This feature assumes that Super-micro redundant power supply units are installed in the chassis. If you only have a single power supply installed, you should not connect anything to this header (JPR1) to prevent false alarms. See the table below:

Alarm Reset Jumper Settings (JPR1)

Jumper Position	Definition
Open	Enabled
Closed	Disabled

Power Force-ON

Jumper JPF allows you to enable or disable the function of Power Force-On. If enabled, the power will always stay on automatically. If this function is disabled, the user needs to press the power button to power on the system.

Power Force-On (JPF)

Jumper Position	Definition
Off	Normal
On	Force On

Onboard Indicators

GLAN LEDs

The G-bit Ethernet LAN ports (located beside the VGA port) have two LEDs. The yellow LED indicates activity while the other LED may be green, orange or off to indicate the speed of the connection. See the table at right for the functions associated with the second LED.

1 Gb LAN Right LED Indicator (Speed LED)

LED Color	Definition
Off	No Connection
Green	10/100 MHz
Amber	1 GHz

1 Gb LAN Left LED Indicator(Activity LED)

LED Color	Definition
Amber	Blinking 10/100MHz/ 1GHz

SATA LED Header

A serial ATA LED header is located at JSLED. See the table below:

SATA LED Pin Definitions (JSLED)

Pin#	Definition
1	6300ESB SATA HD0 Active LED
2	6300ESB SATA HD1 Active LED
3	N/C
4	N/C
5	N/C

Onboard LED Indicators (DS1-DS5, DS7-DS8)

In addition to the LAN LEDs and the SATA LED, there are other LED indicators (DS1-DS5, DS7-DS8) on the VIG700P. DS7 and DS8 are PSOY Codes LEDs See the table below:

On board LED Pin Definitions

DS#	Definition
DS1	CPU PWR good or CPU +12V PWR Cable must be connected.
DS2	CPU2 VRM Overheat
DS3	SCSI LED
DS4	CPU1 VRM Overheat
DS5	PWR LED
DS7-8	POST LED -

System LED (DS9)

There is a system LED (DS9) on the motherboard. DS9 (System LED) indicated the status of the system. See the table below:

System Alert LED (DS9) Pin Definitions

DS9	Definition
Green	System: On & OK
Amber	System: Off, PWR Cable Connected
Red	PWR or CPU Failure, CPU Overheat

Parallel Port, Floppy/Hard Disk Drive and SCSI Connections

Note the following when connecting the floppy and hard disk drive cables:

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.

Parallel (Printer) Port Connector

The parallel (printer) port is located on J10. See the table below for pin definitions.

Parallel (Printer) Port Pin Definitions (J10)

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

Floppy Connector

The floppy connector is located on J24. See the table below for pin definitions.

Floppy Connector Pin Definitions (J24)

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

IDE Connectors

There are no jumpers to configure the onboard IDE 1 and IDE 2 connectors (at J44 and J38, respectively). See the table below for pin definitions.

IDE Connector Pin Definitions (J44, J38)

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

Ultra 320 SCSI Connectors

Refer to the table below for the pin definitions of the Ultra320 SCSI connectors located at J28.

68-pin Ultra320 SCSI Connector

Connector Contact Number	Signal Names	Connector Contact Number	Signal Names
1	+DB(12)	35	-DB(12)
2	+DB(13)	36	-DB(13)
3	+DB(14)	37	-DB(14)
4	+DB(15)	38	-DB(15)
5	+DB(P1)	39	-DB(P1)
6	+DB(0)	40	-DB(0)
7	+DB(1)	41	-DB(1)
8	+DB(2)	42	-DB(2)
9	+DB(3)	43	-DB(3)
10	+DB(4)	44	-DB(4)
11	+DB(5)	45	-DB(5)
12	+DB(6)	46	-DB(6)
13	+DB(7)	47	-DB(7)
14	+DB(P)	48	-DB(P)
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	RESERVED
20	GROUND	54	GROUND
21	+ATN	55	-ATN
22	GROUND	56	GROUND
23	+BSY	57	-BSY
24	+ACK	58	-ACK
25	+RST	59	-RST
26	+MSG	60	-MSG
27	+SEL	61	-SEL
28	+C/D	62	-C/D
29	+REQ	63	-REQ
30	+I/O	64	-I/O
31	+DB(8)	65	-DB(8)
32	+DB(9)	66	-DB(9)
33	+DB(10)	67	-DB(10)
34	+DB(11)	68	-DB(11)

Installing Software Drivers

After all the hardware has been installed you must install the software drivers. The necessary drivers are all included on the System Resource CD that comes packaged with the Viglen SX140 Server. After inserting this CD into your CD-ROM drive, the display shown in Figure 20 should appear. (If this display does not appear, click on the “My Computer” icon and then on the icon representing your CD-ROM drive. Finally, double click on the S "Setup" icon.)

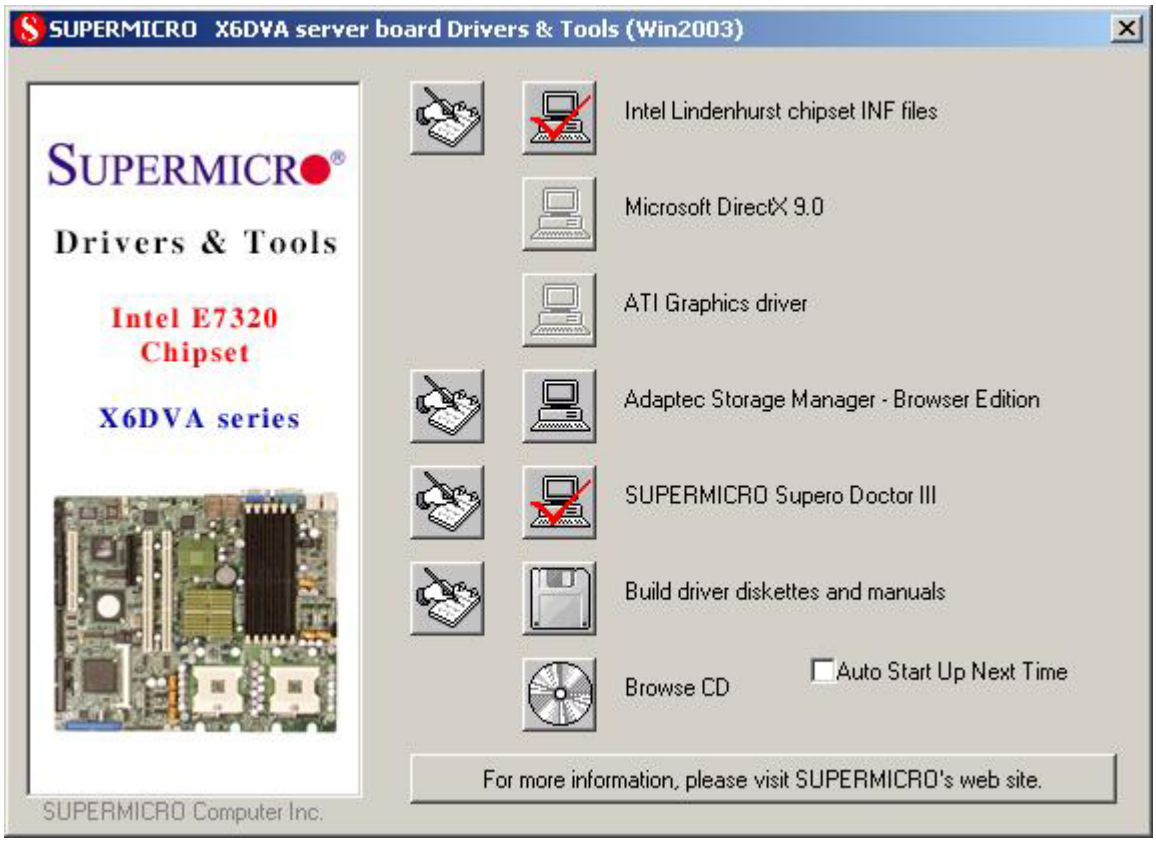


Figure 20: Driver/Tool Installation Display Screen

Click the icons showing hand writing on paper to view the readme files for each item. The bottom icon with a CD on it allows you to view the entire contents of the CD.

Please Note: he SCSI (Super) GEM Driver will be available the Viglen Server driver cd and on the Viglen FTP site ftp://ftp.viglen.co.uk

5. System BIOS

Introduction

This chapter describes the AMIBIOS for the VIG700P motherboard. The AMI ROM BIOS is stored in a Flash EEPROM and can be easily upgraded using a floppy disk-based program.

Note!

Due to periodic changes to BIOS, some settings may have been added or deleted and might not yet be recorded in this manual. Refer to the Manual Download area of our web site for any changes to BIOS that are not reflected in this manual.

System BIOS

The BIOS is the Basic Input Output System used in all IBM ® PC, XT™, AT ®, and PS/2 ® compatible computers. The BIOS ROM stores the system parameters, such as amount of memory, type of disk drives and video displays, etc. BIOS ROM requires very little power. When the computer is turned off, a back-up battery provides power to the BIOS ROM, enabling it to retain the system parameters. Each time the computer is powered-on, the computer is then configured with the values stored in the BIOS ROM by the system BIOS, which gains control when the computer is powered on.

How to Change the Configuration Data

The configuration data that determines the system parameters may be changed by entering the BIOS Setup utility. This Setup utility can be accessed by pressing <Del> at the appropriate time during system boot.

Starting the Setup Utility

Normally, the only visible POST (Power On Self Test) routine is the memory test. As the memory is being tested, press the <Delete> key to enter the main menu of the BIOS Setup utility. From the main menu, you can access the other setup screens, such as the Chipset and Power menus.

An AMIBIOS identification string is displayed at the left bottom corner of the screen, below the copyright message.

BIOS Features

- Supports Plug and Play V1.0A and DMI 2.3
- Supports Intel PCI (Peripheral Component Interconnect) (PME) local bus specification 2.2
- Supports Advanced Power Management (APM) specification v 1.1
- Supports ACPI
- Supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- Can be used as a boot device
- Is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- Chassis intrusion detector
- Five positive voltage inputs
- Three fan speed monitor inputs

Running Setup

Note!

** Optional default settings are in bold text unless otherwise noted*

The BIOS setup options described in this section are selected by choosing the appropriate text from the Standard Setup screen. All displayed text is described in this section; although the screen display is often all you need to understand how to set the options (see on next page).

The Main BIOS Setup Menu

Press the <Delete> key during the POST (Power On Self Test) to enter the Main Menu of the BIOS Setup Utility. All Main Setup options are described in this section. The Main BIOS Setup screen is displayed below.

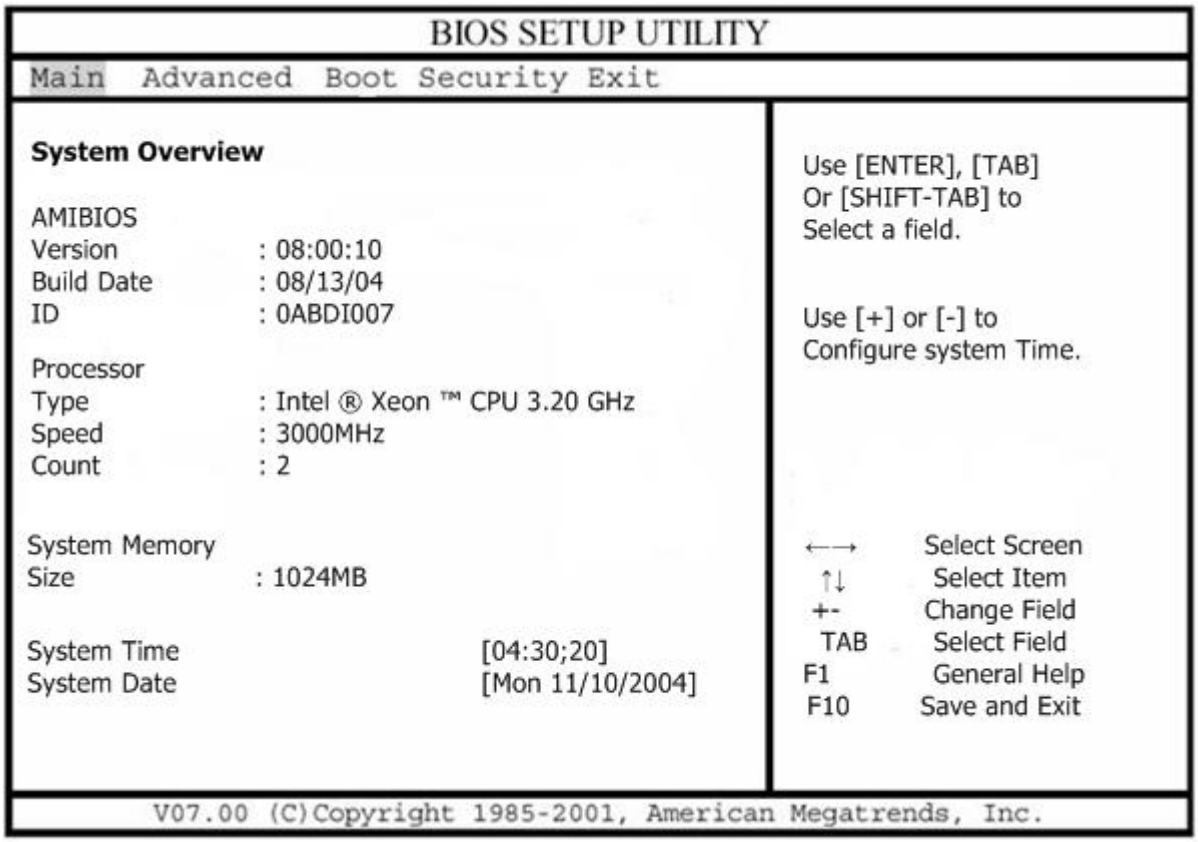


Figure 21: Main BIOS Setup Menu

Use the Up/Down arrow keys or the <Tab> key to move between the different settings in the above menu.

When the items "System Time" and "System Date" are highlighted type in the correct time/date in the time field, and then press "Enter". The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format. The time is in also 24-hour format. For example, 5:30 a.m. appears as 05:30:00 and 5:30 p.m. as 17:30:00.

Press the <ESC> key to exit the Main Menu and use the Left/Right arrow keys to enter the other categories of BIOS settings. The next section is described in detail to illustrate how to navigate through the menus.

Note!

Items displayed in gray are preset and cannot be selected. Items with a blue arrow are commands, not options (i.e. discard changes).

Advanced BIOS Setup Menu

Choose Advanced BIOS Setup from the AMIBIOS Setup Utility main menu with the Left/Right arrow keys. You should see the following display. Select one of the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub screen for that item. Advanced BIOS Setup options are displayed by highlighting the option using the arrow keys. All Advanced BIOS Setup options are described in this section.

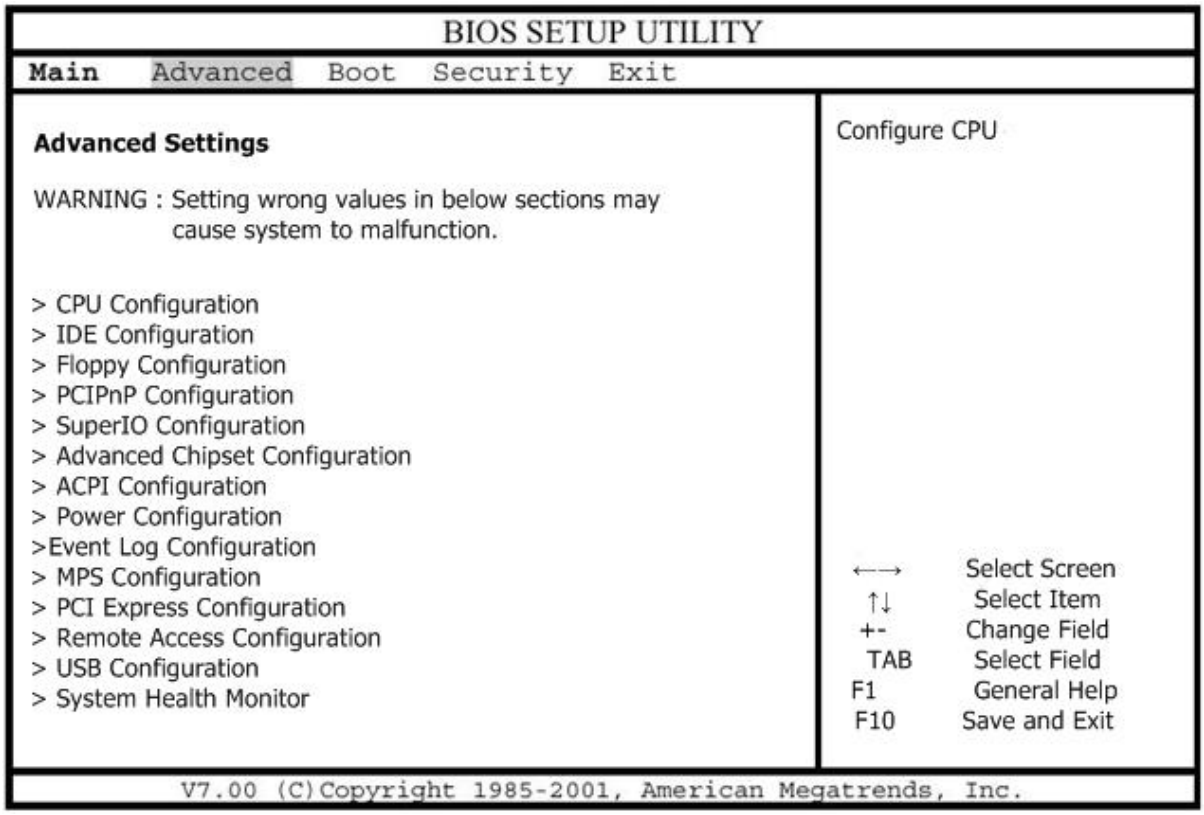


Figure 22: Advanced BIOS Setup Menu

Use the Up/Down arrow keys to select the "Super I/O Configuration line. When the "Super IO Configuration" line is highlighted, hit "ENTER" to display its menu. The following Super IO Configuration screen will appear. Here you can select your options for the computer's I/O (Input/Output) devices.

CPU Configuration Sub-Menu

Configure Advanced CPU Settings

This option allows the user to configure Advanced CPU settings for the processor(s) installed in the system.

Ratio CMOS Setting

This option allows the user to set the ratio between the CPU Core Clock and the FSB Frequency. (*Note: if an invalid ratio is entered, AMIBIOS will restore the setting to the previous state.)

Max CPUID Value Limit

This feature allows the user to set the maximum CPU ID value. Enable this function to boot legacy OS that cannot support processors with extended CPUID functions. The options are Enabled, and **Disabled**.

Hardware Prefetcher

This feature allows the user to enable the Hardware Prefetcher function. If "**Disabled**", the CPU will prefetch data at 64-bit per cache line. If "Enabled", it will fetch data at 128-bit per cache line.

Adjacent Cache Line Prefetch

This feature allows the user to enable the function of Adjacent Cache Line Prefetch. The options are Enabled and **Disabled**.

Hyper-Threading Function

This setting allows you to Enable or Disable the function of hyper-threading. Enabling hyper-threading results in increased CPU performance.

Intel® Speed Step™ Tech

This setting allows you to enable the function of Intel Speedstep Tech to set the CPU speeds. The options are: Maximum Speed, Minimum speed, Automatic **(controlled by OS)**, and Disabled.

CPU Force PR#

If Enabled, the FORCEP# will function as an input pin. If disabled, the state of FORCEPR# will be ignored by the CPU. The options are: **Enabled** and Disabled.

VRM Protection Temperature

This setting allows you to set the VRM Protection Temperature, These options are: 72°C, 88°C, **98°C**, and 108°C.

Select TM2 VID

This setting allows you to set the TM2 VID value. Enter a number from 14 to 35 to select the desired voltage value (from 1.000V to 1.2625V.)

IDE Configuration Sub-Menu

When you select this Sub-menu, AMI BIOS automatically displays the following items:

IDE Configuration

This feature allows the user to configure the IDE mode. The options are: Disabled, P-ATA (Parallel ATA) only, S-ATA (Serial ATA) only, **P-ATA & S-ATA.**

S-ATA Ports Definition

This feature allows the user to configure Serial ATA Ports. The options are: P0-Master/P1-Slave, P0-Slave/P1-Master.

Combined Mode Operation

This feature allows the user to select the IDE Combined Mode. The options are: P-ATA 1st Channel and **S-ATA 1st Channel.**

Primary IDE Master/Slave, Secondary IDE Master/Slave, Third IDE Master/Slave, Fourth IDE Master/Slave Sub-Menu

From the Advanced Setup screen, press <Enter> to access this sub menu for the primary, secondary, third and fourth IDE master and slave drives. Use this screen to select options for the Primary and Secondary IDE drives. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

TYPE

Select the type of device connected to the system. The options are Not Installed, **Auto**, CDROM and ARMD.

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. In the LBA mode, the maximum drive capacity is 137 GB. For drive capacities over 137 GB, your system must be equipped with 48-bit LBA mode addressing. If not, contact your manufacturer or install an ATA/133 IDE controller card that supports 48-bit LBA mode. The options are Disabled or **Auto**.

Block (Multi-Sector Transfer)

Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt.

Select "Disabled" to allow the data to be transferred from and to the device one sector at a time. Select "Auto" to allow the data transfer from and to the device occurs multiple sectors at a time if the device supports it. The options are **Auto** and Disabled.

PIO Mode

IDE PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The options are **Auto**, 0, 1, 2, 3, and 4. Select Auto to allow AMI BIOS to auto detect the PIO mode. Use this value if the IDE disk drive support cannot be determined. Select 0 to allow AMI BIOS to use PIO mode 0. It has a data transfer rate of 3.3 MBs. Select 1 to allow AMI BIOS to use PIO mode 1. It has a data transfer rate of 5.2 MBs. Select 2 to allow AMI BIOS to use PIO mode 2. It has a data transfer rate of 8.3 MBs. Select 3 to allow AMI BIOS to use PIO mode 3. It has a data transfer rate of 11.1 MBs. Select 4 to allow AMI BIOS to use PIO mode 4. It has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.

S.M.A.R.T. For Hard disk drives

Self-Monitoring Analysis and Reporting Technology (SMART) can help predict impending drive failures. Select "Auto" to allow BIOS to auto detect hard disk drive support. Select "Disabled" to prevent AMI BIOS from using the S.M.A.R.T. Select "Enabled" to allow AMI BIOS to use the S.M.A.R.T. to support hard drive disk. The options are Disabled, Enabled, and **Auto**.

32 Bit Data Transfer

Select "Enabled" to activate the function of 32-Bit data transfer. Select "Disabled" to deactivate the function. The options are Enabled and **Disabled**.

Hard Disk Write Protect

Select Enabled to enable the function of Hard Disk Write Protect to prevent data from being written to HDD. The options are Enabled or **Disabled**.

IDE Detect Time Out

This feature allows the user to set the time-out value for detecting ATA, ATA PI devices installed in the system. The options are 0 (sec), 5, Mode 1.0, 15, 20, 25, 30, and **35**.

ATA(PI) 80 pin Cable Detection

This feature allows AMI BIOS to auto-detect 80Pin ATA(PI) Cable. The options are: **"Host & Device"**, "Host" and "Device."

Floppy Configuration

This option allows the user to configure the settings for the Floppy Drived installed in the system.

Floppy A

Move the cursor to these fields via up and down <arrow> keys to select the floppy type. The options are Disabled, 360 KB 5 1/4", 1.2 MB 5 1/4", 720 KB 3½", **1.44 MB 3½"**, and 2.88 MB 3½".

Onboard Floppy Controller

Select "Enabled" to enable the Onboard Floppy Controller. The options are "Disabled", and "**Enabled**."

PCI/PnP Configuration

This feature allows the user to set PCI/PnP configurations for the following items:

Plug & Play OS

Select Yes to allow the OS to configure Plug & Play devices. (*This is not required for system boot if you system has an OS that supports Plug & Play.) Select **No** to allow AMIBIOS to configure all devices in the system.

PCI Latency Timer

This option sets the latency of all PCI devices on the PCI bus. The default setting is "64." Select **"32"** to set the PCI latency to 32 PCI clock cycles. Select "64" to set the PCI latency to 64 PCI clock cycles. Select "96" to set the PCI latency to 96 PCI clock cycles. Select "128" to set the PCI latency to 128 PCI clock cycles. Select "160" to set the PCI latency to 160 PCI clock cycles. Select "192" to set the PCI latency to 192 PCI clock cycles. Select "224" to set the PCI latency to 224 PCI clock cycles. Select "248" to set the PCI latency to 248 PCI clock cycles.

Allocate IRQ to PCI VGA

Set this value to allow or restrict the system from giving the VGA adapter card an interrupt address. The options are **Yes** and No.

Palette Snooping

Select Enabled to inform the PCI devices that an ISA graphics device is installed in the system in order for the graphics card to function properly. The options are Enabled and **Disabled**.

PCI IDE BusMaster

Set this value to allow or prevent the use of PCI IDE busmastering. Select "Enabled" to allow AMI BIOS to use PCI busmaster for reading and writing to IDE drives. The options are "**Disabled**" and "Enabled".

Offboard PCI/ISA IDE Card

This option allows the user to assign a PCI slot number to an Off-board PCI/ISA IDE card in order for it to function properly. The options are: **Auto**, PCI Slot1, PCI Slot2, PCI Slot3, PCI Slot4, PCI Slot5, and PCI Slot6.

IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15

This feature specifies the availability of an IRQ to be used by a PCI, PnP device. Select Reserved for the IRQ to be used by a Legacy ISA device. The options are: **Available**, Reserved.

DMA Channel 0/Channel 1/Channel 3/Channel 5/Channel 6/Channel 7

Select Available to indicate that a specific DMA channel is available to be used by a PCI/PnP device. Select Reserved, if the DMA channel specified is reserved for a Legacy ISA device.

Reserved Memory Size

This feature specifies the size of memory block to be reserved for Legacy ISA devices. The options are: **Disabled**, 16K, 32K, 64K.

Super IO Configuration Sub-Menu

Serial Port Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable. Select "3F8/IRQ4" to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. The options are Disabled, **3F8/IRQ4**, 3E8/IRQ4, 2E8/IRQ3.

Serial Port2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to "Disabled", the serial port physically becomes unavailable. Select "2F8/IRQ3" to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. The options are Disabled, **2F8/IRQ3**, 3E8/IRQ4, 2E8/IRQ3.

Parallel Port Address

This option specifies the I/O address used by the parallel port. Select Disabled to prevent the parallel port from accessing any system resources. When the value of this option is set to Disabled, the printer port becomes unavailable. Select **378** to allow the parallel port to use 378 as its I/O port address. The majority of parallel ports on computer systems use IRQ7 and I/O Port 378H as the standard setting. Select 278 to allow the parallel port to use 278 as its I/O port address. Select 3BC to allow the parallel port to use 3BC as its I/O port address.

Parallel Port Mode

Specify the parallel port mode. The options are **Normal**, Bi-directional, EPP and ECP.

Parallel Port IRQ

Select the IRQ (interrupt request) for the parallel port. The options are IRQ5 and **IRQ7**.

Advanced Chipset Settings

This item allows the user to configure the Advanced Chipset settings for the system.

NorthBridge Configuration

This feature allows the user to configure the settings for Intel Lindenhurst NorthBridge chipset.

Memory Remap Feature

Select Enabled to allow remapping of overlapped PCI memory above the total physical memory. The options are **Enabled** and Disabled.

Memory Mirroring/Sparing

This feature allows the user to enable the function of Memory Mirroring and Sparing if memory configuration supports this function the options are **Disabled** and Sparing.

SouthBridge Configuration

This feature allows the user to configure the settings for Intel ICH SouthBridge chipset.

CPU B.I.S.T. Enable

Select Enabled to enable the function of CPU Built In Self Test. The options are Enabled and **Disabled**.

ICH Delayed Transaction

Select Enabled to enable the function of ICH Delayed Transaction. The options are **Enabled** and Disabled.

ICH DCB

Select Enabled to enable the function of ICH DCB. The options are **Enabled** and Disabled.

Onboard AC97

Select Auto to allow the Onboard AC97 Audio to be automatically activated. The options are **Auto** and Disabled.

Intel PCI-X Hub Configuration

This feature allows the user to configure the settings for Intel PCI-X Hub chipset.

PXH Channel A/Channel B Bus Frequency

This feature allows the user to set the maximum PCI bus speed to be programmed. The options are Auto, 33MHz PCI, 66MHz PCI, 66MHz PCI-X M1, 100MHz PCI-X M1, and 133MHz PCI-X M1. The default setting for PCI-X CHA is 100MHz PCI-X M1. The default setting for PCI-X CHB is 133MHz PCI-X M1.

I/O Port decode

Select the decode range for IO. The options are **4K Decode** and 1K Decode.

RAS Sticky Error Handling

Select the method for AMI BIOS to handle Sticky RAS Errors. The options are **Clear Errors** and Leave Errors.

VGA 16-bit Decode

Select Enabled to enable the function of decoding of VGA for the devices installed behind PHX. The options are **Enabled** and Disabled.

PCI-X Slot5/Slot6 Option ROM

Select Enabled to enable the function of Option ROM for PCI-X Slot5/Slot6. The options are **Enabled** and Disabled.

ACPI Configuration

This item allows the user to enable or disable ACPI support for the operating system.

ACPI Configuration

Use this feature to configure additional ACPI options. Select "Yes" if the operating system supports ACPI. Select No if the operating system does not support ACPI. The options are No and **Yes**.

ACPI 2.0 Features

Select Yes to allow RSDP pointers to point to the 64-bit Fixed System Description Tables. Select No to deactivate this function. The options are Yes and **No**.

ACPI APIC Support

Select Enabled to allow the ACPI APIC Table Pointer to be included in the RSDP pointer list. The options are **Enable**, and Disabled.

AMI OEMB Table

Select Enabled to allow the OEMB Table Pointer to be included in the R(x)SDT pointer lists. The options are **Enabled**, and Disabled".

Headless Mode

Select Enabled to activate the Headless Operation Mode through ACPI. The options are Enabled, and **Disabled**.

Power Configuration

This feature allows the user to configure PnP settings.

Restore on AC Power Loss

This setting allows you to choose how the system will react when power returns after an unexpected loss of power. The options are Stay Off, Power On and **Last State**.

Watch Dog Timer

This setting is used to enable or disabled the Watch Dog Timer function. It must be used in conjunction with the WD jumper (see Chapter 2 for details). The options are **Disabled** and Enabled.

Event Logo Configuration

Highlight this item and press <Enter> to view the contents of the event log.

View Event Log

This feature allows the user to view all unread events.

Mark All Events as Read

Highlight this item and press <Enter> to mark the DMI events as read.

Clear Event Log

This setting will clear all event logs when set to "OK". The options are "OK" and **"Cancel"**.

ECC Event Logging

This setting allows you to enable or disable ECC Event logging. The options are Enabled or **Disabled**.

Hub Interface Event Logging

This setting allows you to enable or disable Hub Interface Event logging. The options are Enabled or **Disabled**.

System Bus Event Logging

This setting allows you to enable or disable System Bus Error Event logging. The options are Enabled or **Disabled**.

Memory Buffer Event Logging

This setting allows you to enable or disable Memory Buffer Event logging. The options are Enabled or **Disabled**.

PCI/PCI Express Error Logging

This setting allows you to enable or disable PCI or PCI Express Error logging. The options are Enabled or **Disabled**.

MPS Configuration

This section allows the user to configure the multiprocessors table.
MPS RevisionThis feature allows the user to select MPS Revision. Please follow the instructions given on the screen to select the MPS Revision Number. The options are 1.1 and **1.4.**

PCI Express Configuration

This section allows the user to configure PCI Express slots.

Active State Power Management

Select Enabled to activate the function of power management for signal transactions between PCI Express L0 and L1 Link. The options are Enabled and **Disabled**.

I/O Expander Mode

This feature allows the user to set the IO Expand Mode for Hot Plug support. The options are **PCA9555,** Two PCA9554, One PCA9554 (Low), One PCA9554 (High), Two PCA9554A, One PCA9554A (Low), and Two PCA9554.

PCI Express Port2 (PXH)

This feature allows the user to configure the PCI Express slot. The options are Auto, **Enabled**, and Disabled.

PCI Express Port3 (Slot 4)

This feature allows the user to configure the PCI Express slot. The options are Auto, **Enabled**, and Disabled.

PCI Express Compliance Mode

Select Enabled to enable MCH to activate PCI Express Compliance Mode.The options are **Disabled** and Enabled.

Spread Spectrum

Select Enabled to enable Spread Spectrum. The options are **Disabled** and Enabled.

Remote Access Configuration

You can use this screen to select options for the Remote Access Configuration. Use the up and down <Arrow> keys to select an item. Use the <Plus> and <Minus> keys to change the value of the selected option.

Remote Access

This feature allows the user to disable the function of Remote Access. If Disabled is not select, then you can select a Remote Access type. The options are Enabled and **Disabled**.

USB Configuration

This feature allows the user to configure USB settings.

USB Function

This feature allows you to enable 2 USB Ports or 4 USB Ports. The options are Disabled, 2 USB Ports, and **4 USB Ports**.

Legacy USB Support

Select "Enabled" to enable the support for USB Legacy. Disable legacy support if there are no USB devices installed in the system. The options are Disabled, **Enabled** and Auto.

USB 2.0 Controller

This setting allows you to enable or disable USB 2.0 Controller. The options are Disabled and **Enabled**.

USB 2.0 Controller Mode

This setting allows you to configure USB 2.0 Controller Mode. The options are **Hi-Speed (480 Mbps)** and Full Speed-(12Mbps). This feature allows you to enable 2 USB Ports or 4 USB Ports. The options are Disabled, 2 USB Ports, and **4 USB Ports**.

System Health Monitor

This feature allows AMI BIOS to automatically display the status of the following items:

System Health Function

Select "Enabled" to enable the function of Hardware Health Monitoring Device. The Options are "**Enabled**" and "Disabled".

CPU Temperature

The feature allows the user to set the CPU temperature threshold. The options range from 65°C to 90°C. The default setting is "**78°C**. If System Health Function is enabled, BIOS will automatically display the status of the following items:

CPU1 Temperature, CPU2 Temperature, System Temperature

AMI BIOS will automatically display the following information:

CPU1 VCORE/CPU2 VCORE (*for 2U systems),

3.3V Vcc(V), +5 Vin, 12V Vcc(V), -12V Vcc (V), DRAM VTT, 1.2V Vcc, 2.5V for DIMM, 1.5V Standby Power, 5V Standby, 3.3V Standby.

Fan Speed Control Modules:

This feature allows the user to decide how the system controls the speeds of the onboard fans. If the option is set to "3-pin fan", the fan speed is controlled based upon the CPU die temperature. When the CPU die temperature is higher, the fan speed will be higher as well. If the option is set to "4-pin", the fan speed will be controlled by the Thermal Management Settings pre-configured by the user at this feature. Select "3-pin" if your chassis came with 3-pin fan headers. Select "4-pin" if your chassis came with 4-pin fan headers. Select "Workstation" if your system is used as a Workstation. Select "Server" if your system is used as a Server. Select "Disable" to disable the fan speed control function to allow the onboard fans to run at the full speed (12V) at all time. The Options are: **1. Disable,** 2. 3-pin (Server), 3. 3-pin (Workstation), 4. 4-pin (Server), 5. 4-pin (Workstation). **Fan1 Speed to Fan6 Speed**

Boot Setup menu

Choose Boot Setup from the AMIBIOS Setup main menu. All Boot Setup options are described in this section. The Boot Setup screen is shown below.

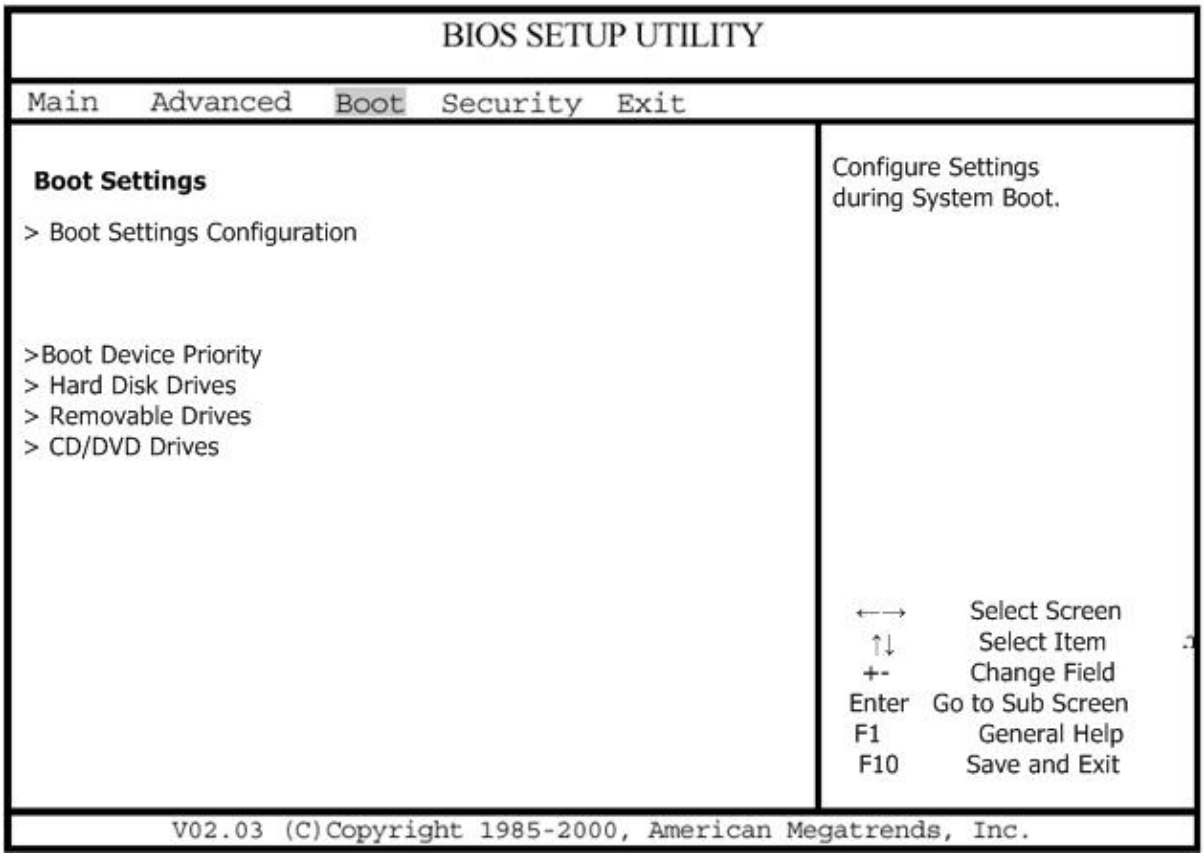


Figure 23: Boot Setup Menu

BIOS Settings Configuration

Quick Boot

If Enabled, this option will skip certain tests during POST to reduce the time needed for the system to boot up. The options are **Enabled**, and Disabled.

Quiet Boot

Set this value to allow the boot up screen options to be modified between POST messages or OEM logo. The default setting is **Enabled**. Select Disabled to allow the computer system to display the POST messages. Select Enabled to allow the computer system to display the OEM logo.

Add-On ROM Display Mode

Set this option to display add-on ROM (read-only memory) messages. The default setting is **Force BIOS**. Select "Force BIOS" to allow the computer system to force a third party BIOS to display during system boot. Select "Keep Current" to allow the computer system to display the BIOS information during system boot. The options are Force BIOS and Keep Current.

Boot up Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up. The default setting is **On**. The options are On and Off.

PS/2 Mouse Support

Set this value to allow the PS/2 mouse support to be modified. The options are **Auto**, Enabled and Disabled.

Wait for 'F1' If Error
Select Enable to activate the function of Wait for F1 if Error. The options are **Enabled** and Disabled.

Hit 'DEL' Message Display
Select Enabled to display Setup Message when the user hits the DEL key. The options are **Enabled** and Disabled.

Interrupt 19 Capture
Select Enabled to allow ROMs to trap Interrupt 19. The options are Enabled and **Disabled**.

Boot Device Priority

This feature allows the user to specify the sequence of priority for the Boot Device.

The settings are "1st Floppy Drive", "CD ROM", "ATAPI CDROM", and "Disabled."

The default settings are:

1st boot device – Floppy Drive

2nd boot device – S1 MPI Boot Support

3rd boot device – SATA0-#0 Mirror

4th boot device – IBA GE Slot 0508V

5th boot device – IBA GE Slot 0510V

Hard Disk Drives

This feature allows the user to specify the Boot sequence from available Hard Drives.

1st Drive/2nd Drive/3rd Drive

Specify the boot sequence for 1st Hard Drive, 2nd Hard Drive, and 3rd Hard Drive. The options are HDD and Disabled.

Removable Drives

This feature allows the user to specify the Boot sequence from available Removable Drives.

1st Drive

Specify the boot sequence for 1st Removable Drive. The Options are **1st Floppy Drive** and Disabled.

CD/DVD Drives
This feature allows the user to specify the boot sequence from available CDROM Drives.

1st Drive
Specify the boot sequence for 1st Hard Drive. The options are **CD ROM** and Disabled.

Security Setup Menu

Choose Security Setup from the AMIBIOS Setup main menu. All Security Setup options are described in this section. The Security Setup screen is shown below.

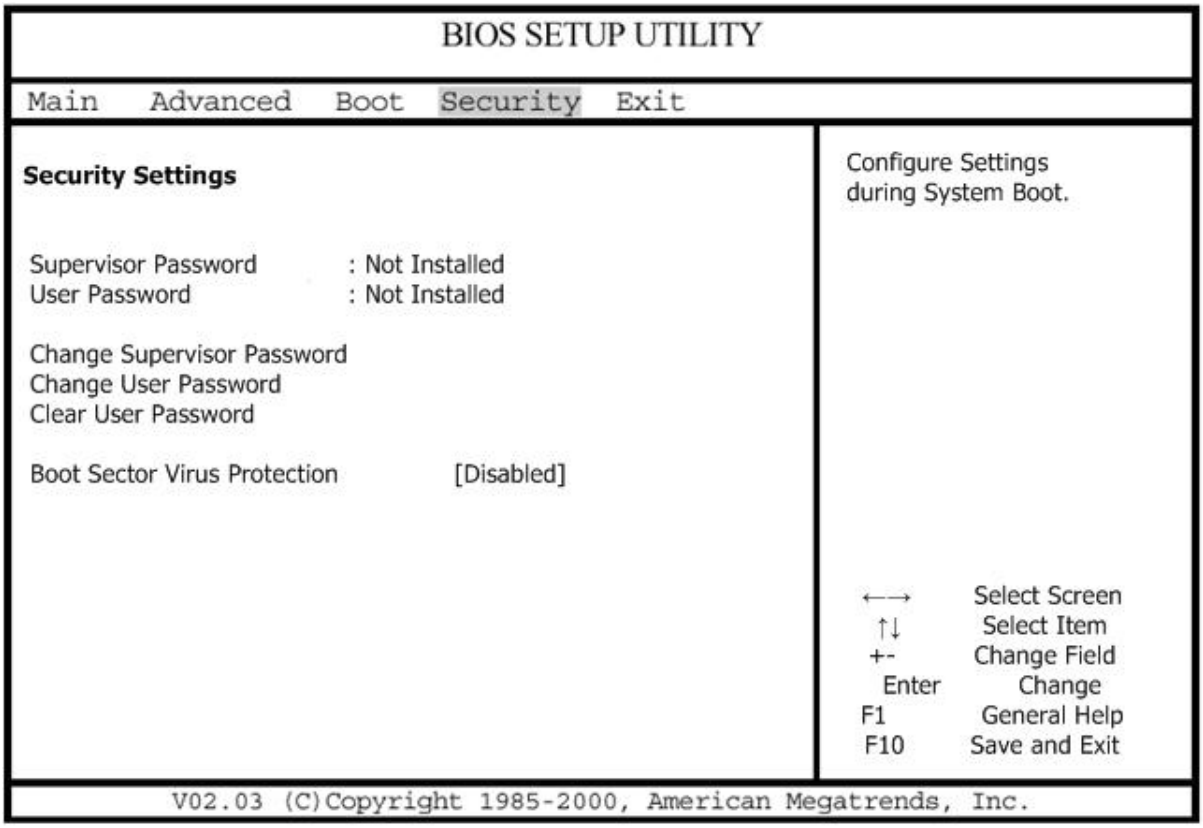


Figure 24: Security Setup Menu

Change Supervisor Password & User Password

AMIBIOS provides both Supervisor and User password functions. If you use both passwords, the Supervisor password must be set first. The system can be configured so that all users must enter a password every time the system boots or when AMIBIOS Setup is executed, using either or both the Supervisor password or User password. The Supervisor and User passwords activate two different levels of password security. If you select password support, you are prompted for a 1 – 6 character password. Type the password on the keyboard. The password does not appear on the screen when typed. Make sure you write it down. If you forget it, you must clear CMOS and reconfigure. **Remember your Password!** Keep a record of the new password when the password is changed. If you forget the password, you must erase the system configuration information in CMOS.

Change Supervisor Password

This option allows you to change a supervisor password that was entered previously.

Change User Password

This option allows you to change a user password that was entered previously.

Clear User Password

Use this option to clear the user password so that it is not required to be entered when the system boots up.

Boot Sector Virus Protection
This option allows you to enable or disable a virus detection program to protect the boot sector of your hard disk drive. The settings for this option **Disabled** and Enabled. If Enabled, AMIBIOS will display a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

Exit Setup Menu

Choose Exit Setup from the AMIBIOS Setup main menu. All Exit Setup options are described in this section. The Exit Setup screen is shown below.

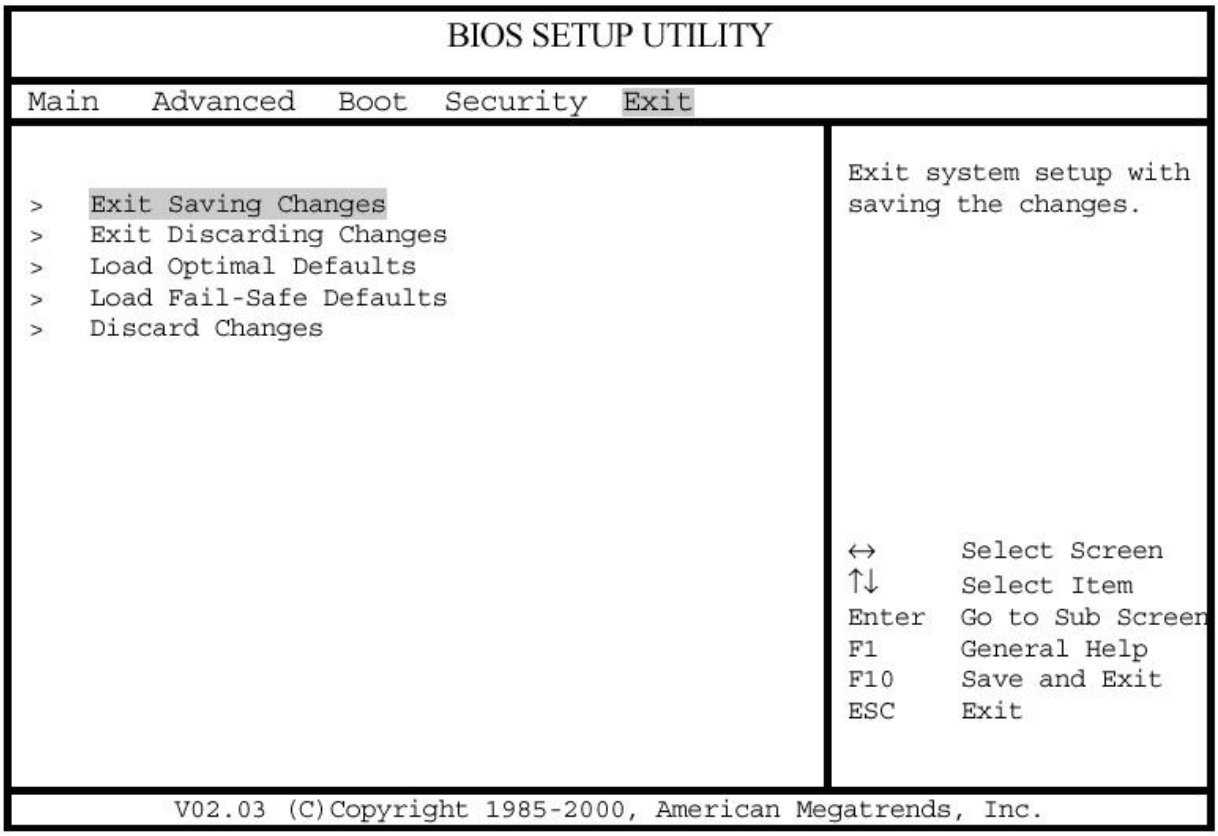


Figure 25: Exit Setup Menu

Exit Saving Changes

Highlighting this setting and then pressing <Enter> will save any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

Exit Discarding changes

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program and then exit. Your system should then continue with the boot up procedure.

Load Optimal Defaults

Highlighting this setting and then pressing <Enter> provides the optimum performance settings for all devices and system features.

Load Failsafe Defaults

Highlighting this setting and then pressing <Enter> provides the safest set of parameters for the system. Use them if the system is behaving erratically.

Discard Changes

Highlighting this setting and then pressing <Enter> will ignore any changes you made in the BIOS Setup program but will not exit the BIOS Setup program

6. Appendices

Appendix A: BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors. POST codes may be read on the debug LEDs located beside the LAN port on the motherboard backplane.

A1 AMIBIOS Error Beep Codes

Beep Code	Error Message	Description
1 beep	Refresh	Circuits have been reset. (Ready to power up.)
5 short, 1 long	Memory error	No memory detected in the system.
8 beeps	Display memory read/write error	Video adapter missing or with faulty memory.

A2 DS7/DS8 LED Post Codes

LED Indicators		Description/Message
DS7	DS8	
On	On	PWR On
On	Off	SPD Read OK
Off	On	Memory Size-OK
Off	Off	Starting Bus Initialization

Appendix B: BIOS POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes checkpoint codes to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h.

B-1 Uncompressed Initialization Codes

Checkpoint	Code Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the Stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Controls in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. otherwise, going to checkpoint code D7h.

B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint	Code Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling interna cache memory.
Edh	Initializing the floppy drive.
Eeh	Looking for a floppy diskette in drive A:. Reading the first sector o the diskette.
Efh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution.
These codes are uncompressed in F0000h shadow RAM.

Checkpoint	Code Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required

	initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the *Initialize CMOS RAM in every boot* AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.

Checkpoint	Code Description
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices will be done next, if present. See the last page for additional information.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/ write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information.
39h	Displaying bus initialization error messages. See the last page of this chapter for additional information.
3Ah	The new cursor position has been read and saved. Displaying the *Hit <DEL>* message next.
3Bh	The *Hit <DEL>* message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.

Checkpoint	Code Description
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the *Hit <DEL>* message next.
59h	The *Hit <DEL>* message is cleared. The *<WAIT...>* message is displayed. Starting the DMA and interrupt controller test next.

Checkpoint	Code Description
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message has been displayed. The <*WAIT...*> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.

Checkpoint	Code Description
95h	Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
Aah	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
Abh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

Appendix C: Glossary

A	Ampere, This is a term of measurement for electric Current.
AC	Alternating Current used to describe the mains voltage.
Ampere	This is a term of measurement of electric current.
Analog	Pertaining to data in the form of continuously variable quantities. Contrasts with Digital.
ANSI	American National Standards Institute.
ASCII	American Standard Coded for Information Interchange. This is a special 7/8 bit code that is given to identify characters.
Asynchronous	a Method of transmission of data in which the bits included in a character or block of characters occur during a specific time interval. The start of each character block can occur at any time during this interval. Contrasts with synchronous.
AUTOEXEC.BAT	A special batch file, which contains a series of commands that are to be executed when the computer is started up.
BASIC	Beginner's All-purpose Symbolic Instruction Code. This is a simple programming language.
Battery-Backed RAM	A type of memory that holds information even when the computer is switched off.
Baud	A term used to measure modem data rates.
Binary	Involving a choice of two conditions, such as "yes" or "no", "1" or "0", base-2 mathematics.
BIOS	Basic Input Output System. This is the program held in the computer's ROM which handles all the input and output functions.
Bit	Synonym for Binary digit. A single unit of information which can hold a value of 0 or 1.
Boot	The name given to the program that runs on the computer when it is first switched on. Can also be a verb related to running the program.

BSI	British Standards Institute.
Bps	Bits per second.
Buffer	An area of temporary storage.
Bus	One or more conductors used for transmitting signals.
Byte	A unit of data made up of eight Bits.
C / C++	A programming language.
Cache	A small area of high-speed memory.
Cathode Ray Tube (CRT)	Normally referred to as a monitor or VDU.
Character	A symbol on the screen or same as a Byte.
CMOS	Complementary Metal Oxide Semiconductor. A logic circuit family that uses very little power.
COM1, COM2 COM3, COM4	The names given to the serial communications ports in DOS.
CONFIG.SYS	A special purpose file which has the configuration details for the computer to set itself to when powered up.
CPS	Characters per second.
CSA	Canadian Standards Association.
Cursor	A bar on the screen that indicates where the input from the keyboard will be displayed.
DC	Direct current. Normally associated with battery current.
Digital	Pertaining to data in the form of binary digits. Contrasts with Analogue.
DIN	Deutsche Industrie Norm specifies major connector types.
DIP	Dual In-Line Package. ICs that have two parallel rows of connections.
DMA	Direct Memory Access. A method of transferring data between main storage and I/O devices without processor intervention.

Disk	See Floppy Disk.
DOS or MS-DOS®	Disk Operating System or Microsoft® Disk Operating System. This is a low-level program that instructs the computer on basic file handling.#
DRAM	Dynamic RAM. A type of RAM that requires a periodic refresh to maintain data.
DVD	Digital Versatile Disk
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference.
EPROM	Erasable Programmable Read-Only Memory.
ESDI	Enhanced Small Device Interface, which specifies a fast hard disk interface.
FCC	Federal Communications Commission.
Firmware	A program that is resident in Read Only Memory (ROM).
Floppy Disk	A storage device consisting of a flexible magnetic disk inside a protective cover.
G	A symbol used to represent the prefix Giga. i.e. GB (Giga Byte).
GB	Gigabyte, represents 1,073,741,824 bytes (1024MB).
Hard Disk	A disk of rigid magnetic material used for mass storage.
Hardware	The physical equipment which makes up the computer system.
Hertz (Hz)	A unit of measurement of frequency amounting to one cycle per second.
Hex	Hexadecimal. Base-16 mathematics.
IC	Integrated Circuit.
Icon	A graphical symbol.
IDE	Integrated device interface. An AT bus specification for a fast hard disk.

IEC	International Electrotechnical Commission. Specifies standards of safety.
I/O	Input/Output. Refers to data being sent to or received from a computer.
K	Symbol used to represent Kilobyte which is 1024 bytes.
KB	Abbreviation for Kilobyte, i.e. 1024 bytes.
Kb	Abbreviation for Kilo bit, i.e. 1024 bits.
Keylock	A locking device which can deactivate a keyboard.
KHz	KiloHertz. 1000 Hertz.
LIM	Lotus/Intel/ Microsoft® Expanded Memory Manager specification.
LED	Light Emitting Diode. These are normally used as the lights on a computers front panel.
LPT1, LPT2, LPT3	Names given to the printer ports by DOS.
M	Prefix mega. Equivalent to 1024K.
mA	Milliampere. 0.001 Ampere.
MB	Abbreviation for Mega Byte i.e. 1024K Bytes.
Mb	Abbreviation for Mega Bits, i.e. 1024K bits.
Memory	An electronic component, which remembers data, stored in it.
MHz	Mega Hertz. 1,000,000 Hertz.
ns	Nano Second 0.000 000 001 second.
Pixel	The smallest displayable unit on a monitor or picture tube.
POST	Power-On Self Test.
RAM	Random Access Memory. Fast Read/Write memory.
RFI	Radio Frequency Interface.

ROM	Read Only Memory.
RS-232C	A standard for asynchronous serial communication.
SCSI	Small Computer Systems Interface. A multimedia bus and interface specification for fast Hard Disks, Tape Backup Units, CD ROMs and other Devices.
SIMM	Single In-Line Memory Module.
Software	Another name for a computer program.
SRAM	Static RAM. Synchronous Transmission of data between devices which are maintaining the same frequency relationship. Contrasts with asynchronous.
TPI	Tracks Per Inch.
TTL	Transistor Transistor Logic.
TUV	Technischer Uberwachungs-Verein. Organisation which tests and certifies electronic equipment.
UL	Underwriter Laboratories. American Organisation specifying standards for safety of electronic equipment.
USB	Universal Serial Bus
V	Volt. Unit of measurement of potential difference.
VAC	Volts (Alternating Current).
VDE	Verband Deutscher Electrotechniker. German organisation specifying EMI suppression.
Video	Computer data or graphics displayed on a monitor or screen.
W	Watt.
Watt	Basic unit of measurement of electrical power.

Appendix D: Notes

Appendix E: Suggestions

Viglen is interested in continuing to improve the quality and information provided in their manuals. Viglen has listed some questions that you may like to answer and return to Viglen. This will help Viglen help to keep and improve the standard of their manuals.

1. Is the information provided in this and other manuals clear enough?

2. What could be added to the manual to improve it?

3. Does the manual go into enough detail?

4. Would you like an on-line version of this manual?

5. How do you rate the Viglen Technical support and Service Departments?

6. Are there any technological improvements that could be made to the system?

1. Other points you would like to mention?

Please return this slip to: Product Development Department
Viglen Ltd
Viglen House
Alperton Lane
Alperton
Middlesex
HA0 1DX