MINOS Far Detector Electronics
- User's Manual –

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1 Overview

1.1 General Description

The MINOS Far Detector Electronics readout architecture makes inherent use of the low rate environment of the Far Detector. The signal rate is expected to be dominated by dark noise from the photomultipliers which is specified to be less than 1 kHz per PMT on average. Given this low data rate, reasonably high speed digitizers residing on VME boards can be allocated to many PMTs and still operate with very low dead time.

The readout is based on the multi-channel VA chip series from IDE Corp. (Oslo, Norway). This chip provides a charge sensitive preamplifier, a shaper, sample/hold for each channel and is followed by an analog output multiplexer. The VA chip series was originally designed and used for silicon detectors with the per channel circuitry constructed on 42 micron pitch to match the 50 micron pitch of a typical silicon detector. Versions have been constructed with 128, 64, and 32 channels per chip. The MINOS Far Detector uses a 32 channel version optimized for our particular constraints. One such chip is used for each PMT. Triggering is based on the common dynode signal of the PMT. Thus each PMT provides a single trigger signal in common to all anodes.

The readout is organized into VA Frontend Boards (VFBs) and VA Readout Controllers (VARCs). The VFBs reside on the muxboxes while the VARCs are located in VME crates in electronics racks some distance away. The VFBs house three VA chips and their associated support circuitry. No digitization nor digital control takes place on the VFB.

Signal digitization, trigger time-stamping, and control of the VA devices take place on the VARC. All analog portions of the VARC including signal receiving and digitization take place on VARC Mezzanine Modules (VMMs). One VMM services two VFBs. The VARC contains up to six VMMs and can thus service up to 36 PMTs or 576 pixels.

A block diagram of the readout structure is shown below in Figure 1.

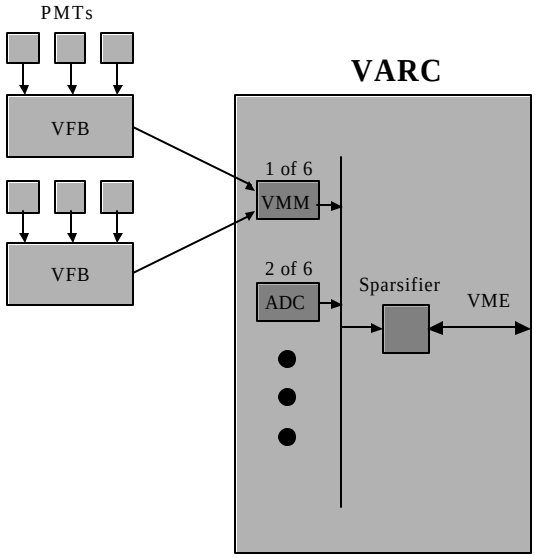


Figure 1-Readout Architecture

Analog, trigger, and control signals are transmitted between the VFBs and VARCs on cables of approximately 26' in length. All signals are differential. The analog signal is transmitted on a low loss shielded twisted pair, while the trigger and control signals use a miniature twist and flat. For reasons of cable length limitation, only three VARCs are housed in each of the 16 distributed readout crates. Thus there are 48 VARCs in the readout system.

There are two levels of sparsification in the readout. The first level is the common dynode signal discriminator threshold. This is an analog level which can discriminate single photoelectrons but is subject to the wide pixel to pixel gain variations. The second level is done in the VARC after digitization and is on a per pixel basis after all pixel gains have been calibrated.

1.2 Front End Specification

1.2.1 PMT specs

Nominal PMT Gain	$1 \cdot 10^6$
PMT gain spread	3:1
Single pe signal - Anode	-160 fc nominal (-53 fc min)
Max signal	200 pe → 32 pcoul
Dynamic range requirement [see below]	12.5 bits
Single pe signal – Dynode	+80 fc max (+27 fc min)

1.2.2 Dynamic Range

Dynamic range requirement is estimated as follows. In order to get good efficiency for accepting single photoelectrons, we need to set a threshold of 1/3 pe. The noise level, in turn, must be 1/3 of the threshold or 1/9 pe. Ignoring pixel gain variations, this would imply dynamic range requirement of 1,800:1. If we include factor of 3 for pixel gain variation, this brings the requirement up to ~ 5400:1 or just over 12 bits. Erring on the conservative side, we set the goal at ~6000:1 or 12.5 bits. Using a 14 bit ADC, this implies a pedestal width of ~2.7 ADC counts with full scale signal of 200 photoelectrons.

1.2.3 Dead Time

Dead time is estimated as follows. The PMTs on average deliver 1 kHz of triggers due to dark noise each. It takes of order 5 -10 μs to completely read out each of the VA chips, thus if one ADC were allocated to each VA chip, the deadtime would be 0.6%-1%. Each ADC is, however, allocated to six VA chips. The VARC handles this by queuing trigger requests received while already processing a trigger. Thus no additional deadtime is incurred.

2 PMT Base

2.1 Introduction

The MINOS experiment uses two types of multi-anode phototubes (PMTs). The two supermodules of the Far detector will be equipped with 1,452 16-anode R5900-00-M16 PMTs, the Near detector will have 225 64-anode R5900-00-M64 PMTs, both manufactured by Hamamatsu Photonics K. K., Japan (1). All PMTs will be biased and read out by bases designed by MINOS. In this note we document the design and operational principles behind the bases for M16 PMTs.

The M16 base was designed by Joe Ting and John England of The University of Texas (2). The printed circuit boards for these bases were manufactured by Grande Industries (3), the microcomponents were installed by Texatronics Inc. (4), all the testing of the bases was performed by the technical staff and undergraduates at the University of Texas.

2.2 General description of M16 and the base

The M16 PMT is housed in a glass-KOVAR casing. The flat glass window and the photocathode is about 2.5 cm square. The 16 anodes (or pixels) are arranged in a 4mm x 4mm grid. A common set of metal channel dynodes allows a single resistor chain for biasing. M16 has 12 dynodes that must have increasing positive voltages starting from the photo-cathode to the anodes. The manufacturer's recommendation and extensive tests by MINOS led to the choice of the ratio of resistors which optimizes the gain and linearity range for M16 PMTs (5). The ratio of resistor values from the photocathode to the anode is as follows:

$$2.4 : 2.4 : 2.4 : 1 : 1 : 1 : 1 : 1 : 1 : 1 : 1 : 1.2 : 2.4$$

The value of (1) is set at 100kΩ and gives a bias current of ~ 500μA at maximum voltage of 1000 volts. The total resistance of the base is 1.9 MΩ.

The base design has evolved to a two-board circuit. One board is used for biasing components, and the other is used for the anode signals and for the connector receptacles. The larger board measures about 3 inches by 1.9 inches, and is known as the signal board. The other is 1.9 inches by 1.1 inches, and is called the bias board. The signal board has "Mill-Max" pin receptacles for the PMT, also two "header" connectors for the anode signals. The protection diodes are also included on this board, and also a coupling capacitor to Dynode 12. The anode signals use short pin receptacles, while the bias connections use long pin receptacles, which connect the two boards. Nylon spacers are

used to separate the boards, and are placed over the "near ground" pins and the "high voltage" pin. The 20-pin connectors each have 8 anode signals, and the D12 signal is connected to pin 1 of connector "1".

2.3 Bias board

The bias components are placed on the top surface of the bias board so that repairs can easily be made. The components are vulnerable to damage from careless handling, but the boards are ultimately installed into light tight MUX boxes for the duration of the experiment.

The supply for the base is a negative voltage of less than 1000 volts. The connector for this high voltage is a "4 pin header" connector, and only the end pins are used. The high voltage supply is limited with a small resistor of 10kΩ, and then decoupled with a capacitor, (1000 pF, 2000 volts).

A 1 MΩ resistor is used in series with the photo-cathode, to limit the maximum current flow. The resistor does not affect normal operation, as only a few electrons are produced by the action of a photon striking the photo-cathode. Additional resistors are added in series with dynodes D10, D11, and D12. These resistors have values of 50, 50, 500Ω, respectively. Small capacitors are connected across resistors R11, R12, and the series combination of R13 and R14. The capacitors are 0.01μF and are rated for at least 200 volts. They are included to stabilize the voltages at dynodes D10 and D11, which may vary when photons are detected. The anodes are normally operated at close to ground potential, but it is very important that voltages remain low, when the PMT is connected to the detector amplifiers. This is achieved by connecting reverse biased diodes to each anode. The "reverse bias" voltage is generated, by including a 10kΩ resistor in the bias resistor chain. This produces about –5 volts, and this is connected to the anode of each low leakage diode. The cathode of this diode is connected to each anode of the PMT. The 10KΩ resistor is bypassed with a 0.047-uF capacitor, to stabilize the "reverse bias" voltage.

2.4 Connector board

The MUX box contains 3 PMT assemblies, and the signals from these boards are directed to the amplifiers through an intermediate connector board. This board is about 5.7 inches by 3 inches, and has 6 "20-pin header" connectors on the input side, and 3 "40-pin stacker" connectors on the output side. The board is constructed of black FR-10 material and is made light proof by means of a gasket and black epoxy.

2.5 SHV board

The high voltage connects to PMTs housed in a MUX through an SHV board. It is a 9.5 cm by 4.5 cm board made out of black FR-10 material with 3 SHV bulkhead connectors mounted in punched D-type holes. In compliance with the grounding convention adopted by MINOS these connectors are insulated from the body of a MUX box and are connected to it via a 1kΩ resistor which also breaks the cable's ground continuity.

2.5.1 Schematic and layout drawings

See MINOS Far Detector Electronics Technical Reference Manual

2.6 Testing of bases

All bases are cleaned and thoroughly tested at the University of Texas. The following procedures are followed:

1. The bases are cleaned for 30 seconds in a mild alcohol solution and ultrasonic cleaner
2. All components of the bases are tested on the base tester (7)
3. The bases are "baked" for about 24 hrs in a 80C oven
4. The bases are "burned-in" at 1000 V for about 24 hrs
5. The HV is turned on-and-off 50 times
6. Using pico-ammeter the anode leakage currents are checked
7. Capacitance across the C4 dynode capacitor is checked
8. Resistance across the C4 dynode capacitor is checked
9. Resistance across C4-R4 on the bias board is checked.
10. After a PMT-base is tested in a test station the dynode-to-anode ratio of signals is checked on the scope

2.6.1 Operational MUSTs

When high voltage is applied to a tube, all anodes have to be terminated to ground (through at least a 10KΩ resistor) to avoid charging and discharging.

2.7 Known problems

2.7.1 ***Coupling (blocking) capacitor C4*** *on the signal board has plagued the manufacturing, installation, and testing. The likely reasons are bad batch of components, improper temperature steering in soldering, or mechanical damage due to exposure of the part. The known failures have been:*

a. capacitance too small (by a factor of several)
b. capacitance too large (by a factor of several to about 100)
c. finite resistance across (either due to a solder bridge or internal damage)

Symptoms:

If a) is the problem: the ratio of voltage signals on the dynode to an anode is far smaller than a typical ~.75. **This typically causes the tubes to look dead as the dynode does not trigger even a low VFB trigger level for a readout.**

If b) is the problem no external symptoms can be detected but this indicates a likely broken or otherwise damaged capacitor which should be replaced.

If c) is the problem the dynode signal is likely to develop a negative multi-mV baseline shift.

2.7.2 The C4 capacitor in series with an R4 10kW resistor which produces the –5V diode bias bus shows sometimes a finite resistance leading to too low "-5" voltage.

Symptoms:

This **cannot be easily detected externally** but is **relatively easy to measure on the base.** If –5V is not there the tube is not read out by the DAQ system.

2.7.3 The protection diodes coupled to anodes are low current-leakage diodes. However we have found 2 which leaked current of the order of mA (thus were replaced). In general, the leakage current are no more than few nano-amps (6).

Symptoms:

The **leakage current** would saturate the VA chip and the channel would appear dead.

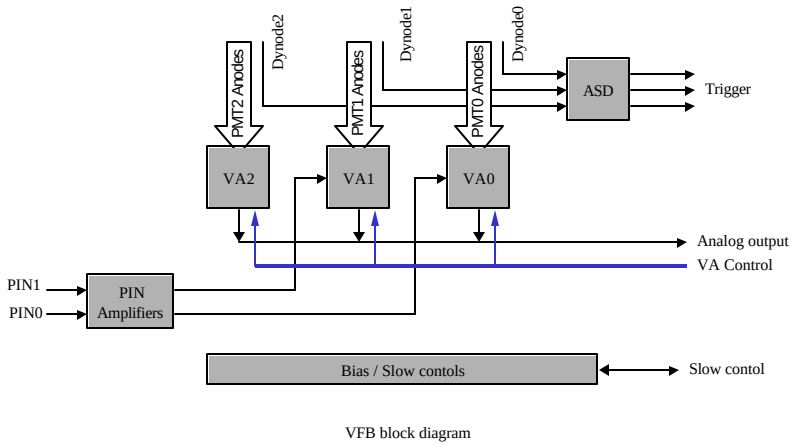
2.8 References

1. Hamamatsu Photonics K. K., Hamamatsu City, Toyooka, Japan,
2. *The Voltage Divider for R5900-00-M16 Phototubes for MINOS*, J. England, R. Hasdorf, J. Ting, and K. Lang, NuMI-L-564 (UTKL-149), November, 1999;
   A Note on M16 bias, Joe Ting and Karol Lang, UTKL-132, February, 1998.
3. Grande Industries, Taylor, TX.
4. Texatronics, Inc., Austin, TX 78744.
5. *Results of Base Taper Modification Tests for M16 PMTs*, Mike Kordosky and Karol Lang, NuMI-L-748 (UTKL-183), June, 2001.
6. *Current Leakage Analysis of M16 Bases for the MINOS Experiment*, Jason Day and Karol Lang, NuMI-L-749 (UTKL-182), May, 2001.
7. *A Testing Device of Voltage Dividers for R5900-00-M16 Phototubes for MINOS*, Jim Parnell, John England, Robert Hasdorff, and Karol Lang, NuMI-L-565 (UTKL-150), November, 1999.

3 VFB

3.1 General description

The VFB (VA Frontend Board) interfaces directly with the three PMTs within the Muxbox and provides the first level in the chain of readout electronics. Its main function is to provide anode readout for three Hamamatsu M16 PMTs and trigger output signals in response to signals from the PMT's common dynodes. Anode readout is implemented using specially fabricated VA chips. Triggers are processed by a multi-channel ASD (Amp-Shaper-Discriminator) chip. Support circuitry is provided for power distribution and biasing of the VA chips. A serial slow control interface is provided to adjust VA bias levels, enable critical voltage regulators, and monitor voltages and temperature. A block diagram is shown below in Figure 2.



VFB block diagram

Figure 2-VFB Block Diagram

The VFB is considered to be a slave module as it has no autonomous operation of its own. In normal operation, a signal from any of its three PMTs causes a trigger signal to be sent to the VARC which in turn handles all sequencing necessary to read out the VA chip. In addition to the "normal" mode of operation, the VFB also has the ability to inject test pulses into the VA chips for calibration.

Finally, one channel for each of two of the VA chips are dedicated to monitoring light from the Flasher system. This is done by means of PIN diode receivers and amplifiers to boost their signal to the appropriate size for the VA chips.

3.2 VA chip

3.2.1 Summary

The VA32_HDR11 chip is a customized version of the VA32_HDR2, a standard product made by IDE AS of Oslo.

It is a CMOS chip, analog with some digital control logic, in an AMS 0.8um process. There are 32 channels, each with a charge sensitive preamp, a shaper, a track and hold stage, and an output switch. The output from a selected channel can be switched to an output buffer, which provides a differential current output able to drive a significant length of cable to a remote DAQ system. In addition there is a second multiplexer that can route charge from a separate input into a selected channel for test and calibration.

It is designed to handle negative inputs from a PMT up to 30pC with reasonable linearity. The shaping is unipolar, with a peaking time of approximately 500ns. Operating conditions, including the shaping, are adjustable over a small range by five external biases. Readout can scan the channels at up to 10MHz. A signal to noise ratio of up to 14,000 is possible under test conditions, though slightly less will be attained in a practical system.

A VA module is a VA32_HDR11 chip mounted on a small pcb to plug onto a VFB. Only 17 of the channels of the chip are brought out; 22 are tested, to include ones used for common mode noise correction.

3.2.2 Background

The design derives from work done at CERN, starting with the AMPLEX chip described in 1990 (NIM A288, p286), and the subsequent Viking described in 1992 (NIM A315, p425; also A340 p572). The firm of IDE was established in 1992 to commercialize this work, a designer of the Viking chip (Einar Nygard) being one of its founders. Their VA series of chips represents further development of the same basic architecture.

Their standard VA chips were designed primarily for silicon detectors. Low noise was the major requirement, while signals tended to be small so large signal capability was not needed. When MINOS was considering using HPDs as the photodetector, they looked quite close to what was required.

When the decision was made to go with PMTs, noise was no longer an issue; large signal handling and high dynamic range were. Both had to be considerably better than any of their standard chips. However, IDE were confident that one of their chips, the VA32_HDR2 ('high dynamic range') could be modified relatively easily to meet MINOS requirements.

They produced a first customized version in 1999 which modified the preamp to handle signals up to 30pC (corresponding to 200 photoelectrons with a PMT gain of 1 million). This needed a very much larger integrating capacitor, and resizing of transistors to charge it fast enough. Other changes were very limited, though some reduction in peaking time was made. This was the VA32_HDR10.

The VA32_HDR10 was a fully usable chip. The modified preamp worked perfectly: this had been the most critical but uncertain change needed. It did however fall somewhat short of what we would like, and it was considered worthwhile going to a second version making minor changes, especially to improve the dynamic range. This was done in 2000, and became the VA32_HDR11. The improvements were significant, and the chip exceeded MINOS requirements by a comfortable margin.

3.2.3 Description

The following sections contain detailed descriptions of the sub-circuits.

3.2.3.1 Preamp

Each channel input goes into a charge sensitive preamp. This has a PMOS input stage in a folded cascode configuration. There is a 17pF feedback capacitor, in parallel with an NMOS FET acting as a high value resistance. Normal biasing, established by the feedback, puts the input at –1.2V.

It was designed to handle negative inputs up to 32pC with good linearity. In practice it works well to over 40pC, which is above the limit set by the subsequent circuits. Signal handling is asymmetric; the limit for positive inputs is lower.

For small signals the amplifier is fast, but for large it slew-rate limits because of the limited current available to charge the feedback capacitor. For normal biasing, this gives approximately a 100ns risetime for a 30pC signal.

3.2.3.2 Shaper

The output of the preamp is AC coupled into the shaper. This is of similar architecture to the preamp, but working at lower currents and arranged to shape the signal into a unipolar pulse. The peak occurs approximately 500ns after the input signal. This is adjustable, mostly upwards, by varying two biases.

Note that this stage is the most serious source of non-linearity. This includes a displacement of the peak at large amplitudes, which makes the observed non-linearity depend on the point at which the waveform is sampled.

3.2.3.3 Track and Hold

The shaper is connected to a capacitor through a CMOS transmission gate. The capacitor voltage tracks the shaper output, until an external hold input puts the gate into high impedance.

The chip has a single hold input, which acts on all channels simultaneously. The hold signal has to be generated externally correctly timed to sample at the peak of the shaped signals. In MINOS it is derived from the last dynode of the PMT, detected by the ASD-LITE on the VFB, and delayed on the VARC.

Valid data requires that all nominally input signals from derived from one event occur within a time that is short compared with the peaking time.

3.2.3.4 Readout

The voltage on the hold capacitor is buffered and passed through another transmission gate. The outputs from all channels are wired together, so the gates form a multiplexer. Any output can be selected and applied to a differential output buffer,

The signal path up to the buffer is single ended with large offset voltages relative to ground. Reference circuitry generates a nominally identical offset, which is applied to the other side of the output buffer. The reference voltage appears on the Vref pin of the module, which is left unconnected except for a decoupling capacitor. The scheme gives reasonably accurate cancellation of the offset and its dependence on temperature.

The buffer produces a differential current output to go off chip to the DAQ system. This is the other main source of non-linearity, but with normal biasing it this significantly less than that from the shaper, and is easily predictable.

3.2.3.5 Charge Injection

Each channel has a third transmission gate, this one connected to the preamp input. These are wired together as another multiplexer, and are used to route charge injected at the Cal pin to any channel. This is used for test and calibration.

The on resistance of the gate seems to be about 500Ω. This makes the charge injection rather slower than typical MINOS signals. With the charge generated by a voltage step into a 33pF capacitor on the VFB, plus about 20pF total stray capacitance to ground, a time constant of about 35ns can be expected. This should not be significant. For large charges, the slew rate limitation, which is the same for both signal and calibration, dominates, and further reduces the difference.

3.2.3.6 Control Logic

The gates forming the output multiplexer are each controlled by one stage of a shift register. One bit clocked into and along the shift register (by the Shift_in and Clock pins) selects one channel of the multiplexer.

The charge injection multiplexer is controlled in the same way. Control is shared with the output multiplexer: asserting Test_on causes the input bit to be shifted into both shift registers.

Note that when misoperated, more than one bit can be set in a shift register. This will turn on two or more multiplexer channels simultaneously, which is harmless but very confusing...

Also note that the output buffer is only enabled when an output multiplexer channel is selected. This allows outputs of multiple chips to be paralleled, without those not being read out contributing noise. This is done by toggling the buffer on when a bit is shifted into the register, and off when a bit first appears at the end. If misoperated, this can add even more confusion.

The Dreset input clears both shift registers (and hence turns off both multiplexers), and disable the output buffer.

3.2.4 Further Information

The design is proprietary to IDE, and circuit details cannot be given. For application information, refer to the IDE data sheet. The VA32_HDR10 sheet applies, and is not affected by the changes made in going to the HDR11.

3.2.5 Operating Notes, bias settings

3.2.5.1 General

The VA chips are powered by +/- 2.5V power rails and ground. Each chip has several adjustable bias settings which control its operation. Three of these settings are considered critical and therefore have been made externally adjustable by means of the serial slow control link. These signals are described below and further information can be obtained from IDE's documentation.

- Vfp : This voltage is applied to the gate of a fet in the feedback circuit of the VA's preamps. It controls the fet's on-resistance and therefore, along with the feedback capacitor, controls the feedback time constant of the integrator. By adjusting Vfb higher, one lowers the feedback resistance and therefore lowers the time-constant. This also has the effect of making the preamps more tolerant to PMT base leakage currents. Shorter time constants tend to produce a more pronounced undershoot and faster recovery. Longer time constants produce less undershoot, but require longer time to fully recover. Typically, this time constant is set to order ten microseconds or so.
- Vfs : In a similar manner to Vfp, this voltage adjusts one of the poles of the shaping network.
- Sha_bias : This is a current input to the VA chip and controls the second pole comprising the shaping network. Along with Vfs, this is adjusted for the desired peaking time, typically around 500ns.

These three setting are externally programmable for the three VAs as a group, but not individually.

Internally, the VA chip runs between +/- 2.5 volt rails. The chip's main amplification device, its input fet, is however, connected only to the -2.5 volt rail and ground. This is done for reasons of minimizing power dissipation as the input fet consumes most of the total current. Thus, the bulk of the chip's current flows between ground and the -2.5 volt rail. In order to insure quiet operation and minimal crosstalk between the three VAs on the board, a single positive 2.5 volt regulator and *individual* negative 2.5 volt regulators are used to power them. The complete power distribution scheme is described in a later section.

3.2.5.2 Prebias (typical: 600mA, pin is at -650mV)

A current that sets the operating current of the preamp. The nominal value is chosen to give an acceptable speed of response to large signals. The preamp is slew-rate limited for large input signals of short duration, so they will seem to be somewhat delayed. Which with a fixed sampling delay causes non-linearity. Biasing to a lower current would increase this delay and non-linearity. There is no reason to modify prebias, and no adjustment is provided on the VFB.

3.2.5.3 Vfp (typical: +100mV to allow 10nA DC. Cutoff below -400mV)

A voltage that sets the effective resistance of the FET providing a DC feedback path around the preamp. This is very non-linear: this will be disregarded, but it does significantly modify this simplified picture.

Set very negative the FET is cut off and there is no DC feedback. The preamp then acts as a pure integrator. Leakage currents (and any DC input component) cause the output to drift until it reaches saturation. The signal gain then drops to zero, and the output signal disappears. Note that this can be a very slow process, in some cases taking minutes, so a setting that initially appears satisfactory may in fact be too low.

At a slightly more positive setting the FET is biased on sufficiently for the feedback to be effective at stabilizing the operating point. The initial step output from the preamp in response to an input charge pulse decays, but only slowly. There is thus a negligible effect on the shape produced by the shaper. An overshoot is introduced, but although very long, it is negligibly small. This is the 'ideal' operating condition. However, it has a very limited ability to accept a DC input, either leakage current or from high rate, large amplitude PMT signals during light injection. Also, it can be quite sensitive to photocurrents produced by light penetrating the black epoxy, and electro-statically coupled mains frequencies: these can cause anomalous and puzzling behavior during lab tests, but are not significant for operation on MINOS.

A rather higher setting gives an acceptable ability to handle DC components, at the price of perceptible overshoot. A reasonable compromise should be possible, able to accept around 10nA, but at which the overshoot can be ignored.

Higher settings, up to the maximum possible with the VFB or even up to the supply rail, still give acceptable operation. Currents into the μA range can be accepted, and the overshoot becomes shorter but larger. In the limit the output shaping approaches bipolar, with 10 to 20% overshoot.

Note that in the normal use of a charge sensitive preamp, a low feedback resistance is unacceptable because of an increase in noise. This is not an issue with this chip. Because of its design modifications to handle large signals, other noise sources are limiting. Some slight deterioration may be noted at very high Vfp.

3.2.5.4 Shabias (typical: 100mA, pin is at -700mV)

A current that sets the operating current of the shaper. This controls the transconductance of its amplifier, which is one of the factors determining its shaping time constants. A high bias makes it faster. It needs to be adjusted in conjunction with Vfs to get the required shaping.

This bias also affects its linearity. Large departures in either direction from its design value will impair linearity. Extreme settings should be used with caution, and the overall performance checked.

3.2.5.5 Vfs (typical: +900mV)

A voltage that sets the effective resistance of the FET providing feedback around the shaper amplifier. This, together with Shabias, determines the shaping time constants. A high value makes for faster shaping. Sensible shaping requires Vfs set to at least a moderately high value. A very negative bias will cut off the FET and upset the DC conditions. However, this is a long way removed from any realistic operating point.

3.2.5.6 Ibuf (typical: 200mA, pin is at +120mV)

A current that sets the operating current of the output buffer. The output buffer is a differential pair, the tail current of which is set to 5*Ibuf. This current is steered between the two outputs. A pair of current sources cancel out the quiescent current, so each of the two output currents vary between +/-2.5*Ibuf.

The nominal value is designed to give the best dynamic range, so major departures would be undesirable. It is not adjustable from the VFB.

Note that Ibuf is only accepted when a channel of the output multiplexer is enabled. So on the VFB, the voltage at the Ibuf pin will not be constant. The same applies on the VA-MCR II.

3.2.5.7 Power supplies (typical: 19mA from +2.5V, 31mA from -2.5V)

These are nominally +/-2.5V. Operation will not be significantly affected down to +/-2V, except for some reduction in signal handling capability. Total voltage should not exceed 5.5V.

3.2.5.8 Signal Inputs

The signal inputs are at about -1.2V when the preamp is operating correctly. This is set by the feedback around the preamp, through the FET acting as a high value resistor. Hence there must be essentially no DC path to ground. The input current, from whatever source, needs to be about 10nA or less for normal preamp biasing (though more is acceptable if a very high Vfp is chosen)..

The input impedance at signal frequencies should be about 150 Ω, but this was not a design requirement and has not been checked.

The signal inputs have protection diodes, clamping them to the supply rails. Hence they are reasonably resistant to ESD, and will not be destroyed by currents from a PMT even if there is no clamping in the tube base. However, they are unlikely to withstand connection to cable from a live PMT that has charged to last dynode potential.

Large input signals of short duration cannot immediately be accepted by the feedback capacitor because the available current is limited. Hence it is necessary that there is sufficient external capacitance on the input node to limit the voltage swing so that charge is not lost through the protection diodes. The swing should be limited to under 2.0V, which for 32pC implies a total capacitance of at least 16pF (part of which will be provided by the chip and module strays). Since this will be considerably exceeded by the input cable, quite apart from the VFB, adapter board, and PMT assembly strays, this is of no concern in the standard MINOS installation. Caution is advised if installed in a

system in which the capacitances are much reduced: different non-linearity at high levels seems likely, but this operating regime has not been investigated.

3.2.5.9 Signal Outputs

The chip provides a differential current output designed to operate into a low impedance load at about 0.8V below ground.

3.2.5.10 Logic Inputs

Logic inputs are CMOS, with their threshold about midway between the supply rails. That is, about ground.

3.2.6 Performance

Typical performance, biasing set to give peak at 0.6us after input:

Largest signal for 10% deviation from linearity: -32pC
Corresponding signal/noise: 14,000

Noise is with slow readout, and common mode noise (that is, shifts in pedestal common to all channels) and readout noise subtracted. Operational S/N will be somewhat less.

3.2.7 Variation

Gain within chip: average spread 1% (full range). 95% of chips under 5%.
Gain between chips: standard deviation of mean gain appears to be under 4%.
Pedestals: rms value 0.5% of maximum signal, largest +/-5%.

Variation between chips assumes they are operated under similar conditions. Some IDE production test data shows considerably wider gain spreads, systematically varying between different test sessions. Note that variations are not gaussian; because, for example, chips from the edge of wafers are systematically worse than average.

3.2.8 Temperature sensitivity:

Operates acceptably up to substrate temperature of at least 80C
Peaking time increase about 14% from 30C to 80C
Gain decreases about 6% from 30C to 80C.

80C was the maximum temperature normally used in testing. Temperature variation seems quite linear and consistent, except that a few chips have been seen with an order of magnitude worse variation. This constitutes a fault, the cause of which is not yet known, which is not detected by our routine testing.

3.3 VA Module

The VA chip is packaged as a module for use in MINOS. This is a small pcb, 26mm square. The chip is mounted on top, wire bonded, and covered with black epoxy. Two pin headers, each 12 x 2 way, are fitted underneath. One has the signal input and power connections; the other all the interface lines. Only seventeen of the signal inputs on the chip are wire bonded and brought to pins.

Three of the resistors needed for setting VA chip bias currents are also fitted to the pcb, and five decoupling capacitors. The chip pads to which the resistors are connected are also brought out to module pins: these are not used on the VFB, but permit the standard VA-DAQ test system made by IDE to be used.

In operation there is a temperature rise of about 10C above ambient at the module underneath the chip.

3.3.1 Components on Module

Component	Value	Function
R1	12k	to set Ibuf
R2	33k	to set sha_bias
R3	47k	to set pre_bias
C1-C5	100nf	bypass caps

3.3.2 Pinout

Left header				**Right header**			
1	-2.5V A	**2**	+2.5V A	**1**	/Hold	**2**	[Hold]
3	-2.5V D	**4**	+2.5V D	**3**	Dreset	**4**	[/Dreset]
5	GND	**6**	GND	**5**	/Shift_in	**6**	/Clk
7	Ch1	**8**	Ch2	**7**	[Clk]	**8**	/Shift_out
9	Ch3	**10**	Ch4	**9**	Test_on	**10**	nu
11	Ch5	**12**	Ch6	**11**	GND	**12**	GND
13	Ch7	**14**	Ch8	**13**	Pre_bias	**14**	Pre_bias_r
15	Ch9	**16**	Ch10	**15**	Sha_bias	**16**	Sha_bias_r
17	Ch11	**18**	Ch12	**17**	Vref	**18**	Ibuf_r
19	Ch13	**20**	Ch14	**19**	Ibuf	**20**	Outm
21	Ch15	**22**	Ch16	**21**	Outp	**22**	Vfs
23	Ch17	**24**	GND	**23**	Vfp	**24**	Cal

3.3.3 Notes

a) Input channels are ch1...ch17. Channels on chip are ch0...ch31, with ch0...ch21 tested.

b) The separate analog and digital power pins are connected on the VFB.

c) A / prefix to a digital input shows it is active low.

d) [...] about a digital signal shows it is dummy used to reduce noise
e) A _r suffix indicates connection through a series resistor.
f) Elsewhere a 'b' or '_b' suffix has been used to denote active low.

3.3.4 Handling

The module should be inserted by pressure over the connectors. Pressing on the epoxy topping (however tempting) is not advised, since the epoxy is quite soft and it is in principle possible to damage the wire bonds by doing this.

Removal needs a firm grip on the edges of the module. A DIL removal tool used carefully works and is much easier. If a tool such as a small screwdriver is used to ease the module up, great care is necessary to neither damage components on the VFB nor bend pins on the module.

It is not mechanically keyed for orientation or transverse positioning, so care should be taken to ensure it is correctly inserted: orientation of the module is indicated by a small arrow marked on the pcb, which should point towards the end of the VFB with the electrical connectors.

The VA chip and module are static sensitive. The following rules should be applied at all times.

- **VA module should not be "hot swapped" with power on the VFB.**
- **When handling modules, grounded antistatic wrist straps should be used at all times**
- **Modules should be stored on antistatic foam in antistatic boxes or bags.** Sandwiching between sheets of antistatic foam with a sheet of stiff cardboard at top and bottom and the whole stack tightly taped up is recommended.

3.3.5 Hold Delay Problem

There was a problem with the first 1600 modules as originally produced. This has been corrected, and should be of no concern to users, but a brief description is included as background.

The VA chip has on it an analog time delay circuit that can be inserted into the path from the hold input to the hold switches. This was included in the very first version of the VA ever made by IDE, in case it would reduce the effect of switching noise from the hold input. It was never needed, but was never removed from the design so as to avoid unnecessary changes, and is still present in our version.

The hold function is controlled by two pads. A bias current into delay_adjust sets the delay; a logic level on delay_on selects if the delay is to be used. IDE state delay_on has to be tied to the negative supply, which disables the delay. They also recommend delay_adjust is tied to ground, but connection to the negative supply is equally acceptable.

Unfortunately in going from the first version of the module pcb to an improved one for production, IDE removed the connections from these two pads, and they were left floating. Because the delay_on is a CMOS input, this meant that whether or not the delay was active was ill determined.

By evil mischance, conditions under standard testing using the VA-DAQ, and during initial tests on the VFB, were such that no problem was ever seen. It was only when electronics for the MINOS Calibration Detector was being commissioned that the problem manifested, taking the form of an apparent complete failure of the hold function when the temperature was raised slightly above ambient.

It turned out that leakage currents, increasing with temperature, tend to turn on the input. Opposed to this are currents injected through the substrate by overshoots on digital inputs causing conduction of their clamping diodes. This leads to operation at high rates tending to give correct operation, especially with poor quality drive signals to the chip. Photocurrents, caused by light leaking through the black epoxy, could also force correct operation.

The fix was to modify the modules to connect the delay_adjust and delay_on pads to the negative supply. Fortunately the pads had been wire bonded to pads on the pcb, and the three that had to be joined were adjacent. IDE were able to do it by cutting away epoxy to expose the pads, and applying a tiny spot of conductive epoxy. Once the repair was effected, the modules operated correctly at arbitrary low rates and temperatures to at least 80C.

3.4 Trigger circuits

Triggers are derived from the M16's common dynode which produces a short pulse of opposite polarity to that of the anodes and about half the amplitude. Pixel gain spread is also reflected in the amplitude of the dynode signal. Three such dynode signals are received by a four channel Amplifier/Shaper/Discriminator chip called ASD-lite. Each of the four channels of this device contains a pair of differentially connected preamplifiers, a shaper stage, and a differential discriminator with LVDS outputs as shown below in the block diagram, Figure 3.

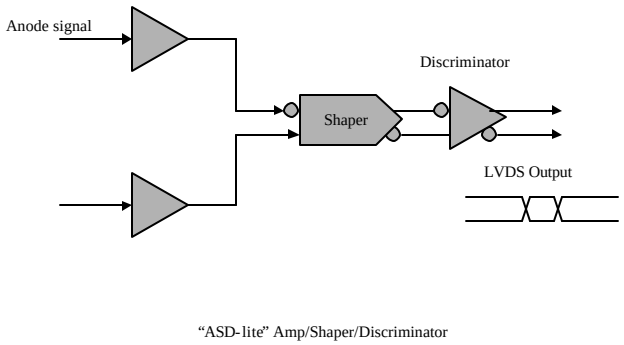


Figure 3-ASD-lite

The input stage is "pseudo-differential" and consists of a pair of single ended transimpedance amplifiers. Beyond the preamps, the chip is fully differential. This feature provides high stability as well as immunity to pickup and crosstalk. In general, the device may be used in either polarity with signals injected into either input preamp. Key specifications of ASD-lite are given below.

- Preamp input impedance 120 Ω
- Shaper peaking time 13ns
- Sensitivity 15mv/fc (differential)
- Equivalent noise charge ~ 0.5 fc
- Dynamic range < 80fc full scale
- Process HP 0.5u nwell CMOS
- Power supply voltage 3.3V

PMT dynode signals are approximately half the amplitude of the corresponding anode signal and therefore a single photoelectron corresponds to about 40fc or about 600mv in the ASD-lite. The ASD-lite's dynamic range therefore corresponds to about 0 to 2 photoelectrons and can easily trigger at a fraction of a photoelectron.

Threshold settings are applied to the device as a differential voltage centered about the mid-point of the 3.3 volt supply. For example, a 0.5 pe threshold corresponds to ~20 femtocoulomb from the dynode. This, in turn, corresponds to 300 mv differential threshold setting. Thus, the two threshold inputs would be set to 1.50V and 1.80 volts respectively. This is accomplished by setting a single 7-bit threshold DAC which is

scaled to correspond to –80 fc to +80 fc threshold setting. Although the dynode signals are positive, an inversion occurs in the DAC threshold setting circuits. Thus, for dynode signals, the bottom half of the total DAC range is used. Thus, threshold settings of 0…80 fc corresponds to DAC settings of 63…0 and one count on the DAC corresponds to 1.25 fc or 1/32 of a photoelectron (nominal gain pixel only).

3.5 Cal Injection

The VA chip has internal provision for calibration. To do this, it has a CMOS switch for each of its input amplifiers. One side of this switch is tied to the corresponding preamp input while the other sides of all switches are tied together and made available on a package pin. A single cal_inject capacitor is tied to this common pin for injection. Channels are selected by means of a shift register internal to the VA chip. Thus, cal_inject cycles are distinct from normal operation of the chip.

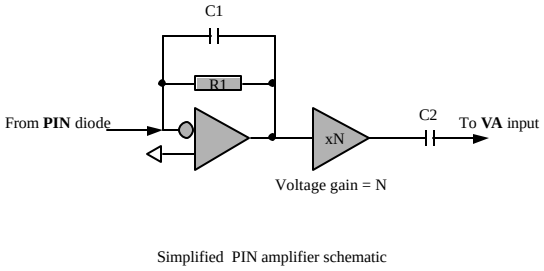
Cal_injection is done in the usual manner by pre-charging a capacitor to a programmable voltage and then discharging it through a cal_inject capacitor using a simple fet switch. The cal_inject capacitor is programmed by a 7-bit DAC, accessible through the slow control interface. Absolute accuracy is set by the accuracy of the cal_inject capacitor and other passive components and is of order ~15%. Linearity is limited by DAC resolution to about +/- ½ LSB or approximately +/- ½ % of full scale setting. Calibration fet non-linearities are also present at approximately this level. When viewed on the 14 bit scale of the VA readout, these non-linearities are clearly visible.

3.5.1 Interaction with PMT base

The PMT base contains protection diodes which prevent the anodes from charging up when the VFB is not present to absorb their current. These diodes are reverse biased when high voltage is applied to the PMT and are thus normally “invisible” to the VA chip. One side effect of this protection diode is that if high voltage is off, the diode will **not** be reverse biased and the VA chip will **not** operate properly. ***Thus, some high voltage is required while doing Cal_inject runs***. A high voltage setting of order one half nominal operating voltage is sufficient to completely reverse bias the protection diodes and insure proper operation of the VA inputs.

3.6 PIN amplifiers

Two PIN diodes and amplifiers are provided to monitor light from the Flasher system. The diodes are placed directly onto the VFBs rather than remotely to eliminate the possibility of ground loop problems. Thus signals are coupled to the pin diodes by means of fiber optic cables. Signals from these diodes are first amplified by a factor of 20, and then input into an unused channel of the VA chip. A simplified schematic of the PIN amplifiers is shown below.



Simplified PIN amplifier schematic

Figure 4-PIN Diode Amplifier

This is a simple two stage amplifier consisting of an integrator followed by a gain stage. The second stage output is coupled to the VA input by a capacitor which acts as a differentiator. Thus, the net transfer function is that of a current amplifier whose response rolls off at low frequencies. Thus PIN diode leakage current, provided it is not so large as to saturate the integrator, has no effect on the VA channel that handles the signal. The overall gain of this amplifier is given by

$$N \cdot C2 / C1$$

Values have been chosen such that the capacitor ratio gives a gain of 2 with an additional 10x gain in the second stage for an overall gain of 20.

The two amplifiers have been chosen for different criteria. The integrator amplifier is typically the dominant noise source in the signal processing chain and has therefore been chosen for low noise. The second stage gain requires high bandwidth at reasonable power levels, while noise is not the major consideration. The bandwidth is chosen such that a delta function light injection will result in a signal into the VA chip of approximately 30-50 ns peaking time. This time is small compared with the VA's 500 ns shaping time. Thus, minimal delay of the VA's peaking time is incurred.

In contrast to PMT anode signals, which are accompanied by a dynode trigger, the PIN signal produces no trigger directly. It must therefore be accompanied by a dynode trigger from the PMT associated with the particular VA chip which handles its signal. Fiber optic cable delays must be such that "near" simultaneous arrival of the Flasher light

and the associated dynode trigger is assured. Ideally, the Flasher light should arrive somewhat earlier than the dynode trigger to allow for the delay time incurred in the PIN amplifiers.

3.7 Digital i/o

Digital i/o on the control cable uses the LVDS standard. These signals are used for;

- Trigger
- Slow control interface
- Calibration charge injection
- VA chip control

Externally, all signals are LVDS. Internally on the VFB, there are three categories of logic swings.

a. The dynode trigger signals are LVDS both internally and externally. LVDS driver chips are used in this case simply to buffer the ASD-lite's LVDS output to drive the 26' long cable to the VARC.
b. The next category uses (0, +5V) levels. These are used in the slow control section and for calibration injection.
c. The third category utilizes (-2.5V, +2.5V) swings to interface directly to the VA chips. Level shifting is implemented by opto-couplers in a configuration suggested by IDE and used in their proprietary VA readout controllers.

3.8 Power distribution

VA devices are known to be quite sensitive to noise on their power supply lines. In particular, power supply noise manifests itself in a common mode noise component on each channel of the VA chip. To minimize these problems, local regulators are used extensively on the VFB. Some of these regulators have "shut-down" inputs which are accessible via slow control interface. Others are fixed and are continuously enabled. The individual regulators used in the VFB are listed in the table below.

Regulator	Voltage	Remote Shutdown
VA-common Vdd	+2.5V	Yes
VA-2 Vss	-2.5V	Yes
VA-1 Vss	-2.5V	Yes
VA-0 Vss	-2.5V	Yes
ASD-lite Vdd	+3.3V	Yes
VA-logic level shifter Vdd	+2.5V	No
VA-logic level shifter Vss	-2.5V	No

Total power consumption is shown in the table below.

Supply	Current (ma)
+ 5V	280
- 5V	190

The overall connection scheme of these regulators is shown in Figure 5.

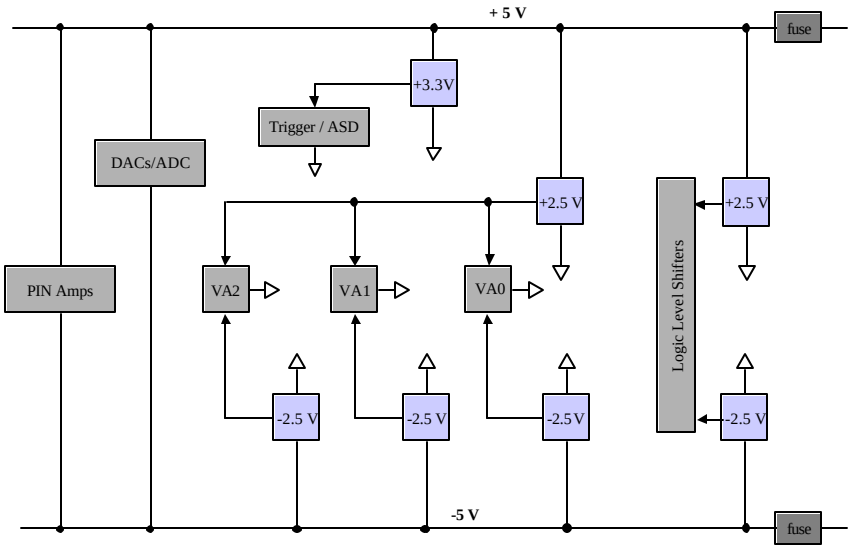


Figure 5-VFB Power Distribution

In addition to providing crosstalk isolation, the VA chip's individually addressable negative regulators make it possible to selectively shut down one chip in the event of catastrophic failure. The fact that the three chips share a common output bus, however, results in the fact that *if one chip is shut down in this way, the remaining two chips will not operate properly*.

3.9 Slow controls

The slow control section is used to set VA biases, enable voltage regulators, and monitor critical VFB voltages and temperature. Communication is implemented by a Xilinx CPLD and uses simple serial interface with a 3-bit address field. The serial interface signals are the following.

a) SDIN : Serial Data In (*into the VFB*)
b) SDOUT : Serial Data Out (*out of the VFB*)
c) SERCLK : 2 MHz serial clock derived from the 40 MHz system clock.
d) SEREN : Asserted preceding serial transfer. On de-asserting, data is latched to appropriate device.

The devices to be addressed on the front end boards are

a) Five DACs, or more correctly, 7-bit programmable potentiometers
b) An octal 12-bit ADC
c) A 5-bit "Shutdown" register corresponding to the five voltage regulators on each front end board.

The serial protocol starts with the assertion of the SEREN line to a particular VFB. Following this, the first three bits transmitted are interpreted as a local Device Address. The bits following the Device Address are the data bits to be sent to the Local Device. In the case of the DACs and Shutdown Register, after the transmission of the appropriate number of data bits is complete, the SEREN line is de-asserted latching the data into the appropriate register locations and completing the transaction. In the case of the ADC, after the Device Address, and 8-bit control byte is sent. Following this, 12 more clocks are issued causing the ADC to output its serially encoded data to the VARC.

In all cases, the MSB of any bit stream appears first, with the LSB arriving last.

3.10 Local Detector Controller (Slave)

The LDC refers to the Xilinx CPLD which implements the serial interface. The LDC recognizes seven register locations, or Device Address', as follows.

3.10.1 Device addresses

Address	Device	Function
0	DAC Ch0	Preamp feedback bias (Vfp)
1	DAC Ch1	Shaper feedback bias (Vfs)
2	DAC Ch2	Shaper bias current (Sha_bias)
3	DAC Ch3	Dynode trigger threshold
4	DAC Ch4	Calibration charge
5	ADC	Octal 12 bit ADC
6	Shutdown Reg	Voltage regulator control
7	Not used	

On receipt of the three Device Address bits, the LDC responds by asserting the appropriate chip select lines (/CS). The data inputs to all devices are connected together (DIN) as are the serial clock lines (SERCLK). The only function of the LDC is to decode the address and assert the /CS lines at the appropriate time. Formatting the data stream for the individual devices is, thus, not the responsibility of the LDC but is handled by a corresponding controller in the VARC.

3.10.2 DACs

The DACs have 7-bit resolution and are more correctly programmable potentiometers. Thus DAC programming requires 10 bits : three bits of Device Address followed by seven bits of data.

3.10.3 ADC

The ADC is an octal 12 bit device and accepts inputs in both unipolar (0,+Vref) and bipolar (-Vref/2, +Vref/2) modes with Vref=4.096 volts. Following the Device Address, an 8 bit code is sent with the following bit assignments.

3.10.3.1 Control code

Bit	Name	Description
7	Start	Defines beginning of code transmission
6	SEL2	Channel select code MSB
5	SEL1	Channel select code
4	SEL0	Channel select code LSB
3	UNI/BIP	Hi=Unipolar mode, LO=Bipolar mode
2	SGL/DIF	Hi=Single ended mode (always used)
1	PD1	Chip Mode 11=ext clock, 10=int clk
0	PD0	Chip Mode

Note that the master controller in the VARC will set up the ADC in the External Clock mode automatically.

The SEL[2:0] bits determine the ADC channel for digitization. The SEL code is a mapping onto the channel number given in the following table. The UNIpolar mode should be used for all positive voltages and the BIPolar mode for all negative ones. Since the BIPolar mode only goes down to –2.048 volts, the –2 Volt supplies go through 2:1 voltage dividers before the ADC.

3.10.3.2 Channel addresses

SEL[2:0]	ADC Channel	Data	Use MODE
7	7	*Vmon**	UNI
6	5	-2.5V_2	BIP
5	3	-2.5V_0	BIP
4	1	+3.3V	UNI
3	6	Vtemp	UNI
2	4	-2.5V_0	BIP
1	2	+2.5V	UNI
0	0	GND	BIP

Note that *Vmon* is a voltage which is halfway between +2.5V_1 (common +2.5V rail) and -2.5V_3 (common -2.5V digital rail). This is nominally close to zero and enables the monitoring the health of both voltages with the only remaining ADC channel. The GND monitor, channel 0, directly measures the ADC offset from zero. This turned out to have been unnecessary as it is always zero.

Following the control signal byte, the VARC must send 12 additional clocks which are used to clock the successive approximation data out of the ADC, one bit at a time starting with the MSB.

3.10.4 Shutdown Register

A 5-bit register corresponding to the five individual voltage regulators as follows.

Bit	Name	Description
4	/SHDN4	-2.5V_2 (VA_C negative rail)
3	/SHDN3	-2.5V_1 (VA_C negative rail)
2	/SHDN2	-2.5V_0 (VA_C negative rail)
1	/SHDN1	+2.5V_1 (VA Common positive rail)
0	/SHDN0	+3.3V (Trigger ASD supply)

3.11 Cables and connectors

3.11.1 Control cable

The Control Cable is a 50 conductor fine pitch (0.025") twisted pair that connects the VFB to the VARC. A table of the Control Cable signals is shown below.

Signal	Function	(+) pin	(-) pin	Dir	VFB logic swing
TRIG0	Dynode trigger 0	1	2	READ	LVDS
TRIG1	Dynode trigger 1	3	4	READ	LVDS
TRIG2	Dynode trigger 2	5	6	READ	LVDS
SDOUT	Serial data out of VFB	7	8	READ	(0,+5V)
SERCLK	Slo control serial clk	9	10	WRITE	(0,+5V)
SDIN	Serial data into VFB	11	12	WRITE	(0,+5V)
SEREN	Enable serial data transfer	13	14	WRITE	(0,+5V)
Spare	not used	15	16	WRITE	(0,+5V)
TEST	Test Mode (common)	17	18	WRITE	(-2.5V,+2.5V)
CAL0	Hit cal-inject VA0	19	20	WRITE	(0,+5V)
CAL1	Hit cal-inject VA1	21	22	WRITE	(0,+5V)
CAL2	Hit cal-inject VA2	23	24	WRITE	(0,+5V)
SHIFT-IN0	Shift in VA0	25	26	WRITE	(-2.5V,+2.5V)
HOLD0	Sample/hold VA0	27	28	WRITE	(-2.5V,+2.5V)
CLK0	Clock signal VA0	29	30	WRITE	(-2.5V,+2.5V)
RES0	Reset VA0	31	32	WRITE	(-2.5V,+2.5V)
SHIFT-IN1	Shift in VA1	33	34	WRITE	(-2.5V,+2.5V)
HOLD1	Sample/hold VA1	35	36	WRITE	(-2.5V,+2.5V)
CLK1	Clock signal VA1	37	38	WRITE	(-2.5V,+2.5V)
RES1	Reset VA1	39	40	WRITE	(-2.5V,+2.5V)
SHIFT-IN2	Shift in VA2	41	42	WRITE	(-2.5V,+2.5V)
HOLD2	Sample/hold VA2	43	44	WRITE	(-2.5V,+2.5V)
CLK2	Clock signal VA2	45	46	WRITE	(-2.5V,+2.5V)
RES2	Reset VA2	47	48	WRITE	(-2.5V,+2.5V)
GND	AC Gnd at VFB	49	50		

3.11.2 Power cable

Power comes into the board from the Power Distribution Panel (PDP) on a separate power cable which consists of two individually shielded twisted pairs with an additional

bulk shield. The shields are an integral part of the grounding system and are used to tie the VFBs to the global ground.

Pin	Signal
1	+ 5V
2	+ 5V Return (GND)
3	Shield (GND)
4	- 5V
5	- 5V Return (GND)
6	Shield (GND)
7	Shield (GND)
8	nc

3.11.3 Analog Signal cable

The Analog Signal cable is a low loss / low dispersion shielded twisted pair (Gore Quiet Zone™) which connects the VFB to the VARC. This cable carries the multiplexed outputs of all three VA chips. The connector is a proprietary Gore product and has only three pins.

Pin	Signal
1	Shield (GND)
2	Out +
3	Out -

3.11.4 PMT/muxbox connector

The VFB connects to three PMT bases by means of three identical miniature board-to-board connectors on the back of the VFB. These plug into mating connectors on the light-tight connector panel of the muxbox. An interleaved signal/ground pattern is used to insure minimal crosstalk between the anode channels. The connector is a 2 row x 20 pin header on 0.050" centers. The connections are shown below.

Pin no	Signal	Pin no	Signal
1	GND	2	GND
3	Anode 0	4	GND
5	GND	6	Anode 1
7	Anode 2	8	GND
9	GND	10	Anode 3
11	Anode 4	12	GND
13	GND	14	Anode 5
15	Anode 6	16	GND
17	GND	18	Anode 7
19	Anode 8	20	GND
21	GND	22	Anode 9
23	Anode 10	24	GND
25	GND	26	Anode 11
27	Anode 12	28	GND
29	GND	30	Anode 13
31	Anode 14	32	GND
33	GND	34	Anode 15
35	GND	36	GND
37	Dynode	38	GND
39	GND	40	GND

3.12 Printed circuit layout

The VFB is a 3.00” x 8.00” six layer printed circuit board. Both top and bottom outer layers are ground. The VFB layout is shown below in Figure 6

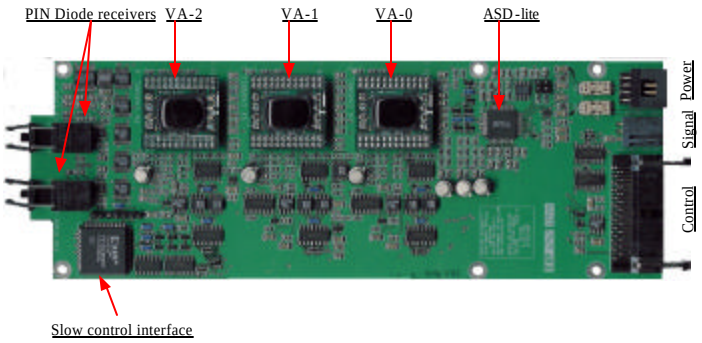


Figure 6-VFB Assembly

4 VMM

4.1 General description

The VMM (Varc Mezzanine Module) receives, amplifies, and digitizes VA output signals from the VFB and sends the digitized data to the VARC. Up to six VMMs may reside on each VARC. The VMM uses a high speed 14 bit ADC which is capable of digitization rates of up to 10 MHz but is typically operated at 3-4 MHz. Given the small event rate in the MINOS far detector, demand on this digitizer is extremely low. The VMM is thus able to share this digitizer between two VFBs without incurring any more dead time than that inherent in the VA chip.

The VMM's digitizer (AD9240) has fully differential inputs To insure quiet operation, immunity from crosstalk and power supply noise, the VMM also maintains differential swings from input through to the digitizer. Local +/- 5V voltage regulators are used and are powered by bulk a +/- 6V power bus on the VARC. A block diagram is shown in Figure 7.

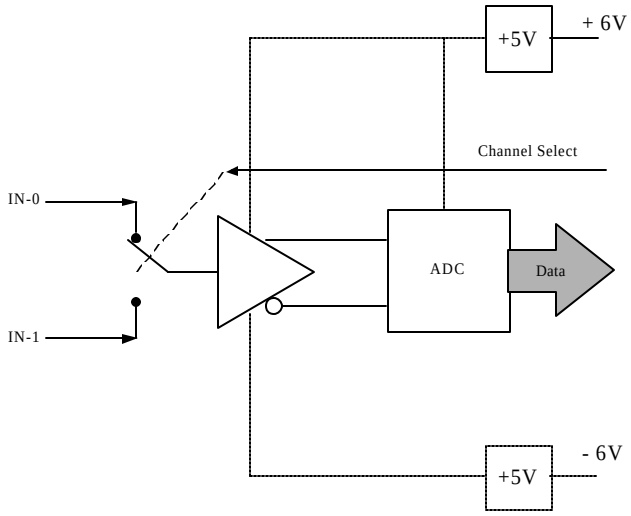


Figure 7-VMM Block Diagram

4.2 Input stage

A typical receiver for VA chip signals consists of a pair of simple common base transistors. The VMM's input consists of a pair of such receiver circuits and is shown in Figure 8.

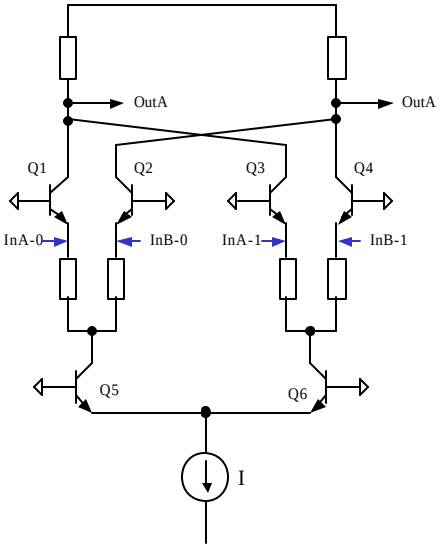


Figure 8-VMM Input Stage

The lower transistor pair, Q5/Q6 acts as a current switch to select between the two pairs of common base transistors Q1/Q2 or Q3/Q4. The current I, flows through the selected pair and then goes on to the later stages of the amplifier to the ADC. This circuit has the advantage of simplicity, but has two adverse effects which need to be fully understood to insure proper operation. These are described below.

4.2.1 Thermal effects.

The current *I*, has a self heating effect on the selected transistor pair. This self heating is quite small, typically of order several milliwatts per transistor. However, given the small size of the surface mount transistor packages, this is sufficient to raise the junction temperature by a half degree C or so. While this heating is quite small, *its effect is measurable by the high resolution (14 bit) ADC* and can cause pedestal shifts of order 5 to 10 ADC counts. The time constant of this shift is of order hundreds of milliseconds, typical for thermal effects.

To compensate this effect, the switch must be operated in such a fashion as to insure uniform self heating of both input receivers. *To accomplish this, the VARC switches between the two VFB channels* when the VMM is in its idle state which, in the MINOS far detector, is most of the time.

4.2.2 Cable capacitance effects

The VA chips have the feature that their output cable driver stage is disabled except when there is a readout in progress. In the idle state, the VMM alternately selects between the two VFB inputs for thermal balance (see above). As the VMM switches

away from a particular channel, the analog cable for that channel is left completely floating and is slowly discharged by the VMM's corresponding input transistors, Q1…Q4. The functional shape of this decaying current has the characteristic form

$$i(t) = \frac{i_0}{1 + t/t_0}$$

where i_0 is the initial current flowing in the transistor. The constant t_0 has units of time and is expressed in terms of initial current i_0 and cable capacitance C as follows.

$$t_0 = \frac{kT}{i_0 \cdot q} \cdot C$$

The constant t_0 has a value of order ~2ns. Thus in ~20 ns, the transistor's current will drop to 10% of its initial value. In ~200ns it will drop to 1%, in ~2us, to 0.1% and so on. This decaying current of the unselected channel is summed into the current of the selected channel, and even at 2us, it is observable by the 14 bit ADC. At 200ns, the effect is actually smaller than the expected 1% full scale because of the differential nature of the VMM but is, nonetheless, several tens of counts in the pedestal data. This effect is particularly noticeable when doing triggerless pedestal runs if these are done asynchronously with respect to the clock which controls the input switch.

The VARC handles this situation as follows. When doing triggerless pedestal runs for VAs on a particular VFB, the VARC switches first to the opposite channel for a fixed time, then switches back to the desired channel for several hundred nanoseconds before beginning a readout. This is sufficient time to allow the current to drain to the 1% level. Pedestals are then taken with the decaying current included. Likewise, triggered readouts due to real events are handled in an identical manner. Thus, on-line pedestal subtraction on the VARC removes the effect from the data before it is read out. Pedestal widths taken in this manner are ~ 3 ADC counts (out of 16k). This completely consistent with the natural pedestal width of the system; no addition pedestal width is incurred by this procedure.

4.2.3 Offset adjustment

Each channel of input receiver has an offset adjustment potentiometer (not shown in schematic). This is set to optimize the location of the pedestal within the dynamic range of the adc. Typically, the VMMs are adjusted so that the VA chip's pedestal lies at approximately 500 ADC counts out of 16,384.

4.3 Printed circuit board

The VMM is a 2.00" x 6.00" four layer printed circuit board as shown below.

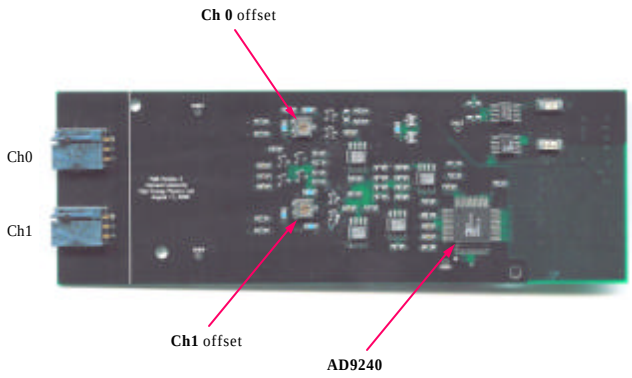


Figure 9-VMM Assembly

5 Power Distribution Panel

The Power Distribution Panel (PDP) is situated in the Electronics Rack and distributes power to up to 36 VFBs located at the Muxboxes some 20' away. The PDP is physically packaged into a 4U rack mounted enclosure with output connectors on the front panel. The PDP also provides connections for global grounding of the far detector front as described below.

5.1 Grounding

VFB power is transmitted via 26' cables which incur voltage drops in their power lines and their returns. These drops are of order 100mv or so in each leg. In order to maintain the VFBs at ground potential, the PDP bulk power supplies are floated with respect to ground. The cable shields are then used to tie the VFB's ground to the PDP ground. Since the cable shields carry no current, zero potential difference between VFB and PDP is maintained. The grounding scheme is shown in Figure 10.

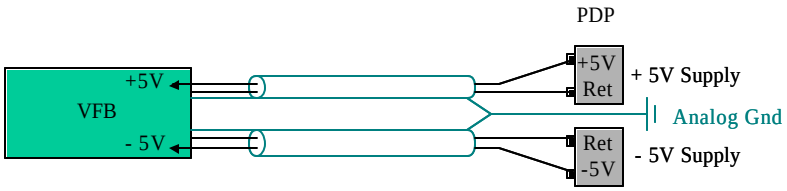


Figure 10-VFB Grounding

Each VFB is attached to its respective Muxbox by screws which carry its ground to the Muxbox case. Thus to avoid ground loops, each Muxbox is mounted to its rack by means of insulated mounting hardware.

5.1.1 Grounding strip

The rear panel of the PDP has a mounting strip which carries Analog (or "Clean") ground. This Clean Ground is isolated from the chassis of the PDP and is connected to the cavern ground system at one point. ***In the MINOS Far Detector, the structural steel is considered to function as "Clean GND".***

5.1.2 VARC grounding

In order to insure that VFBs and VARCs communicate properly, their respective grounds must be within a few hundred millivolts of each other. ***This is insured by tying the VARC crate backplane ground to the Grounding Strip on the back of the PDP***. This insures that VARC and VFB grounds are within millivolts of each other. Note that the VARC / VFB control cable contains no dc ground conductors as these would constitute an additional ground loop.

5.1.3 Safety ground

In normal operation, the power supply returns within the box are constrained to be of order ~100mv different from Clean Ground to account for the power cable ground drops. In the case that no VFBs are plugged in, the constrain is removed and the supplies are floating. Under these circumstances, series diodes on the PDP prevent the supplies from floating more than two diode drops (~ 1.5 V) from Clean Ground.

5.1.4 Grounding straps

In normal operation, the Muxboxes are constrained to be a zero potential. In the case that the power connector is not attached, this constraint is removed. In this case, the Muxbox high voltage connectors provide a separate path from the Muxbox to ground through 1k resistors in the Muxbox. As a secondary safety measure, a ground strap with 1k resistor taps to each Muxbox may be connected back to the Clean Ground terminal strip on the back of the PDP. Alternatively, this strap may be connected to the local steel structure at the site of the Muxbox.

5.2 Front Panel

The front panel is a six layer printed circuit board which busses the +/- 5 V power and their returns to each of the 36 connectors. The front panel power connector is shown below. The colors in the diagram correspond to the conductors in the PDP/VFB power cable.

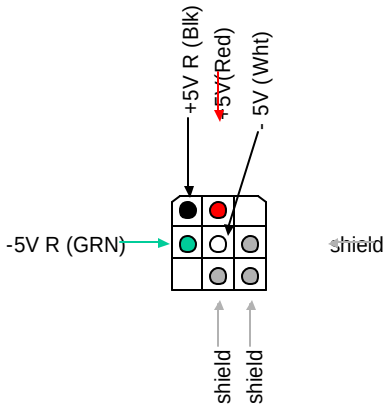


Figure 11-PDP Front Panel Connector

Each connector's power lines is fused (@750 ma) by a fuse which resides in a holder on the back side of the panel. In addition, each connector is associated with a two color LED to monitor its fused supply lines. The + 5 V and – 5 V supplies are connected to red and green LEDs respectively. Thus the state of the LED is as follows.

LED Color	**Condition**
Amber	Both supplies/fuses ok
Green	Blown - 5 V fuse
Red	Blown + 5 V fuse
Off	Both fuses blown

Replacing a blown fuse is possible but not easy as the front panel must be removed for this operation.

5.3 Monitor Connector

In addition to the power switch and grounding strip, the PDP's back panel contains a miniature D type connector for monitoring voltages and temperature. The connections are shown below.

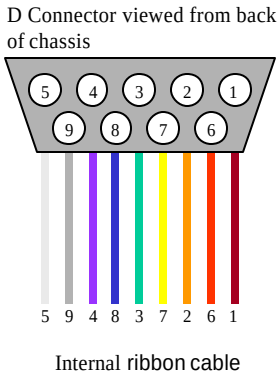


Figure 12-PDP Monitor Connector

Pin assignments are shown below.

Pin no	Signal
1	+ 5 V & temp sense (positive)
2	+ 5 V return
3	nc
4	- 5 V
5	- 5 V return
6	nc
7	Temp sense (negative)
8	nc

5.3.1 Temperature sensor

The temperature sensor is an AD590 from Analog Devices which is placed in the center top of the enclosure. Its primary function is to allow detection of cooling fan failure.

5.4 Internal connections

5.4.1 DC connections

Internal DC connections are shown below

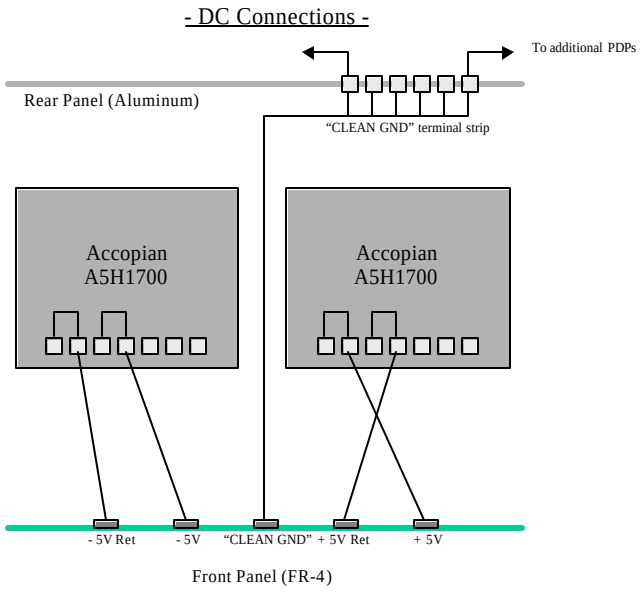


Figure 13-PDP DC Connections

5.4.2 AC connections

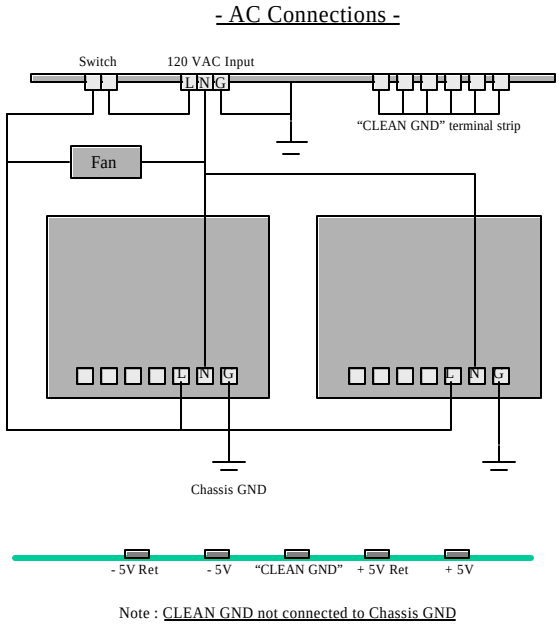


Figure 14-PDP AC Connections

5.5 Cooling air flow

The PDP rear panel has a 4” diameter fan drawing air out of the enclosure. Since the top and bottom of the PDP may be obstructed by other objects in the rack, primary input cooling air comes through an array of ½” diameter holes in the PDP front panel, and three 1” holes on the PDP side panels as shown in Figure 15.

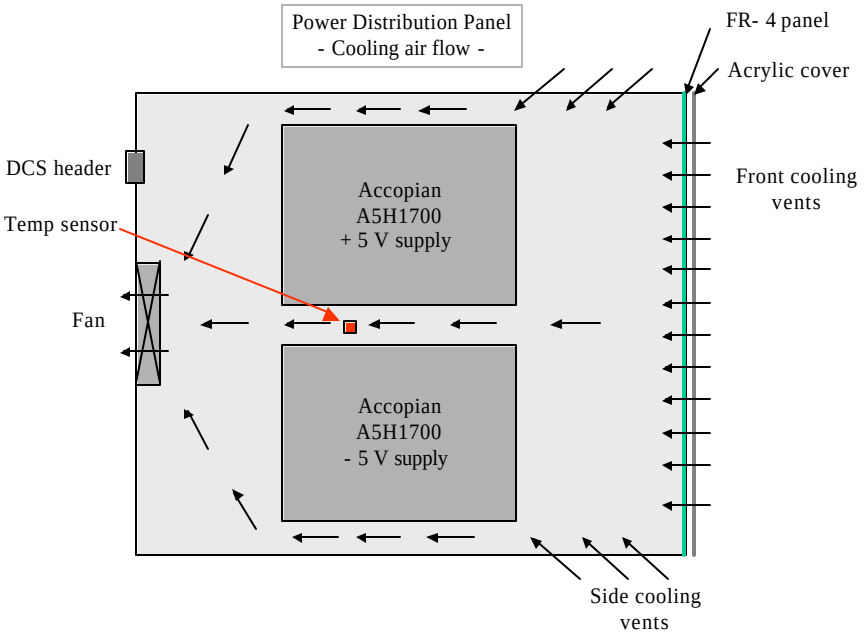


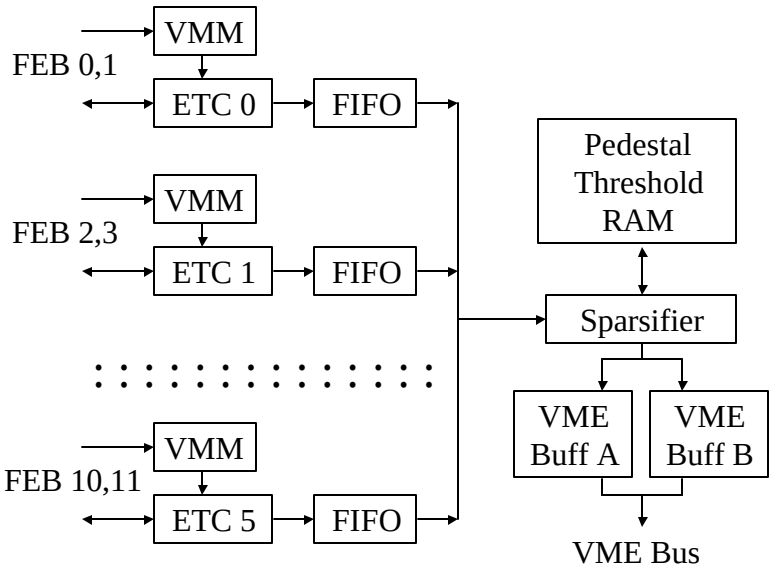
Figure 15-PDP Cooling

6 VARC

6.1 Overview

The purpose of the VARC (VA Readout Controller) in the MINOS far detector is to coordinate the readout process of the VA chips, which reside on the VFB (Varc Front end Board). The ROP (Read Out Processor) controls the VARC using various registers accessed via VME. The VARC in turn will control the operations of the VFB and VA chips. The Analog VA chip data, digitized by the VMM (Varc Mezzanine Module), is timestamped, processed and sparsified by the VARC and made available for VME readout for the ROP.

Each VARC can handle 12 VFBs or 36 VA chips. Two VFBs are paired and correspond to one VMM and one ETC (Event Timestamp Controller). The VMM is responsible for the VA chip Analog to digital conversion. In response to a trigger from the VFB, the ETC timestamps and coordinates the VA chip readout. Each VARC has six ETC / VMM pairs. The data from each ETC is buffered with one of six FIFOs. One Sparsifier processes the data from all six FIFOs. The data is then sent from the Sparsifier to one of two VME Buffers where it is read out via VME. A diagram of the data flow through the VARC can be seen in Figure 16.This figure shows all of the major components of the VARC with exception of the Master clock, Slow-Controls and VME Interface chipset.



Data flow from VFB to VME

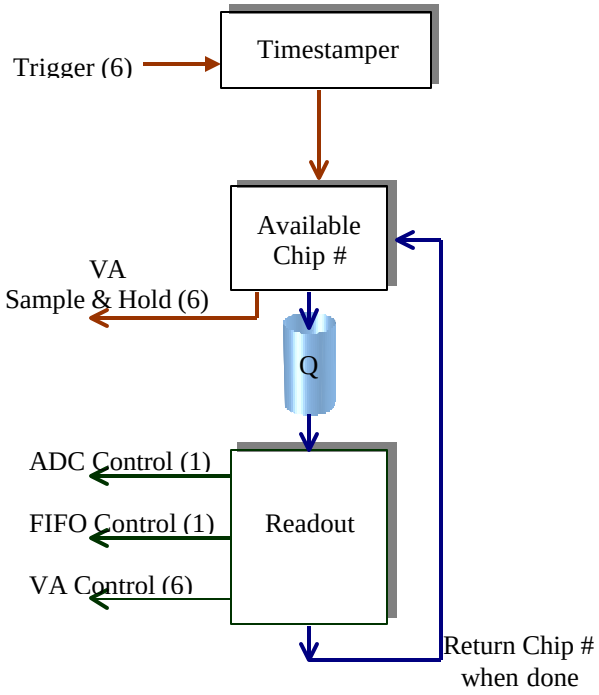
Figure 16-VARC Block Diagram

6.2 ETC (Event Timestamp Controller)

Each VARC has 6 ETCs. Each ETC has the task of coordinating the readout process of 2 VFBs or 6 VA chips. The functional subsections of this FPGA include the Timestamp, Readout Controller and some Error Checking. The I/O includes dynode trigger inputs, VA control, FIFO control, ADC control and VME interface I/O.

6.2.1 ETC Data Flow

Figure 17 shows the data flow diagram of the ETC. The ETC coordinates the digitization and readout of the data from the VA chips to the VARC FIFO. The readout process is initiated with a dynode trigger from the VFB. The ETC receives 6 triggers, one trigger for each VA chip it handles. In response to a VFB trigger, the ETC checks to see if the chip is in a readout process or waiting to be read out. If the VA Chip is not currently busy, the VA chip is sent the sample and hold command. The hold signal is always sent at a predetermined amount of time after receiving the dynode signal. This peaking time is set in the SAMPLE_DELAY_REGISTER. The timestamped event then gets queued and waits until the readout resources are free to process the data from the VA chip. Each ETC can read out only one VA chip at a time. After all of the VA chip data has been shipped off to the Sparsifier via a FIFO; the VA chip is then considered available for another readout. Dynode triggers that arrive while a chip is waiting to be read out are ignored.



Data Flow of the Event Timestamp Controller (ETC)

Figure 17-ETC Block Diagram

6.2.2 Timestamp Design

Immediately upon receiving a trigger from the VFB, the event is timestamped. We have come up with a unique method of using a FPGA to achieve 1.5625 ns bins which utilizes the Delay Locked Loop (DLL) capability of the Xilinx Virtex FPGA.

The timestamp design uses a 40 MHz clock that is doubled to 80 MHz with a DLL internal to the FPGA. Using a second DLL we can get four phases of this 80 MHz clock. The trigger input is then registered at each phase and decoded giving us 3.125 ns bins. Delaying the trigger by 1/2 bin with an external RC delay and using the delayed trigger as an input into a second timestamp circuit made an improvement to this design. The delayed trigger has the effect of cutting the bin size in half. The diagram for this circuit cam be seen in Figure 18.The decoded bits are combined with a coarse counter counting at 80 MHz. The result is a timestamp which rolls-over every second with a bin size of 1.5625 ns.

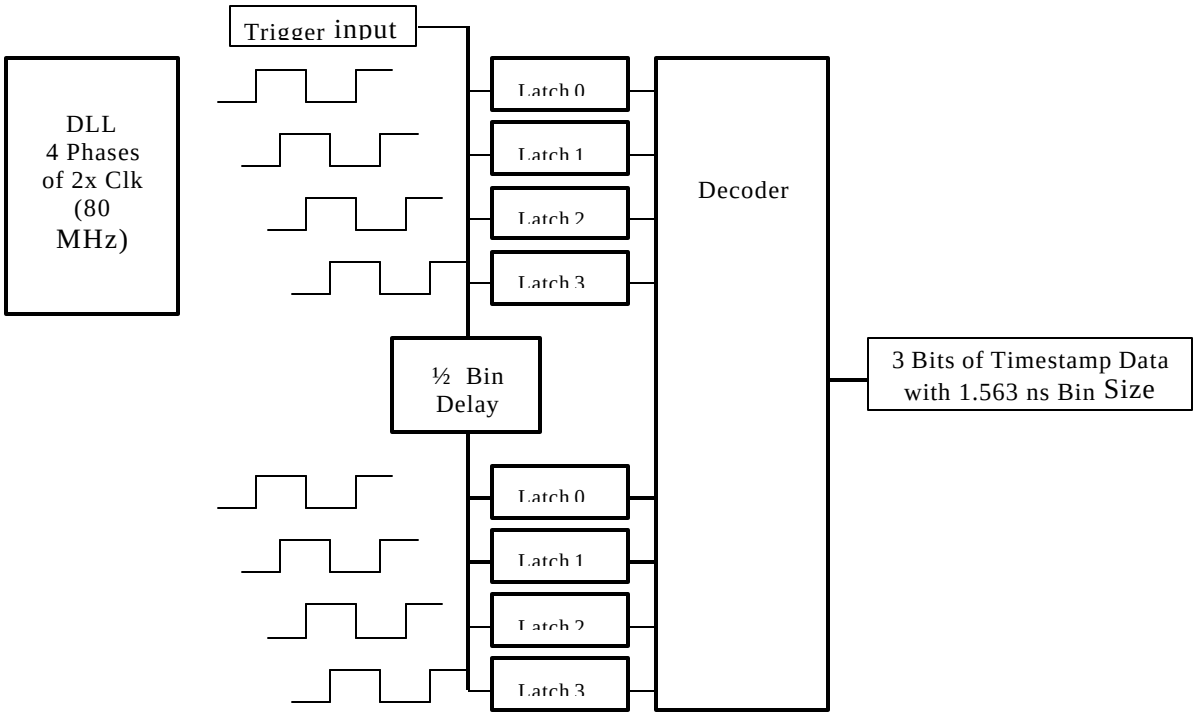


Figure 18-Timestamp Operation

6.2.3 Modes of Operation

Each ETC will be set to operate under one of four modes of operation. The mode of each ETC will determine the procedure of data processing for two VFBs. The modes of operation are Normal, Cal-Inject, Triggerless-pedestal and Disabled. Each chip has an individual register to select its mode. Since each ETC's running mode only effects that particular ETC and its corresponding VFBs, the ETCs on one VARC can be running in different modes. Specific register information concerning the mode of operation can be found in the in the section on registers.

The mode is changed using the ETC's CONTROL register. When the mode of operation is changed, the VARC will disable all triggers and finish processing the current event. In order to have all of the VARCs synchronized at the start of a run, the ETCs will enable the dynode triggers only after the first VME readout buffer swap signal.

6.2.3.1 Normal

In Normal mode, readout of a particular VA chip is initiated by the corresponding dynode trigger signal. In this mode, a specific VA chip on a VFB can be disabled using the CHIP_TRIG_ENABLE register.

6.2.3.2 Cal-Inject

The cal-inject gives us a way of injecting charge into a selected channel and reading this charge with the DAQ. Using the slow controls we can adjust the amount of charge injected. In this manner, we can observe certain system characteristics such as a VA chip gain for a particular channel. When the VFB is connected to the MUX box it has been found that the high voltage needs to be on for proper cal-inject results. If the high voltage is not on, the anode charge buildup protection diodes on the PMT base are not properly biased and will eat our cal-inject charge. The common mode correction, sparsification and pedestal subtraction are automatically disabled during cal-inject mode, just as it is in the triggerless-pedestal mode. There are two methods for producing Cal-Inject data, automatic and single-shot, specified in the ETC's CONTROL register

6.2.3.3 Automatic

In automatic mode, two things need to be set up on the VARC prior to injection, pulse height and chip selection. Writing to the slow controls sets the pulse height. The ETC does not need this information. Chip selection is set up using the CHIP_TRIG_ENABLE as a mask register. Each bit has the effect of enabling its corresponding chip. The VARC will perform cal-injects by sequentially cycling through all channels of all enabled chips. After setup, each cal-inject operation is triggered asynchronously by the global XQT signal, which is part of the system clock. Specifically, in response to the XQT signal, the VARC issues the Cal-Inject signal. This causes charge to be injected into both the VA chip and the ASD-lite trigger chip. The charge injected into the ASD-lite is a fixed charge and is not pulse height dependent. This will produce a trigger output back to the VARC that responds by initiating a readout cycle in a normal manner. To reduce the effect of data being corrupted with triggers from real events, the ETC will open a trigger window when it expects to receive a trigger back from the ASD-lite. The automatic method of cal-injects greatly reduces the amount of VME traffic needed to complete many cal-inject operations.

In this mode of operation we should expect to see one 64-bit data word for every XQT signal. The data sequence in the output buffer of coarse depends on the chips that are enabled in the CHIP_TRIG_ENABLE register and which mode each ETC is in. If all chips are enabled and every ETC is in auto cal-inject mode, the data words in the output buffer will be organized as follows:

VFB0 Chip0 Channel0

VFB2 Chip0 Channel0

VFB4 Chip0 Channel0

: : : : : : : : : : : : : : : : :

VFB10 Chip0 Channel0

VFB0 Chip1 Channel0

VFB2 Chip1 Channel0

: : : : : : : : : : : : : : : : :

VFB10 Chip1 Channel0

VFB0 Chip1 Channel0

VFB2 Chip1 Channel0

: : : : : : : : : : : : : : : : :

VFB10 Chip2 Channel0

VFB1 Chip0 Channel0

VFB3 Chip0 Channel0

VFB5 Chip0 Channel0

: : : : : : : : : : : : : : : : :

VFB11 Chip2 Channel0

VFB0 Chip0 Channel1

VFB2 Chip0 Channel1

VFB4 Chip0 Channel1

The pattern of the VFB results from the fact that two VFBs are paired with one ETC. The Sparsifier sequentially scans each ETC producing the even and odd VFB pattern. One caveat is that the Sparsifier is always scanning for data packets. This means that the first even VFB number might not be 0. If the first VFB is not 0, it will follow VFB 10. Still, all even VFBs are grouped together and all odd VFBs are grouped together. Following the VFB even and odd groups, the next thing to be incremented is the chip number. The chip number will be incremented after a group of even VFBs and after a group of odd VFBs. After all chips for a given VA channel are processed, the channel number is then incremented and the pattern is repeated.

6.2.3.4 Single-shot

The single shot method is similar to the automatic mode except charge is injected into only one channel of one chip. The cal-inject event is initiated with the writing of the VME register CAL_TRIG_XQT_CTRL and no XQT signal is required. This method will be useful for testing where a simple cal-inject is desired.

In this mode of operation we should expect to see one 64-bit data word every time CAL_TRIG_XQT_CTRL is written to.

6.2.3.5 Triggerless-Pedestal run

The different channels of the VA chips will inherently have a certain offset or pedestal. The data we read from a channel with no charge will still have a number of ADC counts above zero. The offsets of one VFB can be adjusted as a whole with the VMM; however, we have no control over the differences from channel to channel.

When we want to determine the pedestals for a VA chip we need to read the channels of the VA chip with no charge. This means we need to read out the VA chip in the absence of a dynode trigger. In a triggerless-pedestal run, a VA readout cycle is initiated without the need for a trigger signal from the ASD-lite trigger chip. When enabled in normal run mode, the pedestals will be subtracted from the ADC data resulting in a pedestal offset of 0. The common mode correction, sparsification and pedestal subtraction are automatically disabled during triggerless-pedestal mode just as it is in the cal-inject mode. There are two methods for producing a triggerless-pedestal run, automatic and single-shot specified in the ETC's CONTROL register. For more information on pedestal subtraction please see section 5.1.1 below

6.2.3.6 Automatic

In automatic mode, the triggerless-pedestal operation is triggered asynchronously by the global XQT signal, which is part of the system clock. Specifically, in response to the XQT signal, the VA controller internally issues a trigger signal just as if it had been produced by a dynode, initiating a readout cycle in a normal manner. In this mode the VARC will cycle through all enabled VA chips performing a triggerless-pedestal operation on one chip for every XQT signal it receives. Chip selection is set up using the CHIP_TRIG_ENABLE as a mask register.

Since the triggerless-pedestal does not use a trigger from the dynode, the resolution of the timestamp is limited to 25ns. This should not be a concern.

In this mode of operation we should expect to see 22 64-bit data words for every XQT signal, times the number of ETCs that are in auto triggerless-pedestal mode. The data pattern we will see in the output buffer is the same as that described in the automatic cal-inject. The only difference is when doing a triggerless-pedestal run we will see all of the chip's channels grouped together for every XQT.

VFB0 Chip0 All channels

VFB2 Chip0 All channels

VFB4 Chip0 All channels

: : : : : : : : : : : : : : : : :

VFB10 Chip0 All channels

VFB0 Chip1 All channels

VFB2 Chip1 All channels

: : : : : : : : : : : : : : : : :

VFB10 Chip1 All channels

VFB0 Chip1 All channels

VFB2 Chip1 All channels

: : : : : : : : : : : : : : : : :

VFB10 Chip2 All channels

VFB1 Chip0 All channels

VFB3 Chip0 All channels

VFB5 Chip0 All channels

: : : : : : : : : : : : : : : : :

VFB11 Chip2 All channels

VFB0 Chip0 All channels

VFB2 Chip0 All channels

VFB4 Chip0 All channels

As in the cal-inject, the pattern of the VFB results from the fact that two VFBs are paired with one ETC. The Sparsifier sequentially scans each ETC producing the even and odd VFB pattern. One caveat is that the Sparsifier is always scanning for data packets. This means that the first even VFB number might not be 0. If the first VFB is not 0, it will follow VFB 10. Still, all even VFBs are grouped together and all odd VFBs are grouped together. Following the VFB even and odd groups, the next thing to be incremented is the chip number. The chip number will be incremented after a group of even VFBs and after a group of odd VFBs. After all chips for a given VA channel are processed, the pattern is repeated.

6.2.3.7 Single-shot

The single shot method is similar to the automatic mode except pedestals are read out from only one VA chip. The triggerless-pedestal event is initiated with the writing of the VME register CAL_TRIG_XQT_CTRL. No XQT signal is required. This method will be useful for testing where a simple triggerless-pedestal of one set of VA chips is desired.

In this mode of operation we should expect to see 22 64-bit data words for every chip we request a triggerless-pedestal from every time CAL_TRIG_XQT_CTRL is written to.

Disabled

When the VARC is in Disabled mode it will ignore the dynode triggers it receives from the VFBs. While it is in this mode it will be in a quiescent state. Access to registers and memory is still valid in this mode. Since the running mode is set in the ETC, each ETC being disabled only effects that particular ETC and its corresponding VFBs. Other ETCs can be in a different mode.

6.3 ETC to Sparsifier Data FIFO

For each ETC the VARC uses a 1K FIFO to buffer data being read out by the ETC. This FIFO has the capacity to hold 40 complete events. The Data flows from the ETC to the FIFO where it waits to be processed by the Sparsifier. The Sparsifier has the capability of processing events at the rate of ~250 KHz.. Since all of the ETCs working together can fill the FIFOs faster then they can be drained, it is possible to create a

situation where the VARC runs out of buffer space in the FIFOs. When a FIFO fills up to a point where it can only hold 6 more events, it will flag that it is almost full. The corresponding ETC will see this and stop accepting any new dynode triggers. The almost full flag is set to 6 because this is the maximum number of words that can be in the ETC's queue. Any queued triggers are guaranteed to have a normal readout. The only difference is that they will be tagged with a FIFO almost full flag, which will be seen in the output data. When this flag is seen, it is likely that data in the following 144μs has been lost. The 120μs is the result of the Sparsifier's round-robin approach to draining the FIFOS.

The FIFO data packet consists of a header, timestamp information and digitized VA channel data. In each case the 2 most significant FIFO bits will designate what the remaining 16 bits represent. These 2 designation bits will always be under the control of the ETC. The header information includes chip number, VFB selection, error code and ETC mode. The timestamp data needs to be split into a lower word and upper word to accommodate the number of timestamp bits. The coordination of the data from the VA chip to the FIFO data packet will be handled by the ETC. The 2 most significant FIFO bits will designate the last VA channel read out as such, completing the FIFO data packet. The data packet can be seen in Table 1.

		Fifo data bits																	
	09-Aug-01	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Header	0	0	EC	x	x	C4	C3	C2	C1	C0	x	x	x	HC1	HC2	SEL	VA1	VA0
1	Timestamp	0	1	Time stamp lower															
2	Timestamp	0	1	Time stamp upper															
3	ADC Data Ch0	1	0	0	OTR	ADC_ch0 (unbonded)													
4	ADC Data Ch1	1	0	0	OTR	ADC_ch1 Common mode reference													
5	ADC Data Ch2	1	0	0	OTR	ADC_ch2 PMT Anode													
6	ADC Data Ch3	1	0	0	OTR	ADC_ch3 PMT Anode													
7	ADC Data Ch4	1	0	0	OTR	ADC_ch4 PMT Anode													
8	ADC Data Ch5	1	0	0	OTR	ADC_ch5 PMT Anode													
9	ADC Data Ch6	1	0	0	OTR	ADC_ch6 PMT Anode													
10	ADC Data Ch7	1	0	0	OTR	ADC_ch7 PMT Anode													
11	ADC Data Ch8	1	0	0	OTR	ADC_ch8 PMT Anode													
12	ADC Data Ch9	1	0	0	OTR	ADC_ch9 PMT Anode													
13	ADC Data Ch10	1	0	0	OTR	ADC_ch10 PMT Anode													
14	ADC Data Ch11	1	0	0	OTR	ADC_ch11 PMT Anode													
15	ADC Data Ch12	1	0	0	OTR	ADC_ch12 PMT Anode													
16	ADC Data Ch13	1	0	0	OTR	ADC_ch13 PMT Anode													
17	ADC Data Ch14	1	0	0	OTR	ADC_ch14 PMT Anode													
18	ADC Data Ch15	1	0	0	OTR	ADC_ch15 PMT Anode													
19	ADC Data Ch16	1	0	0	OTR	ADC_ch16 PMT Anode													
20	ADC Data Ch17	1	0	0	OTR	ADC_ch17 PMT Anode													
21	ADC Data Ch 18	1	0	0	OTR	ADC_ch18 (PIN diode)													
22	ADC Data Ch 19	1	0	0	OTR	ADC_ch19 Common mode reference													
23	ADC Data Ch 20	1	0	0	OTR	ADC_ch20 Common mode reference													
24	ADC Data Ch 21 (EOI	1	1	0	OTR	ADC_ch21 Common mode reference													

Note: EOR code (1,1) used only once at End Of Record

OTR indecates the analog input is out of the range of the ADC
During Cal-inject C[4:0] is channel number

HC 00 - not defined
HC 10 - Cal-nj
HC 01 - Trig-ped
HC 11 - Normal Run

EC In Normal Mode
0- FIFO is OK
1- FIFO is almost full
EC In Cal-Inject Mode
0- Cal-inject data is OK
1- No dynode trigger received from Cal-inject operation

Table 1

6.4 Sparsifier

The Sparsifier has two modes of operation, run mode and test mode. The mode is controlled using the Sparsifier's CONTROL register.

6.4.1 Run Mode

Run mode is the normal operating mode of the Sparsifier. When in this mode the Sparsifier will process data and send it along to the VME readout buffer. The Sparsifier will take data from the 6 FIFOs in a round-robin fashion only when a complete event is in

a FIFO. It will take the Sparsifier ~3.3us to read and process one event from a FIFO. The processing options are pedestal subtraction, common mode correction and sparsification. The processing method is set in the Sparsifier's CONTROL register.

6.4.2 Pedestal Subtraction

The different channels of the VA chips will inherently have a certain offset or pedestal. The data we read from a channel with no charge will still have a number of ADC counts above zero. The offsets of one VFB can be adjusted as a whole with the VMM; however, we have no control over the differences from channel to channel.

When we want to determine the pedestals for a VA chip we simply do several triggerless-pedestals and use an average of the ADC values read. It is possible for ADC data during a triggerless-pedestal run to become corrupted by charge from an actual event. This should be rare but still identifiable. For a detailed explanation on doing a triggerless-pedestal run refer to the section 3.3.3 above.

Once the pedestal values have been determined they need to be written to the pedestal RAM on the VARC. Each channel on every VA chip has a corresponding pedestal value. While in normal run mode the pedestal RAM value is subtracted from the channels ADC value. The result is ADC values of all channels having an offset of zero. The user has the option of disabling pedestal subtraction. The VARC will automatically disable pedestal subtraction during a triggerless-pedestal and cal-inject run. For a detailed explanation on writing to the pedestal RAM, refer to the section 9 below.

6.4.3 Common Mode Correction

When reading ADC values there will be inherent noise in the system. It has been found that a portion of the noise changes the ADC values of every channel on one VA chip by the same amount. This is known as common mode noise. We can subtract the common noise from the ADC values of the channels we are reading thereby reducing the effect of the noise. This is known as the common mode correction. The common mode noise is found by taking the average of ADC values from channels that are not bonded to pads on the VA chip. These channels are 1, 19, 20 and 21.

The common mode correction is done entirely on the VARC. The user simply will need to enable or disable the correction.

6.4.4 Sparsification Threshold

There are two types of settings that are considered thresholds, the dynode threshold and the sparsification threshold. The dynode threshold is set on the VFBs using the slow controls. This is the first condition that must be satisfied before the VFB triggers a readout. The other threshold is used for data sparsification. Since this involves the digitized anode signal you might refer to this as the anode threshold. When the VARC receives a trigger from the VFB it will read all of the channels from the corresponding VA chip. Since we will only be interested in channels that have charge, we can use sparsification as a way to discard data we are not concerned with. During sparsification, the VA channel's ADC value is compared to its corresponding sparsification threshold.

If the ADC value is less than or equal to the threshold, the data is discarded. Sparsification is done after Pedestal subtraction and common mode correction Using the sparsification in the in this manner will greatly reduce the amount of data being transferred via VME. If desired, the user can disable sparsification to read the ADC data from every channel regardless of the value.

Each channel in every VA chip has its own sparsification threshold stored in the threshold RAM similar to the pedestal RAM. It is the responsibility of the user to determine the threshold values and write them to the memory on the VARC. For a detailed explanation on writing to the threshold RAM, refer to the section 9 below.

6.4.5 Test mode

The Sparsifier includes a test pattern generator that can be used to load the output buffer with a known test pattern. This test pattern can then be read via VME to check for errors and test the transfer rate of the VME interface. The test mode is set in the Sparsifier's CONTROL register.

The buffers cannot be accessed while they are busy being written to and only one buffer can be written to at once. The buffer status can be read from the status register in the Sparsifier. This register should be checked before a test pattern is written and before the test pattern is read. The control register in the Sparsifier selects test mode and selects which buffer the test pattern will be written to. The control register also initiates the writing of the test pattern.

The pattern written to the buffers is a 1 shifted left through 32 bits followed by a long word, which is incremented. The incremented long word is actually 1 word, which is just duplicated in the upper word and lower word. This can be seen in Table 2.

```
0000 0000 0000 0000 0000 0000 0000 0001     <Shift Left
0000 0000 0000 0000 0000 0000 0000 0010     <Shift Left
0000 0000 0000 0000 0000 0000 0000 0100     <Shift Left
. . . . . .
. . . . . .
0100 0000 0000 0000 0000 0000 0000 0000     <Shift Left
1000 0000 0000 0000 0000 0000 0000 0000     <Shift Left
0000 0000 0000 0001 0000 0000 0000 0001     <Increment Count
0000 0000 0000 0000 0000 0000 0000 0001     <Shift Left
0000 0000 0000 0000 0000 0000 0000 0010     <Shift Left
. . . . . .
. . . . . .
0100 0000 0000 0000 0000 0000 0000 0000     <Shift Left
1000 0000 0000 0000 0000 0000 0000 0000     <Shift Left
0000 0000 0000 0010 0000 0000 0000 0010     <Increment Count
```

```
0000 0000 0000 0000 0000 0000 0000 0001     <Shift Left
0000 0000 0000 0000 0000 0000 0000 0010     <Shift Left
. . . . . . . . . . . . . . . . . . . . .
. . . . . . . . . . . . . . . . . . . . .
0100 0000 0000 0000 0000 0000 0000 0000     <Shift Left
1000 0000 0000 0000 0000 0000 0000 0000     <Shift Left
0000 0000 0000 0011 0000 0000 0000 0011     <Increment Count
0000 0000 0000 0000 0000 0000 0000 0001     <Shift Left
0000 0000 0000 0000 0000 0000 0000 0010     <Shift Left
. . . . . . . . . . . . . . . . . . . . .
```

Table 2

6.5 VME Output buffer

The Sparsifier uses 2 32k long-word RAM to buffer the data that is ready to be read out by the VME processor. The RAM is split in two, buffer A and buffer B. When the VARC is writing to one buffer the other is free to be read via VME. When a buffer is busy being written into it is not available for VME access. Each data packet can be read out using two long-word transfers or one 64-bit transfer. This data includes information such as chip ADC data, timestamp data and which channel the data came from. The data packet is shown in Table 3.

Last modified
16-Jul-01

	ID																														
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Upper LWORD	1	P	EC	VID1	VID0	F2	F1	F0	SEL	VA1	VA0	MUX[4:0]					HC	ADC data														
Lower LWORD	0	P	TS[29:16] Time Stamp Upper														TS[15:0]Time Stamp Lower															

ID	Data Identifier : 0 = timestamp, 1 = ADC address, data
P	Parity (including ID)
HC	0 = Data is from a cal-inject or triggerless pedestal, 1 = Data is from a dynode trigger in normal operating mode
F[2:0]	ADC channel address (one of six ETCs)
SEL	Input mux address (one of two)
VA[1:0]	VA chip select (one of three)
MUX[4:0]	VA channel address (one of 22)
ADC[14:0]	2's complement ADC data
VID[1:0]	Identify VARC in crate
TS[29:0]	Time-stamp
Error code	
EC	**In Normal Mode**
	0- FIFO is OK
	1- FIFO is almost full
EC	**In Cal-Inject Mode**
	0- Cal-inject data is OK
	1- No dynode trigger received from Cal-inject operation

Table 3

6.6 Master Clock and Slow Control interface

The Master Clock and Slow Control interface is implemented using one Xilinx Spartan FPGA. Since this FPGA is not a Vertex type, as is the ETC and Sparsifier, we

are required to use a dedicated configuration PROM just for this chip. The serial PROM we use for this is an 8 pin DIP.

6.6.1 VARC Master Clock

The Master Clock basically takes care of all clock signals on the board. Since we want all of the VARC boards to operate synchronically, the clocks will be provided to the board via the J3 backplane. If we are running without signals from the J3 backplane the Master clock will automatically detect the absence of clocks on the backplane and generate the clocks internally. There is also a bit in the Master clock to force the clocks to be generated internally.

6.6.2 40 MHz Clock

You guessed it! The 40 MHz clock signal is in fact, a 40 MHz clock.

6.6.3 VME buffer switch signal

The 50ms buffer switch signal is used in conjunction with the VME output buffers. This signal has a period of 100ms and a duty cycle of 50%. The purpose of this signal is to coordinate the readout of the two VME output buffers by selecting which buffer is being filled with new data and which buffer is being emptied via VME. Each time the buffer is switched the readout processor will be issued a VME interrupt by the clock module. When the clock module is not present to provide the interrupt, the readout processor will need to poll the status of the VARC register BUFFER_LEVEL_U to determine the buffer synchronization.

The buffer switch signal will also synchronize the startup of all of the VARC boards. When the mode of operation is changed, the VARC will disable all triggers and finish processing the current event. The ETCs will enable the dynode triggers only after the first VME readout buffer swap signal.

6.6.4 One second signal

This clock signal is used to synchronize the timestamps between the VARC boards. On the rising edge of this pulse, the timestamp counter will be reset to 0. This will occur every second.

6.6.5 Execute AKA XQT

This signal is meant to coordinate different modes of operation on the VARC. During Cal-Inject or Triggerless-Pedestals all of the boards can be set to automatically carry out an operation synchronously for every XQT signal they see. This gives us an easy way to perform many operations automatically with little effort. Since the Cal-

Injects will be done asynchronously with every XQT, adjusting the phase of the XQT with respect to the 40 MHZ clock will give us system timing information.

6.7 Slow Control

The Slow Control is used to monitor voltages and change settings on the VFBs. Each VFB has its own Slow-Control settings. These settings are responsible for changing the operating parameters for the three VA chips on each VFB. Since this will be done relatively infrequently the speed is not a concern. There is a detailed explanation on use of the slow controls in section 10.2.

6.7.1 VFB Bias and Thresholds

The Slow control address used to adjust the bias settings can be determined using the VFB number and the parameter you want to set. This gives you control over Vfp,Vfs, Sha-bias, trigger threshold and cal-inject charge. Each VFB can have different setting but the settings on one VFB will effect the operation of three VA chips. The setting of VFB threshold and bias setting for each VA chip cannot be individually set.

There are two types of settings that are considered thresholds, the dynode threshold and the sparsification threshold. The dynode threshold is set on the VFBs using the slow controls. This is the first condition that must be satisfied before the VFB triggers a readout. Each VFB has one value that is specific to that VFB. The other threshold is used for data sparsification. Since this involves the digitized anode signal you might refer to this as the anode threshold. For more information on the sparsification threshold please refer to the Sparsifier section.

6.7.2 VEB Voltage Disables

Using the voltage disable, the voltage regulators on the VFB can be disabled. This controls the +3.3 V ASD supply, +2.5 V Rail, -2.5 V Rail for VA Chip 0, -2.5 V Rail VA for Chip 1 and -2.5 V Rail for VA Chip 2.

6.7.3 Monitoring VFB Voltages

The VFB contains a 12 bit ADC for monitoring the voltages and temperature on the VFB. The Voltages that can be monitored are the ground plane voltage, ASD +3.3 V supply voltage, positive VA chip rail, negative VA chip rails and temperature. There are handy magic formulas in section 10.2.6.2 that simplify the conversion from ADC value to a value in useable units.

6.7.4 Slow control test

The Master Clock has a Test register that when enabled a test pattern can be written to the serial communication lines of VFB0 and VFB1. This feature will only be used during VFB testing and should otherwise remain in the default disabled state.

6.8 VME interface

The VARC uses a VME interface chipset from Cypress. A special consideration must be met when doing block transfers with this interface. The chipset is not capable of block transfers that cross 256-byte boundaries; therefore, the VME interface must reissue the VME address at every 256-byte boundary. This is a problem that makes the cypress interface not truly VME64 compliant.

6.8.1 Pedestal and Threshold memory

Once the pedestal and threshold has been determined for each channel of each chip, the value must be written to the memory on the VARC.

Since this memory is not dual-ported, you will not be able to write to this memory while VA chip data is being processed, this means during run mode, cal-inject operations or triggerless-pedestal operations. It is valid to access this memory when in triggerless-pedestal and cal-inject mode when no data is being processed, as is when in disabled mode. You can only write to this memory when the memory is not otherwise busy. The memory is not busy in disabled mode. The memory is also not busy when in triggerless-pedestal or cal-inject mode when not processing data.

Given the VARC is in the correct operating mode, the memory is accessed with a VME read or write transaction. The mapping of chip channel pedestals and thresholds is a simple one. This does result in holes of unused memory, which we don't care about because this area has memory to spare. The format of the RAM address bits is as follows:

Bit0 Always 0

Bit1 Always 0

Bit[6:2] Select VA Channel 0-21 (1 of 22)

Bit[8:7] Select VA chip 0-2 (1 of 3)

Bit9 Select VFB 0-1 (1 of 2)

Bit[12:10] Select ETC 0-5 (1 of 6)

Bit13
0 Select Threshold

1 Select Pedestal

6.8.2 VME Register definitions

This section contains detailed information on specific register addresses and their specific function. It is intended to be a reference when communicating with the VARC. There are a lot of bits that control the VARC and they are all described here. For detailed examples of register values and suggested configurations, please refer to the VARC Programmers Guide. The Programmers Guide will lead you through the maze of bits for every functional mode of the VARC.

The VARC board address is determined by the physical crate slot it sits in. The J1 uses a VME 64x (5 row) connector providing global addressing. This is five binary encoded bits. The VARC compares these bits to the five most significant bits of the 32-bit VME address when deciding when to respond to a VME request. This is how every VARC can be uniquely identified, depending on the crate slot it is in.

After a VARC has been addressed, it uses a VME address space that is split into logical regions to further categorize each address. The regions and their address range can be seen in Table 4.

Each region is broken down to address registers of each region's device, such as FPGAs and RAM. The actual VME address is a 32 bit value that can be assembled with the board address, region address and register address.

For example, if we wanted to access the control register of the Master clock region of a board that is sitting in the second 9u slot in a MINOS crate, we would use the following address:

second 9u slot in a MINOS crate	address 0x38
Master clock region	address 0x10 00
control register	address 0x18

Therefore, putting it all together the VME address would be 0x3810 0018

VME Interface		Region Decoding	August 9, 2001
Address Range	Region	Width	Function
0x100000 - 0x1000F8	Master Clock	Word	Clock Controller
0x200000 - 0x2001F8	Slow Ctrl	Word	FEB Slow Controls
0x300000 - 0x3000F8	ETC 0	Word	Event Timestamp Controller 0
0x310000 - 0x3100F8	ETC 1	Word	Event Timestamp Controller 1
0x320000 - 0x3200F8	ETC 2	Word	Event Timestamp Controller 2
0x330000 - 0x3300F8	ETC 3	Word	Event Timestamp Controller 3
0x340000 - 0x3400F8	ETC 4	Word	Event Timestamp Controller 4
0x350000 - 0x3500F8	ETC 5	Word	Event Timestamp Controller 5
0x400000 - 0x4000FC	Sparsifier	Word	Event Sparsification
0x500000 - 0x51FFFC	RAM A	L Word	VME Output Buffer A
0x520000 - 0x53FFFC	RAM B	L Word	VME Output Buffer B
0x600000 - 0x601FFC	Threshold Memory	L Word	VA Chip Threshold Memory
0x602000 - 0x603FFC	Pedestal Memory	L Word	VA Chip Pedestal Memory

Table 4

6.8.3 Master Clock Registers

In normal day-to-day VARC operation there should not be a need to modify any Master Clock registers; however, the Master clock FPGA has several features that might be handy in certain circumstances. These registers are listed in Table 5.

MASTER CLOCK FPGA				August 9, 2001
Address	**Register**	**Width**	**Dir**	**Function**
0x00	REVISION	Byte	R	Firmware Version and revision #
0x08	not used	~		
0x10	not used	~		
0x18	CONTROL	Word	R/W	Value determines mode of the FPGA
0x20	STATUS	Byte	R/W	Indicates status of the chip
0x28	not used	~		
0x30	XQT_RATE	Word	R/W	Set the rate the XQT is given when the clocks are generated by the VARC
0x38	GO_XQT	~	W	Generate one XQT
0x40	SLOW_CONTROL_TEST	Byte	R/W	Manual Slow control for FEB 0 and 1

Table 5

6.8.3.1 Revision Register

The byte-wide revision register will contain information on the version of firmware currently loaded in the FPGA. The most significant four bits will indicate the version number. The least significant four bits will indicate the revision number. Both the version and revision numbers start at 1.

6.8.3.2 Control

The Control Register is used to control the operating mode of the Master Clock FPGA. The modes are encoded in the following manner.

Bit0

0 Automatically detect and choose clock on backplane, otherwise generate clock signals internally
1 Force VARC to ignore backplane and generate clock signals internally

Bit1
0 Configure external LEMO connector to be an input
1 Configure external LEMO connector to be an output

Bit2 Enable slow control test mode.

6.8.3.3 Status

This register reports the status of the FPGA and operations.

Bit0 Clock source is backplane

Bit1 Error somewhere on the board. One or more board errors reported by ETCs, Sparsifier and / or the Master Clock itself

Bit2 Slow Control is Busy, repeat of Slow-control status

6.8.3.4 XQT Rate

When the Master Clock is internally generating board clocks, the XQT signal can be periodically issued using this register. The period of XQTs is equal to the register value in units of 100us. This feature is turned off with a register value of 0.

6.8.3.5 Go XQT

When the Master Clock is internally generating board clocks, the XQT signal can be internally generated using this register. Each time this register is written to a XQT signal is generated.

6.8.3.6 Slow_control_test

The SLOW_CONTROL_TEST register is used as manual control of the slow control lines on VFB 0 and 1. This feature will enable a test pattern to be generated with the software during VFB testing and will only be used when this aspect of the VFB is being tested. Manual controlled is enabled with bit 2 in the control register. The slow control bits can be toggled using register 0xbb10 0040. The bits are negative true.

Bit0 /Serial enable VFB0
Bit1 /Serial enable VFB1
Bit2 /Serial clock

Bit3 /Serial data

For example, writing the values 0xA and 0xE toggle the Serial clock of VFB0.

6.8.4 Slow Control Registers

Slow Controls				August 9, 2001
Address	**Register**	**Width**	**Dir**	**Function**
0x1A0	REVISION	Byte	R	Firmware Version and revision #
0x1C0	ADC	12-Bits	R	Read FEB ADCs
0x1E0	Status	Bit	R	Check to see if slow control is busy
0x00-0x160	DC Operation	Byte	W	Write serial Command

Table 6

6.8.4.1 Revision Register

The byte-wide revision register will contain information on the version of firmware currently loaded in the FPGA. The most significant four bits will indicate the version number. The least significant four bits will indicate the revision number. Both the version and revision numbers start at 1.

6.8.4.2 ADC Register

Please refer to the section 10.2.6 below on monitoring VFB voltages.

6.8.4.3 Status

This register reports the status of the FPGA and operations.

Bit0 Slow-Control busy

After every Slow Control interaction the Slow Control will require time to process the command with the VFB. This status bit is used to indicate the Slow Control is busy and currently unavailable to process new commands.

6.8.4.4 Setting the VFB Bias Settings

The Slow control address used to adjust the bias settings can be determined using the VFB number and the parameter you want to set. The address can be established using the following bit structure:

Bit[1:0]

00 Constant

Bit[4:2]
- 000 set Vfp
- 001 set Vfs
- 010 set Sha-bias
- 011 set Trigger threshold
- 100 set cal-inject charge

Bit[8:5] Select VFB number 0 – 11

For example, writing 0x7D to address 0x***bb***20 0008 where ***bb*** is the board address will set the sha-bias on VFB 0 to 0x7D.

6.8.4.5 VFB Voltage Disables

The Slow control address used to power-up the VFB can be determined using the VFB number. The address can be established using the following bit structure:

Bit[1:0]
- 00 Constant

Bit[4:2]
- 110 disable VFB voltages (0x00 will turn on all voltages)

Bit[8:5] Select VFB number 0 – 11

The voltages we want to disable determine the data we write to the given address. The bits correspond to voltages as follows:

Bit0 +3.3 V ASD supply

Bit1 +2.5 V Rail

Bit2 -2.5 V Rail VA Chip 0

Bit3 -2.5 V Rail VA Chip 1

Bit4 -2.5 V Rail VA Chip 2

For example, writing 0x00 to address 0x***bb***20 0158 where ***bb*** is the board address will enable all the voltages on VFB 10.

6.8.5 Monitoring VFB Voltages

The VFB contains a 12 bit ADC for monitoring the voltages on the VFB. The voltages can be obtained in the following manner.

6.8.6 Getting the ADC value

The reading of this ADC is actually a two-step process. First you need to tell the Slow-Control which ADC channel on which VFB you are interested in reading. The Slow-Control then performs the ADC readout and stores the result in the ADC register. This value can then accessed with a VME read operation.

The Slow control address used to access the ADC can be determined using the VFB number. The address can be established using the following bit structure:

Bit[1:0]
  00 Constant

Bit[4:2]
  101 Address ADC

Bit[8:5] Select VFB number 0 – 11

The data we write to the given address is determined by ADC channel we want to read.

0x80	Read ground plane voltage.
0xC8	Read ASD +3.3 V supply voltage
0x98	Positive VA chip rail
0xD0	Negative VA chip 0 rail
0xA0	Negative VA chip 1 rail
0xE0	Negative VA chip 2 rail
0xB8	VFB Temperature

For example, writing 0x98 to address 0x***bb***20 0154 where ***bb*** is the board address will tell the Slow-Control to put the ADC value of the Positive VA chip rail into the ADC register which is 0x***bb***20 01C0.

6.8.6.1 What does that ADC value mean?

After the command to read a VFB voltage has been issued, the ADC value will be stored in the ADC register. The process of converting the ADC value to a number we can use depends on what we are measuring. The ADC register address is 0x***bb***20 01C0.

Ground plane voltage. Obviously this should be right around 0 V

If ADC is => 2048 then the value in volts is = (ADC - 4096) * 0.002

If ADC is < 2048 then the value in volts is = ADC * 0.002

ASD +3.3 V supply voltage

The value in volts is = ADC * 0.001

Positive VA chip rail

The value in volts is = ADC * 0.001

Negative VA chip rails

If ADC is => 2048 then the value in volts is = (ADC - 4096) * 0.002

If ADC is < 2048 then the value in volts is = ADC * 0.002

Temperature

The temperature in degrees C is = (ADC/18.432) – 61.111

6.8.7 ETC Registers

The ETC FPGA has several VME accessible registers used to control its operation. A list of the registers can be seen in Table 7

VA READOUT CONTROLLER FPGA				***August 9, 2001***
Address	***Register***	***Width***	***Dir***	***Function***
0x00	REVISION	Byte	R	Firmware Version and revision #
0x08	RESET_FPGA	~	W	Writing to this register will reset all internal FPGA logic to a post configured state
0x10	RESET_READOUT	~	W	Writing to this register will reset all readout logic but retain the register values
0x18	CONTROL	Word	R/W	Value determines mode of the FPGA
0x20	STATUS	Byte	R/W	Indicates status of the chip
0x28	not used	Byte	R/W	
0x30	not used	Word	R/W	
0x38	CAL_TRIG_XQT_CTRL	Word	R/W	Controls how the Cal-Injects and Triggerless Pedistals are handled.
0x40	CHIP_TRIG_ENABLE	6 bits	R/W	Ignores triggers from all disabled chips. Use this for the cal-inject enable also.
0x48	SAMPLE_DELAY	Byte	R/W	Sets the sample delay to corespond to the VA chip peaking time
0x50	VA_CLOCK_PERIOD	Nibble	R/W	sets the VA readout clock period
0x58	not used			
0x60	ERRORS_REGISTER	Byte	R	Information on readout errors

Table 7

6.8.7.1 Revision Register

The byte-wide revision register will contain information on the version of firmware currently loaded in the FPGA. The most significant four bits will indicate the version

number. The least significant four bits will indicate the revision number. Both the version and revision numbers start at 1.

6.8.7.2 Reset FPGA Register

When any value is written to the Reset FPGA register all internal logic is reset to a state as if the FPGA had just finished configuration.

6.8.7.3 Reset Readout Register

When any value is written to the Reset Readout register, all readout logic is reset and all event queues and buffers are cleared of pending events. All Registers will retain their current value.

6.8.7.4 Control

The Control Register is used to control the operating mode of the ETC FPGA. The modes are encoded in the following manner.

Bit [1:0]

00	Disabled
01	cal-inject
10	triggerless-pedestal run
11	Normal run mode enabled

Bit2

0	Use data from VFB
1	Use internally generated test data

Bit3

0	Manual Triggerless-Pedestal and Cal-Inject Mode
1	Automatic Triggerless-Pedestal and Cal-Inject Mode

Bit4

0	Disable external LEMO Connector access (default)
1	Enable external LEMO Connector access (not needed for TOF)

6.8.7.5 Status

This register reports the status of the FPGA and operations.

Bit0	This ETC has nothing to do

Bit1 Currently resetting the readout

Bit2 The cal-inject is busy

Bit3 Currently in a readout operation

Bit4 There is an event waiting to be read-out

Bit5 In the process of changing modes

Bit6 Waiting event put in queue

Bit7 Event waiting to be put in queue

6.8.7.6 CAL_TRIG_XQT_CTRL Register

This word is used to control the triggerless-pedestal run or cal-inject depending on the ETC's mode.

6.8.7.7 triggerless-pedestal single-shot mode

Bit[2:0] Each bit has the effect of initiating an external trigger of its corresponding chip. on VFB 0

Bit[5:3] Each bit has the effect of initiating an external trigger of its corresponding chip on VFB 1

6.8.7.8 cal-inject Single-shot mode

Bit[4:0] Selects the channel to be injected with charge. This can be 0 – 21

Bit[9:8] Selects the chip to be injected with charge. This can be 0 – 2

Bit10 Selects the VFB that contains the chip to be injected with charge 0 or 1

6.8.7.9 CHIP_TRIG_ENABLE Register

The CHIP_TRIG_ENABLE register will enable the dynode trigger corresponding to each chip. If a trigger is not enabled it will simply be ignored.

Bit[2:0] Each bit has the effect of enabling its corresponding chip. on VFB0

Bit[5:3] Each bit has the effect of enabling its corresponding chip on VFB1

6.8.7.10 Sample Delay Register

The Sample Delay register gives us a programmable setting to delay the Sample/Hold signal going to the VA chip. This byte-wide value can be set from 0 to 3.2us in 12.5ns increments. There is an offset associated with this setting.

6.8.7.11 VA CLK Period Register

The nibble-wide VA CLK Period Register gives us control of how fast the VA chip is read out or clocked. The setting can have the value of 100ns to 1.5 µs with 50ns increments. This setting must be greater then 0 where 1 corresponds to a period of 100ns. Each increment increases the delay by 50ns.

6.8.7.12 Errors Register

The Errors Register includes information on readout errors. Reading this register will clear the registers of errors and allow new errors to be detected. Any errors will produce the front panel LED to flash red until the error is cleared.

Bit0 The ETC's FIFO has overflowed

Bit1 Readout was stuck busy

Bit2 VA chip not responding to cal-inject signal

Bit3 Reset signal is stuck resetting

Bit4 There is an event waiting to be read-out but it can't start

Bit5 cal-inject command is not starting

Bit6 Stuck in old mode

Bit7 The dreaded 'FIFO out of sync' (we hate this one!)

6.8.8 Sparsifier Registers

A list of the Sparsifier registers can be seen in Table 8.

SPARSIFIER FPGA				August 9, 2001
Address	**Register**	**Width**	**Dir**	**Function**
0x00	REVISION	Byte	R	Firmware Version and revision #
0x08	RESET_FPGA	~	W	Writing to this register will reset all internal FPGA logic to a post configured state
0x10	RESET_READOUT	~	W	Writing to this register will reset all readout logic but retain the register values
0x18	CONTROL	Word	R/W	Value determines mode of the FPGA
0x20	STATUS	Byte	R/W	Indicates status of the chip
0x28	not used	~	~	
0x30	VARC_ID	2Bits	R/W	Program the 2-Bit VARC ID
0x38	BUFF_LEVEL_L	Byte	R	Buffer Level lower byte
0x40	BUFF_LEVEL_U	Byte	R	Buffer Level upper byte
0x48	SN2VME	Byte	R	Buffer Level upper byte
0x50	not used	Byte	~	Buffer Level upper byte
0x58	not used	Byte	~	Buffer Level upper byte
0x60	ERROR	Byte	R/W	Buffer Level upper byte

Table 8

6.8.8.1 Revision Register

The byte-wide revision register will contain information on the version of firmware currently loaded in the FPGA. The most significant four bits will indicate the version number. The least significant four bits will indicate the revision number. Both the version and revision numbers start at 1.

6.8.8.2 Reset FPGA Register

When any value is written to the Reset FPGA register all internal logic is reset to a state as if the FPGA had just finished configuration.

6.8.8.3 Reset Readout

When any value is written to the Reset Readout register all readout logic is reset and all event queues and buffers are cleared of pending events. All Registers will retain their current value.

6.8.8.4 Control

The Control Register is used to control the operating mode of the Sparsifier FPGA. The modes are encoded in the following manner.

Bit0 A one written to this bit will generate buffer test pattern to the buffer selected. The Sparsifier will not process new events until this bit is cleared.

Bit1 Enables pedestal subtraction

Bit2

0 Ignore external triggers from board LEMO.

1 Insert timestamped external triggers in output data buffers

Bit3 Enables sparsification

Bit4 Enables common mode correction

Bit5
0 Ignore external 50 ms buffer select signal and use VME selected readout buffer specified in Bit6
1 Use external 50 ms signal to select readout buffer

Bit6 only valid when Bit5 is 0
0 Select buffer A to be written to
1 Select buffer B to be written to

BIT7
0 Automatically disable sparsification, common mode correction and pedestal subtraction during pedestal runs
1 Allows manual control of Sparsifier during pedestal runs

6.8.8.5 STATUS

This register includes information on status of the FPGA.

Bit0 Indicates buffer A is busy being written to

Bit1 Indicates buffer B is busy being written to

Bit2 Indicates what buffer is actually selected to be written to

6.8.8.6 VARC_ID

The last nibble of the VARC_ID will end up in the output data word. This value is set by the user to identify the VARC in a crate from which the data came from.

6.8.8.7 BUFFER_LEVEL_L

The BUFFER_LEVEL_L and BUFFER_LEVEL_U REGISTERS form a 15-bit word indicating how many long words have been written to the previously selected buffer. This is the current amount of valid data waiting to be read out.

Bits[7:0] Lower byte

6.8.8.8 BUFFER_LEVEL_U

Bit7

0 Indicates the data has been written to buffer A

1 Indicates the data has been written to buffer B

Bit[6:0] Upper 7 bits of a 15-bit word indicating how many long words have been written to the previously selected buffer

6.8.8.9 Error Register

The Errors Register includes information on sparsification errors. Reading this register will clear the registers of errors and allow new errors to be detected. Any errors will produce the front panel LED to flash red until the error is cleared.

Bit0 The readout FIFO has become corrupt and the Sparsifier has resynchronized to the next packet of data.

Bit1 FIFO is found to be corrupt during expected timestamp data word

Bit2 FIFO is found to be corrupt during expected ADC data word

Bit3 FIFO is found to be corrupt during expected end of packet data word

Bit4 VME readout buffer has overflowed and data has been lost.

Bit5 An output buffer was read from while it was busy being written to

Bit6 Not defined

Bit7 Not defined

6.9 External Input and Output

The VARC has a LEMO connector that can be configured for various tasks. Using the Master Clock control register it can be configured as either an input or an output.

6.9.1 TOF External timestamp trigger

Using the board LEMO we can trigger the VARC to insert a timestamp into the Buffer data. This can be used to produce Time of Flight timestamp data. This timestamp will be tagged as coming from VFB 12. The output word format is seen in Table 9. The

bin size for this timestamp is 25 ns. To set this up in the VARC, the Master Clock must configure the LEMO as an input and the Sparsifier must be in run mode with the external trigger enabled.

Last modified
22-Jan-01

	ID																													
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Upper LWORD	1	P	DC0	VID1	VID0	F2	F1	F0	SEL	VA1	VA0	MUX[4:0]					HD1	HD0	ADC data													
Lower LWORD	0	P	TS[29:16] Time Stamp Upper														TS[15:0]Time Stamp Lower															

ID	Data Identifier : 0 = timestamp, 1 = ADC address, data
P	Parity (including ID)
HD[1:0]	Header code during TOF event (see fifo data packet)
F[2:0]	110 signifies a TOF event
SEL	unused
VA[1:0]	unused
MUX[4:0]	unused
ADC[13:0]	unused
VID[1:0]	Identify VARC in crate
TS[29:0]	Time-stamp
Data code	
DC0	unused

Table 9

6.9.2 Trigger output

The VARC can be configured in the Master Clock to use the LEMO as output trigger. The signal can be used for things such as instrument triggers, clock module trigger or as an input to a second VARC. The output is controlled in the Master Clock by setting the LEMO to output and setting the trigger rate using the XQT_RATE register.

6.10 Rate Limitations

6.10.1 VA chip

Rates are limited in various parts of the readout system. Readout of a particular VA chip takes between 5μs-10μs depending on the readout time setting of the ADC. This time is the sum of the hold time of the VA chip, the time required to digitize 21 VA chip channels, and some settling time after the chip is placed back on line. This limits the trigger rate to an absolute maximum of order ~100kHz for a particular VA chip. At these high rates, however, there will be substantial baseline shift and baseline noise. **Operation at these rates would therefore be extremely noisy and unreliable** and was never intended for this readout architecture.

6.10.2 VMM

The VMM has one digitizer for each six VA chips. The ETC has the feature that if it is busy readout out a particular VA chip, it will accept triggers from other VA chips and hold them in a queue for later readout. Thus, the absolute maximum rate is still established by the maximum single VA chip rate.

6.10.3 Data Fifo & Sparsifier

Data from each trigger is stored in the associated data fifo in packets which are 25 words long. The Sparsifier reads out the fifos in round-robin fashion, one packet at a time, requiring 25 clock cycles. In addition, pedestal and threshold memory locations are accessed for each of the 22 data words in the fifo. After threshold comparison, clock cycles are allocated to writing the results into the output buffer. Each data word requires 6 clock cycles total. Thus, the total number of clock cycles per data packet is

$$25 + 6 \cdot 22 = 157$$

A few clock cycles must also be added to each packet for various overhead functions. Thus the maximum rate established by the Sparsifier is

$$\frac{40 \cdot 10^6}{\sim 160} \cong 250 kHz$$

and is independent of whether or not the sparsification feature is enabled. **This total rate is shared by all of the operating fifos on the VARC**. Thus, if five VMMs are installed, the maximum average rate each is ~50kHz. For six VMMs, this is reduced to ~42kHz. *If this total rate is exceeded, the fifos will begin to fill up and will result in rejection of triggers and loss of data.* Since the average maximum fifo rate is shared by six VA chips, the absolute maximum VA rate is **~8kHz**, down by more than an order of magnitude set by the VA chip and digitizer. This is to be compared with the average specification for PMT dark noise rate of ~1kHz. Thus, the system has a design safety margin for single pe rates, of eight.

6.10.4 VME Output Buffers

Each output buffer can hold 16384 data packets. If a buffer swap signal of 50 ms is used, the maximum number of data packets that can be read out per second from one VARC is 327,680. If each dynode trigger produces one data packet after sparsification, this would mean that the output buffers can handle a maximum rate of 330 kHz per VARC. If the number of data packets is more than one per dynode trigger, the maximum trigger rate will be less than this. Any data which arrives after the output buffer is full is ignored. When an output buffer becomes full, data corruption can occur, so this should be avoided, either by raising thresholds or by providing a faster buffer swap signal.

7 Special Crate Requirements

7.1 J3 Backplane

The J3 backplane is actually a J1 backplane with modified termination fitted in the J3 backplane location. The backplane is responsible for carrying clock signals and power for the VMMs.

7.1.1 Clock Signals

The J3 backplane carries four LVDS clock signals from the Clock Module that sits in the last J3 backplane crate slot. The LVDS signals are tapped by the VARCs and terminated at the end opposite the Clock Module. The termination is 100Ω between the LVDS pairs. The Pairs are listed in Table 10.

J3 Backplane LVDS Pairs			August 9, 2001
Pin	+ Signal	Pin	- Signal
C23	SPARE+_IN	C24	SPARE-_IN
C25	Slow Ctrl	C26	XQT-_IN
C27	XQT+_IN	C28	SEC_TICK-_IN
C29	CLK_40MHZ+_IN	C30	CLK_40MHZ-_IN

Table 10

Our terminator is a simple 8 pin, 4 resistor, SIP pack inserted in an inline socket that plugs nicely into the first backplane connector of the VME crate. Along with this termination we have put a nylon tie-wrap around the first rail to prevent accidental insertion of a card into this slot.

7.1.2 VMM Power

This backplane supplies power to the VMMs through the backplane by redefining power connections on the J1 backplane. Table 11 describes which backplane signals are used for VMM power.

J3 Backplane VMM Power		August 9, 2001
J1 connector	Pin	Used as
-12VDC	A31	-6V_IN
+5VDC	A32	+6V_IN
+5VSTDBY	B31	-6V_IN
+5VDC	B32	+6V_IN
+12VDC	C31	-6V_IN
+5VDC	C32	+6V_IN

Table 11