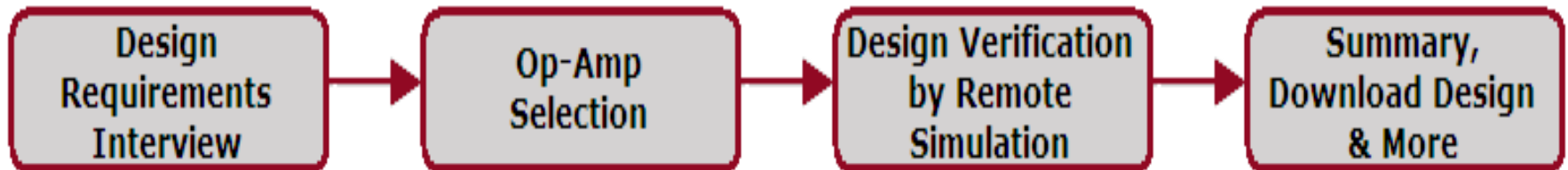


## iSim Active Filter Designer



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# Introduction to the New Active Filter Designer

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- Scope and Intent
- Getting into the tool
- Two Primary Design Flows
  - Semi-automatic design
  - User specified poles and gains for each stage
- From design targets, pick op amps, simulate, and save/share features.
- Example Designs
- Future plans for the tool.

RESOURCES

# Scope and Intent of the Active Filter Designer

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- Intent is to deliver working designs using Intersil's Precision and High Speed Op amps.
- Basic filter types that will be supported
  - Low Pass
  - High Pass
  - Bandpass
- Notch filters are not anticipated – have seen those occasionally, but the required external component precision precludes widespread application.
- The list above will be the rollout sequence. Low pass filter designs are available at this initial Feb. 2010 release.

# Important Terminology

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- Filter “Type” is the highest level classification.
  - Low Pass, High Pass, Notch, Bandpass, Allpass, etc.
- Filter “Order” is the number of poles in the transfer function
  - 1<sup>st</sup> order is just a single energy storage element (like an RC filter)
  - 2<sup>nd</sup> order stages are only complex poles in this tool ( $Q > 0.5$ )
  - 2<sup>nd</sup> through 6<sup>th</sup> order filters supported by the tool (built up as a combination of 1<sup>st</sup> and 2<sup>nd</sup> order stages – no 3<sup>rd</sup> order stages)
- Filter “Shape” describes the pole locations
  - Infinite number of possible combinations of multiple pole locations – some standard ones include Butterworth, Chebyshev, etc.
- Filter “Topology” describes the op amp implementation to achieve a particular 1<sup>st</sup> or 2<sup>nd</sup> order set of filter poles
  - Sallen-Key is one popular one.

# Low Pass Active Filter Design Range

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- The design tool supports a very wide range of requirements
  - Cutoff frequencies from 5Hz to 50Mhz (7 decade range)
  - Total filter gain from 1 to 10V/V in semi-automatic design flow but up to 125V/V (3 stage design) in the manual design flow
  - Filter order from 2 to 6
- The filter order from 2 to 6 implies from 1 to 3 amplifier stages.
- Higher order filters tend to require extreme element precision to hit the higher Q targets that come along with orders > 6.

# Part List with New MacroModels

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- Present (Feb. 2010) table of op amps in the Active Filter Designer – sorted by ascending GBP or BW (for CFA).

Part #	Topology	GBP/BW <sub>n</sub>	Nominal	Typ. Is	Min Vcc	Max Vcc	Single	Dual	Quad
	VFA/CFA	MHz	Total Vcc	mA (at Vcc)			With	Versions	Versions
							Disable		
ISL28194	VFA	0.0035	5	0.00033	1.8	5.5	ISL28194		
ISL28195	VFA	0.01	5	0.001	1.8	5.5	ISL28195		
ISL28158	VFA	0.2	5	0.034	2.4	5.5	ISL28158	ISL28258	
ISL28156	VFA	0.25	5	0.039	2.4	5.5	ISL28156	ISL28256	
ISL28133	VFA	0.4	5	0.018	2	5.5		ISL28233	ISL28433
EL8176	VFA	0.4	5	0.055	2.4	5.5	EL8176	ISL28276	ISL28476
ISL28107	VFA	1	30	0.21	4.5	40		ISL28207	
ISL28117	VFA	1.5	30	0.44	4.5	40		ISL28217	
ISL28113	VFA	2	5	0.09	1.8	5.5		ISL28213	ISL28413
ISL28136	VFA	5.1	5	0.9	2.4	5.5	ISL28136	ISL28236	
ISL28114	VFA	7.7	5	0.4	1.8	5.5		ISL28214	ISL28414
ISL28127	VFA	10	30	2.2	4.5	40		ISL28227	
ISL24021	VFA	15	10	2	4.5	19			
ISL28191	VFA	61	5	2.6	3	5.5	ISL28191	ISL28291	
ISL55001	VFA	68	30	9	8	30	ISL55002		
ISL28190	VFA	83.3	5	8.5	3	5.5	ISL28190	ISL28290	
EL8101	VFA	106	5	2	3	5.5	EL8100	EL8201	EL8401
EL5103	VFA	165	10	5	5	12.6	EL5102	EL5203	
EL5101	VFA	170	10	2.5	5	12.6	EL5100		
EL8103	VFA	198	5	5.6	4	5.5	EL8102		
EL5105	VFA	264	10	5	5	12.6	EL5104	EL5205	
EL5161	CFA	95	10	0.75	5	12.6	EL5160	EL5261	
EL5163	CFA	140	10	1.5	5	12.6	EL5162	EL5263	
EL8108	CFA	190	12	14.3	4.5	13		EL8108	
EL5165	CFA	370	10	5	5	12.6	EL5164		
EL5167	CFA	620	10	8.5	5	12.6	EL5166		

# Feature set for the New/Upgraded Macromodels

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Typical, room temp., nominal power supply voltages used to produce the following characteristics:

- Open and closed loop I/O impedances
- Open loop gain and phase
- Closed loop bandwidth and frequency response peaking under different external conditions
- Loading effects on closed loop frequency response
- Input noise terms including 1/f effects
- Slew rate
- Input and Output Headroom limits to I/O voltage swing
- Supply current at nominal specified supply voltages
- Nominal input DC error terms (1/3 of specified data sheet test or specified limits – intended to give  $1\sigma$  error term on one polarity)
- Load current reflected into the power supply current

# Features not supported by the Macromodels

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- Harmonic distortion effects
- Composite video differential gain and phase errors
- Output current limiting (if any)
- Disable operation (if any)
- Thermal effects and/or over temperature parameter variation
- Limited performance variation vs. supply voltage modeled
- Part to part performance variation due to normal process parameter spread
- Any performance difference arising from different packaging
- Multichannel device crosstalk effects

RESOURCES



# Enhanced Capability Provided by the Tool

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- Semi-automatic design flow for multi-stage filters
  - Spreads the gain (from 1 to 10V/V total) between the stages and sequences the poles (order >2) in a way that reduces non-linear effects.
- Significantly improved circuit implementations.
  - Noise effects considered and reduced if possible
  - 2<sup>nd</sup> order issues in the feedback and gain setting elements considered (loading, noise, BW, phase margin)
- Resistor solutions adjusted to account for amplifier bandwidth effects to hit the desired pole locations more precisely. This also allows reduced amplifier bandwidth vs. target Fo design margin than any currently available design tools.

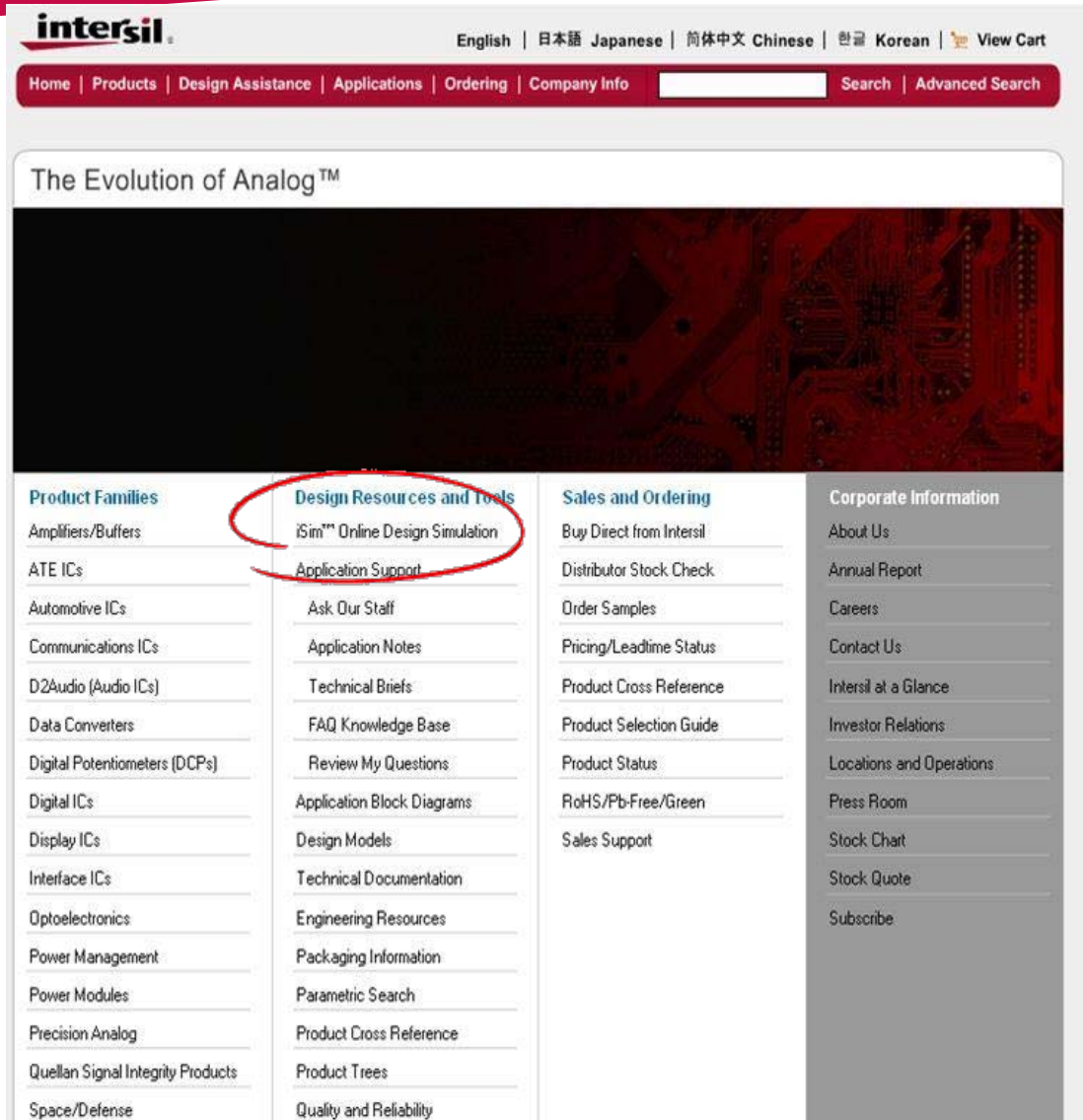
# Some Common Misconceptions about Active Filters

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- The Active Filter Designer includes numerous features that might appear to violate some widespread myths –
  - Current feedback amplifiers (CFA's) cannot be used in active filters.
    - They are in fact very suitable as wideband gain blocks if that is what is needed in the filter stage. Cannot be used (easily) with reactive feedback type topologies such as the MFB (or infinite gain) circuit.
  - Gain of 1 is required for the active filters (or low gain)
    - The gain is a design variable and can be accounted for in setting the R's and C's. But it does interact strongly with the amplifier bandwidth if VFA devices are used – and this is also accounted for in the design algorithms provided in the tool.
  - Equal R or Equal C designs are required or desirable.
    - This comes from simplified academic developments or where the text is headed towards integrated solutions (close cap. ratio's desirable for integrated filters). Not really a required constraint for discrete implementations.

# Entry from the main Intersil Web site

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- Currently, the top listing under the Design Resources and Tools is the “iSim Online Design Simulation”
- Clicking that, takes you to →

resources

# Available Design Tools under the iSim option (3/2010)

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**intersil.** **iSim** Intersil's Interactive web design simulation tool

Home Application Part Selection | Design | Design Summary | Search | Login :: Register

### iSim Application Selection

**Power Management**

- Switching Regulation
- Integrated FET
- Power Modules - **NEW**
- Multi-Phase
- Isolated DC/DC
- Linear Regulators
- MOSFET Drivers
- Power Supply Support
  - Hot Swap Controllers
  - Sequencers
- Battery Management
- LED Drivers
  - Offline LED Drivers
  - DC Input LED Drivers

**Operational Amplifiers**

- Active Filter Designer - NEW**
- Inverting Gain
- Non-Inverting Gain
- Transimpedance
- Differential Amplifier
- Instrumentation Amplifier
- Single Stage Low Pass Filter
- Single Stage High Pass Filter

Intersil's iSim™ is an interactive, web-based tool for selecting and simulating devices from Intersil's broad portfolio. Based on input and output specifications provided by the user, iSim will find all suitable Intersil devices for your application. In many cases, a simulation is also made available for immediate feedback on circuit performance. Currently, iSim is available for Intersil's power management devices and operational amplifiers.

**Power Management**

Intersil's iSim simulator for power is an applications-based Intersil Power Management Solution Selector with dynamic input fields to match your input and output requirements. All applicable Intersil devices will be listed and those with a design button are available for online simulation. When available for simulation, a reference schematic will be generated for simulation, based on your specifications.

**Operational Amplifiers**

Intersil's iSim simulator for Operational Amplifiers provides application oriented solution tools using the broad range of Intersil precision and high speed amplifiers. Tools include an Active Filter Designer, Inverting gain configuration, Non-inverting gain configuration, Transimpedance, Differential Amplifier, Instrumentation Amplifier, Single Stage Low Pass Filter, and Single Stage High Pass Filter. Each tool includes Intersil devices suited to that application along with simulation models in most cases. Taking designer inputs, each tool will help you pick the best Intersil amplifier and deliver designs to hit the desired performance targets.

iSim will filter out only the inputs required for the application group you are interested in. Please select an application from the links on the left to get started.

See AN1243 - Getting Started with iSim and iSim:PE

After using iSim to design your schematic you can download the offline iSim:PE version of the schematic so that you can capture schematics, view waveforms, perform application analysis and more!

**Download iSim:PE**

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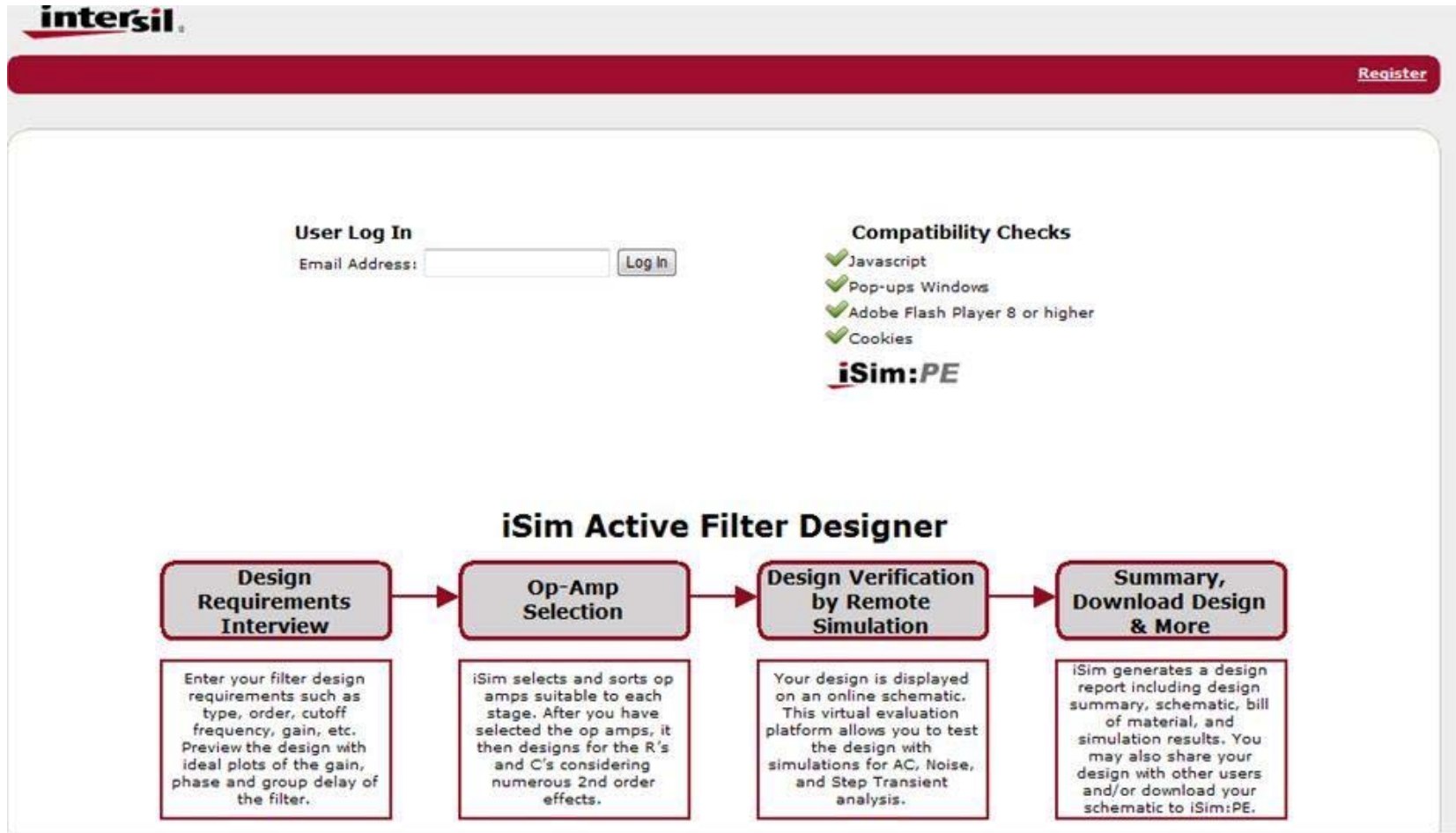
Currently, the iSim application tools are broken into Power and Op amps. The top selection in the op amps is this new design tool.

Clicking the Active Filter Designer takes you to →

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# iSim Active Filter Designer

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# First Step in Getting to a Filter Implementation

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- Coming into the tool fresh will give you the first “Requirements” screen set up to a default condition.

The screenshot shows the Intersil Filter Designer web application. The top navigation bar includes links for Home, Application, Requirements, Setup, Design, Design Summary, and My Designs. The 'Requirements' tab is selected and highlighted with a red circle. The main content area is titled 'Filter Designer' and contains a 'Design Requirements' section with the following fields:

- Select Filter Type: Low Pass
- Select Filter Order: 4
- Enter Poles Manually? ☐ Yes ☒ No
- Filter Cutoff Frequency: 50 kHz
- Pass Band Gain: 2 V/V
- Select Filter Shape: Butterworth

At the bottom of the form are 'Update Preview' and 'Continue' buttons. A callout box on the right provides information about the Butterworth filter shape:

**Filter Shape: Butterworth**

This filter shape offers the flattest passband gain response at the expense of relatively slow rolloff in the transition region. There are no gain ripples in either the passband or stopband region. The step response does show some overshoot that increases with filter order.

$F_{-3dB} = F_{cutoff}$

# The Tool is Mainly an Implementation Aid.

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- Many vendor tools provide some filter shape help as an early step in their tools. This is used to arrive at a desired filter order and pole locations to hit a particular “skirt” shape (how fast the cutoff band rolls off). Usually this is specified in terms of stop band attenuation at a certain frequency above the desired passband.
- The Active Filter Designer assumes you already know the target shape and/or the approximate order or filter poles you want to implement.
- The tool mainly works on getting the right op amp selected and design implemented in a way that will yield a successful board level implementation.

RESOURCES

# The Tool is Mainly an Implementation Aid.

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- If you need help deciding on the filter shape, try this web site – (free download that has a lot of filter shape design tools – just need to get the pole locations from here, or the shape description, to use in the iSim Active Filter Designer)
- Filter Wiz PRO
- [http://www.schematica.com/filter\\_wiz\\_files/FWPRO.htm](http://www.schematica.com/filter_wiz_files/FWPRO.htm)
- Exact pole locations and advanced features may require you to purchase the full version.

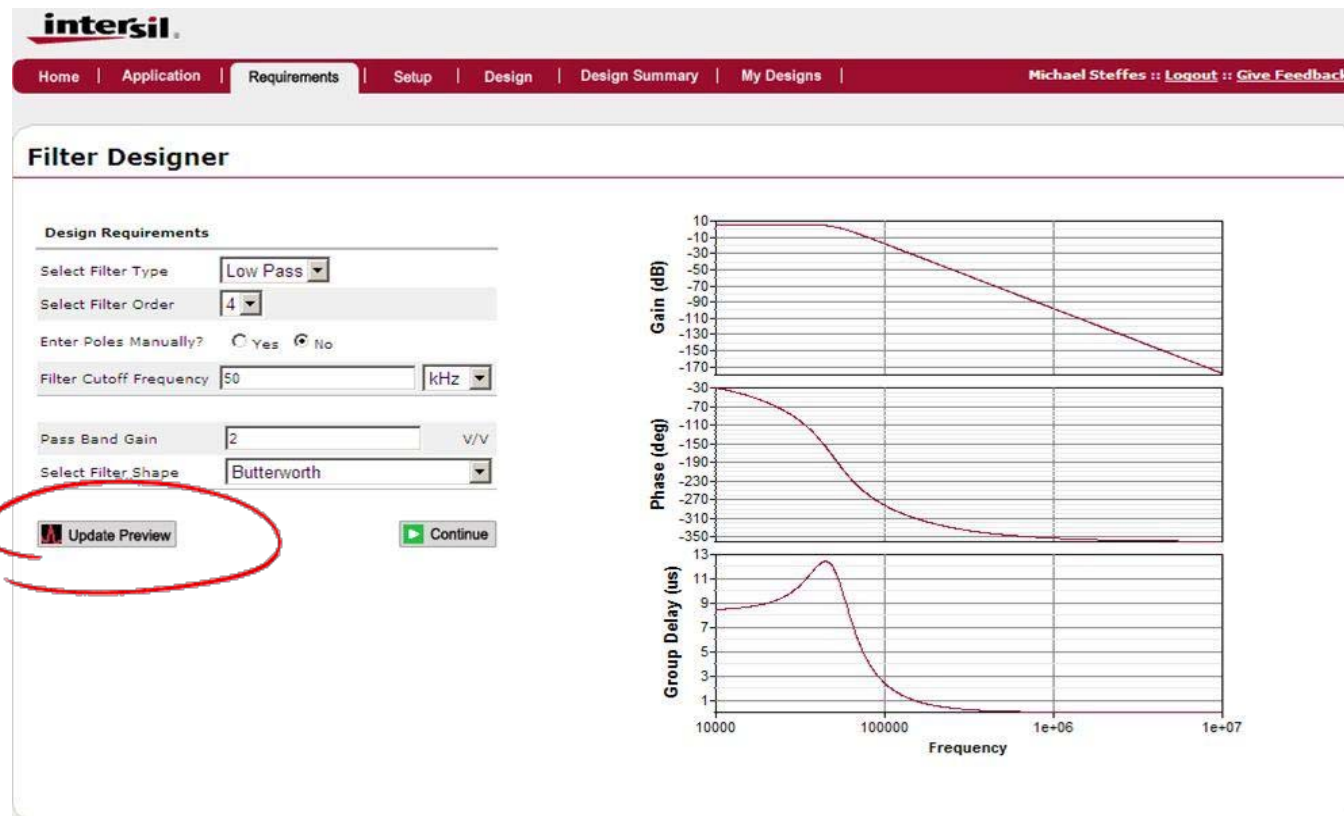
RESOURCES



# AC Response Preview

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- From whatever settings are used in the upper section of the “Requirements” screen, hitting “Update Preview” will generate the ideal Gain, Phase, and Group delay. These are used later to compare to the actual circuit level implementation. Here is the screen after hitting Update Preview.



# Two Primary Flows through the Active Filter Designer

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- 1. Semi-Automatic flow is where you want to use some of the pre-loaded filter shapes and let the tool do most of the work for you. This is the default mode and is what is shown on first entering the tool.
  - This flow also decides for you the sequence of poles (order  $>2$ ) and how to implement the total target gain. It is essentially sequencing from high to low Q stages in low to higher gains in those stages in going from input to output.
- 2. Manual Pole selection is where you have some specific pole locations you wish to implement and want to enter those directly.
  - This also allows you to select the Frequencies, Gains and Q's over a wider range than the semi-automatic path.
  - This is all selected in the row that asks "Enter Poles Manually". This defaults to "No", but clicking "Yes" changes this screen to accept user entry for each stage. The order setting still sets the number of stages and an odd order (3 or 5) forces the real pole to be the last stage.

# Manual Pole Entry Option

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- Here, the entry screen has been changed by clicking "Yes" on the "Enter Poles Manually?" line and we have changed the gain in each stage to 10 giving an overall filter gain of 100 (10 in each stage is the maximum for 2 stage designs) and manually set the Q's to get a 4<sup>th</sup> order Butterworth shape then hit "Update Preview" again. Hitting the "Continue" key from here ->

The screenshot shows the Intersil Filter Designer interface. The 'Design Requirements' section is configured as follows:

- Select Filter Type: Low Pass
- Select Filter Order: 4
- Enter Poles Manually?: ☒ Yes ☐ No
- Intended Filter Cutoff Frequency: 50 kHz
- Pass Band Gain: 100 V/V
- Enter Complex Pole or F0&Q?: F0 and Q

A note states: \* NOTE: Target F0&Q must be un-normalized.

The user is prompted to enter target F0&Q and gain for each stage:

	Gain	F0(Hz)	Q
Stage1	10	50000	1.3
Stage2	10	50000	.541

At the bottom, the 'Continue' button is circled in red.

On the right, three plots are shown against Frequency (log scale from 10000 to 1e+07):

- Gain (dB): Starts at 40 dB and decreases linearly to -140 dB at 1e+07 Hz.
- Phase (deg): Starts at -30 degrees and decreases to -350 degrees at 1e+07 Hz.
- Group Delay (us): Starts at 13 us, peaks at approximately 11.5 us around 50,000 Hz, and then decreases to 1 us at 1e+07 Hz.

102

# Setting up the Design

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- Hitting “Continue” from the “Requirements” page will go the “Setup” page where numerous implementation parameters are considered and available for modification. This step starts out with some default assumptions.
- This is where the real work begins in matching op amps to the desired filter implementations.
- For multi-stage filters, the most important thing to notice on this next screen is which stage is “active” in the setup screen. This is the red color on the Stage # tab. It comes into this step with the last stage as the default “active” stage. This is where the design constraints can be updated. Those also default to the values shown on the next slide, but can be modified.

# Setting up the Design

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- The main goal for this step is to pick the right op amps for each stage given the topology, filter targets, and constraints.

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Home | Application | Requirements | **Setup** | Design | Design Summary | My Designs | Michael Steffes :: Logout :: Give Feedback

## Filter Designer

**Stage1**  
 F0: 50 kHz Q: 1.3 Gain: 10  
 Topology: Sallen Key  
 Selected OPAMP: ISL28191

**Stage2**  
 F0: 50 kHz Q: 0.541 Gain: 10  
 Topology: Sallen Key  
 Selected OPAMP: ISL28127

IS Design

Stage1

Stage2

---

**Design Constraints**

Total Supply Voltage:  V

Max. Vopp at Last Stage Output:  V

Intended Linearity Specifications:

Target SFDR Range:  dBc

Maximum Expected Signal Frequency:  kHz

Required Vipp: 0.2V  
 Required Max Peak Vopp: 2V  
 Estimated minimum required slew rate: 2.134V/us

☒ Apply

Select Resistor Precision:  %

Topology:

Filter set for overall non-inverting gain

Estimated Minimum Closed Loop Amplifier Bandwidth required: 994.706 kHz

	Part Number	Feedback Type	GBP/BW (MHz)	Slew Rate (V/us)	En (nV)	Nominal Vcc (V)	Nominal Is (mA)	Vout Headroom (V)	Vcc Min (V)	Vcc Max (V)	1k MSRP Price	Description
Select	ISL28127	VFA	10	3.6	2.8	30	2.2	1.5	4.5	40	\$1.05	Prec. WideVccRange
Select	ISL24021	VFA	15	18	12	10	2	0.025	4.5	19	\$1.27	1A peak I/O, RailRail I/O
Select	ISL28191	VFA	61	17	1.7	5	2.6	0.02	3	5.5	\$1.32	Prec. Low Noise
Select	ISL28190	VFA	83.3	50	1	5	8.5	0.02	3	5.5	\$1.58	Prec. Low Noise
Select	EL8101	VFA	106	200	10	5	2	0.3	3	5.5	\$1.09	LowPwr HighSpeed
Select	EL8103	VFA	198	600	12	5	5.6	0.3	4	5.5	\$1.35	MedPwr HighSpeed
Select	EL8108	CFA	190	800	6	12	14.3	1	4.5	13	\$1.88	Dual, High Output Current
Select	EL5103	VFA	165	2200	12	10	5	1.3	5	12.6	\$1.18	MedPwr High SR

2010

# Setting up the Design

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- The 2<sup>nd</sup> most important thing is that the “Constraints” can only be changed if you sitting on the final stage as the “active” stage. This is mainly related to the final output Vpp target. That can be updated for the last stage, but is then calculated for all previous stages and hence cannot be updated if you are sitting on those earlier stages for amplifier selection purposes.
- While sitting on each “stage” tab, the tool is computing and reporting the implied requirements for that stage. These include
  - Bandwidth if the stage is non-inverting. Since this can be either a VFA or CFA op amp, gain bandwidth is not used in this line. So, taking the required BW number times the stage gain will give you the required GainBandwidth Product if you want to use a VFA op amp in this stage.
  - If you change the stage to be inverting, only VFA devices can be used and this computation reports the required Gain Bandwidth Product (GBP)

# Adjustments Available on the Setup stage

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- On any given stage, you can change the topology from non-inverting (default) to inverting and that immediately updates the recommended amplifier list at the bottom (this is the only thing that can be changed when you are sitting on earlier stages)
- Sitting on the last stage, you can change the following global constraints –
  - Desired total supply voltage (range here is 1.8V to 40V). This supply voltage is assumed to be the same for all stages.
  - Maximum final stage Output Swing  $V_{pp}$  (limited to be from 10% to 90% of  $V_s$ )
  - Linearity Target – either SFDR if frequency domain or Step if step response
    - If SFDR, also asks for maximum expected frequency and desired distortion range
  - Resistor tolerance (exact, 0.5%, 1%, or 2%)
    - This effects the filter accuracy in that exact R solutions might be snapped to available values probably shifting the achieved filter shape off somewhat



# Adjustments Available on the Setup stage

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- Several of these constraints are feeding into the “Estimated minimum slew rate required” reported on each stage.
  - Slew rate is estimated to achieve either an SFDR target or step response without slew limiting. The SFDR constraint is a necessary but not sufficient condition to achieve a certain distortion level – you might still not get the SFDR with a device offering the reported slew rate, but you reduce your chances if the device does not have at least the reported slew rate for that stage.
  - For a step response, the tool is looking at the pole locations of that stage and the desired nominal  $V_{opp}$  or  $V_{step}$  at the output. It then computes the peak  $dV/dT$  to produce that output from an ideal input step and takes 2X that number for a design target.
  - Possible op amps to use in each stage use this Slew Rate calculation to constrain the list to op amps that offer at least 90% of this calculated value.



# Picking Suitable Op Amp Solutions

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- The goal of this “Setup” page is to pick a suitable op amp that will work in each stage in the design.
  - If possible, the tool will automatically pick the closest fit as you come into this step, but that can be overridden by picking one of the parts listed at the bottom of the screen.
- These are often different devices auto-filled in each stage, but these can often be made the same device with a little effort.
- Changing the supply voltage will typically show a completely different set of op amps.
- For instance, going to 10V total supply with 6Vpp output will show the following screen. (hit the “Apply” key after you update the supply voltage and output swing fields)

Figure 1-10

# Modifying the Constraints gives new part choices

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- More CFA parts show up here as the prior setting of 5V supply and 2Vpp output violated the 1.6V headroom on those parts

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### Filter Designer

**Stage1**  
F0: 50 kHz Q: 1.3 Gain: 10  
Topology: Sallen Key  
Selected OPAMP: ISL28127

**Stage2**  
F0: 50 kHz Q: 0.541 Gain: 10  
Topology: Sallen Key  
Selected OPAMP: ISL24021

**Design Constraints**

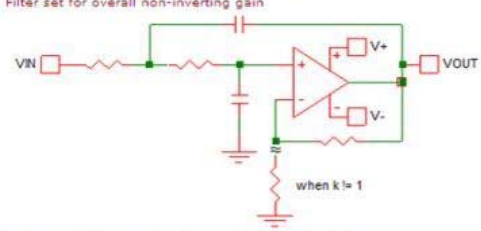
Total Supply Voltage: 10 V  
Max. Vopp at Last Stage Output: 6 V  
Intended Linearity Specifications: SFDR  
Target SFDR Range: 60-69 dBc  
Maximum Expected Signal Frequency: 40 kHz

Required Vpp: 0.6V  
Required Max Peak Vopp: 6V  
Estimated minimum required slew rate: 6.401V/us

☒ Apply

Select Resistor Precision: 1 %

Topology: Sallen Key  
Filter set for overall non-inverting gain



Estimated Minimum Closed Loop Amplifier Bandwidth required: 994.706 kHz

	Part Number	Feedback Type	GBP/BW (MHz)	Slew Rate (V/us)	En (nV)	Nominal Vcc (V)	Nominal Is (mA)	Vout Headroom (V)	Vcc Min (V)	Vcc Max (V)	1k MSRP Price	Description
<input checked="" type="checkbox"/> Select	ISL24021	VFA	15	18	12	10	2	0.025	4.5	19	\$1.27	1A peak Io, RailRail I/O
<input checked="" type="checkbox"/> Select	EL8108	CFA	250	800	6	12	14.3	1	4.5	13	\$1.88	Dual, High Output Current
<input checked="" type="checkbox"/> Select	EL5161	CFA	95	1500	4	10	0.75	1.6	5	12.6	\$0.58	LowPwr HighSpeed
<input checked="" type="checkbox"/> Select	EL5103	VFA	165	2200	12	10	5	1.3	5	12.6	\$1.18	MedPwr High SR
<input checked="" type="checkbox"/> Select	EL5101	VFA	170	2200	10	10	2.5	1.6	5	12.6	\$1.17	LowPwr High SR
<input checked="" type="checkbox"/> Select	EL5105	VFA	264	3000	10	10	5	1.3	5	12.6	\$1.30	Highest Speed VFA
<input checked="" type="checkbox"/> Select	EL5163	CFA	140	3000	3	10	1.5	1.6	5	12.6	\$1.17	MedPwr HighSpeed
<input checked="" type="checkbox"/> Select	EL5165	CFA	370	4500	2.1	10	5	1.6	5	12.6	\$1.26	HighSlewRate

302

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# Picking Suitable Op Amp Solutions

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- The part choices are sorted by minimally acceptable to increasing design margin to the requirements. The top device in the table generated for each stage is deemed minimally suitable and is the default part filled into the top boxes. Going down the list gives more design margin.
- This step requires a device selection for each stage before the next step (hitting “Design”)
- At any time, you can change a stage to inverting, which then constrains the solution op amps to be VFA since CFA devices cannot (easily) be applied to the those topologies.
- The Setup and design process works in gain “magnitudes” but it does report if the overall filter is inverting or non-inverting.

# Picking Suitable Op Amp Solutions

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- To summarize, the computed minimum requirements for each stage shown on this screen include -
  - Bandwidth if the stage is non-inverting, Gain Bandwidth Product if inverting
  - Slew rate
  - Maximum  $V_{opp}$  including any step overshoot or frequency response peaking
  - Maximum input  $V_{ipp}$ .
- These terms are used to constrain and sort the table of op amp selections to parts that –
  - Can operate at the specified total supply voltage
  - Will not clip given that supply voltage and output swing (including any peaking or step overshoot effects) considering the output headroom of each device.
  - Provides at least 90% of the computed BW and slew rate.
  - Will not limit on the input given the supply voltage and input headroom limits of each device considered.

# Executing the Design

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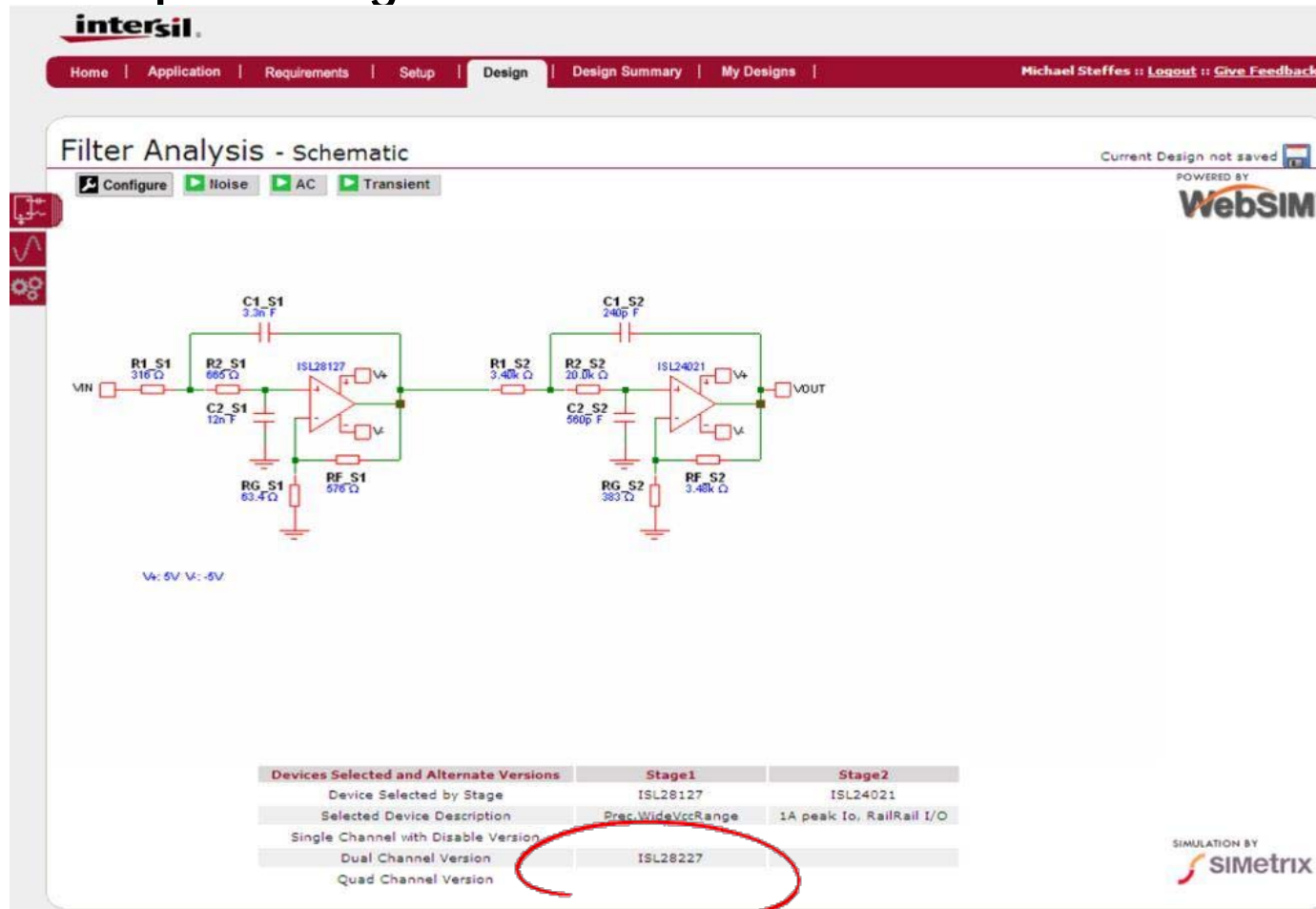
- Once we have design targets for each stage and an op amp selected, hitting the “Design” key will go off and compute the R’s and C’s for each stage and come back with a completed design.
- At that point the total specified supply is split into +/- ( $V_s/2$ ) halves and the design is shown as a DC coupled, ground centered, signal swing implementation.
- Hitting “Design” from the previous screen (10V supply, 6V output swing), gives the following active filter design.

DESIGN

# Example Design Output Page

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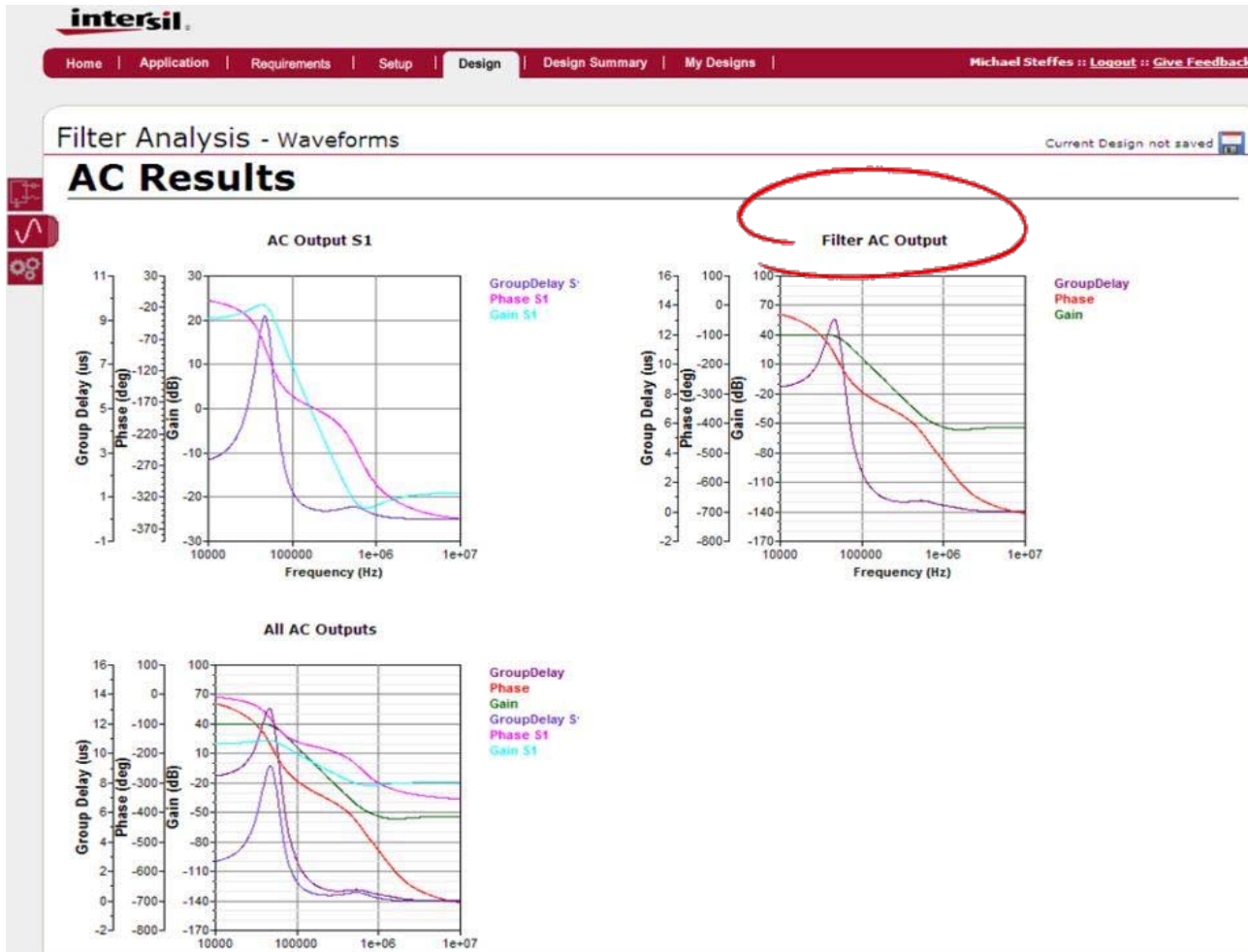
- Note the related parts at the bottom and the simulation options at the top – Hitting the AC tab will run an AC simulation



# Output of the AC simulation key.

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- Clicking on the Filter AC Output opens a waveform viewer where we can add the Ideal Gain, Phase, and Group Delay. Doing that -

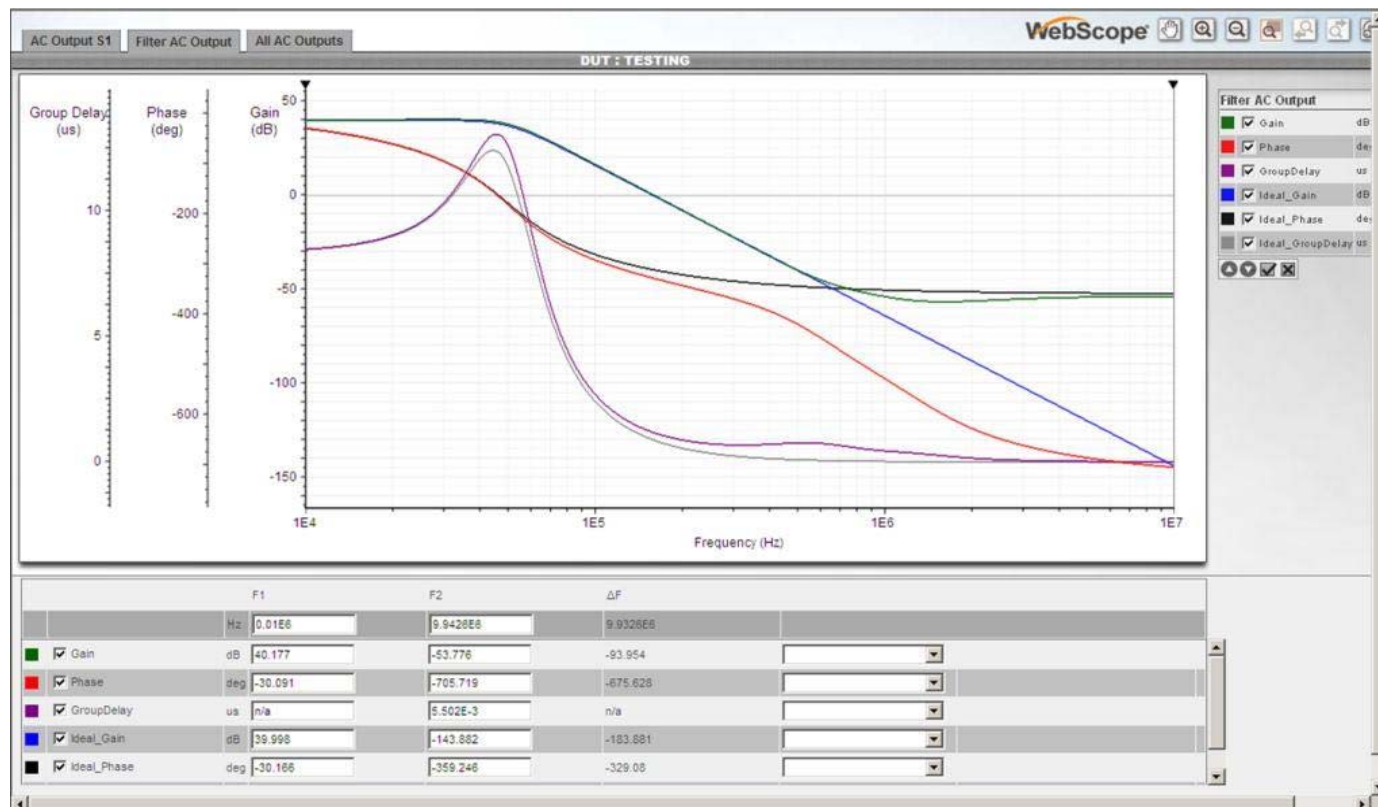




# Comparison of Actual to Ideal AC Response.

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- This viewer also has two cursors that can be moved and a zoom in feature. Here we see very good overall fit for the simulated filter response vs. ideal. Note the 40dB gain at low frequencies.





# Design Summary and Saving/Sharing Options

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- Going back to the Filter tool (from the waveform viewer) and clicking Design Summary, will give the following screen

**Design Summary**

Current Design not saved PDF Download Download Schematic

**Design Requirements**

Select Filter Type	Low Pass
Select Filter Order	4
Enter Poles Manually?	Yes
Filter Cutoff Frequency	50 kHz
Pass Band Gain	100 V/V

Enter Complex Pole or F0&Q? FQ

	Gain	F0(Hz)	Q
Stage1	10	50000	1.3
Stage2	10	50000	0.541

**Stage1**  
F0: 50 kHz Q: 1.3 Gain: 10  
Topology: Sallen Key  
Selected OPAMP: ISL28127

**Stage2**  
F0: 50 kHz Q: 0.541 Gain: 10  
Topology: Sallen Key  
Selected OPAMP: ISL24021

**Specifications**

Total Supply Voltage	10V
Max. Vopp at Last Stage Output	6V
Intended Linearity Specifications	SFDR
Target SFDR Range	60->69dBc
Maximum Expected Signal Frequency	40kHz
Select Resistor Precision	1%

**Schematic**

# Design Summary and Saving/Sharing Options

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- This summarizes the overall targets, the constraints, and the final circuit design.
- Down below on this screen are the BOM the AC, Transient, and/or noise sims that have been done.
- Most importantly, in the upper right are 3 paths to go on from here –
  - Save the design (the little floppy icon). This saves the design locally in your filter tool folder so you open it up and work on it later. Once saved, you can also share the design by emailing it from the “Saved Designs” tab.
  - Download to PDF. This takes the design summary and creates a pdf version that can be saved (and then easily emailed around to colleagues/customers)
  - Download to iSim PE. This ports the schematic into a more general purpose simulator where added operations can be performed. These include MonteCarlo simulations, re-ordering the stages, converting it to a single supply design, etc.

# Added Information and Filter Tool Extensions

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- Full User's manual added March, 2010. "Designer's Manual for the iSim Active Filter Designer" – AN1548
- Additional parts will be easily added to the tool as they become available (new parts) or as needed (older parts not currently included).
- Op Amps in the tool have totally updated/upgraded Spice Macromodels.
- Next addition will be the High Pass Filter flow, followed by the BandPass Filter flow during 2010.
- If you use the tool and find an issue, please try to re-create it keeping track of exactly how you got to that point and report it using the Feedback option. It is also helpful to save the design and share it.