PTKITPSTNUG
Rev. 1, 9/2005

Packet Telephony Development Kit PSTN Card

The public switched telephone network (PSTN) card in the Packet Telephony Development Kit (PDK) connects directly to the PDK baseboard and provides four narrow-band T1/E1 time-division multiplexing (TDM) ports that interface to the PSTN network. The PSTN subsystem also supports four analog telephony ports for direct interface to standard analog voice terminals. It provides a TDM stream for the DSP array (that is, MSC810xPFC card). **Figure 1** shows a snapshot of the PSTN card hardware.

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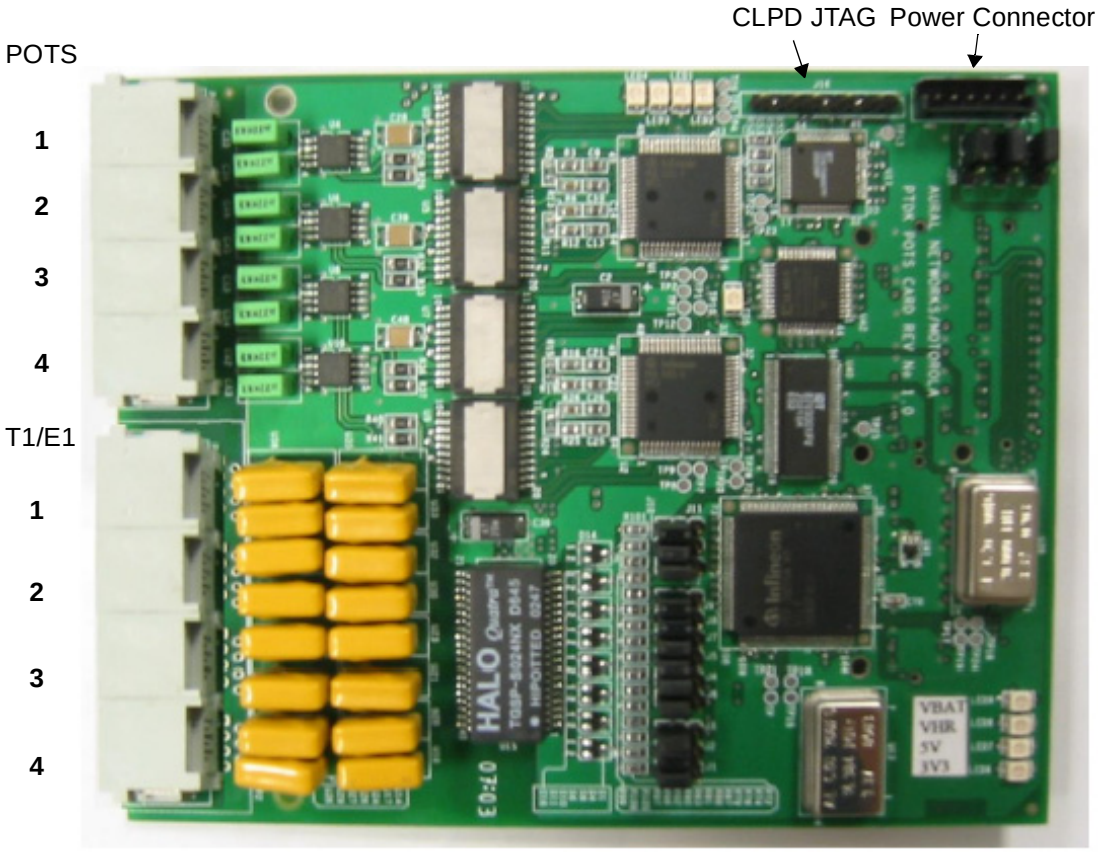


Figure 1. PSTN Hardware Overview

The PSTN card architecture consists of five main functional blocks, as shown in **Figure 2**:

- *Time slot switch.* 3.3 V time slot interchange (TSI) digital switch (IDT72V70800).
- *Digital E1/T1 interface*. Quad E1/T1/J1 framer and line interface component for long haul and short haul applications (PEB22554 V1.3).
- *PLL synchronization module*. WAN PLL with single-reference input (IDT82V30001A).
- *Complex programmable logic device (CPLD).* A low power 3.3V 32 macro-cell device (XCR3032XL) used for PLL control, reset, and chip-select management.
- *Plain Old Telephone Service (POTS)*. Two dual-channel subscriber line interfaces (PEB3264/-2) for analog telephone access.

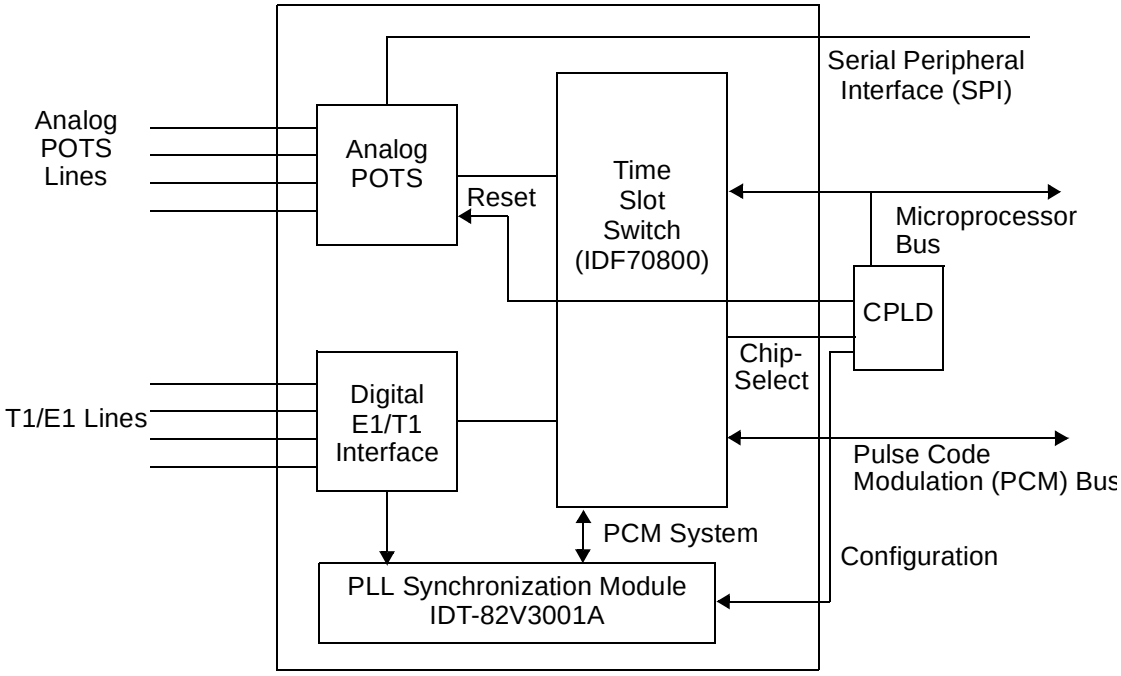


Figure 2. PSTN Card Architecture

1 Packet Telephony Development Kit

The Packet Telephony Development kit (PDK) is a platform for evaluating and developing voiceover packet applications. The PDK has an MPC8260 host network processor that runs Linus, StarCore™ DSP resource cards that run DSP code, and a Public Switched Telephone Network (PSTN) card with interfaces such as E1/T1 and analog telephone lines (see **Figure 3**).

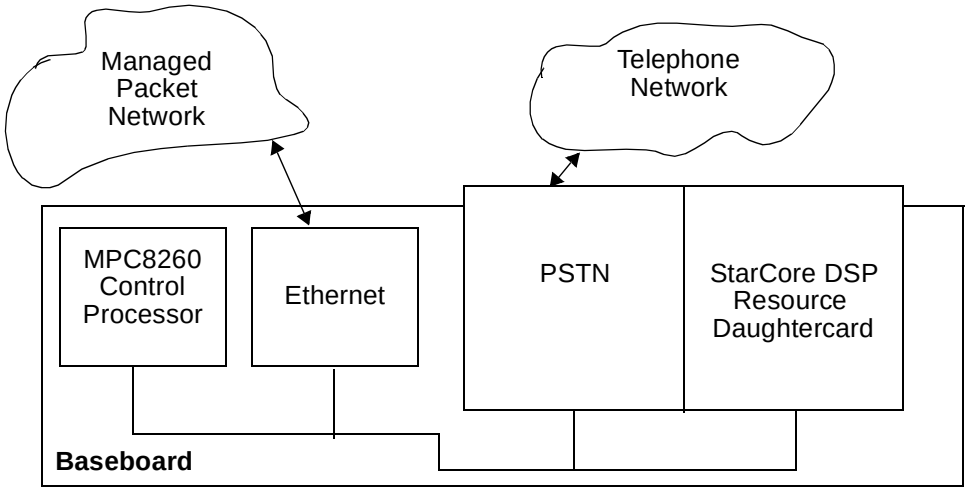


Figure 3. Components of the Packet Telephony Development Kit (PTK)

The documentation for the kit components is as listed in **Table 1**.

Table 1. PTK Components and Their Associated Documents

Component	Document	Document ID
Baseboard	Packet Development Kit Baseboard Hardware User's Guide	PTKITBASEUG
MPC8260 Control Processor	*MPC8260 PowerQUICC II™ Family Reference Manual* (Available at the website listed on the back page of this document.)	MPC8260UM
PSTN Card	*Packet Development Kit PSTN Card User's Guide*	PTKITPSTNUG
StarCore DSP Resource Daughtercard	• *MSC8102 Packet Telephony Farm Card (MSC8102PFC) User's Guide* • *MSC8101 Packet Telephony Farm Card (MSC8101PFC) User's Guide*	PTKIT8101UG PTKIT8102UG
StarCore DSP Resource	Reference manuals and other documentation for the MSC81xx products are located at the website listed on the back page of this user's guide.	
Software	*Packet Telephony Development Kit Software User's Guide*	PTKITSOFTUG

CAUTION: *The Packet Telephony Development Kit includes open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.*

2 Getting Started With the PSTN Card

This section presents unpacking instructions, hardware preparation, and installation instructions for bringing-up the PSTN card.

First, unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping the equipment. If the shipping carton is damaged upon receipt, request the carrier's agent to be present during unpacking and inspection of equipment.

Most systems have a PSTN card already attached to the baseboard. If you have purchased a PSTN card separately, you must plug it in. The PSTN card cannot operate as a stand-alone unit. The procedure for bringing up the PSTN is as follows:

1. Ensure that the PDK baseboard power supply is turned OFF.
2. Ensure that the stands off are connected to the PSTN card.
3. Gently connect the PSTN card PTMC connectors to the PDK baseboard.
4. Twist and tighten the PSTN card stands off to baseboard.
5. Ensure that the PSTN card is properly placed on top of the PDK baseboard.
6. If you plan to use the analog telephones, connect the J17 power connector (see **Section 5**, *Power Connector*, on page 17).
7. Turn on the power supply.

3 PSTN Card Components

This section discusses the main components of the PSTN card, which are the time slot switch, the digital E1/T1 interface, the PLL synchronization module, and the complex programmable logic device.

3.1 Time Slot Switch

The TSI performs time slot switching to set up and tear down voice connections between communicating entities. IDT-72V70800 is a 4-port switch that is dedicated to switch pulse code modulation (PCM) data between any two ports during call control. It is a non-blocking digital switch that has a capacity of 512 × 512 channels at a serial bit rate of 8.192 Mb/s. **Figure 4** shows an overview of the TSI module. Key features of the IDT-72V70800 TSI switch include:

- 64-kbit/s PCM channel switching.
- Freely programmable streams and time slot control.
- Data rate of 8.192 Mb/s equivalents to 128 PCM channels per port.
- Transmit to receive channel loop-back for diagnostics.
- Microprocessor control mode.
- High impedance output control.

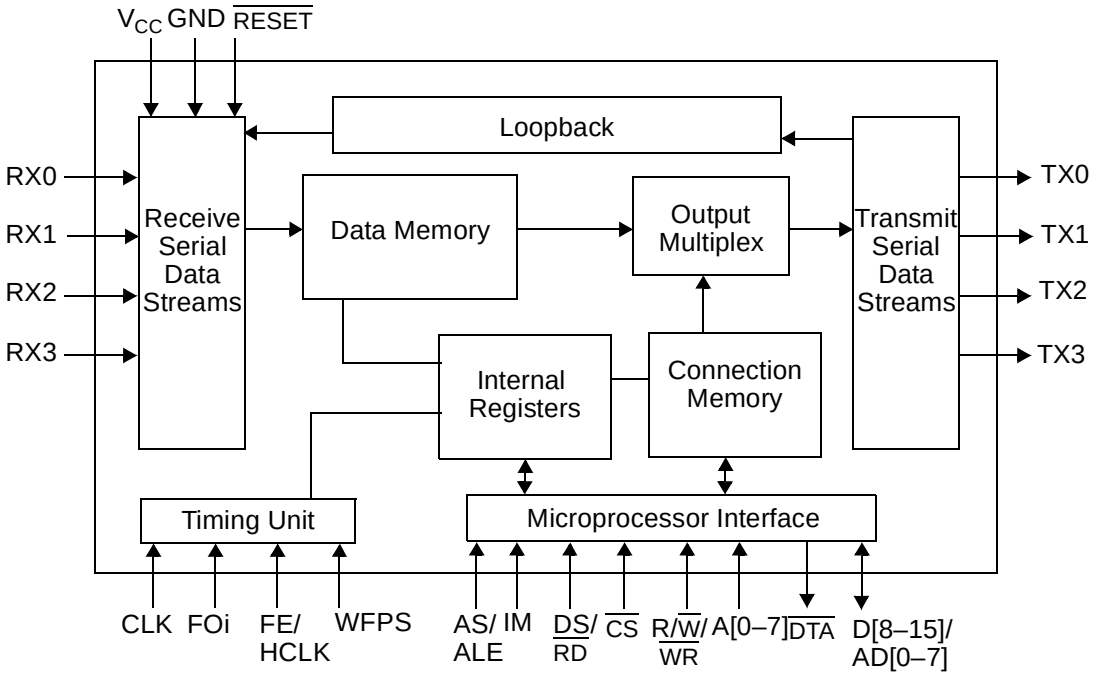


Figure 4. TSI Module

In the PSTN card, the TSI connects to the codec, Duslic (analog part of the PSTN card), QUADFALC (digital part of the PSTN card), and CPLD. **Figure 5** shows an overview of all PSTN modules that connect to the TSI. **Table 2** shows how the TSI connects the TDM streams.

Table 2. TSI Connections

TSI Stream	Connects to
0	Baseboard connector
1	E1/T1 PSTN card interface
3	Plain Old Telephone Service (POTS) Analog Telephony PSTN card interface
4	Baseboard connector

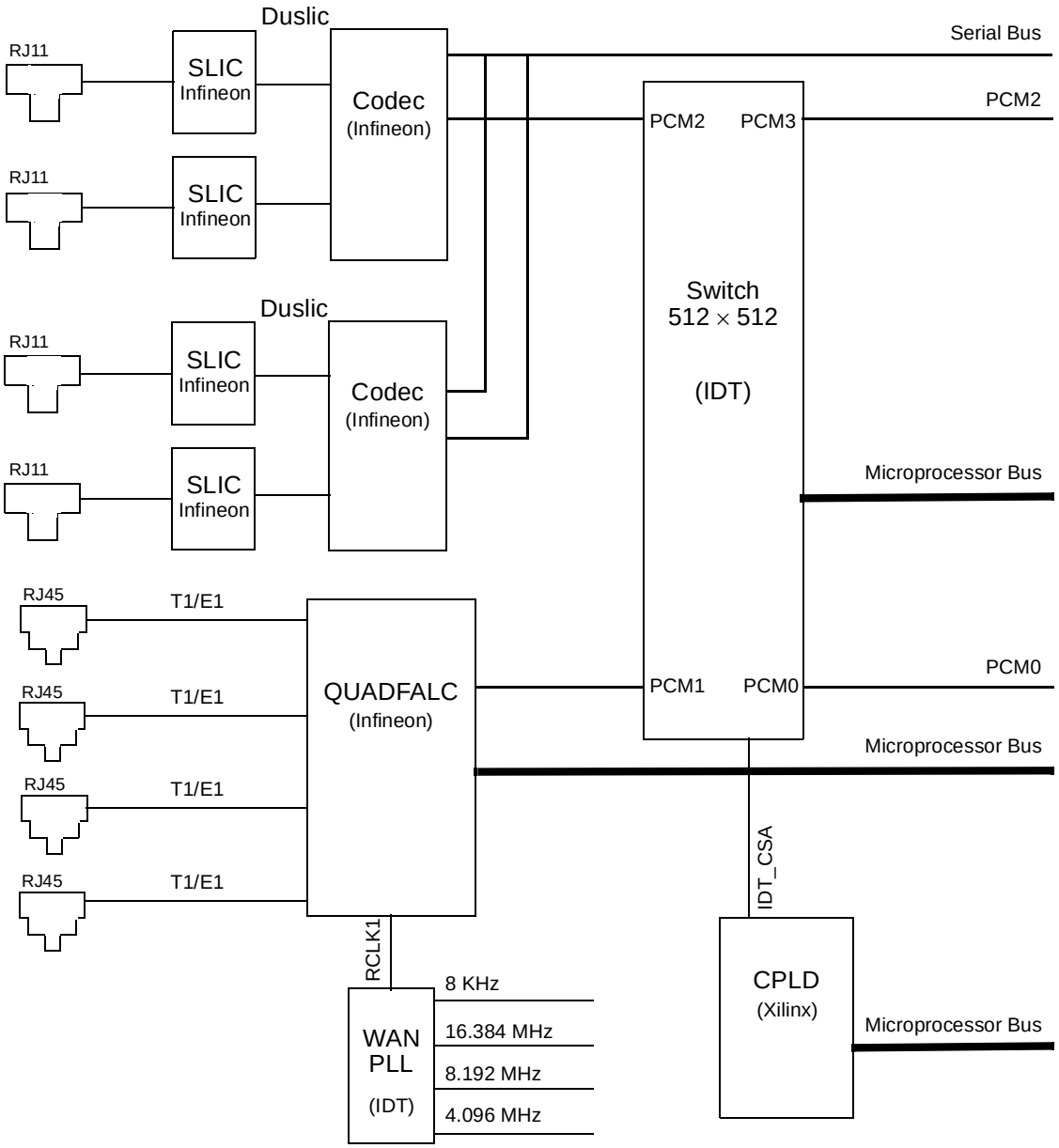


Figure 5. TSI Connections with Other PSTN Card Modules

The TSI is part of the PDK memory map. The MPC8260 device, which resides in the PDK baseboard, can access the TSI via chip select 9. Refer to **Table 3** and**Table 4** for TSI Base and Option Register settings, as well as UPM programming (MPC8260 memory controller programming to access the TSI).

Table 3. TSI Option and Base registers

Registers	Values
BR9 (TSI Base Register)	0xF8010C1
OR9 (TSI Option Register)	0xFFFF8106

Table 4. Initializing the TSI

Operations	Instructions
Single Read	MCMR = 0x10008800 MDR = 0x8FFFF000 MDR = 0x0FFCF380 MDR = 0x0FFCF300 MDR = 0x0FFCF300 MDR = 0x0FFCF300 MDR = 0x0FFCF380 MDR = 0x0FFCF004 MDR = 0x1FFFF001
Single Write	MCMR = 0x10008818 MDR = 0x0FF3F300 MDR = 0x0FF0F380 MDR =0x0FF0F300 MDR = 0x0FF0F300 MDR = 0x0FF0F380 MDR = 0x0FF0F004 MDR = 0x0FF0F300 MDR = 0x3FF3F001
Exception	MCMR=0x1000883C MDR = 0xFFFFCC05, MDR = 0xFFFFFFFF MDR = 0xFFFFFFFF MDR = 0xFFFFFFFF
Run	MCMR = 0x00008800

3.1.1 Duslic Module

The analog PSTN interface supports four loop start telephone subscriber ports. The Infineon Dual-Channel Subscriber Line Interface Concept (Duslic) PEB-3265 and PEB-4265 devices on the card form the interface between the TDM interface to the TSI and the physical twisted copper pair. There are four RJ-11 physical connectors on the PSTN card, as shown in **Figure 6**.

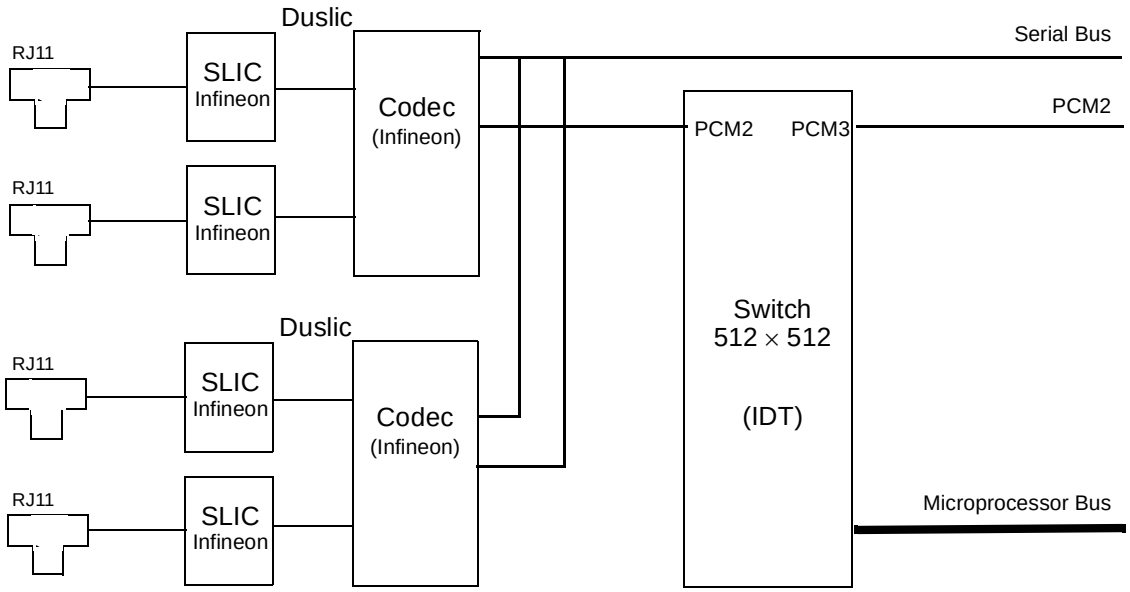


Figure 6. Duslic Connections to other Sub-modules of the PSTN Card

The Duslic requires that reset be applied when all the external clocks are stable. The CPLD ensures that the Duslic reset signal is asserted only after the clocks generated by the PLL device are stable, approximately 300 ns or longer after the PLL device undergoes reset.

The Duslic performs all the line interface functions generally known in the industry as the BORSCHT functions, as follows:

1. *Battery feed [B]*. Represents the voltage and current required to power the telephone equipment connected to the line. Battery voltage of –48 to –24 volts is fed directly into the Duslic devices from the PDK power supply
2. *Over voltage protection [O]*. Protects the PDK from damage to accidental exposure to high voltage, such as those resulting from lightning
3. *Ringing [R]*. The high voltage low frequency signal activated to ring the telephone equipment. Two programmable ringing modes are supported: balanced ringing where ringing voltage is applied differentially between tip and ring and unbalance ringing in which the ringing voltage is applied single-ended to either tip or ring. The ringing voltage of +30 to +60 volts is fed directly into the Duslic devices from the PDK power supply.
4. *Signaling or Supervision [S]*. Detects ON-hook and OFF-hook states for the telephone equipment connected to the line. ON/OFF hook can be detected while a station is ringing, which is referred to as Ring Trip Detection, or it may can detected while the station is not ringing, which is referred to as Switch Hook Detection.
5. *Coding [C]*. Converts the analog signals into PCM and *vice versa*. Two software configurable standard conversion algorithms are supported: A-law and μ-law. The default coding for the PDK is μ-law. The reset value for Duslic is A-law can be programmed to μ-law by changing bit 7 of register BCR3.
6. *Hybrid 2-to-4-wire conversions [H]*. A special network balancing circuit performs this function to match the line impedance so echo generation can be avoided. Hybrid balancing is a Duslic programmable option.
7. *Testing [T*]. Allows access to the loop so that regular diagnostic tests can be performed, including: loop resistance measurement, line capacitance, leakage current, ringing voltage, line feed current, and transversal and longitudinal current.

3.1.2 Duslic Configuration and Operation

The Duslic devices are configured directly by the baseboard host processor through the SPI interface. Specific values are written to Duslic registers to configure, for example, a given line into a specific mode of operation. Refer to the Duslic user's manual for detains on the functions of all registers supported.

During normal operation, specific Duslic registers must be read to determine the signaling exchanged between the subscriber telephone set and the PDK. Dynamic conditions that are constantly monitored by the host processor and appropriate action taken include ON-hook/OFF-hook signaling and DTMF signaling. The host processor can also command the Duslic through the SPI interface to generate ringing voltage or tones such as dial tone, busy tone, and reorder or fast busy tone.

3.2 Digital E1/T1 Interface

The digital E1/T1 interface supports four E1/T1 ports that can connect to central office (CO) lines such as ISDN PRI or PBX trunks. The Infineon QUADFALC FEB-22554 device forms the interface between the TDM interface to the TSI and the physical twisted copper pair. The QUADFALC recovers the PCM signal on the copper pairs and multiplexes them on the TDM bus to the TSI switch. There are four RJ-45 physical connectors on the PSTN card (see **Figure 7**). Each of the four digital interfaces of the QUADFALC includes a framer and a Line Interface Unit (LIU), a PLL circuit for clock recovery, an HDLC controller for signaling, and an 8-bit microprocessor interface for configuration.

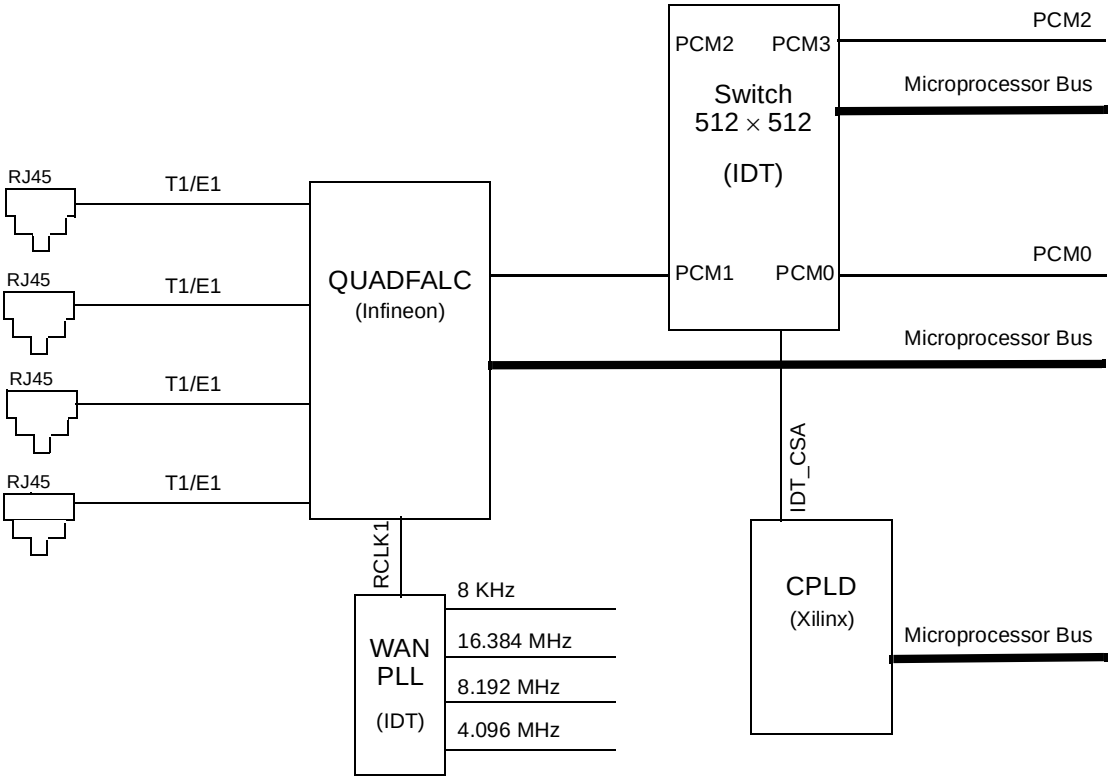


Figure 7. QUADFALC Connecting to Other Sub-modules of the PSTN Card

3.2.1 QUADFALC Clocking Options

The QUADFALC clocking configuration and the WAN-PLL device-clocking configuration jointly determine the timing mode. Two timing modes are supported: master and slave clocking. The combination of master or slave options provides maximum flexibility for telecommunications equipment developers using the PSTN card. In master clocking mode, the QUADFALC derives its timing from its local free running 16.384 MHz free running clock, as shown in **Figure 8**. The derived clock is either 1.544 MHz for T1 operation in North America or 2.048 MHz for E1 operation in Europe. This derived clock becomes the timing reference for the WAN-PLL device, which generates all the system clocks, including the PCM clocks for the PDK.

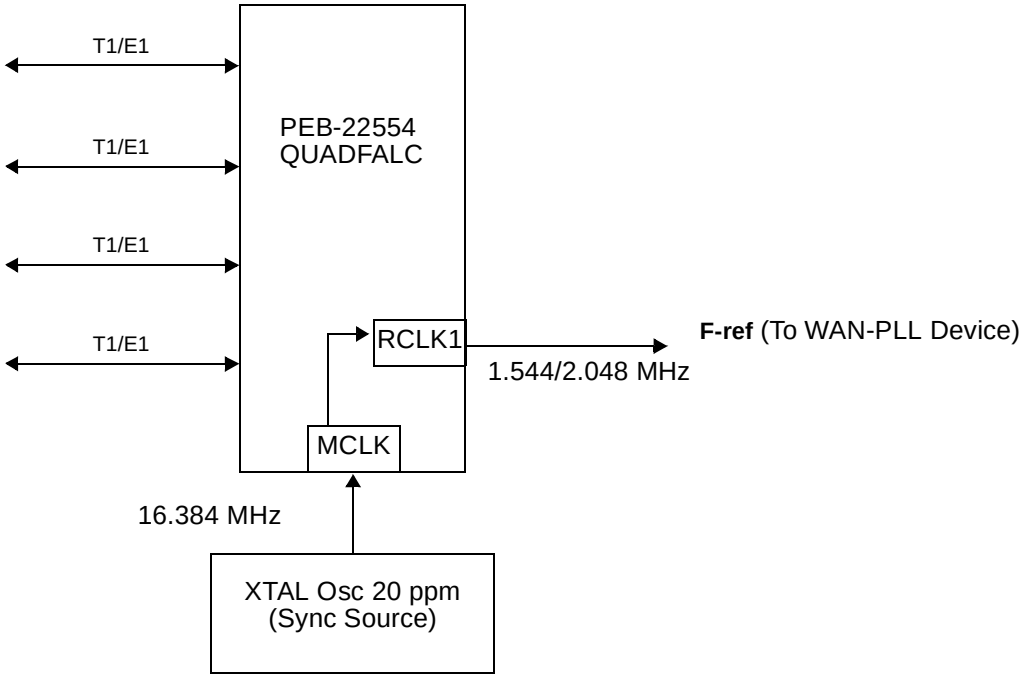


Figure 8. QUADFALC Master Clocking Mode Configuration

In slave clocking mode, the QUADFALC derives its timing reference from one of the four T1/E1 line terminated directly on the QUADFALC device as illustrated in**Figure 9**. The 1.544 MHz or 2.048 MHz derived clock is fed into the WAN-PLL device, which generates the system PCM clocks. Clocking for the QUADFALC is supplied through the MCLK pin; for the PDK this clock has a frequency of 16.384 MHz.

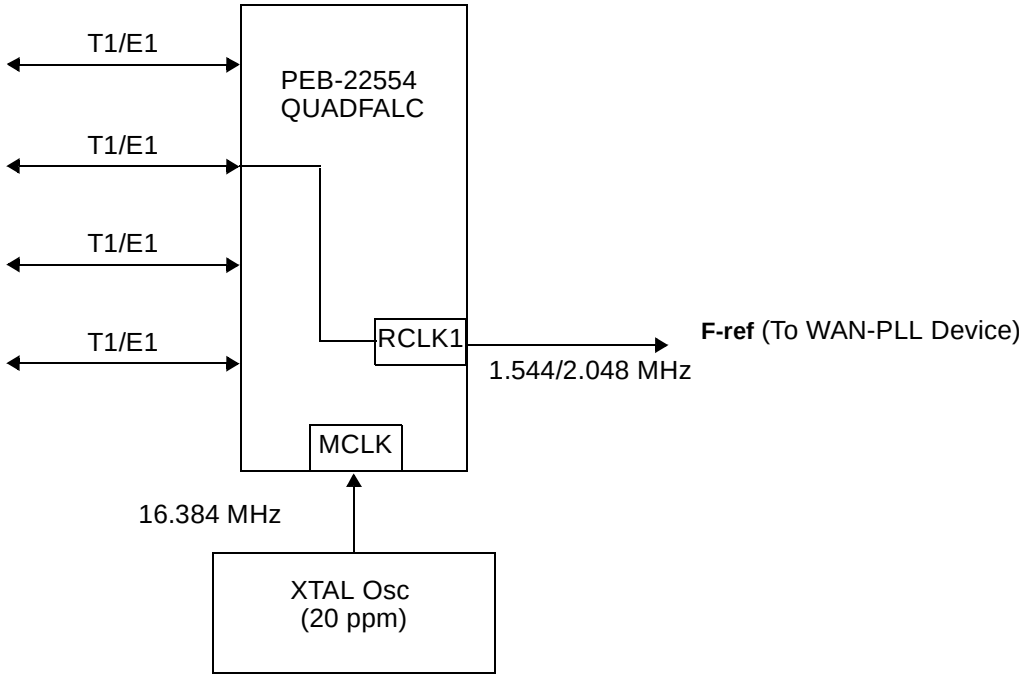


Figure 9. QUADFALC Slave Clocking Mode Configuration

3.2.2 QUADFALC Default Operating Mode

The QUADFALC is part of the PDK memory map, and the MPC8260 device, which resides in the PDK baseboard, can access the QUADFALC via chip select 8. Refer to **Table 5** and **Table 6** for QUADFALC Base and Option Register values, as well as UPM programming

Table 5. QUADFALC Option and Base Registers

Registers	Values
BR8 (QUADFALC Base Register)	0xF70008A1
OR8 (QUADFALC Option Register)	0xFFFF8106

Table 6. QUADFALC UPM Programming

Operations	Instructions
Single Read	MBMR = 0x10015400 MDR = 0x8FFFF000 MDR = 0x0FFCF300 MDR = 0x0FFCF300 MDR = 0x0FFCF004 MDR = 0x0FFFF300 MDR = 0x0FFFF300 MDR = 0x3FFFF001

Table 6. QUADFALC UPM Programming (Continued)

Operations	Instructions
Single Write	MBMR = 0x10015418 MDR = 0x0FF3F000 MDR = 0x0FF0F300 MDR = 0x0FF0F300 MDR = 0x0FF0F004 MDR = 0x0FF3F300 MDR = 0x0FF3F300 MDR = 0x3FF3F001
Exception	MBMR=0x1001543C MDR= 0xFFFFCC05,
Run	MBMR=0x00015400

3.3 PLL Synchronization Module

The IDT-82V3001 PLL device generates timing (clock) and synchronization (framing) signals for the PCM bus. The IDT82V3001A is a WAN PLL with single reference input. It contains a Digital Phase-Lock Loop (DPLL), which generates clock and framing signals that are phase locked to a 2.048 MHz, 1.544 MHz, or 8 kHz input reference. The PLL circuitry generates all TDM synchronization clocks used in the PDK, including the PCM interface clocks. These clocks can either be generated locally (via the QUADFALC device) if the PDK is operating in Master mode or be derived from any one of the T1/E1 lines by the QUADFALC if the PDK is operating in Slave mode. The two relevant modes of operation for the IDT82V3001 are Free Run mode and Normal mode.

3.3.1 Free Run Mode

In Free Run mode, the PLL device uses its local clock (as opposed to the reference frequency) to synthesize the system clock. The Free Run clocking mode for IDT-82V3001 is not used; only the Normal clocking mode is used, as described in the following section.

3.3.2 Normal Mode

When the PLL device is configured in Normal mode, the frequency reference is received from the QUADFALC, as illustrated in **Figure 10**. The timing reference fed into the PLL device is derived from one of the T1/E1 lines. In this case, the second line is used as the timing reference source. However, any of the four digital lines terminated on the PSTN card can be used as the timing reference source. This is a QUADFALC software configuration feature.

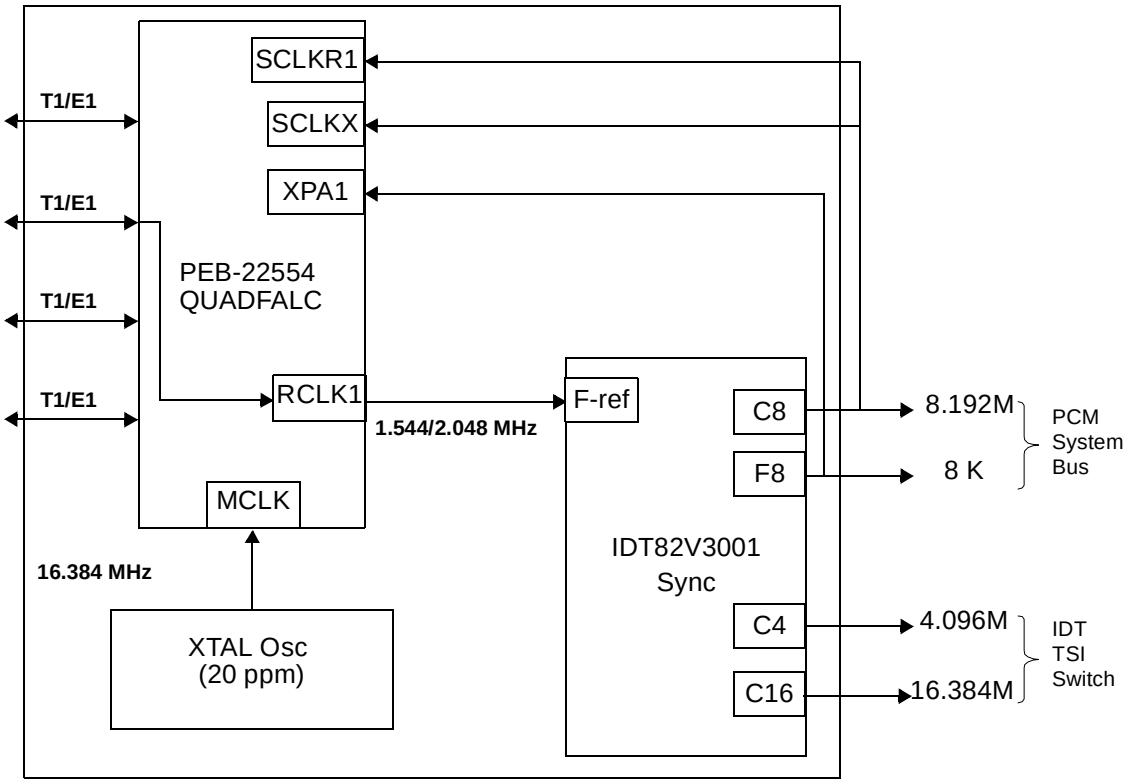


Figure 10. WAN-PLL Device in Support of Slave Clocking Mode

To operate the PLL device in Normal mode, the Mode_sel_0 signal must be set to 0, and the Mode_sel_1 signal must be set to 0 through the CPLD, as shown in **Table 7**. To complete the PLL configuration, the input reference frequency into the PLL must also be selected. In this case, the PRI frequency is 1.544 MHz in North America or 2.048 MHz in Europe. Frequency selection of 1.544 MHz (North America) is achieved by setting Freq_sel_0 = 0 and Freq_sel_1 = 1 via the CPLD. For Europe, the values are Freq_sel_0 = 1 and Freq_sel_1 = 1 via the CPLD.

Table 7. ID72V3001 Normal Mode Configuration

Mode Select		Frequency Select		Comment
mode_sel_1	mode_sel_0	Freq_sel_1	Freq_sel_0	
0	0	1	0	North America
0	0	1	1	Europe

If the PDK is operating in Master clocking mode, the frequency reference is generated locally by the QUADFALC and fed directly into the PLL device. Software can configure the QUADFALC to source a free running clock from it local 16.384 MHz oscillator fed through the MCLK pin. This clock has a stability of 20 ppm, as illustrated in **Figure 11**.

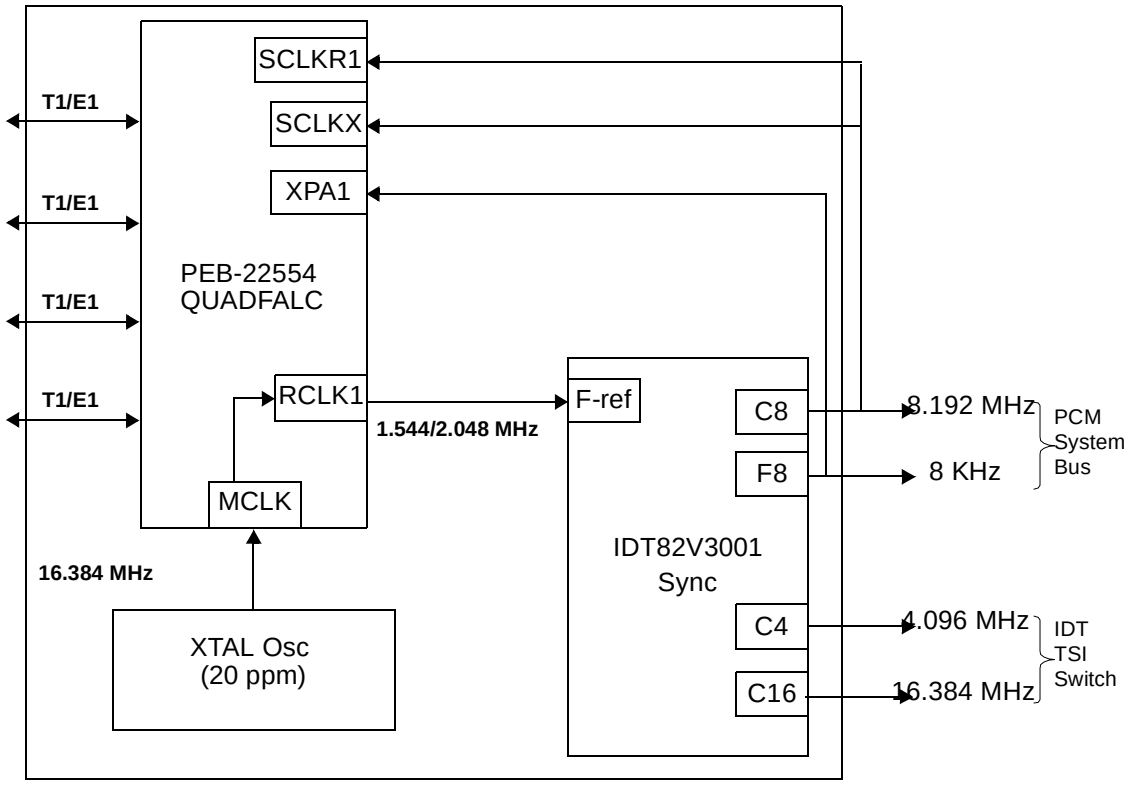


Figure 11. WAN-PLL in support of Master Clocking Mode

The default clocking option for the PDK is Master synchronization as illustrated in **Figure 11**. The default reference clock fed into the PLL device from the QUADFALC is 1.544 MHz, representing the North American digital transmission line standard.

3.4 Complex Programmable Logic Device (CLPD)

The glue logic to help control access and configuration of all devices on the PSTN card is implemented on a CPLD. The CPLD decodes the addresses to generate the chip select for the TSI device and the control signals for the PLL device. The CPLD also monitors the PLL device and generates the Loss of Synchronization signal for the operation status indicator or LED.

3.4.1 Chip-Select Logic

The CPLD uses address line 22 to select between assertion of the IDT time-slot switch and accesses to its own internal registers, as shown in **Table 8**.

Table 8. Chip-Select Truth Table

PQ2_CS_TDM2 Chip Select Input From the Baseboard	CONN_AD22 Address Line Input From the Baseboard	IDT Time Slot Switch Chip Select	Internal CPLD Chip Select
1	X	1	1
0	0	0	1
0	1	1	0

3.4.2 Output Signals

Writes to the memory-mapped registers control the output signals on the CPLD. **Table 9** lists and describes the registers. The address column refers to the address from which to write over the bus A[22–31]. The physical address pins to the CPLD are only A[22–30]. The data bus bit is latched on to the output signal. Thus, to turn off the LED, for example, one would write a value of 0x01 to address 0x20E. The physical address lines CONN_AD[22–30] would be 100000111 and the 1 from D[15] would be latched causing the PLD_LOS_FALC signal to go high.

Table 9. CPLD Memory Map

Address	Output Signal Name	Data Bus Bit	Read/ Write	Default Value	Description
0x200	PLD_MODE_SEL0	D[14]	R/W	0	Determine the state (Normal, Holdover, or Free Run) of the WAN PLL.
	PLD_MODE_SEL1	D[15]	R/W	0	
0x202	PLD_F_SEL0	D[14]	R/W	1	Determine the input reference frequency of the WAN PLL.
	PLD_F_SEL1	D[15]	R/W	1	
0x204	NORMAL_PLD	D[15]	R	—	Goes high when the WAN PLL goes into Normal mode.
0x206	LOCK_PLD	D[15]	R	—	Goes high when the WAN PLL is locked to the input reference frequency.
0x208	PLD_TCLRn	D[15]	R/W	1	Logic low at this signal resets the TIE control block of the WAN PLL, resulting in a realignment of the output phase with the input phase.
0x20A	PLD_TIE_en	D[15]	R/W	1	Logic high at this signal enables the TIE block of the WAN PLL.
0x20C	PLD_DUSLIC_TSI_RSTn	D[15]	R/W	1	Logic low at this signal resets the DuSLIC (U1 & U2) and TSI switch.
0x20E	PLD_LOS_FALC	D[15]	R/W	1	Logic low at this signal lights an LED.
0x210	HOLDOVER_PLD	D[15]	R	—	Goes to a logic high when the WAN PLL goes to Holdover mode.
0x212	PLD_WAN_PLL_RSTn	D[15]	R/W	1	Logic low at this signal resets the WAN PLL.

3.4.3 JTAG

The J16 header is used for programming the CPLD. The PSTN card comes programmed and use of this header should not be needed.

Note: Do not reconfigure the Xilinx chip in the PSTN card. Attempts to do so may lead to instability in the system.

Table 10. Xilinx JTAG Signals

Pin	JTAG Signal
1	+5V
2	GND
3	NC
4	TCK

Table 10. Xilinx JTAG Signals (Continued)

Pin	JTAG Signal
5	NC
6	TDO
7	TDI
8	NC
9	TMS

The only module that connects to the baseboard JTAG chain is the QUADFALC. PTMC connector J15 enables the JTAG chain between the baseboard and the PSTN card.

Note: The baseboard JTAG chain must be configured to add the PSTN JTAG with the baseboard JTAG chain. Refer to the baseboard user's manual for details on JTAG chain configuration.

4 PSTN Card LEDs and Jumpers

This section describes the LEDs and jumpers of the PSTN card.

Table 11. PSTN Card LEDs

LED	Description
1	Indicates the Hook Status of the analog subscriber line 1 (P1.B1). LED1 is controlled by the port IO1B of the PEB3265 It can be programmed to show the ON/OFF hook status for the corresponding subscriber line.
2	Indicates the Hook Status of the analog subscriber line 2 (P1.B1). LED2 is controlled by the port IO1A of the PEB3265 It can be programmed to show the ON/OFF hook status for the corresponding subscriber line.
3	Indicates the Hook Status of the analog subscriber line 3 (P1.D1). LED3 is controlled by the port IO1B of the PEB3265 It can be programmed to show the ON/OFF hook status for the corresponding subscriber line.
4	Indicates the Hook Status of the analog subscriber line 4 (P1.C1). LED4 is controlled by the port IO1A of the PEB3265 It can be programmed to show the ON/OFF hook status for the corresponding subscriber line.
5	Shows the Loss Of Signal/Synchronization status of the QUADFALC device. It connects to a GPIO (pin no. 23) of the CPLD. It is illuminated when the processor determines the Loss of Signal status after reading the Frame Receive Status Register 0 (FRS0) of the QUADFALC.
6	3.3V power indication on PSTN. It is illuminated when 3.3V power rail is active.
7	5V power indication on PSTN card. It is illuminated to indicate that the 3.3V voltage is available on the board.
8	VHR (Ringing Voltage) power indication on PSTN card. It is illuminated to indicate ringing voltage is available.
9	VBATHX (Battery Voltage) power indication on PSTN. It is illuminated to indicate that the battery or line voltage is available on the board.

Note: For the jumper settings, ON means place jumper and OFF means no jumper.

Table 12 summarizes all jumper settings in the PSTN card. Jumper settings are verified before they are shipped to customers.

Table 12. Jumper Settings

Jumper	Meaning	Default Setting
J1–J11	Switches between T1 and E1 termination. Shunt pins 1–2: E1. Shunt pins 2–3: T1.	T1 (Pins 2–3 connected)
J18	Selects source of +3.3V power supply. Shunt pins 1–2: Power comes from power connector J17. Shunt pins 2–3: Power comes from the baseboard	Baseboard power (Pins 2–3 connected)
J19	Selects source of +5V power supply. Shunt pins 1–2: Power comes from power connector J17. Shunt pins 2–3: Power comes from the baseboard.	Baseboard power (Pins 2–3 connected)
J20	Selects source of VHR (Ringing) power supply. Shunt pins 1-2: Power comes from power connector J17. Shunt pins 2-3: Power comes from the baseboard.	Baseboard power (Pins 2–3 connected)

5 Power Connector

Table 13 lists all power supplies used in the PSTN card from J17. The 48 V battery supply must be sourced through this connector. All other supplies can come either from the baseboard or through J17 by using jumpers J18–J20.

Table 13. PSTN Card Power Supply Distribution

Pin	Value	Description
1	3.3 V	I/O power. By default, the 3.3 V power comes from the baseboard. See **Table 12**.
2	+5 V	5 V power. By default, the 5 V power comes from the baseboard. See **Table 12**.
3	+48 V	Ringing voltage for telephones.
4	–48 V	Battery supply for telephones.
5	GND	
6	GND	

6 PSTN Card Interface

The baseboard and the PSTN card share common signals, such as address, data, and control lines. The signals travel through PTMC connectors that connect the PDK baseboard to the PSTN card, as shown in **Figure 12**.

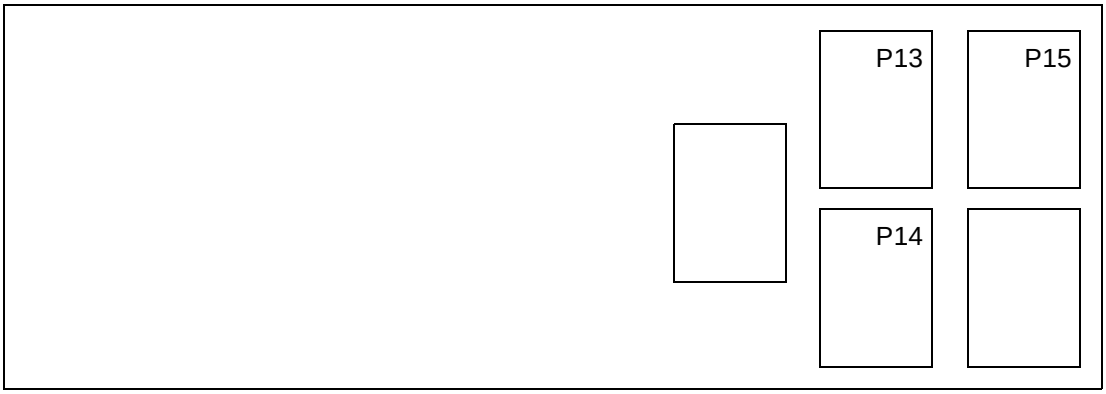


Figure 12. Baseboard PTMC Connected

Table 14. PTMC 15 Header

Pin	Signal	Pin	Signal
1	TDM_SPI_CS1	2	JTAG_TRST
3	JTAG_TMS	4	TDM_TDO
5	TDM_TDI	6	GND
7	GND	8	JTAG_TCK
9	CONN_D0	10	CONN_AD23
11	CONN_D1	12	Vcc (5.0 v)
13	TDM_RESET	14	CONN_AD24
15	Vcc (5.0 v)	16	CONN_AD25
17	CONN_D2	18	GND
19	CONN_D3	20	CONN_AD26
21	GND	22	CONN_AD27
23	CONN_D4	24	Vcc (3.3 v)
25	CONN_D5	26	CONN_AD28
27	Vcc (3.3 v)	28	CONN_AD29
29	CONN_D6	30	GND
31	CONN_D7	32	CONN_AD30
33	GND	34	CONN_AD31
35	CONN_D8	36	Vcc (3.3 v)
37	GND	38	TDM_TO_PQ2_INT1
39	CONN_D9	40	GND
41	Vcc (3.3 v)	42	PQ2_CS_TDM1
43	CONN_D10	44	GND
45	CONN_D11	46	TDM_GPL2

Table 14. PTMC 15 Header (Continued)

Pin	Signal	Pin	Signal
47	GND	48	TDM_GPL1
49	CONN_D12	50	Vcc (3.3 v)
51	CONN_D13	52	PQ2_CS_TDM2
53	Vcc (3.3 v)	54	TDM_SPI_CS0
55	CONN_D14	56	GND
57	CONN_D15	58	TDM_SPIMOSO
59	GND	60	TDM_SPIMOSI
61	CONN_AD22	62	Vcc (3.3 v)
63	GND	64	TDM_SPICLK

Table 15. PTMC 14 Header

Pin	Signal	Pin	Signal
1	NC	2	GND
3	GND	4	V_{CC} (5.0 V)
5	NC	6	NC
7	V_{CC} (5.0 V)	8	GND
9	NC	10	V_{CC} (5.0 V)
11	V_{CC} (5.0 V)	12	NC
13	NC	14	GND
15	GND	16	NC
17	CT_FRAME_A	18	V_{CC} (5.0 V)
19	NC	20	GND
21	NC	22	NC
23	NC	24	V_{CC} (5.0 V)
25	CT_C8_A	26	GND
27	GND	28	NC
29	NC	30	NC
31	NC	32	GND
33	GND	34	NC
35	NC	36	V_{CC} (5.0 V)
37	NC	38	GND
39	NC	40	NC
41	NC	42	V_{CC} (5.0 V)

Table 15. PTMC 14 Header (Continued)

Pin	Signal	Pin	Signal
43	NC	44	GND
45	GND	46	NC
47	NC	48	NC
49	NC	50	NC
51	GND	52	NC
53	NC	54	NC
55	CT_D4	56	GND
57	V_{CC} (5.0 V)	58	CT_D5
59	NC	60	NC
61	CT_D0	62	GND
63	GND	64	CT_D1

Table 16. PTMC 13 Header

Pin	Signal	Pin	Signal
1	NC	2	NC
3	GND	4	NC
5	NC	6	NC
7	NC	8	V_{CC} (5.0 V)
9	NC	10	NC
11	GND	12	NC
13	NC	14	GND
15	GND	16	NC
17	NC	18	V_{CC} (5.0 V)
19	V_{CC} (3.3 V)	20	NC
21	NC	22	NC
23	NC	24	GND
25	GND	26	NC
27	NC	28	NC
29	NC	30	V_{CC} (5.0 V)
31	NC	32	NC
33	NC	34	GND
35	GND	36	NC
37	NC	38	V_{CC} (5.0 V)

Table 16. PTMC 13 Header (Continued)

Pin	Signal	Pin	Signal
39	GND	40	NC
41	NC	42	NC
43	NC	44	GND
45	V_{CC} (3.3 V)	46	NC
47	NC	48	NC
49	NC	50	V_{CC} (5.0 V)
51	GND	52	NC
53	NC	54	NC
55	TDM_GPIO2	56	GND
57	V_{CC} (3.3 V)	58	TDM_TO_PQ2_INT2
59	TDM_GPIO1	60	TDM_TO_PQ2_INT3
61	TDM_GPIO0	62	V_{CC} (5.0 V)
63	GND	64	NC

7 Default TDM Interface Timing

Figure 13 diagrams the PSTN default TDM interface to the DSP daughter card. The default is 128 channels per frame, 8 bits per channel. This yields 8.192 Mbps with an 8 K Hz frame synchronization signal.

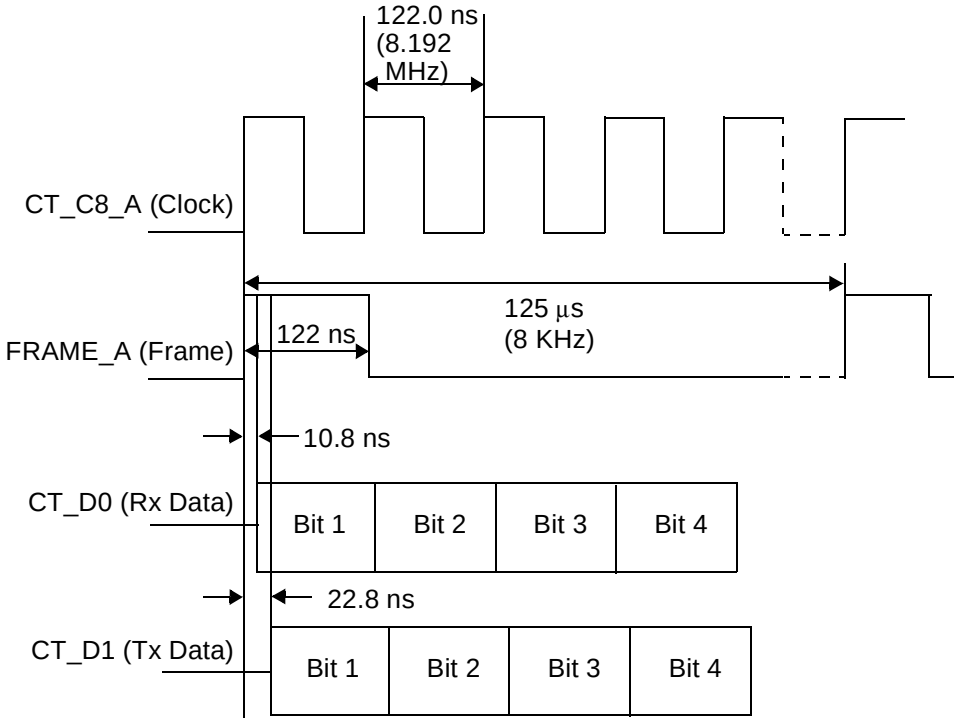


Figure 13. PSTN Card Default TDM Interface

Appendix A CPLD Source

```
        library IEEE;
        use IEEE.STD_LOGIC_1164.ALL;
        use IEEE.STD_LOGIC_ARITH.ALL;
        use IEEE.STD_LOGIC_UNSIGNED.ALL;

        --declaration of INPUT and OUTPUT ports

        entity pdk_cpld is
            Port (
                                                PQ2_CS_TDM2             : in std_logic;
                                                CONN_AD22                       : in std_logic;
                                                CONN_AD                                 : in std_logic_vector(27
to 30);
                                                CONN_D13                                : out std_logic;
                                                CONN_D14                                : in std_logic;
                                                CONN_D15                                : in std_logic;
                                                TDM_GPL1                        : in std_logic;
                                                TDM_GPL2                                : in std_logic;
                                                HOLDOVER_PLD            : in std_logic;
                                                LOCK_PLD                                : in std_logic;
                                                NORMAL_PLD                      : in std_logic;
                                                CT_C8_A                                 : in std_logic;
                                                TDM_RESET                       : in std_logic;
                                                CT_FRAME                                : in std_logic;
                                                CT_STFRAMEn                     : in std_logic;
                                                CT_WFRAMEn                      : in std_logic;
                                                PLD_MODE_SEL0           : out std_logic;
                                                PLD_MODE_SEL1           : out std_logic;
                                                PLD_F_SEL0                      : out std_logic;
                                                PLD_F_SEL1                      : out std_logic;
                                                PLD_TCLRn                       : out std_logic;
                                                PLD_TIE_en                      : out std_logic;
                                                PLD_DuSLIC_TSI_RSTn : out std_logic;
                                                PLD_WAN_PLL_RSTn : out std_logic;
                                                PLD_LOS_FALC            : out std_logic;
                                                PLD_IDT_CSn                     : out std_logic;
                                                CT_FRAME_A                      : out std_logic;
                                                PLD_QFALC_FRAME  : out std_logic);

        end pdk_cpld;

        architecture pdk_cpld of pdk_cpld is

        signal signal_main_dec: std_logic;-- internal signal whic enables address decoder
        signal signal_cpld_dec: std_logic_vector( 11 downto 0 ); -- internal signals which are out from address
decoder
        signal signal_r_w_bar : std_logic;
        signal signal_w_bar   :std_logic;
        signal signal_r  :std_logic;

        signal sel_mux1: std_logic_vector(1 downto 0); -- select signals to select frame sync for Base card
connectors
        signal sel_mux2: std_logic_vector(1 downto 0); -- select signals to select frame sync for QuadFALC
(optional)

        begin

        -- two bit decoder which selects IDT switch or address decoder of CPLD.

        process(PQ2_CS_TDM2,CONN_AD22)
        begin

        --  the selection between IDT switch and cpld address decoder is done depending
        --  upon status of PQ2_CS_TDM2 and CONN_AD22 .If PQ2_CS_TDM2 is 0 the selection
        --  between IDT switch and CPLD address decoder is done based on CONN_AD22,
        --  if CONN_AD22 is 0 then IDT switch is selected or if CONN_AD22 is 1 then
        --  CPLD address decoder is selected,  else if PQ2_CS_TDM2 = 1 then both
        -- IDT switch and CPLD address decoder will be disabled.

         if ( PQ2_CS_TDM2 = '0' and CONN_AD22 ='0')then

                        PLD_IDT_CSn <= '0';
                        signal_main_dec <= '1';

                elsif ( PQ2_CS_TDM2 = '0' and CONN_AD22 = '1')then

                     PLD_IDT_CSn <= '1';
                             signal_main_dec <= '0';
        else
```

```
                PLD_IDT_CSn <= '1';
                signal_main_dec <= '1';

end if;

end process;

--end of two bit decoder

--Following process  is to implement the CPLD address decoder,which will be
--enabled by output signal "signal_main_dec" of two bit decoder.
--Inputs for this decoder are AD[27:30] ,out put will be nine enable signals
--for internal latchs.

process(signal_main_dec,CONN_AD)
begin

if ( signal_main_dec = '0') then
   case CONN_AD is
      when "0000" => signal_cpld_dec <= "111111111110";
      when "0001" => signal_cpld_dec <= "111111111101";
      when "0010" => signal_cpld_dec <= "111111111011";
      when "0011" => signal_cpld_dec <= "111111110111";
      when "0100" => signal_cpld_dec <= "111111101111";
      when "0101" => signal_cpld_dec <= "111111011111";
      when "0110" => signal_cpld_dec <= "111110111111";
      when "0111" => signal_cpld_dec <= "111101111111";
           when "1000" => signal_cpld_dec <= "111011111111";
                when "1001" => signal_cpld_dec <= "110111111111";
                when "1010" => signal_cpld_dec <= "101111111111";
                when "1011" => signal_cpld_dec <= "011111111111";
      when others => signal_cpld_dec <= "111111111111";
   end case;

else

       signal_cpld_dec <= "111111111111";

end if;
end process;

--end of CPLD address decoder

-- Following process  is to implement the two bit latch for mode select signals
-- for WAN PLL.
-- Default mode is NORMAL MODE i.e both signals are 0.
-- WAN PLL mode can be changed by writing into latch at address
-- CONN_AD[22:30] = 1XXXX0000 using CONN_D[14:15]

process (signal_cpld_dec(0),TDM_RESET,CONN_D15,CONN_D14,signal_w_bar)
begin

if TDM_RESET ='0' then

                PLD_MODE_SEL0 <= '0';
                PLD_MODE_SEL1 <= '0';

elsif signal_cpld_dec(0) = '0'  and signal_w_bar = '0' then

                PLD_MODE_SEL0 <= CONN_D15;
                PLD_MODE_SEL1 <= CONN_D14;
end if ;

end process;

-- implementation of two bit latch for Input reference frequency select signals
-- for WAN PLL.
-- Default Input reference frequency is 1.544 MHz(T1 mode).
-- WAN PLL Input reference frequency can be changed by writing into latch
-- at address CONN_AD[22:30] = 1XXXX0001 using CONN_D[14:15]

process (signal_cpld_dec(1),CONN_D15,CONN_D14,signal_w_bar,TDM_RESET)

begin

if TDM_RESET ='0' then


                PLD_F_SEL0 <= '0';
                PLD_F_SEL1 <= '1';

elsif signal_cpld_dec(1) = '0'and signal_w_bar = '0' then
                PLD_F_SEL0 <= CONN_D15;
```

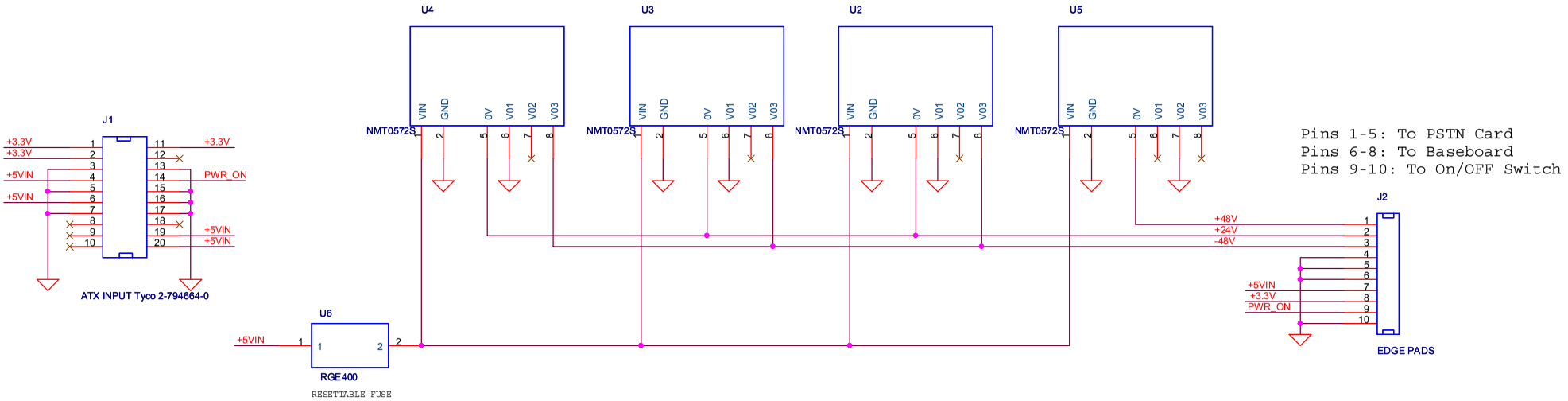
```
                    PLD_F_SEL1 <= CONN_D14;
        end if ;

        end process;

        -- implementation of status read signal (NORMAL_PLD) of WAN PLL at ADDRESS
        -- CONN_AD[22:30] = 1XXXX0010 using CONN_D[15]

        process (
signal_r,NORMAL_PLD,HOLDOVER_PLD,LOCK_PLD,signal_cpld_dec(2),signal_cpld_dec(8),signal_cpld_dec(3))

        begin

        if signal_cpld_dec(2) = '0' and  signal_r = '1' then

                  CONN_D13 <= NORMAL_PLD;

        -- implementation of status read signal(HOLDOVER_PLD) of WAN PLL at ADDRESS
        -- CONN_AD[22:30] = 1XXXX1000 using CONN_D[15]

        elsif signal_cpld_dec(8) = '0' and  signal_r = '1' then

                  CONN_D13 <= HOLDOVER_PLD;

        -- implementation of status read signal(LOCK_PLD) of WAN PLL at ADDRESS
        --CONN_AD[22:30] = 1XXXX0011 using CONN_D[15]

        elsif signal_cpld_dec(3) = '0' and  signal_r = '1' then
                 CONN_D13 <= LOCK_PLD;
        else
          CONN_D13 <= 'Z';
        end if;

        end process;


        -- implementation of one bit latch for signal(PLD_TCLRn)of WAN PLL at ADDRESS
        -- CONN_AD[22:30] = 1XXXX0100 using CONN_D[15]
        -- default PLD_TCLRn <= 1

        process (signal_cpld_dec(4),TDM_RESET,CONN_D15,signal_w_bar)
        begin
        if TDM_RESET ='0' then

                    PLD_TCLRn <= '1';

        elsif signal_cpld_dec(4) = '0' and signal_w_bar = '0' then

                    PLD_TCLRn <= CONN_D15 ;
        end if ;

        end process;

        -- implementation of one bit latch for signal(PLD_TIE_en)of WAN PLL at ADDRESS
        -- CONN_AD[22:30] = 1XXXX0101 using CONN_D[15]
        -- default PLD_TIE_en <= 1

        process (signal_cpld_dec(5),TDM_RESET,CONN_D15,signal_w_bar)
        begin
        if TDM_RESET ='0' then

                    PLD_TIE_en <= '1';


        elsif signal_cpld_dec(5) = '0'and signal_w_bar = '0' then

                    PLD_TIE_en <= CONN_D15;

        end if ;

        end process;

        -- implementation of one bit latch for signal(PLD_DuSLIC_TSI_RSTn) for DuSLIC and TSI reset  at
        -- ADDRESS CONN_AD[22:30] = 1XXXX0110 using CONN_D[15]
        -- default PLD_DuSLIC_TSI_RSTn <= 1


        process (signal_cpld_dec(6),TDM_RESET, CONN_D15,signal_w_bar)
        begin
        if TDM_RESET ='0' then

                    PLD_DuSLIC_TSI_RSTn <= '1';
```

```
elsif signal_cpld_dec(6) = '0' and signal_w_bar = '0'then

                PLD_DuSLIC_TSI_RSTn <= CONN_D15;
end if ;

end process;

-- implementation of one bit latch for signal(PLD_LOS_FALC) for FALC at
-- ADDRESS CONN_AD[22:30] = 1XXXX0111 using CONN_D[15]
-- default PLD_LOS_FALC <= 1

process (signal_cpld_dec(7),TDM_RESET,CONN_D15,signal_w_bar)
begin
if TDM_RESET ='0' then

                PLD_LOS_FALC <= '1';

elsif signal_cpld_dec(7) = '0'and signal_w_bar = '0' then

                PLD_LOS_FALC <= CONN_D15;
end if ;

end process;

-- implementation of one bit latch for signal(PLD_WAN_PLL_RSTn) for WAN PLL reset  at
-- ADDRESS CONN_AD[22:30] = 1XXXX1001 using CONN_D[15]
-- default PLD_WAN_PLL_RSTn <= 1


process (signal_cpld_dec(9),TDM_RESET, CONN_D15,signal_w_bar)
begin
if TDM_RESET ='0' then

                PLD_WAN_PLL_RSTn <= '1';

elsif signal_cpld_dec(9) = '0' and signal_w_bar = '0'then

                PLD_WAN_PLL_RSTn <= CONN_D15;
end if ;

end process;

-- Following process  is to implement the two bit internal latch for select signals
-- of MUX1 used to to select frame sync for base card connectors.
-- Default mode is sel_mux1(0) <= '0'; and sel_mux1(1) <= '1'; i.e
-- CT_FRAME = CT_FRAME_A (F8o from WAN PLL)
-- MUX1 enable signals can be changed by writing into latch at address
-- CONN_AD[22:30] = 1XXXX1010 using CONN_D[14:15]
process (signal_cpld_dec(10),CONN_D15,CONN_D14,signal_w_bar,TDM_RESET)

begin

if TDM_RESET ='0' then
                sel_mux1(0) <= '0';
                sel_mux1(1) <= '1';

elsif signal_cpld_dec(10) = '0'and signal_w_bar = '0' then
                sel_mux1(0) <= CONN_D15;
                sel_mux1(1) <= CONN_D14;
end if ;
end process;

-- 4 to 1 multiplexer design with case construct to select frame sync to base card connectors

process (sel_mux1, CT_FRAME, CT_STFRAMEn, CT_WFRAMEn)
begin
   case sel_mux1 is
      when "00" => CT_FRAME_A <= CT_WFRAMEn;
      when "01" => CT_FRAME_A <= CT_STFRAMEn;
      when "10" => CT_FRAME_A <= CT_FRAME;
      when others => NULL;
   end case;
end process;


-- Following process  is to implement the two bit internal latch for select signals
-- of MUX2 used to to select frame sync for the QuadFALC (optional).
-- Default mode is sel_mux2(0) <= '0'; and sel_mux2(1) <= '1'; i.e
-- PLD_QFALC_FRAME = CT_FRAME_A (F8o from WAN PLL)
-- MUX2 enable signals can be changed by writing into latch at address
-- CONN_AD[22:30] = 1XXXX1011 using CONN_D[14:15]
process (signal_cpld_dec(11),CONN_D15,CONN_D14,signal_w_bar,TDM_RESET)
```

```
begin

if TDM_RESET ='0' then
                sel_mux2(0) <= '0';
                sel_mux2(1) <= '1';

elsif signal_cpld_dec(11) = '0'and signal_w_bar = '0' then
                sel_mux2(0) <= CONN_D15;
                sel_mux2(1) <= CONN_D14;
end if ;

end process;

-- 4 to 1 multiplexer design with case construct to select frame sync to QuadFALC (optional)

process (sel_mux2, CT_FRAME, CT_STFRAMEn, CT_WFRAMEn)
begin
   case sel_mux2 is
      when "00" => PLD_QFALC_FRAME <= CT_WFRAMEn;
      when "01" => PLD_QFALC_FRAME <= CT_STFRAMEn;
      when "10" => PLD_QFALC_FRAME <= CT_FRAME;
      when others => NULL;
   end case;
end process;


-- internal read write signal generation from TDM_GPL1 and TDM_GPL2

process(TDM_GPL2,TDM_GPL1)

begin

        if TDM_GPL2 = '0' and TDM_GPL1 = '0' then

           --signal_r_w_bar <= '0';
           signal_w_bar   <= '0';
           signal_r   <= '0';

        elsif TDM_GPL2 = '0' and TDM_GPL1 = '1' then


          -- signal_r_w_bar <= '1';
           signal_w_bar   <= '1';
           signal_r   <= '1';

           else
                   signal_w_bar   <= '1';
            signal_r   <= '0';

        end if;

end process;


end pdk_cpld;--end of code
```

Appendix B Schematics

The following pages present the schematics for the PSTN card, as well as the board that provides power to the PSTN card.



The purpose of this board is to provide power to the PSTN card of the Smart Packet Telephony Development Kit.

Packet telelphony Motorola Copyright 2001	Title PDK_POTS_PWR	Block Schematic	
	Name Rich Cutler		Rev 0.1
	Date: Tuesday, February 10, 2004	Sheet	of 1

Packet Telephony Development Kit POTS card Rev 2.0

Revision	Change from previous version	DATE
1.0	Initial Revision.	18/11/2002
2.0	Swapping of the SPIMOSI and SPIMOSO signals. Three level reset configuration. -->QuadFALC, CPLD -->WAN PLL -->TSI, DuSLIC Provided narrower frame pulse (F16o/ from WAN PLL) for the TSI to operate in ST-BUS mode. Brought F8o, F0o/, F16o/ (from WAN PLL) to CPLD. Frame Sync for BASE BOARD Connectors is provided from CPLD	06/06/2003

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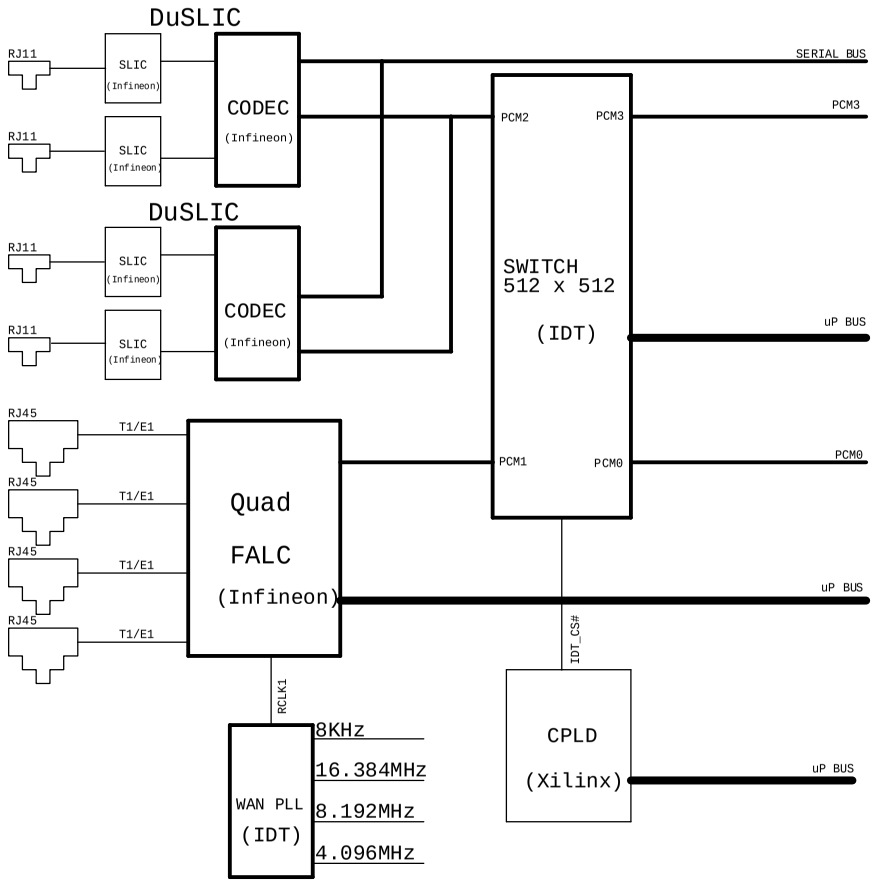
Title: REVISION HISTORY

Size: B | Document Number: <Doc> | Rev: 2.0

Date: Thursday, June 12, 2003 | Sheet 1 of 15

POTS BLOCK SCHEMATIC



TO BASEBOARD CONNECTORS

AURAL NETWORKS		
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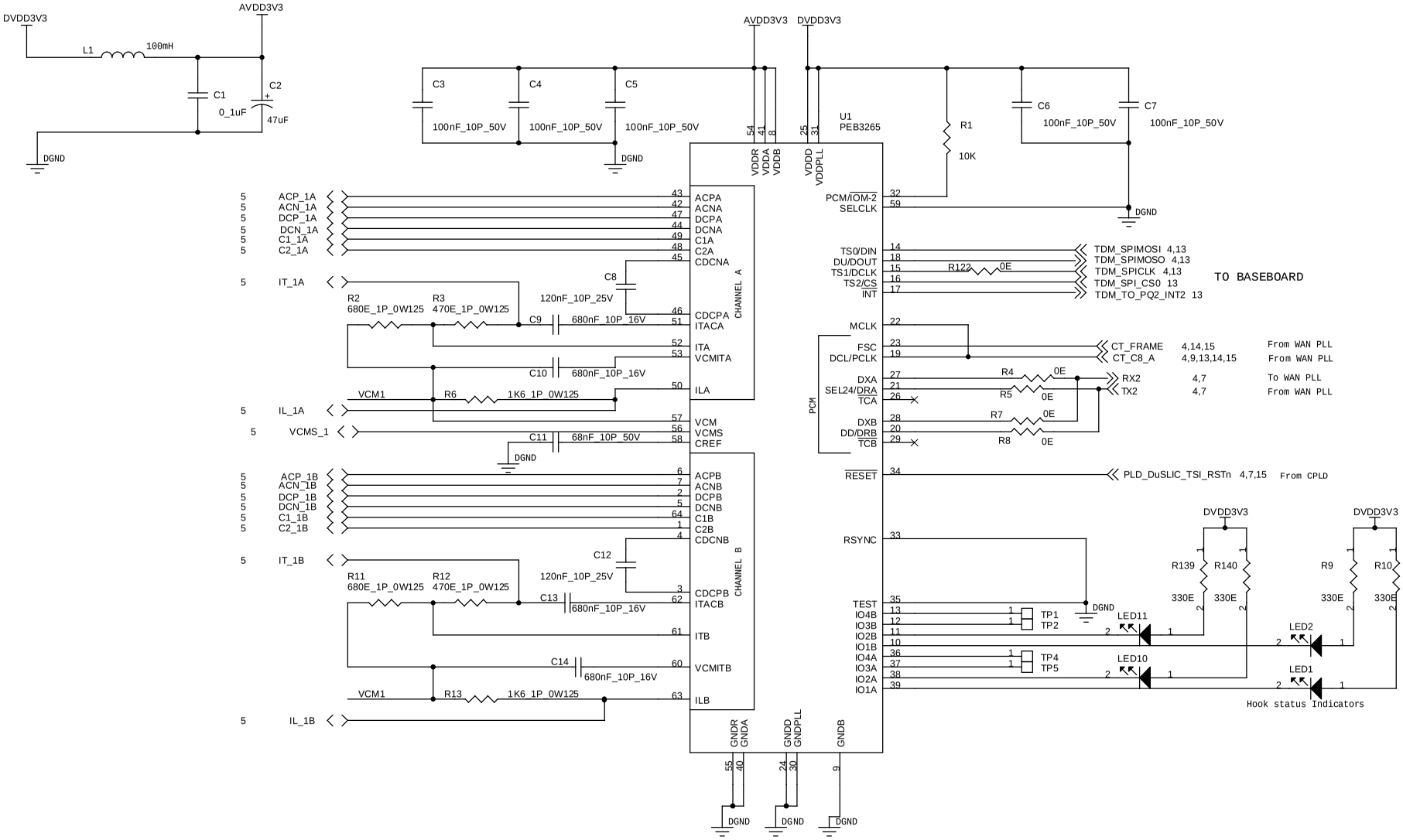
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 2 of 15	



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Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
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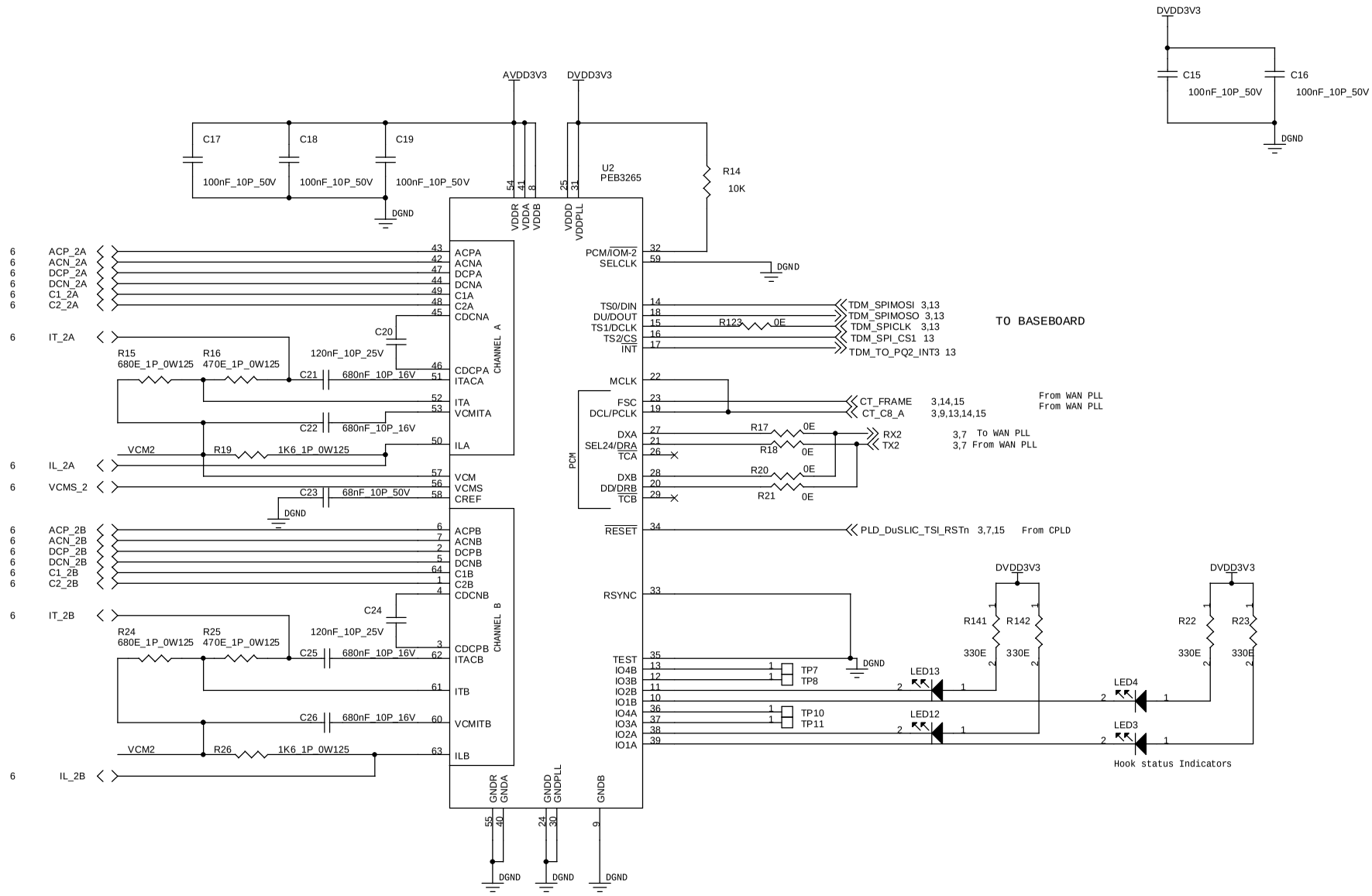

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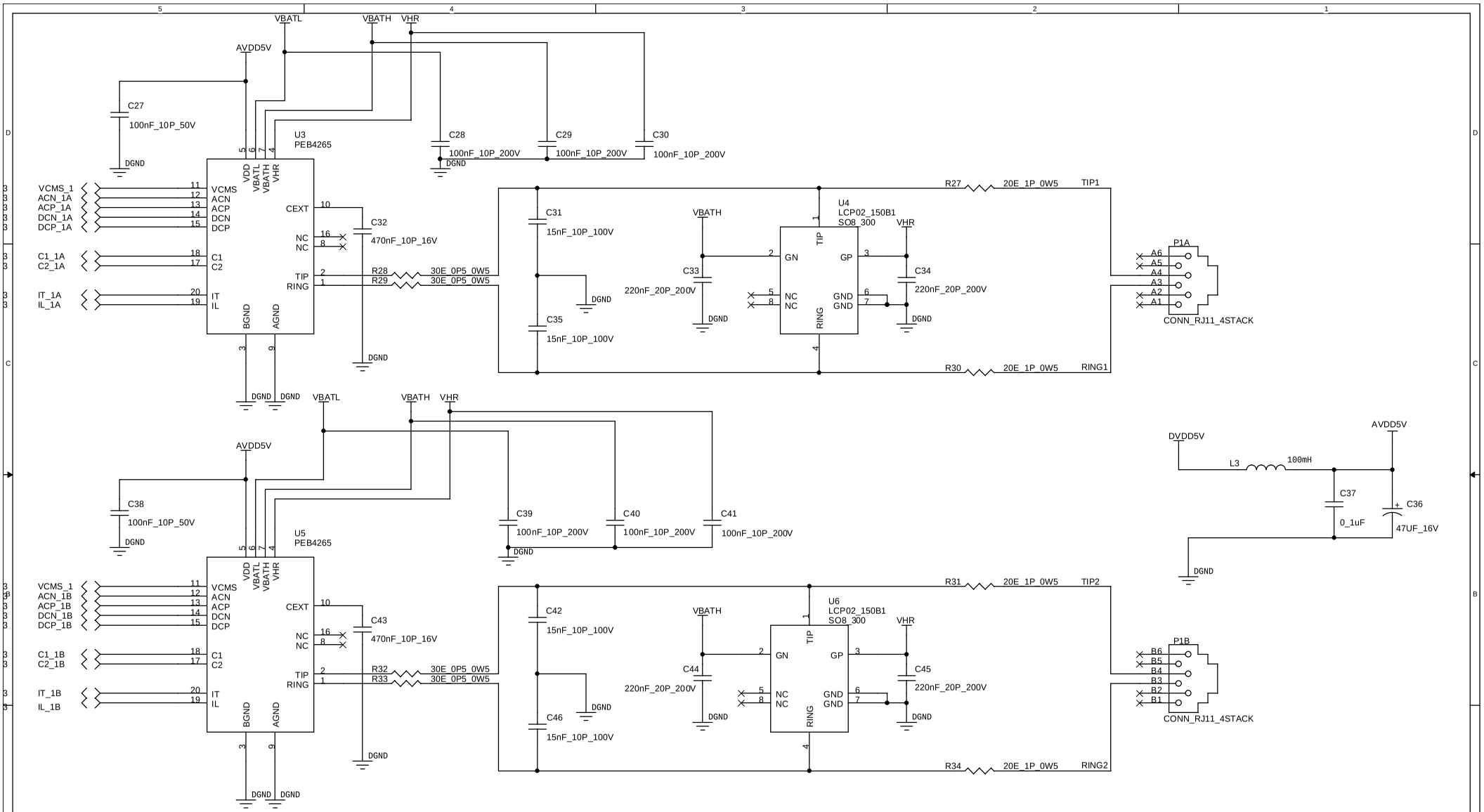
Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 4 of 15	



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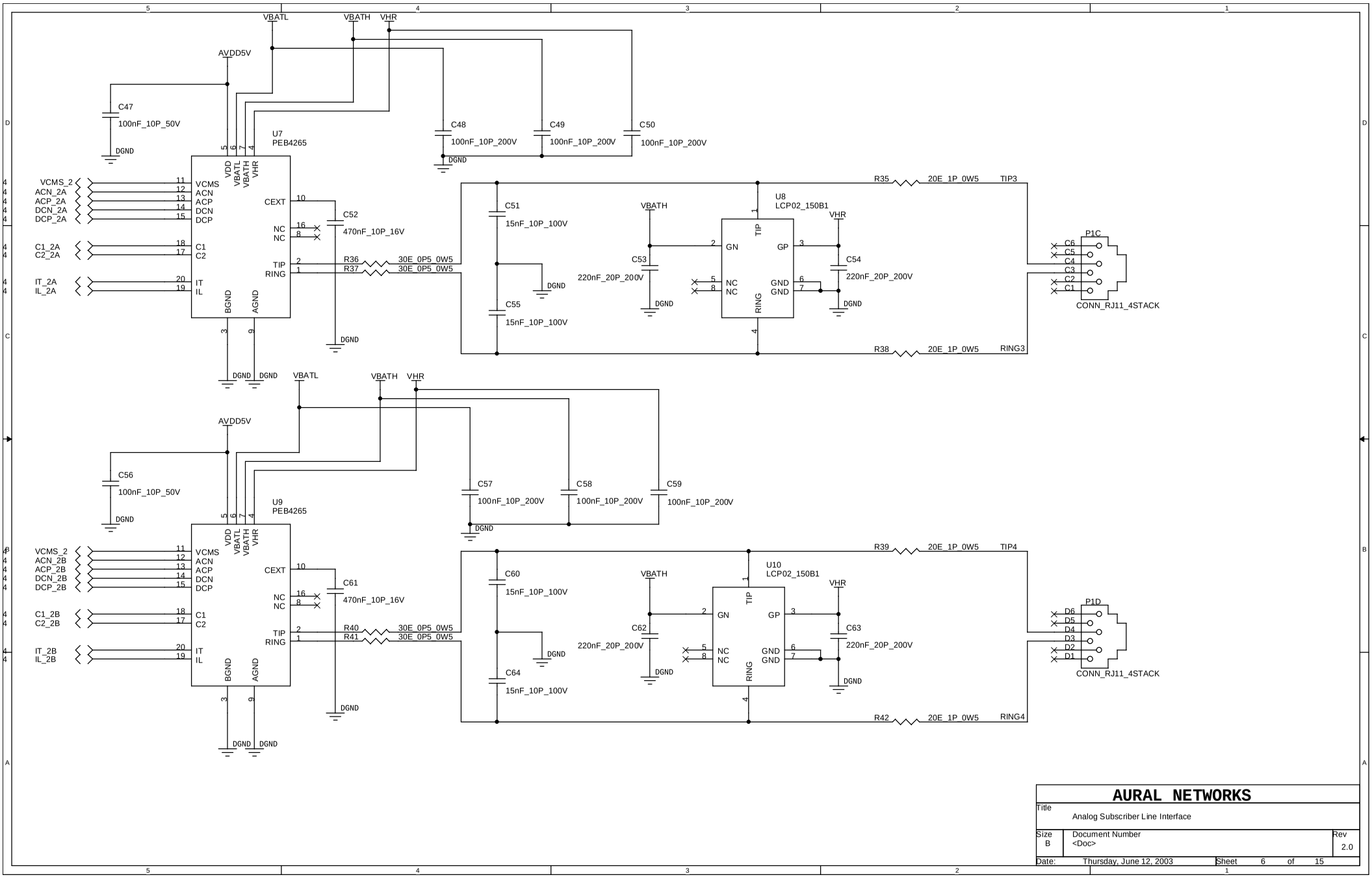
Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 5 of 15	



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Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
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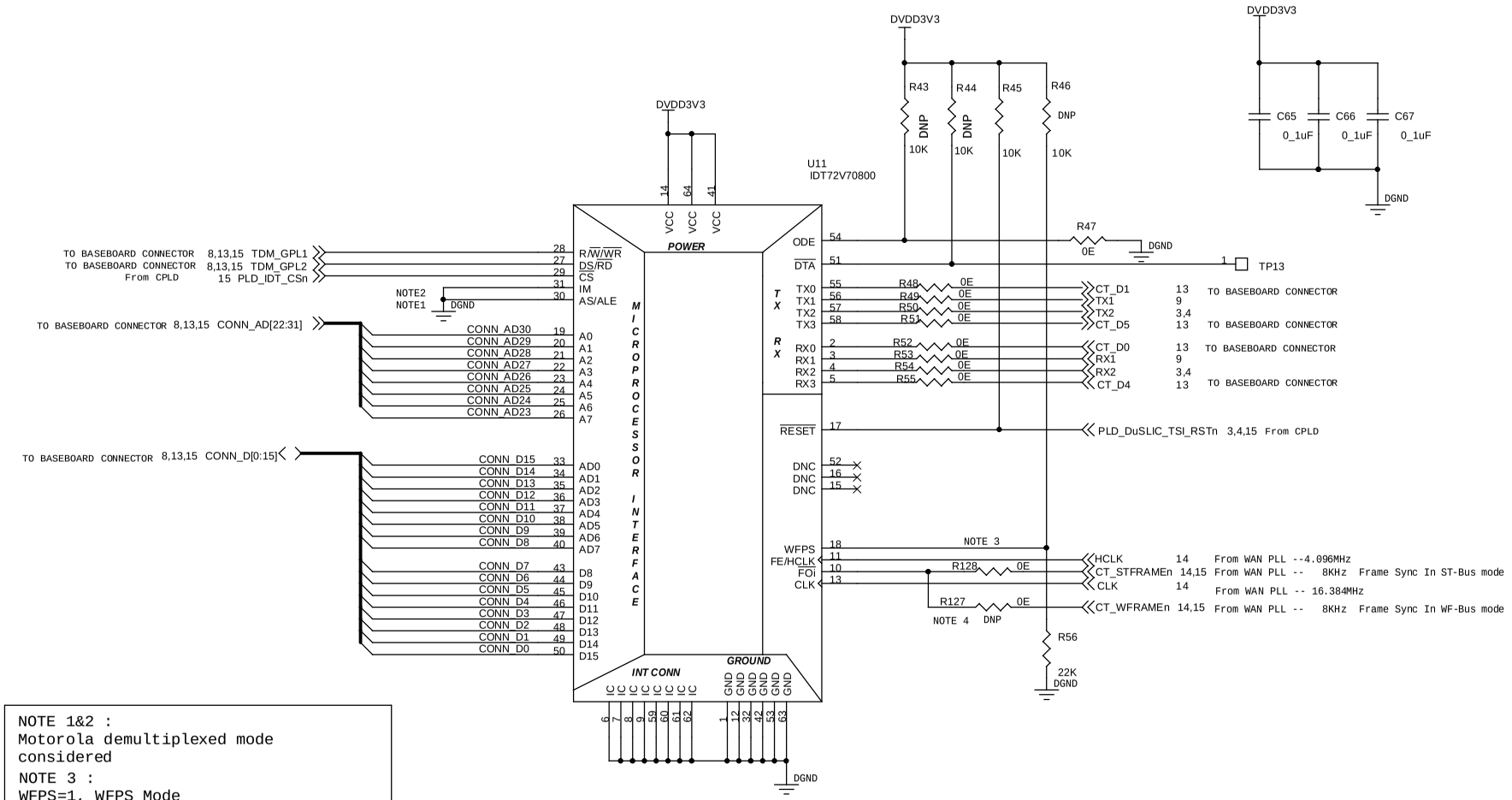


NOTE 1&2 :
Motorola demultiplexed mode considered

NOTE 3 :
WFPS=1, WFPS Mode
WFPS=0, ST_BUS Mode

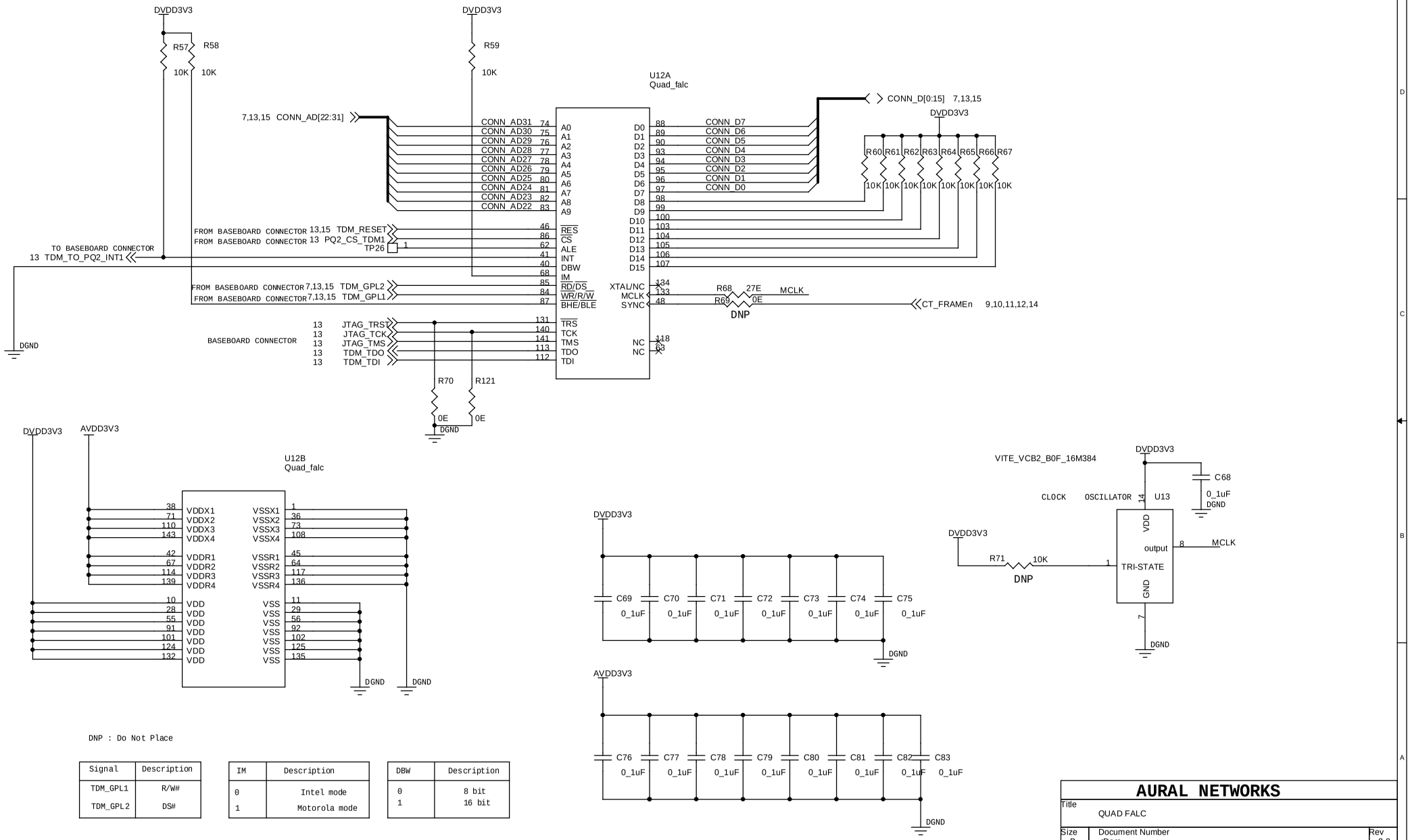
NOTE 4 :
WF Mode -- Place R127
ST_BUS Mode -- Place R128

DNP : Do Not Place

PCM	Description
0	DSP
1	FALC
2	DuSLIC
3	BASE CARD

AURAL NETWORKS

Title: Digital Switch		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 7 of 15	



DNP : Do Not Place

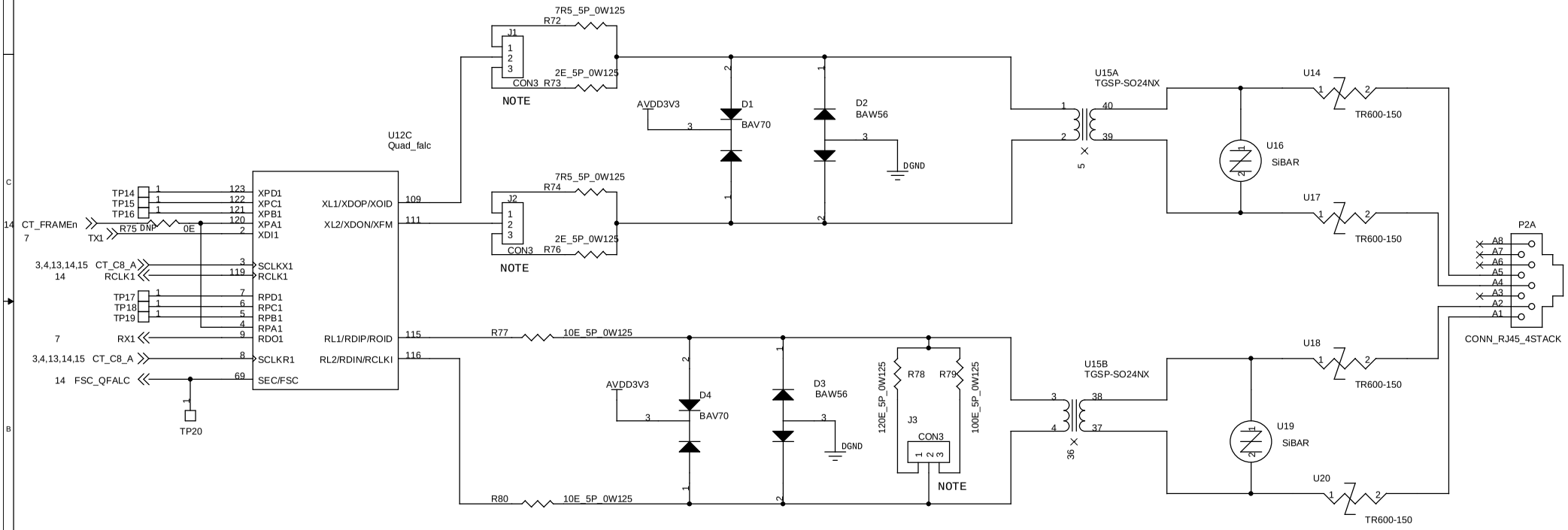
Signal	Description
TDM_GPL1	R/W#
TDM_GPL2	DS#

IM	Description
0	Intel mode
1	Motorola mode

DBW	Description
0	8 bit
1	16 bit

AURAL NETWORKS

Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 8 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

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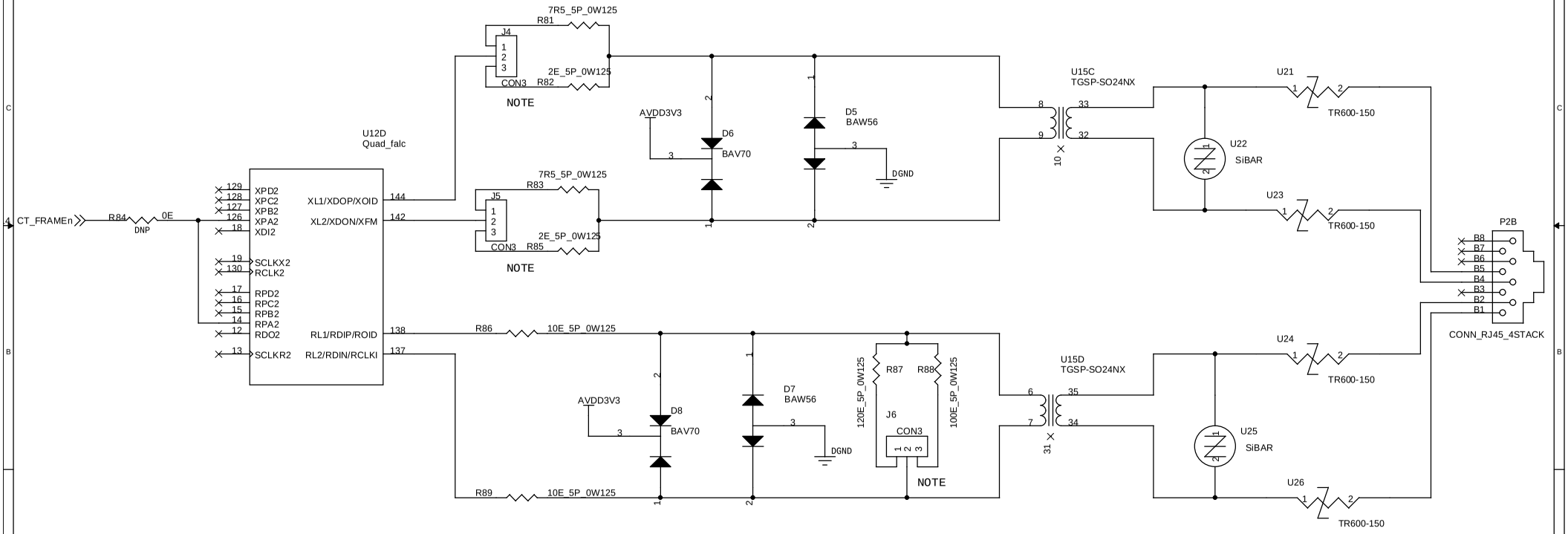
Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 9 of 15	

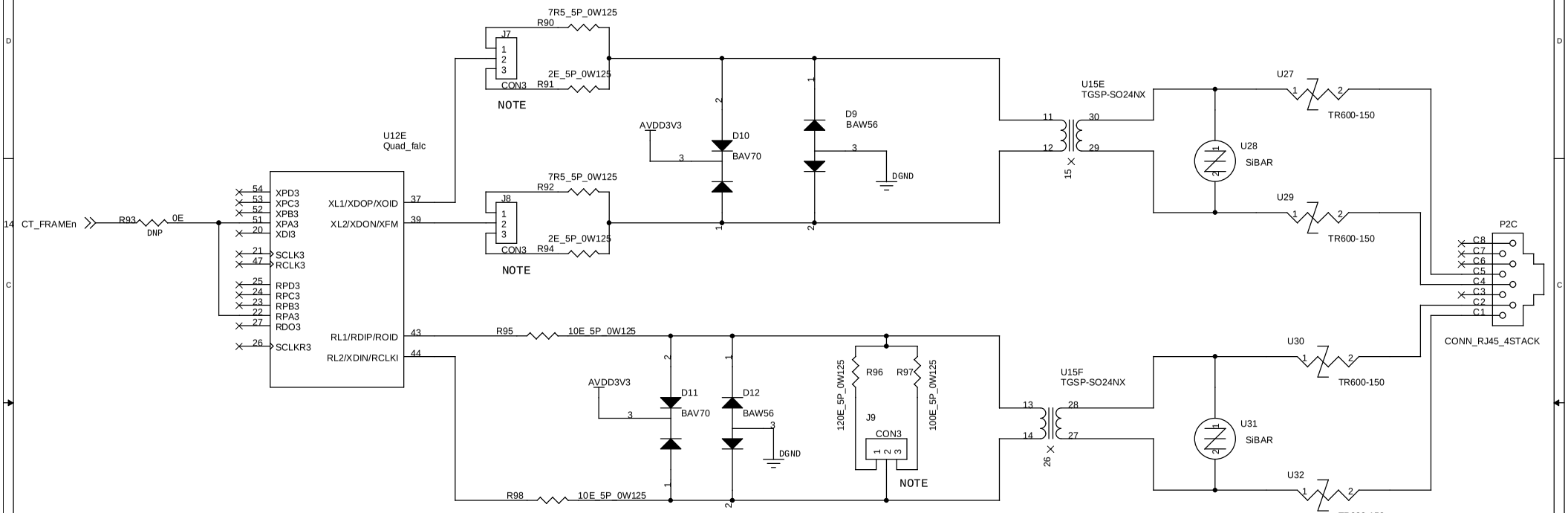


NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

AURAL NETWORKS

Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 10 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

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Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
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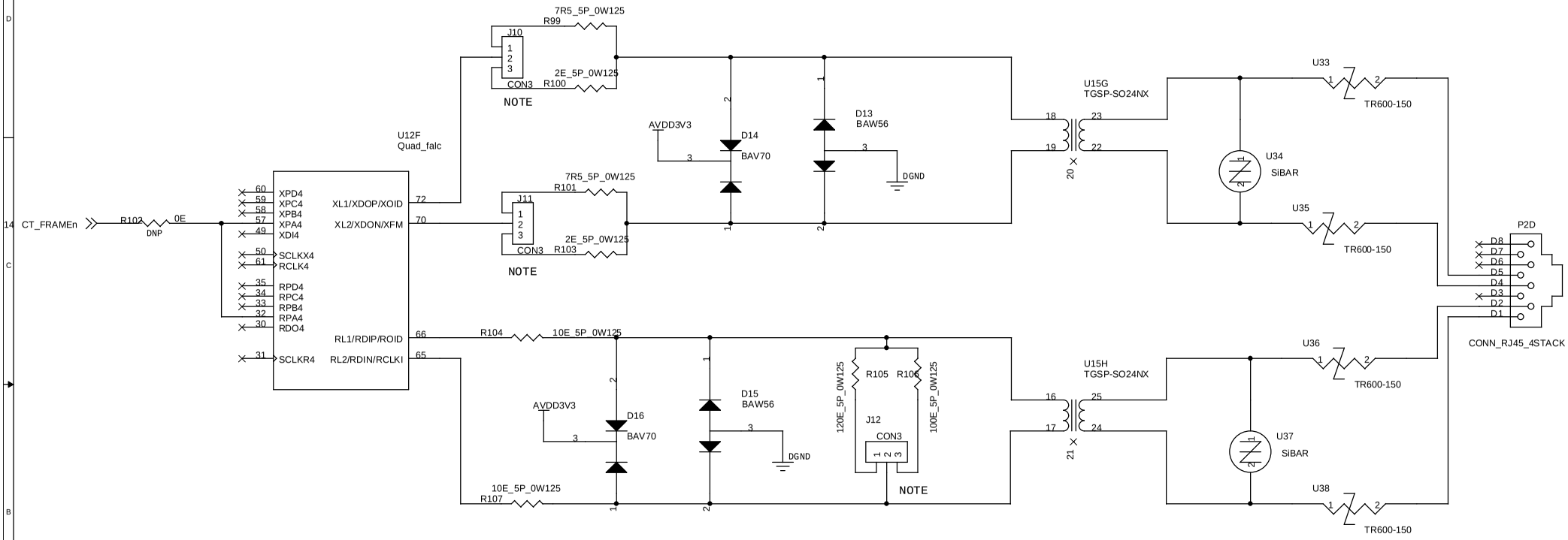

NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

AURAL NETWORKS		
Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
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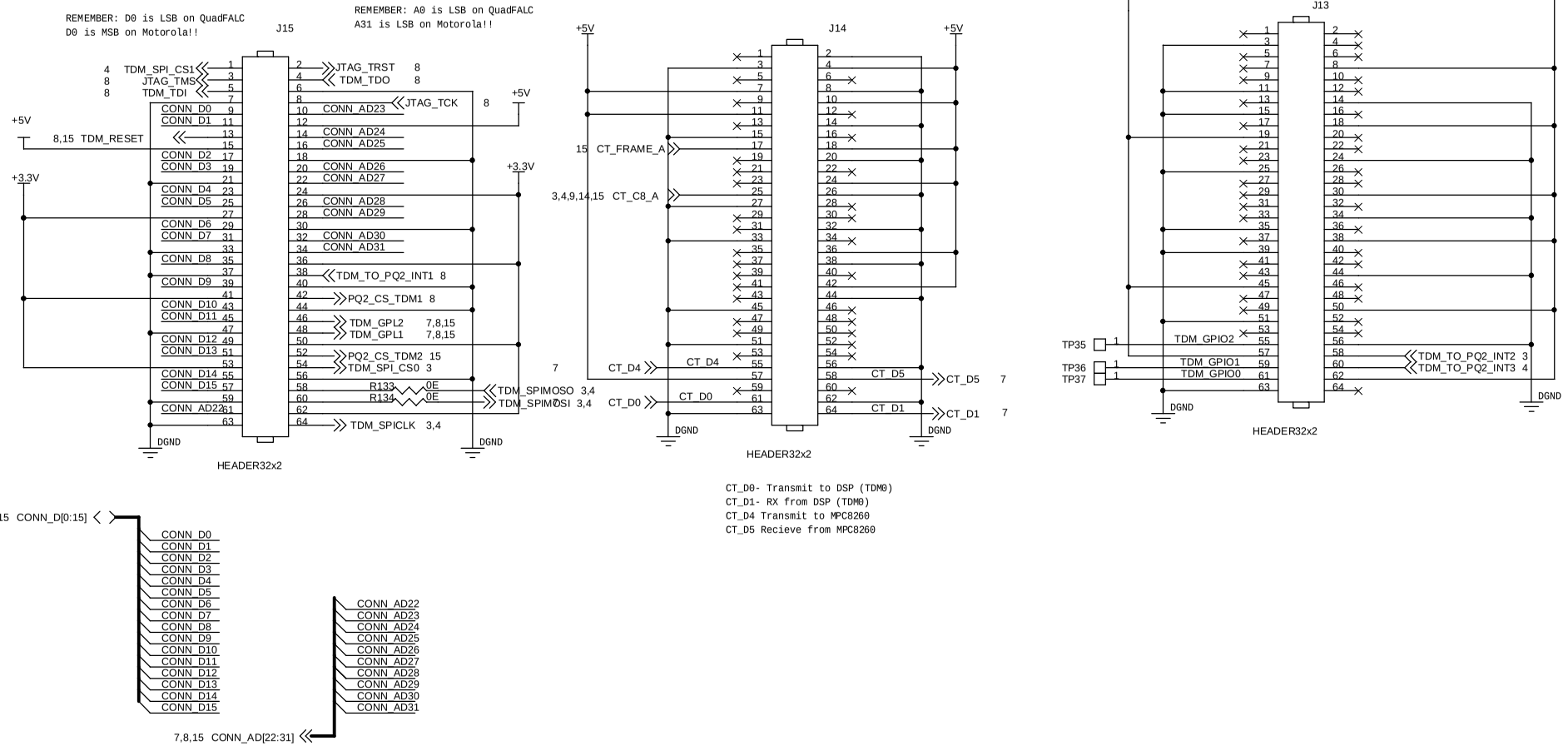
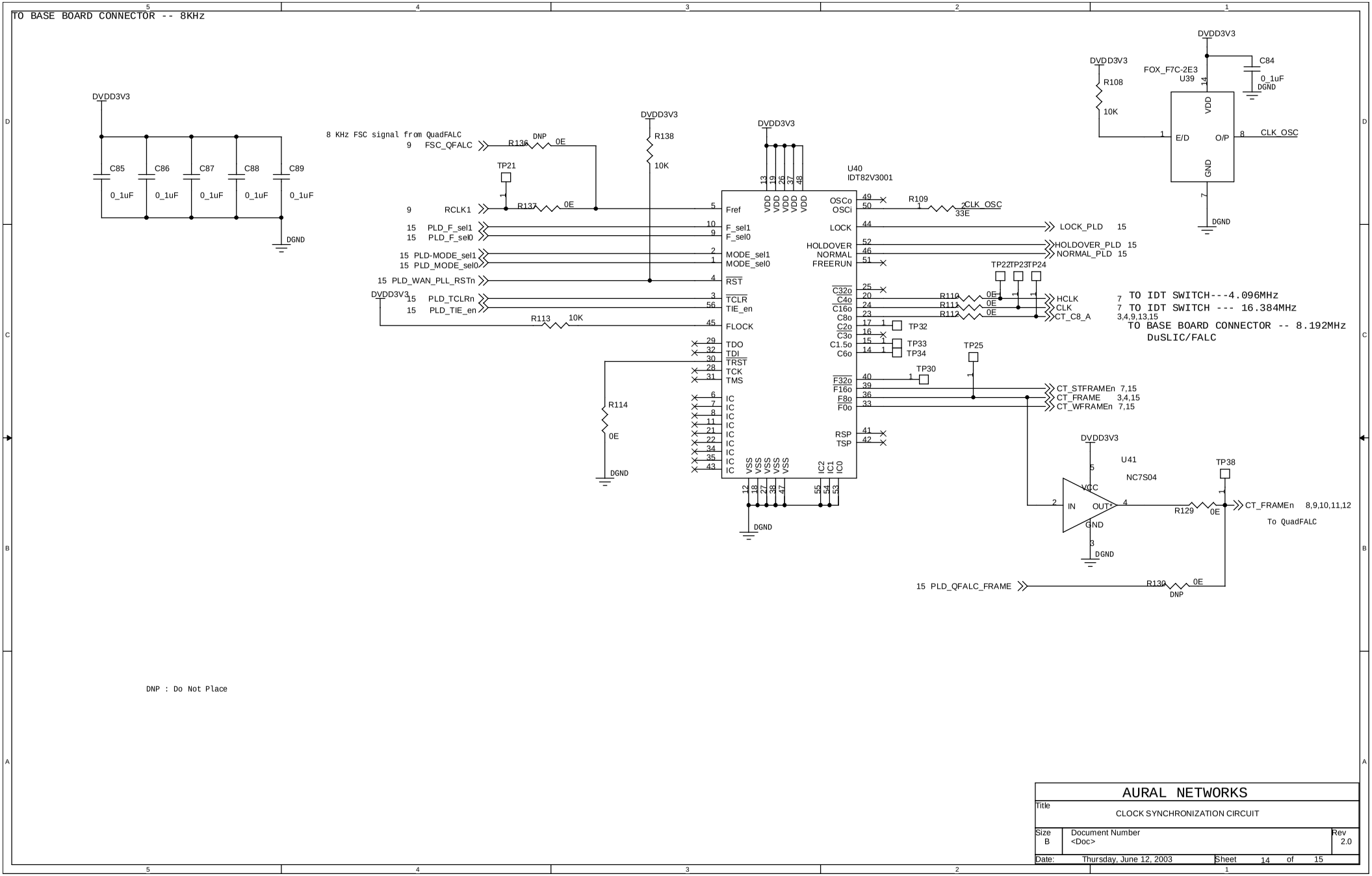
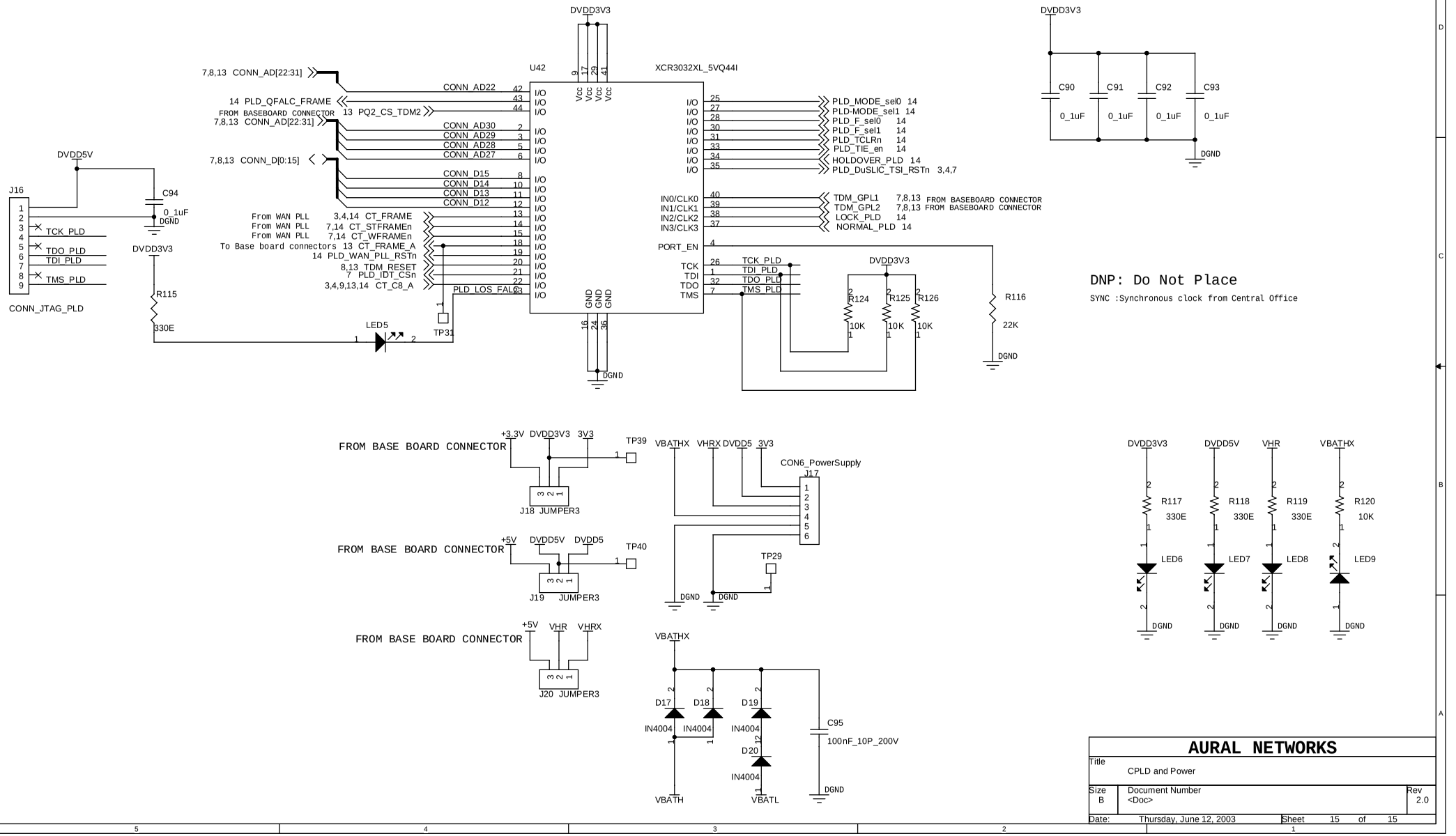


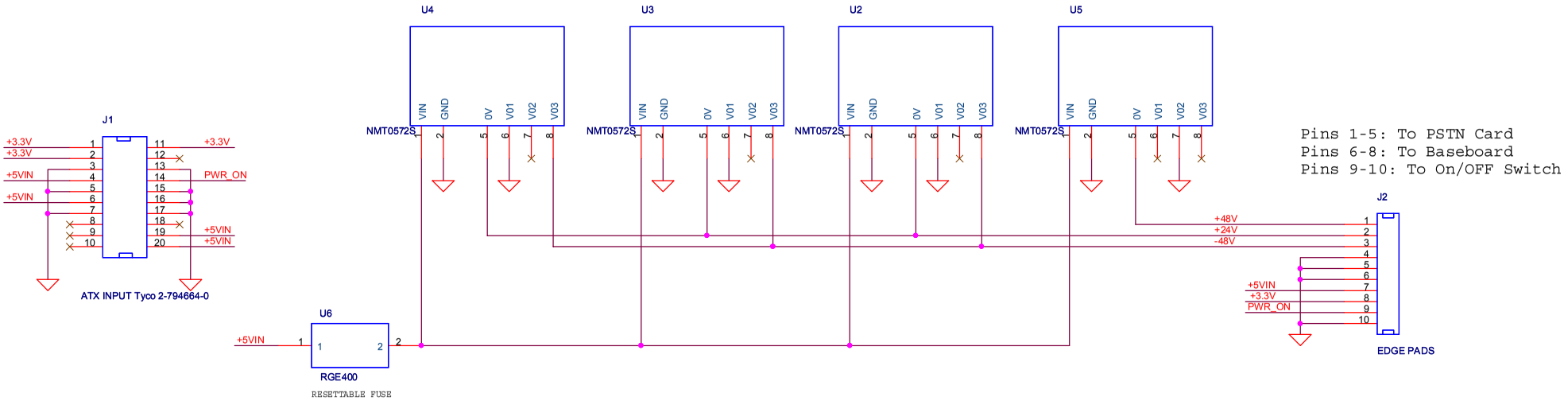
J13 will connect to J9 connector of base card
J14 will connect to J7 connector of base card
J15 will connect to J8 connector of base card

AURAL NETWORKS		
Title: Base Board Connectors		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 13 of 15	


TO BASE BOARD CONNECTOR -- 8KHz
DVDD3V3
C85
C86
C87
C88
C89
0_1uF
DGND
8 KHz FSC signal from QuadFALC
9 FSC_QFALC
R136 DNP 0E
R138 10K
TP21
9 RCLK1
R137 0E
15 PLD_F_sel1
15 PLD_F_sel0
15 PLD-MODE_sel1
15 PLD_MODE_sel0
15 PLD_WAN_PLL_RSTn
15 PLD_TCLRn
15 PLD_TIE_en
R113 10K
U40
IDT82V3001
Fref
F_sel1
F_sel0
MODE_sel1
MODE_sel0
RST
TCLR
TIE_en
FLOCK
TDO
TDI
TRST
TCK
TMS
IC
VDD
VSS
OSCo
OSCi
LOCK
HOLDOVER
NORMAL
FREERUN
C32o
C40
C16o
C8o
C2o
C3o
C1.5o
C6o
F32o
F16o
F8o
F0o
RSP
TSP
R109 2CLK_OSC 33E
LOCK_PLD 15
HOLDOVER_PLD 15
NORMAL_PLD 15
TP22 TP23 TP24
R110 0E
R111 0E
R112 0E
HCLK
CLK
CT_C8_A
3,4,9,13,15
TP32
TP33
TP34
TP25
TP30
CT_STFRAMEn 7,15
CT_FRAME 3,4,15
CT_WFRAMEn 7,15
R114 0E
DVDD3V3
R108 10K
FOX_F7C-2E3
U39
C84 0_1uF
VDD
E/D
O/P
GND
CLK_OSC
7 TO IDT SWITCH---4.096MHz
7 TO IDT SWITCH --- 16.384MHz
TO BASE BOARD CONNECTOR -- 8.192MHz
DuSLIC/FALC
U41
NC7S04
VCC
IN
OUT*
GND
TP38
R129 0E
CT_FRAMEn 8,9,10,11,12
To QuadFALC
15 PLD_QFALC_FRAME
R130 0E DNP
DNP : Do Not Place
AURAL NETWORKS
Title
CLOCK SYNCHRONIZATION CIRCUIT
Size B
Document Number <Doc>
Rev 2.0
Date: Thursday, June 12, 2003
Sheet 14 of 15



AURAL NETWORKS		
Title: CPLD and Power		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 15 of 15	



The purpose of this board is to provide power to the PSTN card of the Smart Packet Telephony Development Kit.

Packet telelphony Motorola Copyright 2001	Title PDK_POTS_PWR	Block Schematic	
	Name Rich Cutler		Rev 0.1
	Date: Tuesday, February 10, 2004	Sheet	of 1

Packet Telephony Development Kit POTS card Rev 2.0

Revision	Change from previous version	DATE
1.0	Initial Revision.	18/11/2002
2.0	Swapping of the SPIMOSI and SPIMOSO signals. Three level reset configuration. -->QuadFALC, CPLD -->WAN PLL -->TSI, DuSLIC Provided narrower frame pulse (F16o/ from WAN PLL) for the TSI to operate in ST-BUS mode. Brought F8o, F0o/, F16o/ (from WAN PLL) to CPLD. Frame Sync for BASE BOARD Connectors is provided from CPLD	06/06/2003

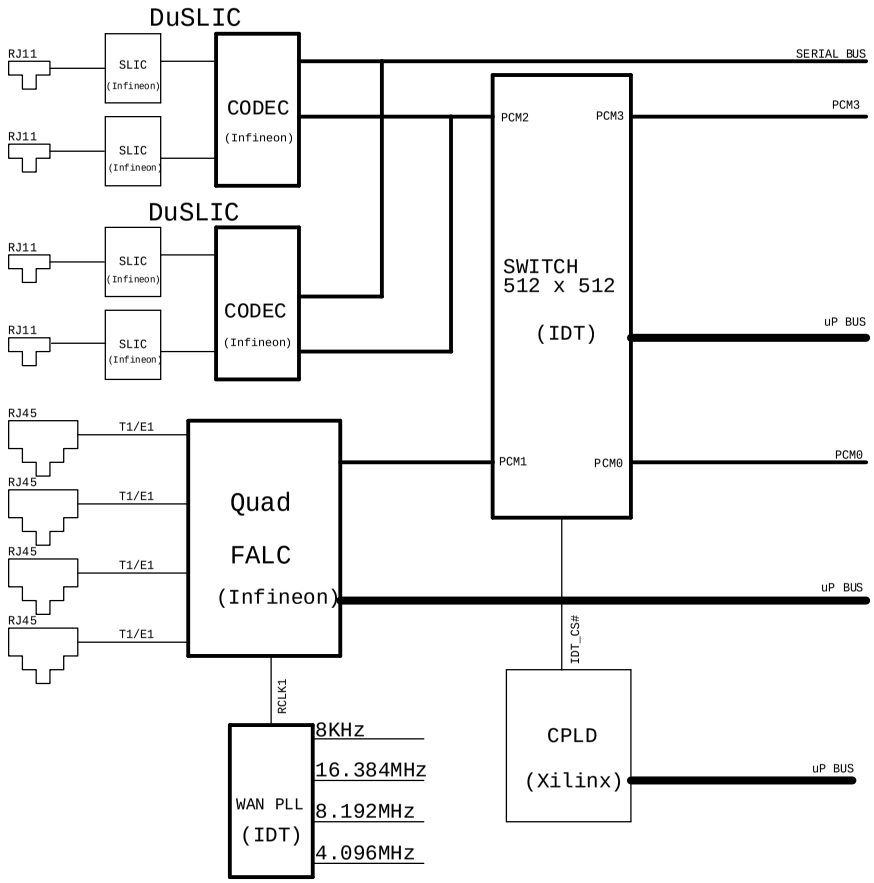
AURAL NETWORKS

Title: REVISION HISTORY

Size: B | Document Number: <Doc> | Rev: 2.0

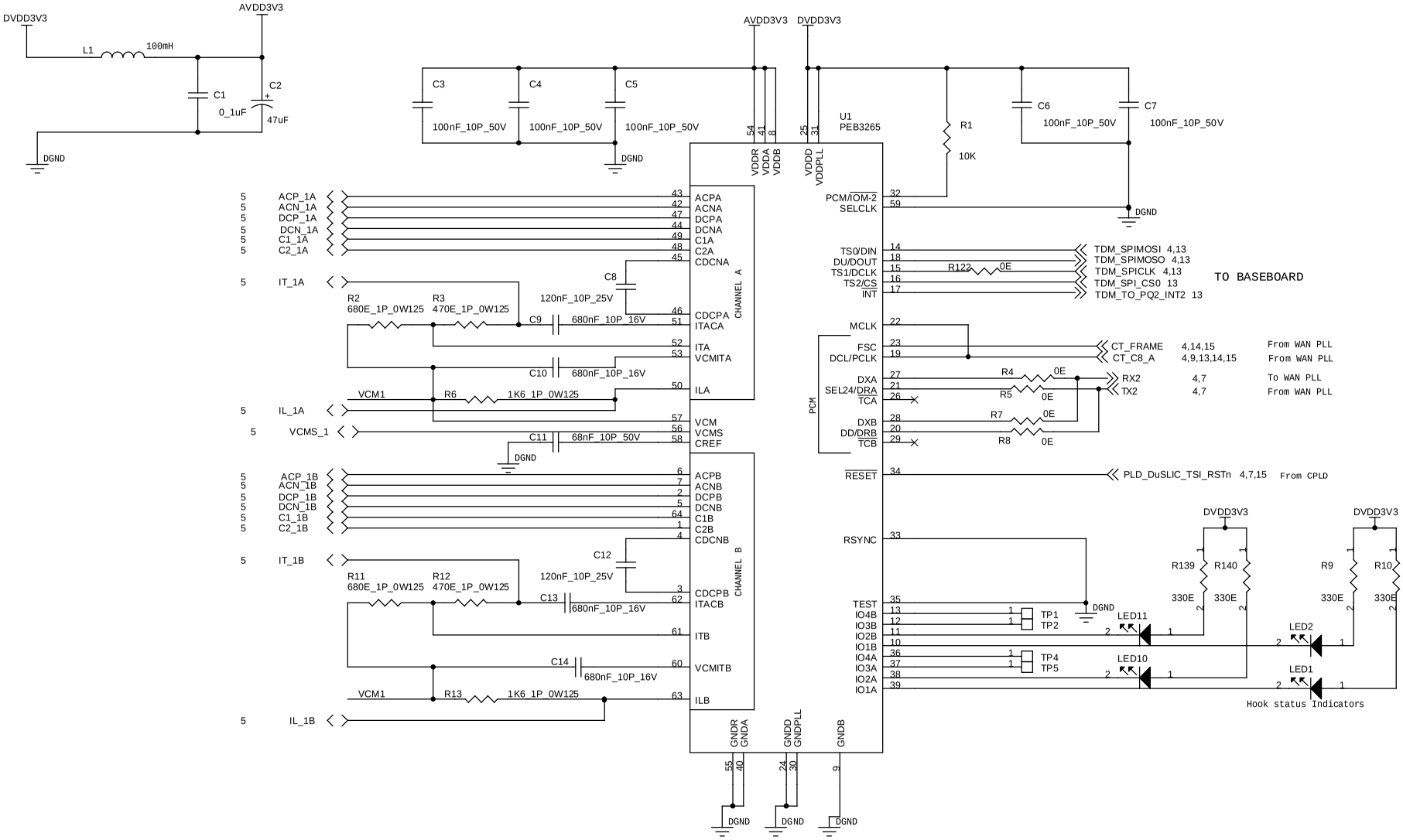
Date: Thursday, June 12, 2003 | Sheet 1 of 15

POTS BLOCK SCHEMATIC

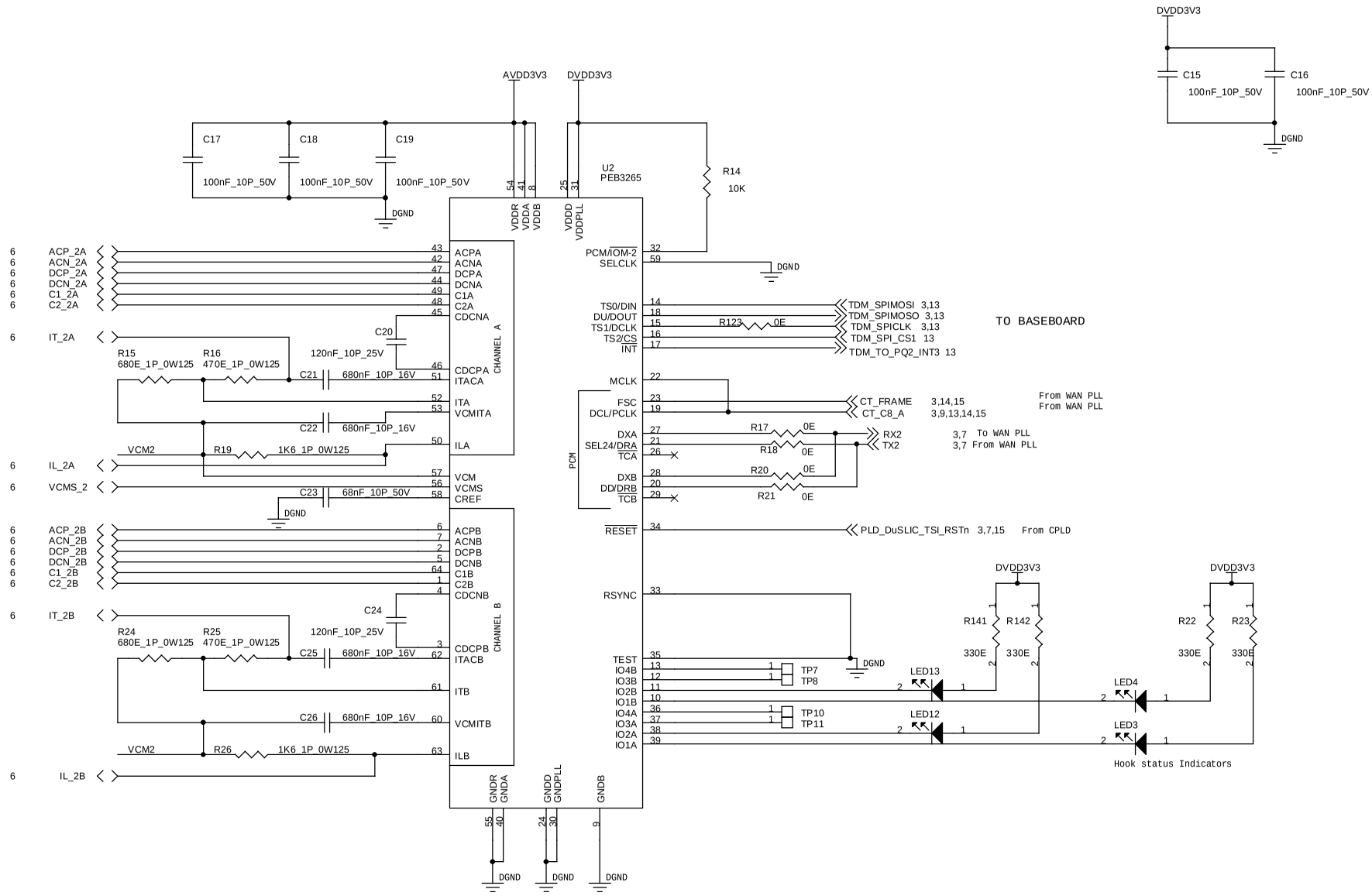


TO BASEBOARD CONNECTORS

AURAL NETWORKS		
Title: Pots Card Block Schematic		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 2 of 15	

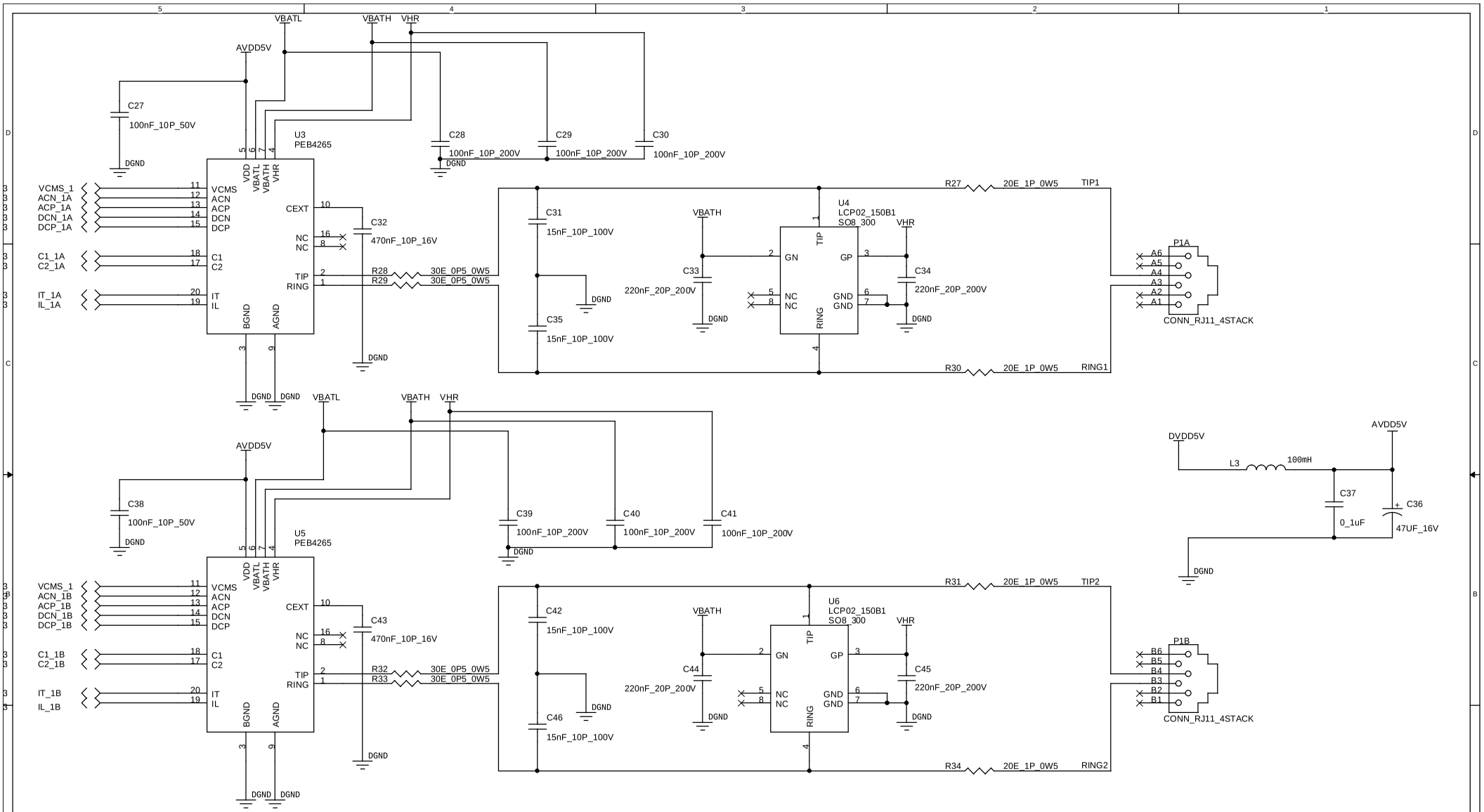


AURAL NETWORKS		
Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 3 of 15	



AURAL NETWORKS

Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 4 of 15	



AURAL NETWORKS		
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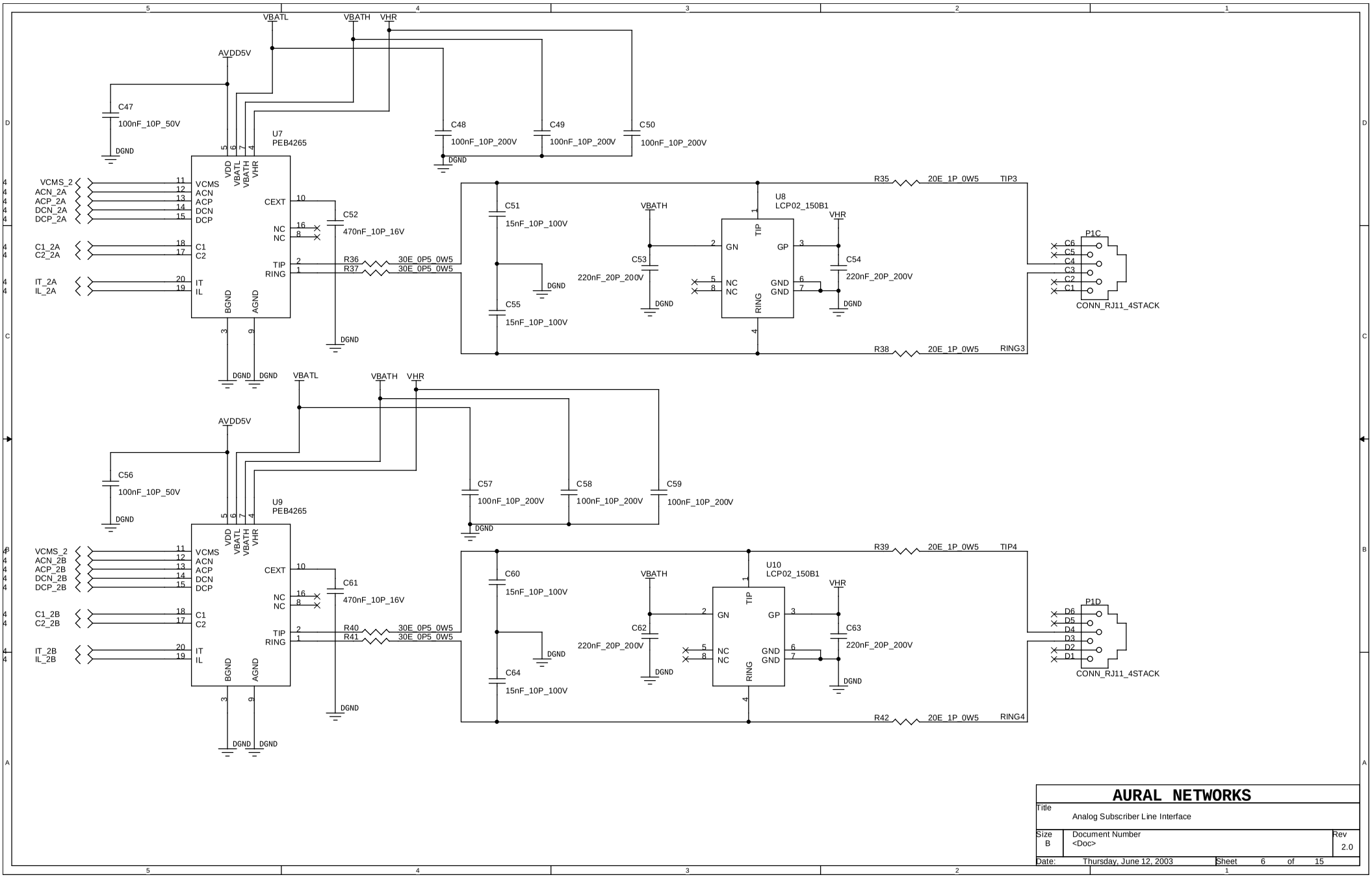
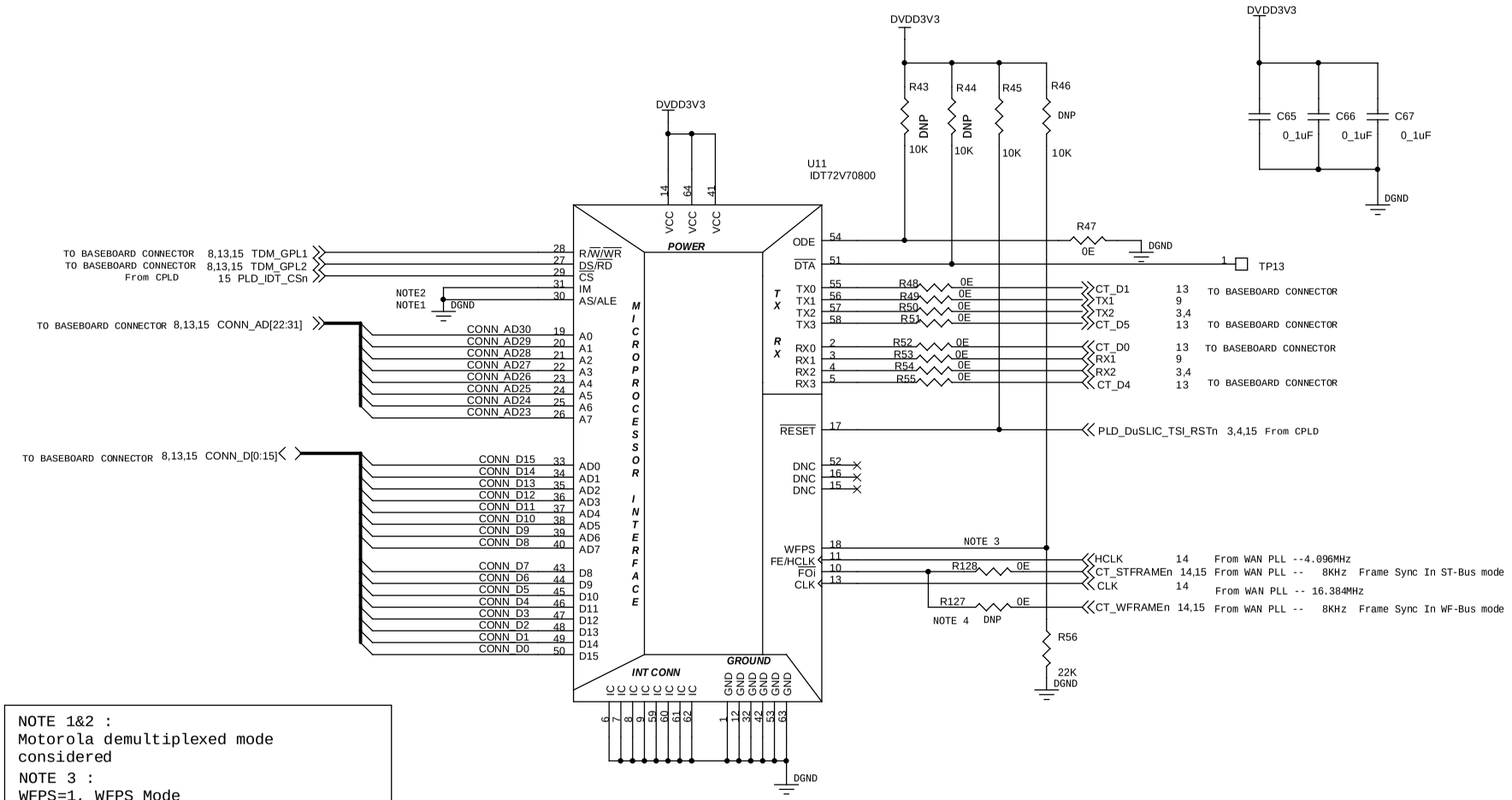
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 5 of 15	



AURAL NETWORKS

Title: Analog Subscriber Line Interface		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 6 of 15	



NOTE 1&2 :
Motorola demultiplexed mode considered

NOTE 3 :
WFPS=1, WFPS Mode
WFPS=0, ST_BUS Mode

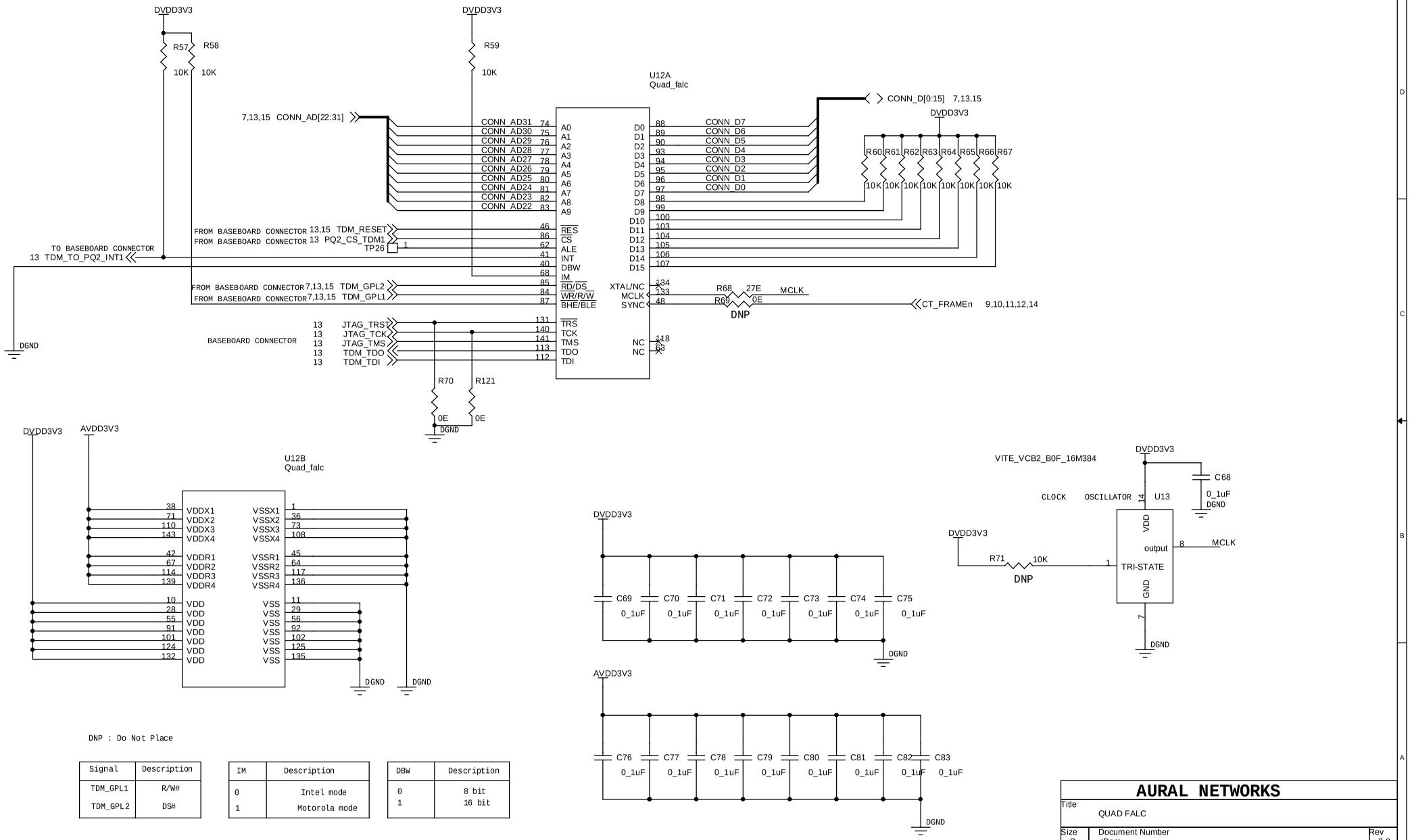
NOTE 4 :
WF Mode -- Place R127
ST_BUS Mode -- Place R128

DNP : Do Not Place

PCM	Description
0	DSP
1	FALC
2	DuSLIC
3	BASE CARD

AURAL NETWORKS

Title: Digital Switch		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 7 of 15	



DNP : Do Not Place

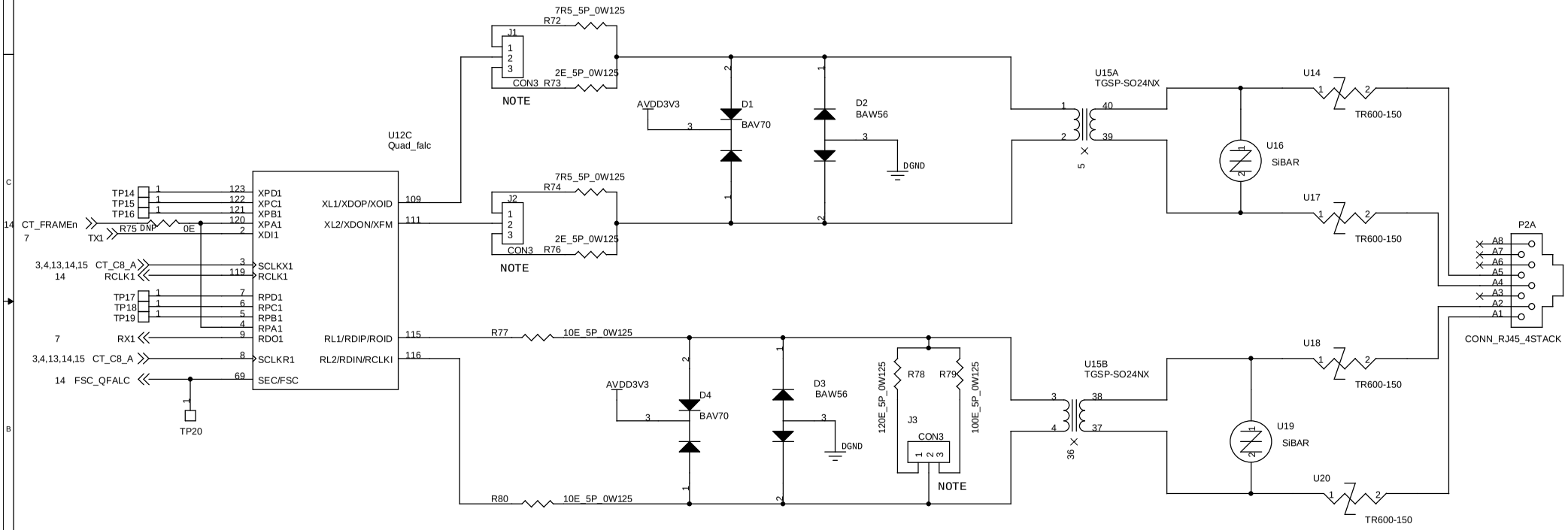
Signal	Description
TDM_GPL1	R/W#
TDM_GPL2	DS#

IM	Description
0	Intel mode
1	Motorola mode

DBW	Description
0	8 bit
1	16 bit

AURAL NETWORKS

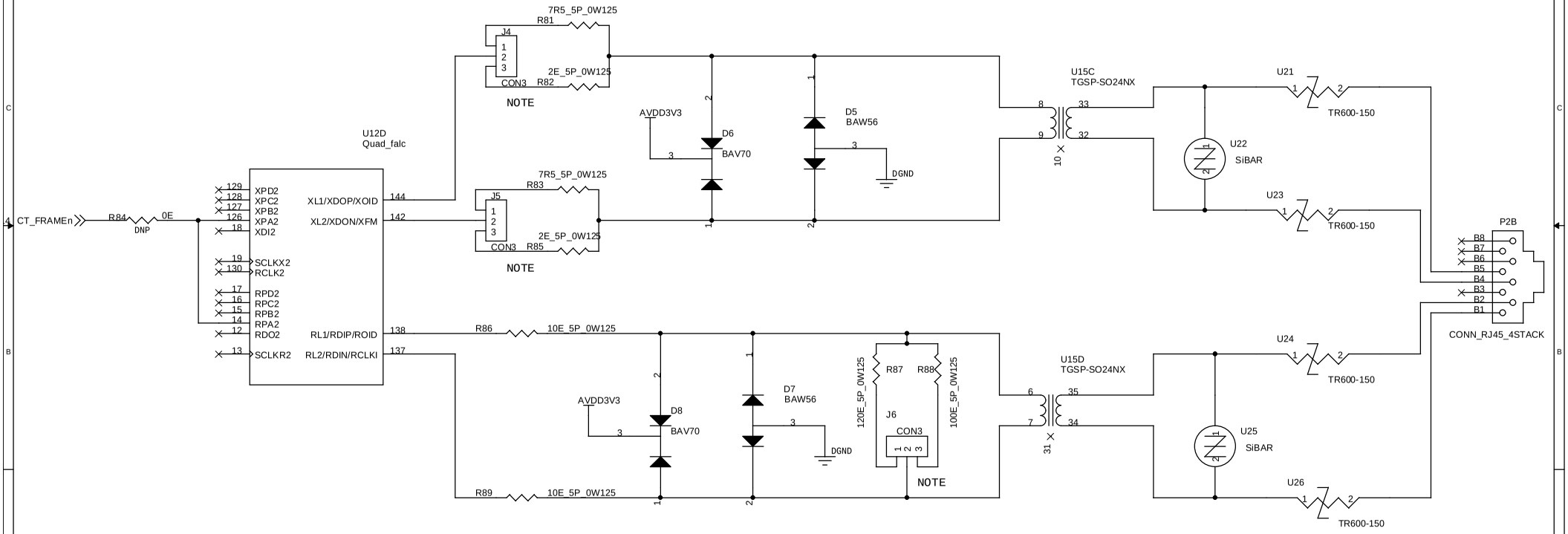
Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 8 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

AURAL NETWORKS		
Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 9 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

AURAL NETWORKS

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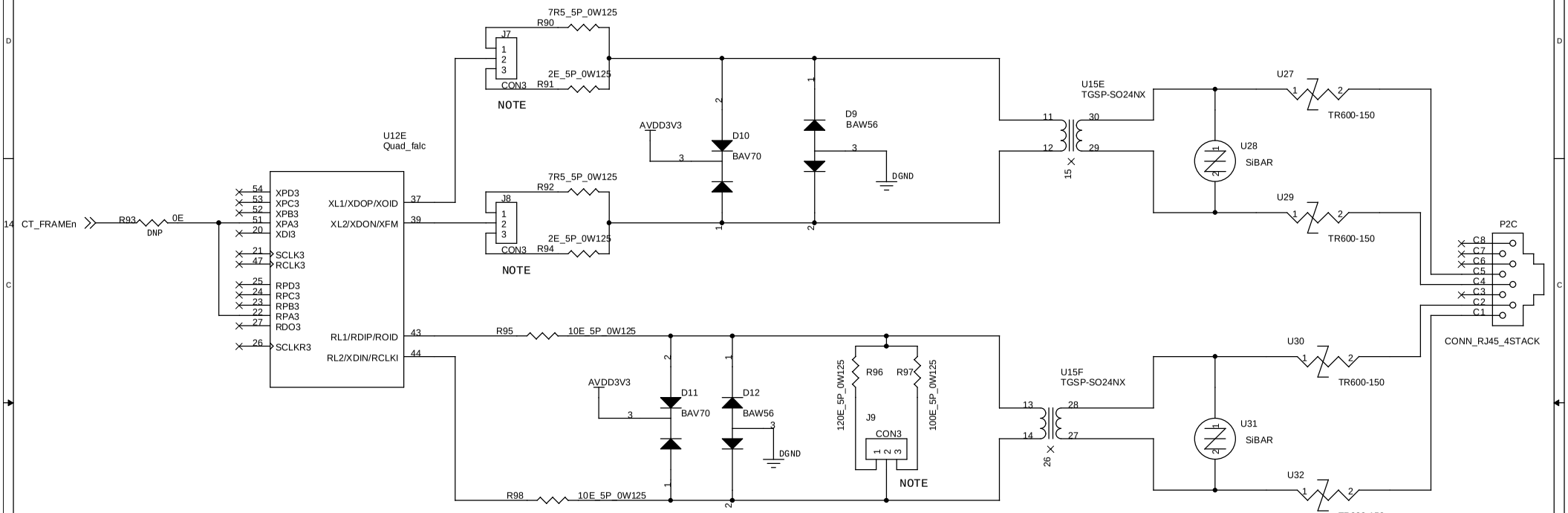
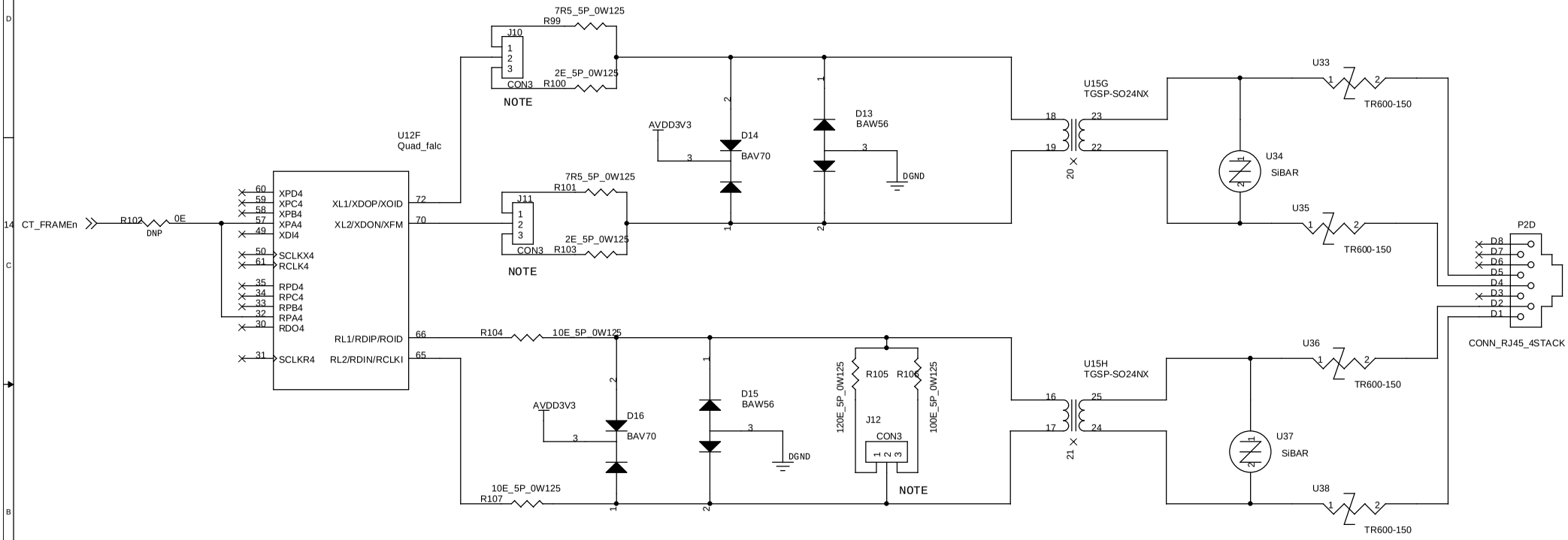
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 10 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

AURAL NETWORKS		
Title: QUAD FALC		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 11 of 15	



NOTE: Connect 1 & 2 for E1
Connect 2 & 3 for T1

DNP: Do Not Place

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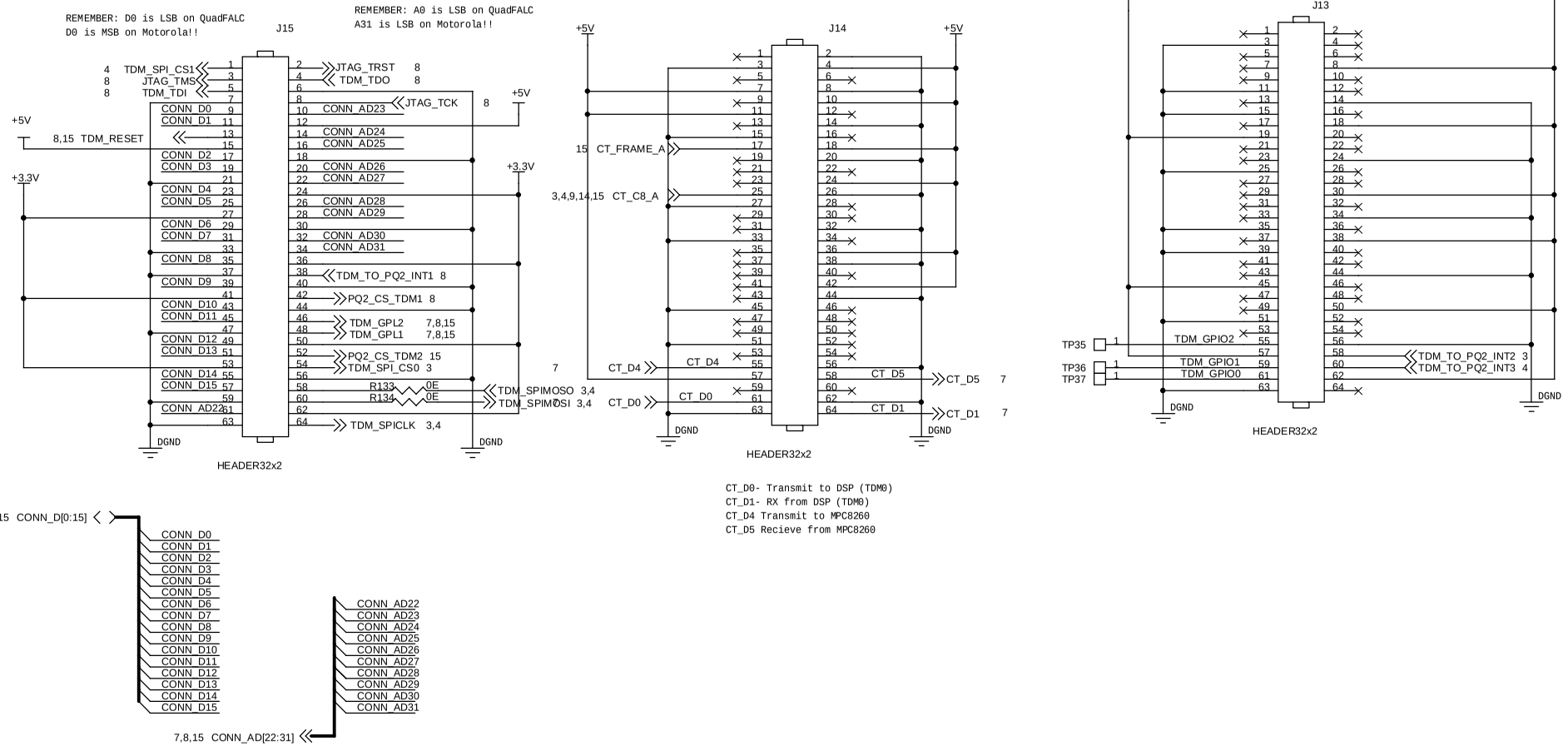
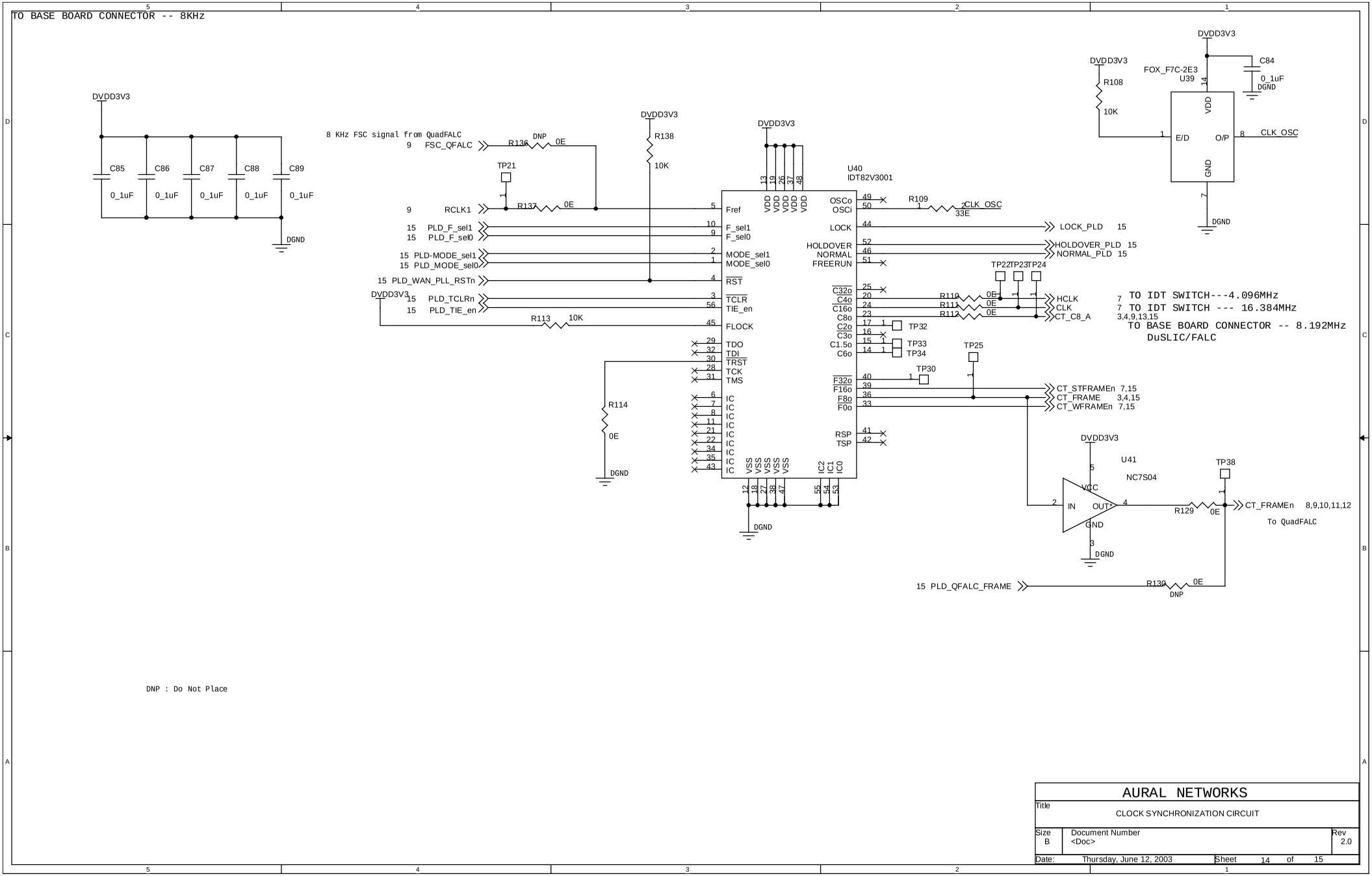
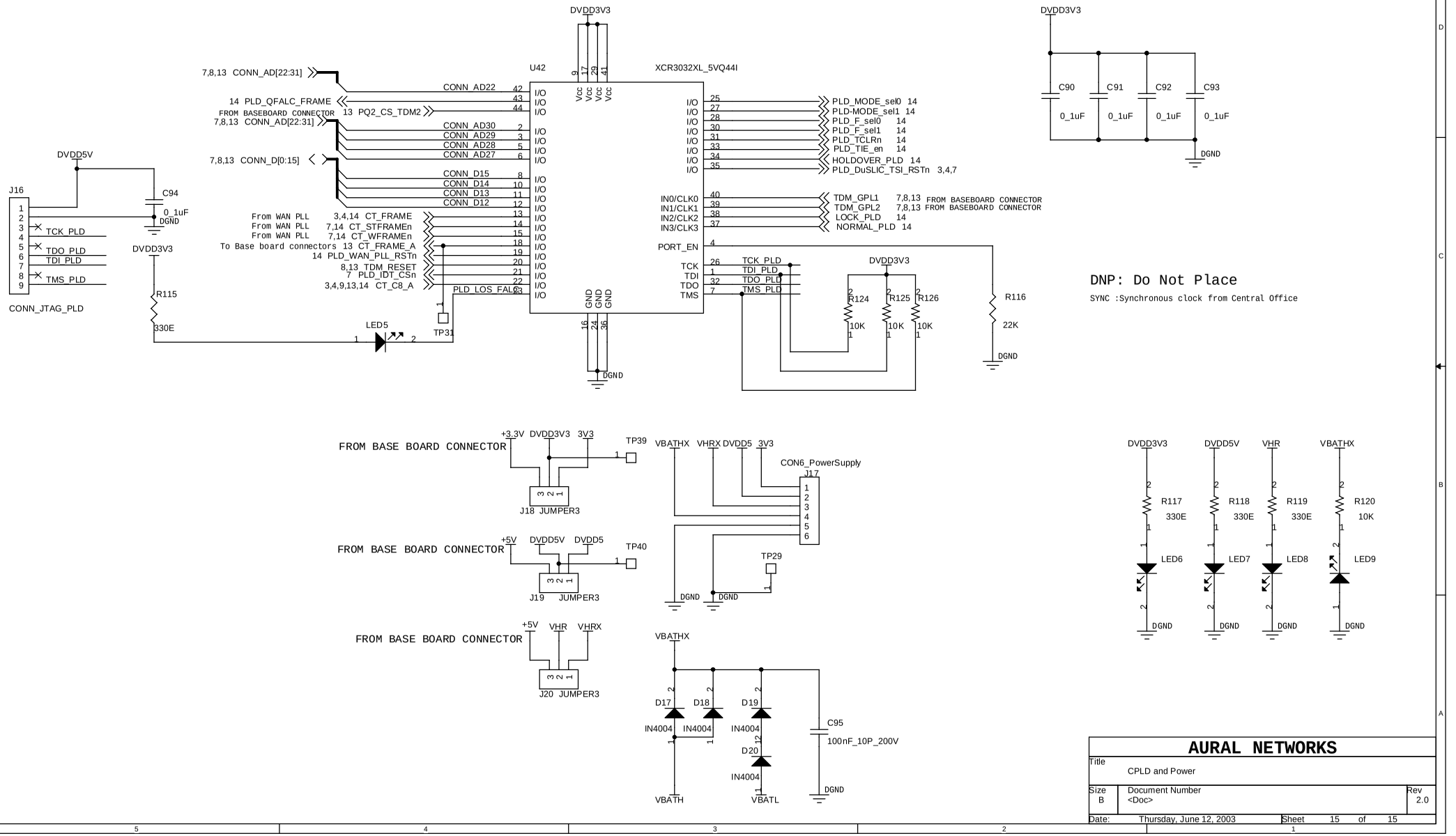
Date: Thursday, June 12, 2003	Sheet 12 of 15	



J13 will connect to J9 connector of base card
J14 will connect to J7 connector of base card
J15 will connect to J8 connector of base card

AURAL NETWORKS		
Title: Base Board Connectors		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 13 of 15	


TO BASE BOARD CONNECTOR -- 8KHz
DVDD3V3
C85
C86
C87
C88
C89
0_1uF
DGND
8 KHz FSC signal from QuadFALC
9 FSC_QFALC
R136 DNP 0E
R138 10K
TP21
9 RCLK1
R137 0E
15 PLD_F_sel1
15 PLD_F_sel0
15 PLD-MODE_sel1
15 PLD_MODE_sel0
15 PLD_WAN_PLL_RSTn
15 PLD_TCLRn
15 PLD_TIE_en
R113 10K
U40
IDT82V3001
Fref
F_sel1
F_sel0
MODE_sel1
MODE_sel0
RST
TCLR
TIE_en
FLOCK
TDO
TDI
TRST
TCK
TMS
IC
VDD
VSS
OSCo
OSCi
LOCK
HOLDOVER
NORMAL
FREERUN
C32o
C40
C16o
C8o
C2o
C3o
C1.5o
C6o
F32o
F16o
F8o
F0o
RSP
TSP
R109 2CLK_OSC 33E
LOCK_PLD 15
HOLDOVER_PLD 15
NORMAL_PLD 15
TP22 TP23 TP24
R110 0E
R111 0E
R112 0E
HCLK
CLK
CT_C8_A
3,4,9,13,15
TP32
TP33
TP34
TP25
TP30
CT_STFRAMEn 7,15
CT_FRAME 3,4,15
CT_WFRAMEn 7,15
R114 0E
DVDD3V3
R108 10K
FOX_F7C-2E3
U39
C84 0_1uF
VDD
E/D
O/P
GND
CLK_OSC
7 TO IDT SWITCH---4.096MHz
7 TO IDT SWITCH --- 16.384MHz
TO BASE BOARD CONNECTOR -- 8.192MHz
DuSLIC/FALC
U41
NC7S04
VCC
IN
OUT*
GND
TP38
R129 0E
CT_FRAMEn 8,9,10,11,12
To QuadFALC
15 PLD_QFALC_FRAME
R130 0E DNP
DNP : Do Not Place
AURAL NETWORKS
Title
CLOCK SYNCHRONIZATION CIRCUIT
Size B
Document Number <Doc>
Rev 2.0
Date: Thursday, June 12, 2003
Sheet 14 of 15



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Title: CPLD and Power		
Size: B	Document Number: <Doc>	Rev: 2.0
Date: Thursday, June 12, 2003	Sheet 15 of 15	

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