XVME-212
6U 32-Channel Digital Input Module

USER'S MANUAL

ACROMAG INCORPORATED
30765 South Wixom Road
P.O. BOX 437
Wixom, MI 48393-7037 U.S.A.

Tel: (248) 295-0885
Fax: (248) 624-9234
Email: xembeddedsales@acromag.com

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xycom
Technical Publications Department
750 North Maple Road
Saline, MI 48176–1292
313-429-4971 (phone)
313-429-1010 (fax)

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The XVME-212 is a 32 channel, opto-isolated, digital input interface, designed to be compatible with the VMEbus structure. The XVME-212 is capable of receiving 32 digital inputs at frequencies up to 3.4 KHz. To ensure signal integrity, the design incorporates integrated "switch" debouncing, as well as the protection provided by the optical isolation of the channel inputs from the system bus structure. In addition, an on-board scanner can be programmed to generate a VMEbus interrupt when any input changes state, thus eliminating the need to poll the input module.

Each digital input is reverse voltage protected and is capable of handling a maximum reverse bias of 50V DC (XVME-212/l) or 6.5V DC (XVME-212/2). Also, the board can be jumpered to occupy any 1K block within the short I/O address space.

The following two versions of the XVME-212 are available:

XVME-212/l -- The **/l** version of the XVME-212 comes with an on-board, 12V DC, isolated power supply. The 12V supply is factory-connected to the input of each channel, thus permitting the system to monitor 12V relay contacts and switches without an external power supply. Voltages other than the 12V may be applied to the inputs (within the l0V-50V input range); however, some board modification will be necessary (i.e., cutting the well identified and easily accessible PC traces to the 12V on-board supply).

XVME-212/2 -- The /2 version of the XVME-212 is very similar to the **/I** version except for the range of allowable input voltage and the absence of an on-board +12V DC power supply. The XVME-212/2 has TTL level inputs with a 6.5V maximum input. In addition, the +12V isolated, on-board power supply is not available, replaced by wire jumpers to the existing +5V supply of the VME backplane.

1.2 MANUAL STRUCTURE

This first chapter provides a functional overview of the XVME-212 and presents the features of Xycom's Standard I/O architecture. Operational aspects of the XVME-212 are then explained in the following fashion:

Chapter 2 - **Installation:** Information required to position the jumpers and switches on the XVME-212, and install the module in a VMEbus chassis.

Chapter 3 - **Programming:** Information required to program the XVME-212 and read digital input signals.

The appendices at the end of this manual provide information on Xycom's Standard I/O Architecture, VMEbus connector/pin descriptions, module schematics, as well as a quick reference guide to the module's jumpers and registers.

1.3 OPERATIONAL BLOCK DIAGRAM

Figure 1-1 shows an operational block diagram of the XVME-212.

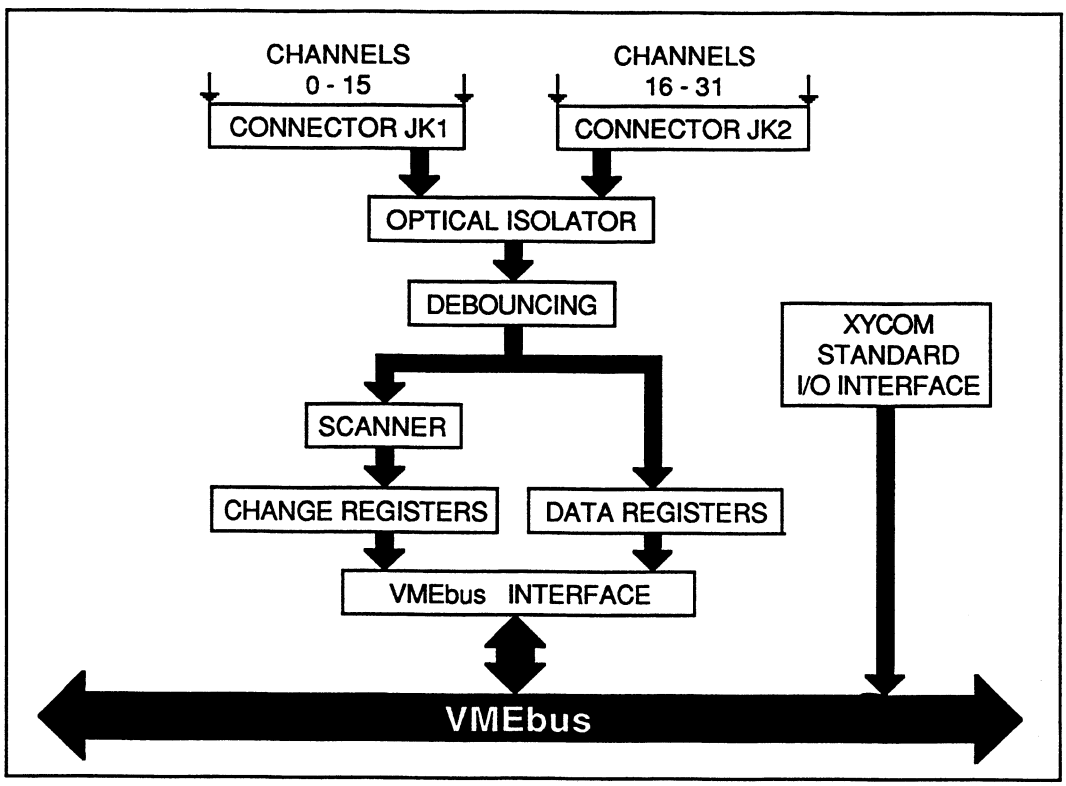


Figure 1-1. Operational Block Diagram of the XVME-212

1.4 FEATURES OF XYCOM'S STANDARD I/O ARCHITECTURE

The XVME-212 and all Xycom I/O modules conform to the unique Xycom VMEbus Standard I/O Architecture. This architecture is intended to make the programming of Xycom VMEbus I/O modules simple and consistent. The following features apply to the operation of the XVME-212:

- Module address space - The XVME-212 and all VMEbus modules are controlled by writing to addresses within the 64K Short I/O Address space. A VMEbus module can be switched to occupy any of the 64 available 1K blocks. This block, known as the I/O Interface Block, contains all of the module's programming registers and ID data. Within the I/O Interface Block, the offsets are standardized so that the user may expect to find the same registers and data at the same offsets across the entire Xycom VMEbus line.

- Module identification - The XVME-212 has ID information which provides its name, model number, manufacturer, and revision level at a location that is consistent **with** other Xycom I/O modules.

- Status/Control Register - This register is always located at address base + 8 lH, and the lower four bits (two Test Status bits, and a red and green LED bit) are standard from module to module.

A detailed description of Xycom I/O Architecture is presented in Appendix A at the rear of this manual.

1.5 **XVME-212 MODULE SPECIFICATIONS**

Table l-l. XVME-2 12 Module Specifications

Characteristic	Specification
Number of Channels	32
Input Voltage Range (XVME-212/l)	+50V DC max. Logic 1 -- 10 to 50V DC Logic 0 -- 0 to lV DC Typical threshold- 3V DC
Input Voltage Range (XVME-212/2)	+65V DC max. Logic 1 -- 2 to 6.5V DC Logic 0 -- 0 to 0.8V DC Typical threshold -- 1.2V DC
Input Impedance (XVME-2 12/ 1)	3.9K +5%
Input Impedance (XVME-2 12/2)	330 +5%
Propagation Delay (with fastest debounce selected)	
Of f-to-on	100 usec max. (l0-25 usec typ.)
On-to-off	600 usec max. (150 usec typ.)
Minimum Detectable Pulse Width	
Positive pulse	100 usec max. (l0-25 usec typ.)
Negative pulse	600 usec max. (150 usec typ.)
Maximum Input Frequency	3.4 KHz typical
Debounce Time	Jumper-selectable from 4.5 usec to 18 msec (8 possible settings)
Reverse Bias Protection (XVME-212/l)	50 V max.
Reverse Bias Protection (XVME-2 12/2)	6.5V max.
Power Requirements	+5V, ±5% 1.7 Amp typ., 2.0 Amp max.

Table l-l. XVME-2 12 Module Specifications (cont'd)

Characteristic	Specification
Isolation	300 VDC channel-to-channel 300 VDC channel to VMEbus ground
Board Dimensions	NEXP board size (160mm x 233.4mm)
Environmental Specifications	
Temperature	
Operating	0° to 65°C (32° to 149°F)
Non-operating	-40° to 85°C (-40° to 158°F)
Humidity	5 to 95% RH, non-condensing (Extremely low humidity conditions may require special protection against static discharge.)
Altitude	
Operating	Sea level to 20,000 ft. (6096m)
Non-operating	Sea level to 50,000 ft. (15240m)
Vibration	
Operating	5 to 2000 Hz .O 15" peak-to-peak displacement 2.5g peak acceleration
Non-operating	5 to 2000 Hz .030" peak-to peak displacement 5.0 g peak (maximum) acceleration
Shock	
Operating	30 g peak acceleration, 11 msec duration
Non-operating	50 g peak acceleration, 11 msec duration

Table 1- 1. XVME-2 12 Module Specifications (cont'd)

Characteristic	Specification
VMEbus Compliance	• Fully compatible with VMEbus standard • Al 6:D16 Data transfer bus slave • Base address jumper-selectable within 64K short I/O address space • Occupies 1K consecutive byte locations • I(1) to I(7) Interrupter (STAT) with programmable vector • Includes Xycom's standard I/O module interface • NEXP

Chapter 2

INSTALLATION

2.1 INTRODUCTION

This chapter provides the information needed to configure the XVME-212 and to install it in a VMEbus backplane card cage.

2.2 SYSTEM REQUIREMENTS

The XVME-212 is a double-high VMEbus compatible module. To operate, it must be properly installed in a VMEbus backplane cardcage. The minimum system requirements for operation of the XVME-212 are one of the following (either A or B below):

A) A host processor properly installed on the same backplane.

A properly installed controller subsystem. An example of such a control subsystem is the Xycom XVME-010 System Resource Module.

-OR-

B) A host processor which incorporates an on-board controller subsystem.

2.3 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers, switches, and connectors on the XVME-212 are illustrated in Figure 2-1.

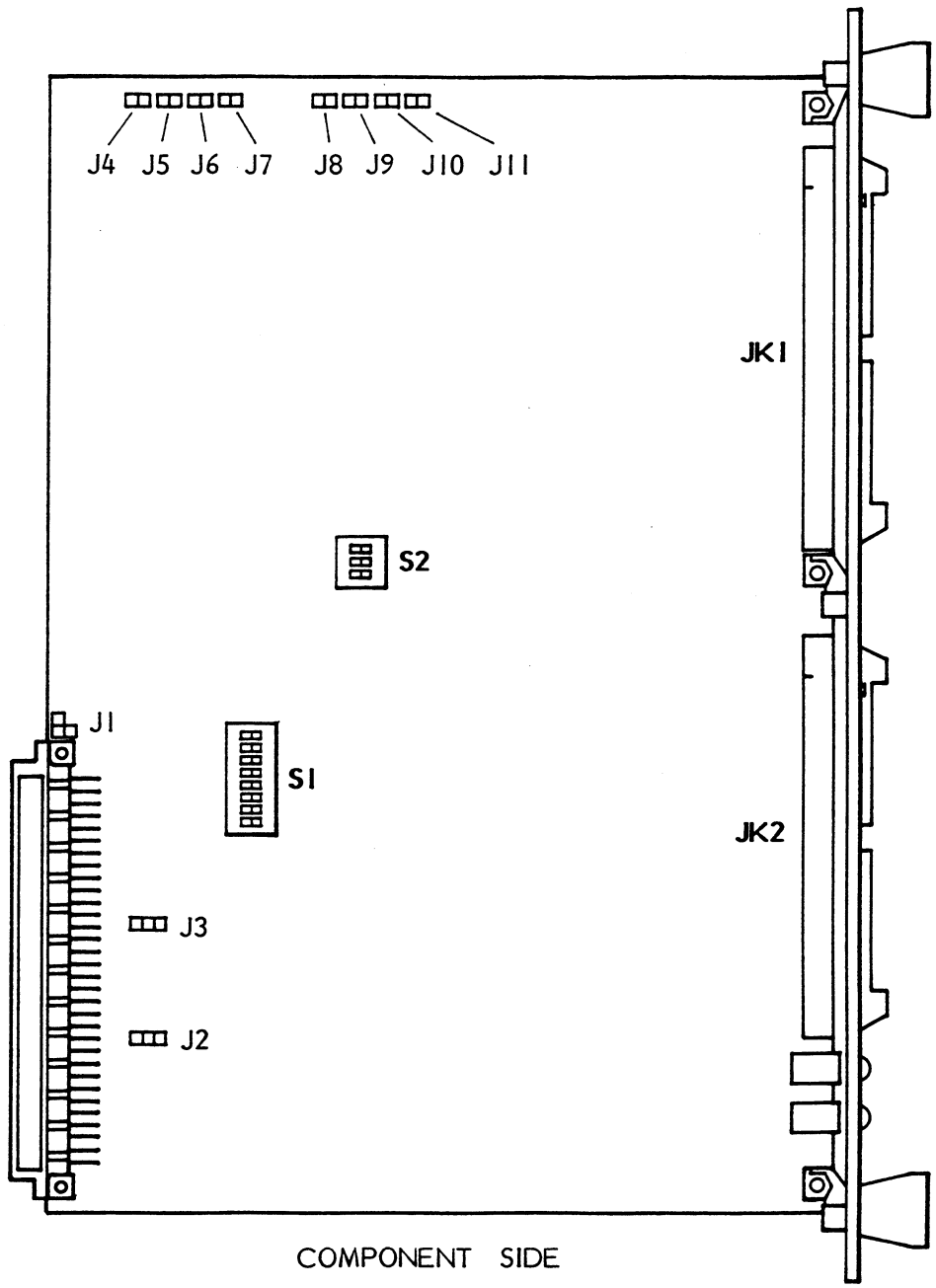


Figure 2-1. XVME-212 jumpers, switches, and connectors.

2.4 JUMPERS/SWITCHES

Prior to installing the XVME-212, it is necessary to choose several jumper/switch selectable options. These options fall into two categories: VMEbus-related options and debounce period jumpers.

VMEbus Options

- Module base address, selected by switches l-6 of the Address Switches (Sl)
- Privilege level required to access the module, selected by Switch 7 of the Address Switches (Sl)
- VMEbus interrupt level, selected by the Interrupt Level Switches (S2)
- Whether to use or bypass the IACK daisy chain, selected by Jumpers Jl and J2

Debounce Period Jumpers

- The length of the debounce period is selected by Jumpers J4 and Jl1.

Table 2-1. XVME-212 Jumper/Switch List

Jumper/Switch	Use
Address Switches (Sl)	
Sl (switches 1-6)	Module Base Address Select
Sl (switch 7)	This switch determines whether the module will respond only to supervisory accesses or to both supervisory and non-privileged accesses.
Sl (switch 8)	This switch works in conjunction with Jumper J3 to determine whether the board operates with address modifiers for Short I/O Address Space or those for Standard Address space. (See note below.)
Interrupt Level Switches (S2)	Selects the interrupts to be generated by a change of state on input lines.
Jl, J2	Selects whether to use or bypass the IACK daisy chain.
J3	This jumper works in conjunction with Sl (Switch 8) for address space selection (i.e., Short I/O Address Space or Standard Address Space. (See note below.)
J4 - Jll	Determines the debounce period.

Note

See also Section 2.4.2, Switch 8 of Switch Bank Sl.

2.4.1 Base Address Selection Switches (Sl-1 to Sl-6)

The XVME-212 module is designed to be addressed within either the VMEbus Short I/O or Standard Memory Space. Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for the XVME I/O modules has been designed to be switch or jumper selectable. When the XVME-212 module is installed in the system, it will occupy a 1 Kbyte block of the Short I/O Memory or Standard Address Space (called the module I/O Interface Block).

The base address decoding scheme for Xycom I/O modules is such that the starting address for each I/O Interface Block resides on a 1K boundary. Thus, the module base address for each I/O Interface Block resides on any one of 64 possible 1K boundaries within the Short I/O Address space or any 1K boundaries within the Standard Address Space's upper 64K.

The module base address is selected by using the switches labeled 1-6 in DIP switch bank S1. Figure 2-2 shows the Switch bank S1 and how the individual switches (1-6) relate to the base address bits.

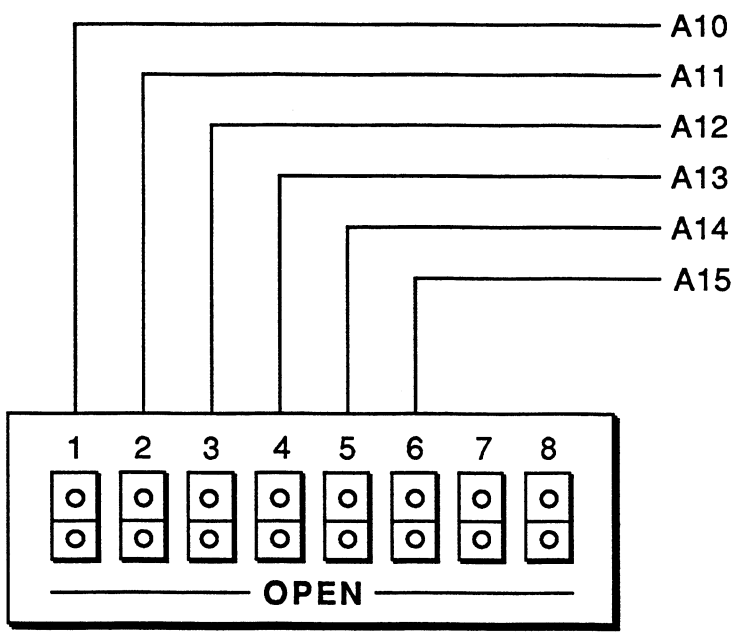


Figure 2-2. Switch Bank S1 - Base Address Switches

When a switch is in the closed position, (i.e., when it is pushed in on the opposite end of the switch bank from the "open" label), the corresponding base address bit will be logic "0". When a switch is set to the open position, the corresponding base address bit will be logic "1".

Table 2-2 shows a list of the 64 1K boundaries which can be used as module base addresses in the Short I/O Address space and the corresponding switch settings (switches 1-6) from S1.

Table 2-2. Base Address Switch Options

Switches						VME base address in VME Short I/O Address space
6(A15)	5(A14)	4(A13)	3(A12)	2(A11)	1(A10)	
0	0	0	0	0	0	0000H
0	0	0	0	0	1	0400H
0	0	0	0	1	0	0800H
0	0	0	0	1	1	0C00H
0	0	0	1	0	0	1000H
0	0	0	1	0	1	1400H
0	0	0	1	1	0	1800H
0	0	0	1	1	1	1C00H
0	0	1	0	0	0	2000H
0	0	1	0	0	1	2400H
0	0	1	0	1	0	2800H
0	0	1	0	1	1	2C00H
0	0	1	1	0	0	3000H
0	0	1	1	0	1	3400H
0	0	1	1	1	0	3800H
0	0	1	1	1	1	3C00H
0	1	0	0	0	0	4000H
0	1	0	0	0	1	4400H
0	1	0	0	1	0	4800H
0	1	0	0	1	1	4C00H
0	1	0	1	0	0	5000H
0	1	0	1	0	1	5400H
0	1	0	1	1	0	5800H
0	1	0	1	1	1	5C00H
0	1	1	0	0	0	6000H
0	1	1	0	0	1	6400H
0	1	1	0	1	0	6800H
0	1	1	0	1	1	6C00H
0	1	1	1	0	0	7000H
0	1	1	1	0	1	7400H
0	1	1	1	1	0	7800H
0	1	1	1	1	1	7C00H
1	0	0	0	0	0	8000H
1	0	0	0	0	1	8400H
1	0	0	0	1	0	8800H
1	0	0	0	1	1	8C00H
1	0	0	1	0	0	9000H
1	0	0	1	0	1	9400H
1	0	0	1	1	0	9800H
1	0	0	1	1	1	9C00H
1	0	1	0	0	0	A000H
1	0	1	0	0	1	A400H
1	0	1	0	1	0	A800H
1	0	1	0	1	1	AC00H
1	0	1	1	0	0	B000H
1	0	1	1	0	1	B400H
1	0	1	1	1	0	B800H
1	0	1	1	1	1	BC00H
1	1	0	0	0	0	C000H
1	1	0	0	0	1	C400H
1	1	0	0	1	0	C800H
1	1	0	0	1	1	CC00H
1	1	0	1	0	0	D000H
1	1	0	1	0	1	D400H
1	1	0	1	1	0	D800H
1	1	0	1	1	1	DC00H
1	1	1	0	0	0	E000H
1	1	1	0	0	1	E400H
1	1	1	0	1	0	E800H
1	1	1	0	1	1	EC00H
1	1	1	1	0	0	F000H
1	1	1	1	0	1	F400H
1	1	1	1	1	0	F800H
1	1	1	1	1	1	FC00H

NOTE

Open = Logic "1"
Closed = Logic "0"

2.4.2 Address Space Selection (J3)

The XVME-212 may be placed in VMEbus Short I/O or Standard Memory Space. The selection is made by configuring Jumper J3 and Switch 8 of Switch Bank Sl (see Figure 2-2) as shown in Table 2-3 below.

Table 2-3. Addressing Options (J3)

Jumper	Switch 8 (Sl)	Option Selected
J3A	Open	Standard Data Access Operation
J3B	Closed	Short I/O Access Operation

If Jumper J3A is installed, Switch 8 (on Switch bank Sl) must be set to OPEN.
If Jumper J3B is installed, Switch 8 must be set to CLOSED.

The Standard I/O Architecture recommends that the XVME-212 operate within the Short I/O Address Space, in order to take advantage of the Standard I/O Architecture's various features, which are described in Appendix A.

If required, the XVME-212 can operate in the Standard Address Space. Note that in this mode, the XVME-212 will always reside within the upper 64 Kbyte segment of the Standard Memory Address Space (i.e., the address range FF0000H through FFFFFFH). Sl switches 1 through 6, then determines which 1K block of the upper 64 Kbyte segment is to be occupied.

2.4.3 Supervisory/Non-Privileged Mode Selection

The XVME-212 can be configured to respond only to supervisory access, or to both non-privileged and supervisory accesses, by selecting the position of Switch 7 (located in Switch Bank Sl, see Figure 2-2), as shown in Table 2-4 below.

Table 2-4. Privilege Options

Switch 7	Privilege Mode Selected
Closed	Supervisory or Non-privileged
Open	Supervisory Only

2.4.4 Address Modifier Reference

Table 2-5 below indicates the actual VMEbus Address Modifier code that the XVME-212 will respond to, based on the position of the options discussed in the previous two sections.

Table 2-5. Address Modifier Code Options

	Switches 7	Switches 8	Jumper J3	XVME-212 Address Modifier Code
Normal	Closed	Closed	B	29H or 2DH
Short I/O	Open	Closed	B	2DH only
Standard	Closed	Open	A	39H or 3DH
Address	Open	Open	A	3DH only

2.45 Interrupt Level Switches (S2)

The three Interrupt Level Switches select which VMEbus interrupt level is to be used by the module. The XVME-212 can be programmed to generate an interrupt whenever a change of state is detected on any input line, and these switches will determine the level of that interrupt. The Interrupt Level Switches are defined in Table 2-6.

Table 2-6. Interrupt Level Switches (S2)

S2-3	S2-2	S2-1	VMEbus Interrupt Level
OPEN	OPEN	OPEN	7
OPEN	OPEN	CLOSED	6
OPEN	CLOSED	OPEN	5
OPEN	CLOSED	CLOSED	4
CLOSED	OPEN	OPEN	3
CLOSED	OPEN	CLOSED	2
CLOSED	CLOSED	OPEN	1
CLOSED	**CLOSED**	**CLOSED**	None, interrupts disabled

2.4.6 IACK Enable Jumpers (Jl, J2)

When operating in an interrupt environment, the module uses the VMEbus IACK daisy chain to determine which module gets acknowledged, if two or more modules share one of the interrupt request lines. When the module is never going to be used in an interrupt environment, the daisy chain through the module can be bypassed to speed up the IACK arbitration. This is controlled by Jumpers Jl and J2, as shown in Table 2-7.

Table 2-7. IACK Enable Jumpers

	Jl	J2
Module uses IACK daisy chain	B	B
Module bypasses IACK daisy chain	A	A

When in the A position, the module cannot respond to interrupts because IACKIN* is not monitored (IACKIN* is connected directly to IACKOUT* instead). When used in this configuration, all poles of S2 should be closed to ensure that a programming bug does not generate VMEbus interrupts.

When interrupts are going to be used, the jumpers must be in the B position.

2.4.7 Debounce Period Jumpers (J4-J 11)

When a mechanical switch closes, several contact bounces can be expected. Several transitions or quickly changing input images can appear while the switch bounces. To eliminate these bounces, circuitry is provided, which works as follows. When a change is detected in an input, the change is not immediately reported to the scanner. Instead, a timer, with time period, T, will start accumulating time. During this time, T, if the input reverts to its original state (bounces), the timer is restarted and the change is not reported. If the input does not bounce for the duration of time, T, the change will be reported to the scanner at the end of time period T. This means that the input must assume the new state and stay in the new state without bouncing for time, T, before the change is reported to the scanner.

The value of time, T, is selectable via eight on-board jumpers. One and onlv one jumper must be installed. This jumper defines the time, T, to be used by all 32 channels. The following table shows the available selections.

Table 2-8. Debounce Period Jumpers

	Jumper	T min	T max
install only one ▶	J11	3.5 us	4.5 us
	Jl0	7 us	9 us
	J9	14 us	18 us
	J8	28 us	36 us
	J7	112 us	144 us
	J5	448 us	576 us
	J4	1.8 ms	2.3 ms
	J6	14 ms	18 ms

Note

One (and only one) of the above jumpers must be installed for proper module operation.

Note that the time associated with Jll is very short with respect to the opto isolator's response time. So selecting this time will essentially defeat the debounce circuitry for users concerned about speed and not concerned about bounce.

2.5 INSTALLATION

The Xycom VMEbus modules are installed in a standard VMEbus backplane. Figure 2-3

shows a standard VME chassis and a typical backplane configuration. Two rows of backplane connectors are depicted: the P1 backplane and the P2 backplane. (However, the XVME-212 uses only the P1 backplane.)

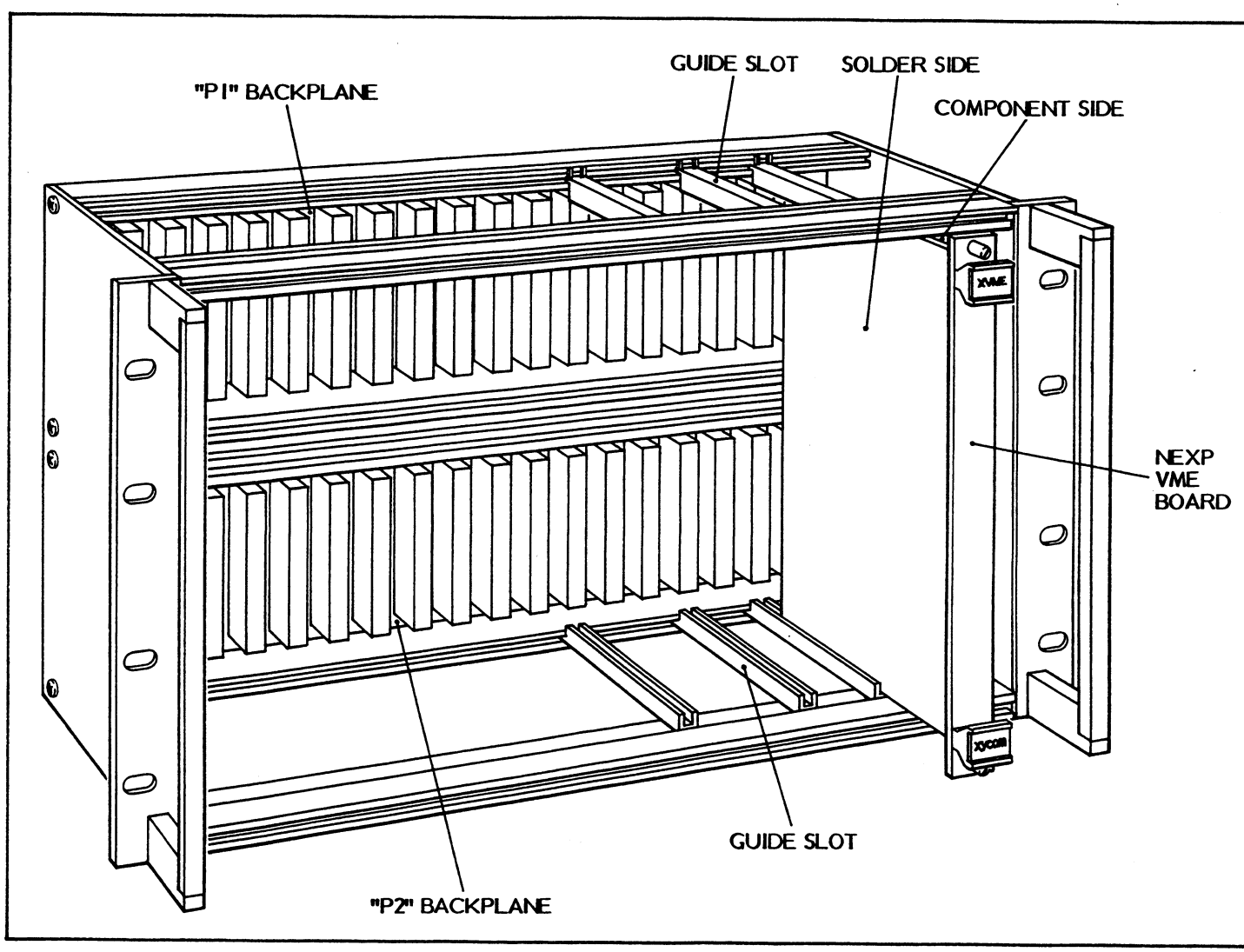


Figure 2-3. VMEbus Chassis

2.5.1 Installation Procedure

CAUTION

Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. (Please check the jumper configuration against the diagrams and lists in this manual.)

To install a board in the card cage, perform the following steps:

1) Make sure the cardcage slot (which will hold the module) is clear and accessible.

2) Center the board on the plastic guides in the slot so that the solder side is facing to the left and the component side is facing to the right (refer to Figure 2-3).

3) Push the board slowly toward the rear of the chassis, until the connector engage (the board should slide freely in the plastic guides).

4) Apply straightforward pressure to the handle on the panel front, until the connector is fully engaged and properly seated.

NOTE

It should not be necessary to use excessive force or pressure to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

5) Once the board is properly seated, secure it to the chassis by tightening the two machine screws at the extreme top and bottom of the board.

2.6 DIGITAL INPUT CONNECTIONS

The module is capable of receiving 32 separate digital inputs. The inputs are accessible on the front edge of the board in the form of two 50-pin ribbon headers. The connectors are labeled JKl and JK2 (see Figure 2-l). The following table shows the pin designations for connectors JKl and JK2.

Table 2-9. Input Connector Signal Definitions

Connector Pin Number	JK 1 Connection	JK2 Connection
1	CHO-	CH16-
2	CHO+	CH16+
3	CHl-	CH17-
4	CHl+	CH17+
5		
6		
7	CH2-	CH18-
8	CH2+	CH18+
9	CH3-	CH19-
10	CH3+	CH19+
11		
12		
13	CH4-	CH20-
14	CH4+	CH20+
15	CH5-	CH21-
16	CH5+	CH21+
17		
18		
19	CH6-	CH22-
20	CH6+	CH22+
21	CH7-	CH23-
22	CH7+	CH23+
23		
24		
25	CH8-	CH24-
26	CH8+	CH24+
27	CH9-	CH25-
28	CH9+	CH25+
29		
30		
31	CHl0-	CH26-
32	CHlO+	CH26+
33	CHIl-	CH27-
34	CHIl+	CH27+
35		
36		
37	CH12-	CH28-
38	CH12+	CH28+
39	CH13-	CH29-
40	CH13+	CH29+
41		
42		
43	CH14-	CH30-
44	CH14+	CH30+
45	CH15-	CH31-
46	CH15+	CH31+
47		
48		
49	12V Return (XVME-212/l) Ground (XVME-2 12/2)	12V Return (XVME-212/l) Ground (XVME-2 12/2)
50	12V Return (XVME-212/l) Ground (XVME-2 12/2)	12VReturn(XVME-212/l) Ground (XVME-2 12/2)

2.7 MECHANICAL SWITCH/RELAY OPERATION

2.7.1 XVME-212/1

With the XVME-212/l, an isolated 12V DC supply is available for use with mechanical switches. The 12V supply's positive terminal is connected to the "+" terminal of each input channel. The 12V supply's return terminal is connected to pins 49 and 50 of the JK connectors (see Table 2-9). The external switch should be connected between the "-" terminal of the particular input channel and pins 49, 50. When the switch closes, the 12V return is connected to the "-" terminal of the input channel which turns the input channel on. No external supplies are required.

Note that all input channels have their "+" terminals connected together (they are all connected to the 12V supply). Some users will want electrical isolation between channels. To facilitate this, break points are available for all 32 input channels. When the breakpoint is cut, the input channel's "+" terminal is disconnected from the isolated supply and the other input channels. The 12V supply cannot be used on a channel when its break point is cut, however. These break points are labeled as CHO - CH31 on the board and are easily accessible from the circuit side of the board under the 32 1 W resistors. Pads are provided on either side of the break point to allow reconnection, if required. The 300V channel-to-channel isolation specification applies onlv to channels which have their break point cut. The 300V channel to VMEbus isolation is maintained whether the break points are cut or not (because the 12V supply is isolated to 300V).

2.7.2 XVME-212/2

With the XVME-212/2, the +5V supply of the VME backplane is used with the mechanical switches. Each "+" terminal of the input channels is connected to +5V (with reference to logic ground) while pins 49 and 50 of the JK ports are connected to logic ground. (See Table 2-9.) The external switch should be connected between the "-" terminal of the particular input channel and pins 49, 50. When the switch closes, logic ground is connected to the "-" terminal of the input channel, which then turns on the input channel.

Note that all input channels have their "+" terminals connected together; they are all connected to +5V. Some users will want electrical isolation between channels. To facilitate this, break points are available for all 32 input channels. When the breakpoint is cut, the input channel's "+" terminal is disconnected from the +5V supply and the other input channels. The +5V cannot be used on a channel once its break point is cut, however. These break points are labeled CHO - CH31 on the board and are easily accessible from the circuit side of the board. Pads are provided on either side of the break point to allow reconnection, if required. The 300V channel-to-channel and the 300V channel-to-VMEbus isolation applies ONLY to channels which have their break point cut.

Chapter 3

PROGRAMMING

3.1 INTRODUCTION

This chapter provides the information required to program the XVME-212, including the following:

- Discussion of base addressing and I/O module address space
- Presentation of module address map showing programming locations

3.2 BASE ADDRESSING

The XVME-212 operates as an I/O module in VMEbus systems and is located in the 64K VMEbus Short I/O Address Space (or the upper 64K of the Standard Address space). It can be located at any one of 64 base addresses at 1K intervals within this address space. The base address is selected via the switches described in Section 2.4.1.

When located at its base address, the XVME-212 is allotted a 1K block of address space for its own use. This 1K block of address space is termed the I/O Interface Block, and contains all of the module's programming locations. Figure 3-l shows the I/O Interface Block of the XVME-212 and its relation to the address space.

When accessing locations in the I/O Interface Block, the addresses shown in Figure 3-1 must be added to the module's base address.

For example, if the XVME-212 is located at Short I/O Base Address 0400H, the address of the Control/Status register is 0481H (base+8lH).

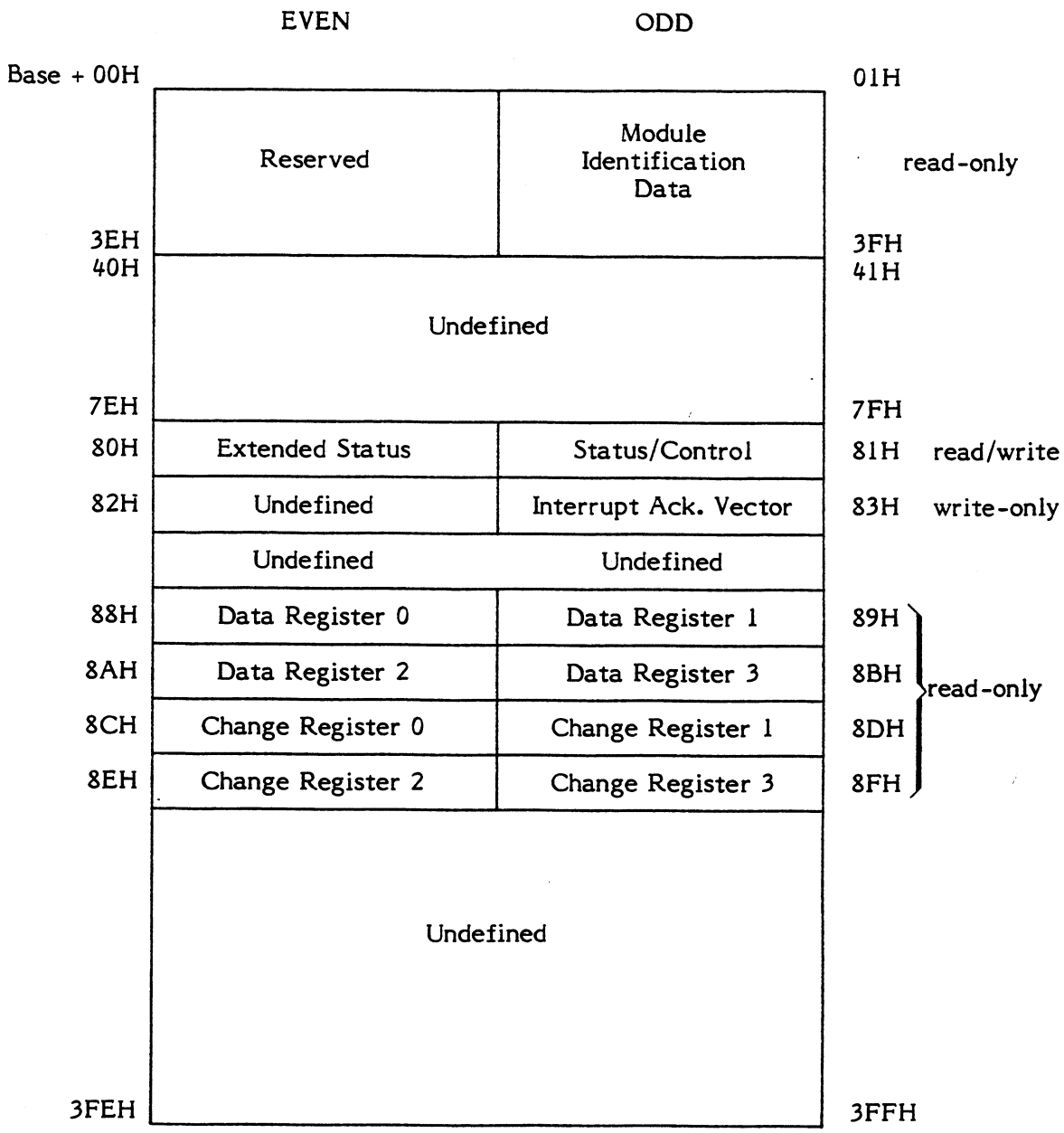


Figure 3-1. XVME-212 I/O Interface Block and its Possible Locations in Short I/O Address Space

3.3 I/O INTERFACE BLOCK

The I/O Interface.Block of the XVME-212 contains the following programming locations (as shown in Figure 3-1) which are defined in greater detail later in the chapter.

- I.D. information (base+OlH to base+3FH): These locations provide information specifying model number, manufacturer, and revision level.
- Extended Status Register (base+80H) and Status/Control Register (base+8 1H): These locations enable/disable interrupts from each of the four ports, indicate if an interrupt is pending, and control the Pass and Fail LEDs.
- Interrupt Acknowledge (IACK) Vector Register (base+83H), which holds the vector to be driven on the VMEbus when a VMEbus interrupt generated by the XVME-2 12 is acknowledged.
- Data Registers which hold the data from the four ports.
- Change registers which indicate whether data on any channel has changed.

> Note
>
> Reading or writing to undefined locations may make application software incompatible with future versions of this module.

3.4 MODULE IDENTIFICATION DATA (Base+0lH to 3FH - odd byte locations only)

The Xycom module identification scheme provides a unique method of registering module-specific information in an ASCII encoded format. The I.D. data is provided as 32 ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K byte blocks occupied by the module, and module functional revision level information. This information can be read by the system processor on power-up to verify the system configuration and operational status. Table 3-1 defines the identification information locations.

Table 3-1. Identification Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier, always "VMEID" (5 characters)
5	E	45	
7	I	49	
9	D	44	
B	X	58	
D	Y	59	Manufacturer's I.D., always "XYC" for XYCOM modules (3 characters)
F	C	43	
11	2	32	
13	1	31	
15	2	32	Module Model Number (3 characters and 4 trailing blanks)
17		20	
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	
23	1	31	Major functional revision level with leading blank (if single digit)
25	1	30	
27		20	Minor functional revision level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		
37	"		Manufacturer Dependent Information, Reserved for future use
39	"		
3B	"		
3D	"		
3F	"		

The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data has been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1H - 3FH).

In this way, I.D. information can be accessed by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex coded ASCII value at each location. Thus, in this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH.

3.5 EXTENDED STATUS (base+80H) and STATUS/CONTROL REGISTERS (base+81H)

Writing to the Status/Control Register controls the red and green LEDs, enables/disables interrupts from any of the four ports, and indicates whether or not an interrupt is pending.

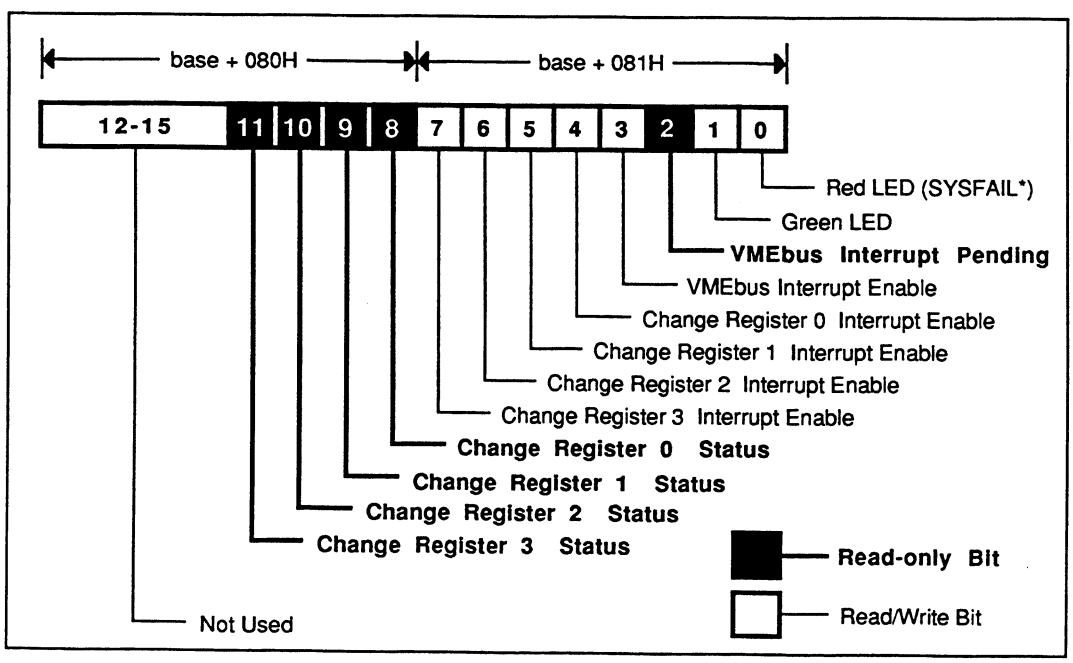


Figure 3-2. Extended Status (080H) and Status/Control Registers (081H)

> Note
>
> The Extended Status and Status/Control Registers can be accessed as a single 16-bit word or as two 8-bit bytes.

3.5.1 Extended Status and Status/Control Register Bit Definitions

0,1: Red LED.. Green LED
These bits control the red and green LEDs. The red and green LEDs provide visual indication of a module status.

- A logic "0" turns on the red LED (D0)
- A logic "1" turns on the green LED (Dl)

The LEDs should be used to indicate the following status (Table 3-2) as set forth by the Xycom architecture (described in Appendix A).

Table 3-2. LED Status

Status Bits		LEDs			
1	0	Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

Note

The XVME-212 is a non-intelligent module, so all diagnostics must be performed by the system host.

2 VMEbus Interrupt Pending
This read-only bit reads 1 whenever BOTH of the following conditions are met:

- One or more of the Change Register n Interrupt Enable bits (bits 4-7 of the Status/Control Register) has been set to 1.

AND

- A bit in one of the interrupt-enabled Change Registers associated with a port has the value 1. A bit value of 1 in a Change Register indicates that a change of state has occurred on a specified input channel.

3 VMEbus Interrupt Enable
This bit enables VMEbus interrupts from the XVME-212 module:

1- a VMEbus interrupt will be generated automatically whenever the XVME-212 sets bit 2 to 1.
2- no VMEbus interrupt will be generated.

4-7: Change Register n Interrupt Enable

These bits individually enable the Change Registers to generate VMEbus interrupts whenever any bit in a Change Register is set. Writing a 1 in one of these bits enables interrupts from a specific Change Register, writing 0 disables interrupts from the register.

Bit 4 -- Enables/disables Change Register 0
Bit 5 -- Enables/disables Change Register 1
Bit 6 -- Enables/disables Change Register 2
Bit 7 -- Enables/disables Change Register 3

8-l1: Change Register n Status

Change Register Status bits:

Bit 8 -- Status of Change Register 0
Bit 9 -- Status of Change Register 1
Bit 10 -- Status of Change Register 2
Bit 11 -- Status of Change Register 3

When the scanner detects a bit set in a Change Register, it will set the appropriate above bit to 1. These bits are reset to zero when the corresponding Data Register is read. These bits may be polled to quickly determine whether any Change Registers have bits set. These bits are not conditioned by any one of the interrupt enable bits 4-7.

12-15: Not used.

3.5.2 Generating VMEbus Interrupts

Bits 4-7 of the Status/Control Register are individually ANDed with bits 8-11. The results of the ANDs are ORed together to produce bit 2. Bit 2 is ANDed with bit 3 and when the result of this AND is 1, a VMEbus interrupt will be generated. The level of the VMEbus interrupt is determined by the setting of Switch bank S2 (see Section 2.4.5). Section 3.8 describes in detail how interrupts are generated.

3.6 INTERRUPT ACKNOWLEDGE (IACK) VECTOR REGISTER (base+83H)

This write-only register holds the vector to be driven on the VMEbus when a VMEbus interrupt generated by the XVME-212 is acknowledged.

3.7 DATA REGISTERS

Four read-only Data Registers hold the state of the XVME-212's four input ports (see Figure 3-3).

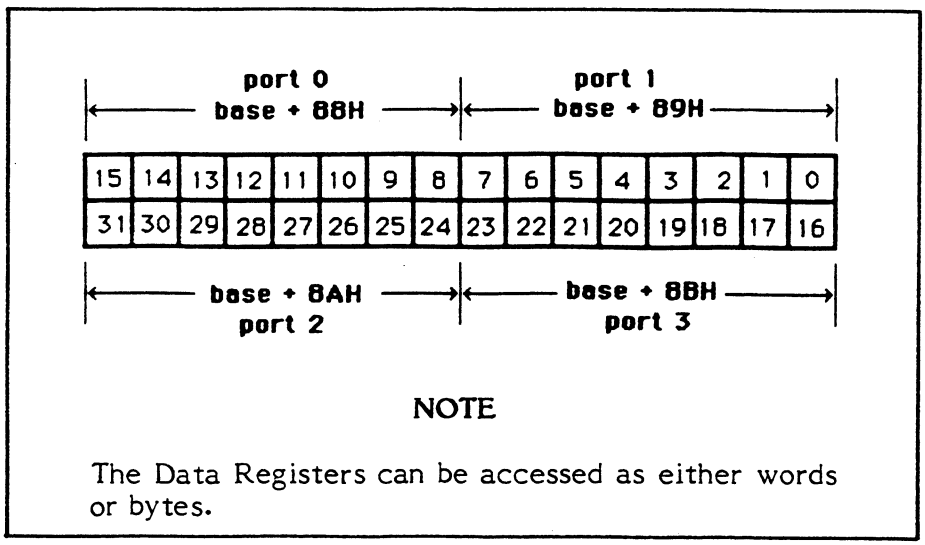


Figure 3-3. Data Registers (read-only)

The numbers in each bit position indicate the input channel associated with each bit of the data registers.

When an input channel is on (voltage greater than 10V for XVME-212/1 or greater than 2.0V for XVME-212/2), its state will be read as 1. When an input channel is off (voltage less than 1V for XVME-212/1 and less than .81V for XVME-212/2), its state will be read as 0.

When Data Registers are read, the corresponding Change Registers (8 change bits) will be zeroed. This is true for word or byte data reads. This is the only mechanism (with the exception of VMEbus resets) which will reset the Change Register bits. Each Change Register bit will be set again when the input state is different from the image in the Data Registers. This alerts the CPU that an input has changed state since the CPU last read the Data Registers (because the Change Register was zeroed the last time the Data Register was read). The Data Registers should be read again to clear the corresponding Change Register bits.

3.8 CHANGE REGISTERS

These four read-only registers contain the change bits for the 32 input channels. These bits are set by the scanner when it detects a state transition in an input channel. Each input channel has one change bit (see Figure 3-4). Each Change Register corresponds to one Data Register (compare with Figure 3-3).

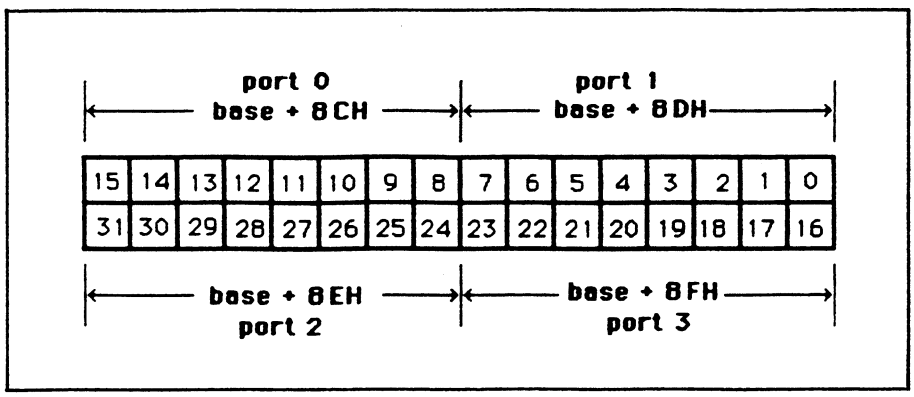


Figure 3-4. Change Registers (read-only)

These bits are reset when the corresponding data register is read. These registers may be read as either words or bytes.

3.9 SCANNER

The scanner consists of circuitry which monitors the input channels and detects state transitions. When a state transition is detected in any input channels, the Change Register bit for that channel will be set. Both on-to-off and off-to-on transitions will be detected. The Change Register bit remains set even if the input channel reverts to its original state, providing the ability to detect pulses in any of the input channels. The Change Register bits can be interrogated to determine which individual channel experienced a pulse.

3.9.1 Scanner Operation

The scanner sequentially executes scans in which the input channels are checked one nibble (four inputs) at a time for state transitions. Eight nibbles (32 input channels) must be checked to complete one scan. The architecture of the scanner does not allow it to be stopped in the middle of a scan. The scanner must complete its scan and stop before meaningful information can be read from the Data or Change registers. The assertion of DTACK* is delayed until the scanner completes its scan and stops when the VMEbus reads the Data or Change registers. The scanner requires 1.25 us to execute one scan. The delay introduced into a given bus cycle is random value between 0 and 1.125 us (in .125 us increments). If the registers are read at the point where the scanner is at the end of a scan, no delay will result. If the registers are read at the point where the scanner just started, the maximum delay will be encountered.

3.9.2 Stopping the Scanner

Reading the Change or Data Register forces the scanner to stop. The scanner is restarted immediately after a Data Register is read. However, it remains stopped after a Change

Register is read. This ensures that the data read from the Change and Data Registers is from the same scan (when a Change Register read is followed by a Data Register read). If the scanner were allowed to run, a Change Register bit could be set after the Change register was read but before the Data Register is read. Because reading a Data Register zeros the Change Register, any Change Register bits set between the two reads would be lost. Stopping the scanner in this fashion ensures that no change Register bits will be lost.

3.9.3 Restarting the Scanner

If the scanner is stopped due to reading the Change Register, it can be restarted by reading the Data Register, the Extended Status, or the Status/Control Register. The scanner is also started up automatically after the XVME-212 is reset.

3.10 VMEbus INTERRUPTS

Each of the four Change Registers has an interrupt enable bit in the Status/Control Register (bits 4-7). When this bit is set, a VMEbus interrupt will be generated when any bit of the corresponding Change Register is set and the VMEbus Interrupt Enable bit (bit 3 of the Status/Control Register) is set. This alerts the CPU that an input has changed state since the last time the CPU read the data registers.

Figure 3-5 illustrates the logic involved in generating a VMEbus interrupt. Reading the corresponding Data Register will reset the VMEbus interrupt (because reading the Data Registers will reset the corresponding Status/Control bit 8-11). When the VMEbus interrupt enable (bit 3) is reset no VMEbus interrupt will be generated. By using the interrupt mechanism, the VMEbus is relieved of the traffic required to constantly poll the module.

The level of the VMEbus interrupt generated by the XVME-212 is determined by the setting of Switch bank S2 (see Section 2.4.5). The IACK vector is determined by the contents of the IACK Vector Register at location base+83H (see Section 3.6).

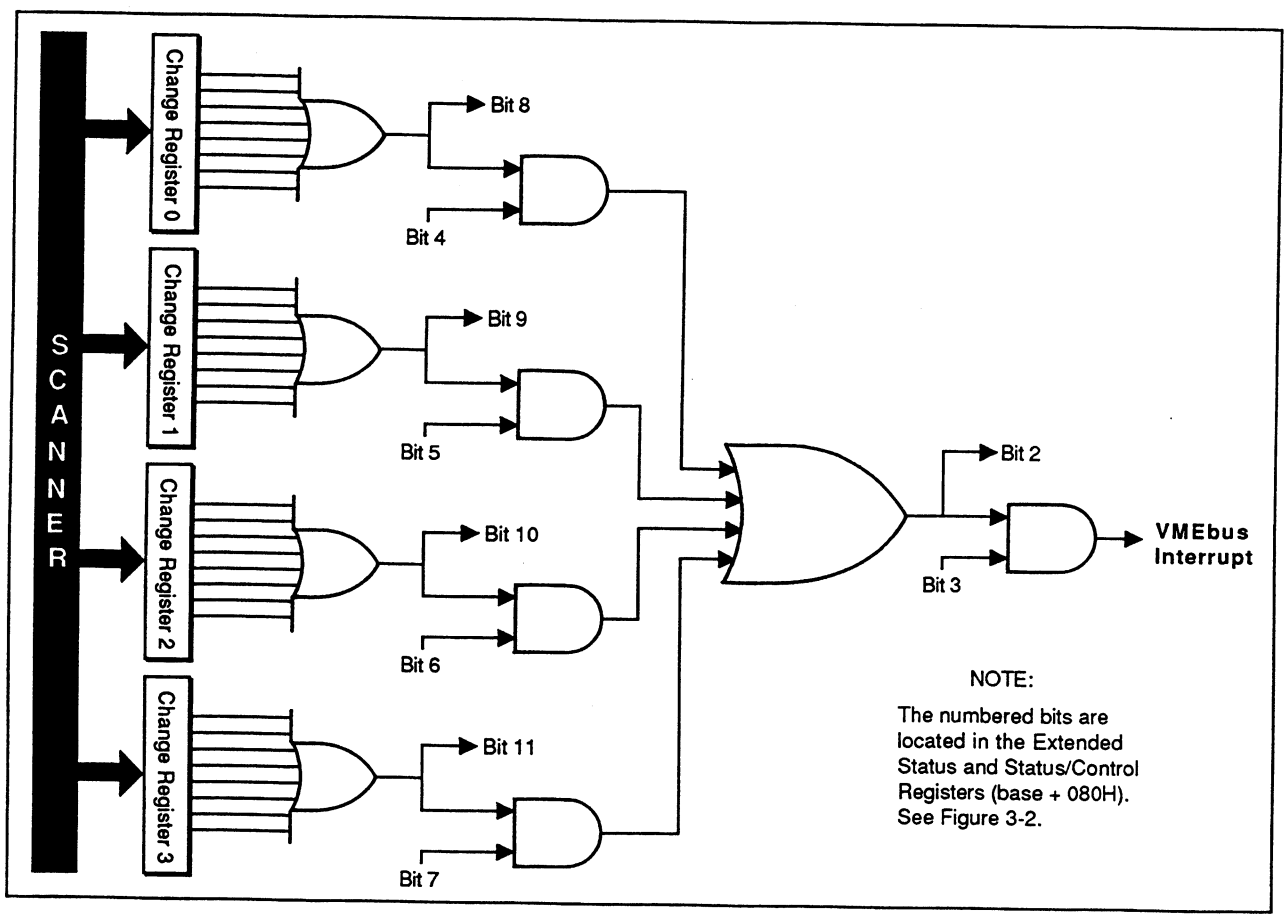


Figure 3-5. Generating a VMEbus Interrupt

3.11 PROGRAMMING CONSIDERATIONS

Use the following procedure to ensure that no change bits in a Change Register are zeroed before they are read. The Change Register must be read first, which will stop the scanner. Then the Data Register is read, which will zero the Change Register and restart the scanner. The reason for this sequence is explained in Section 3.9.2. Reading any Change Register stops the scanner and reading any Data Register restarts it. The user-should therefore read the Data registers as logical pairs (i.e., read Change Register 3, then Data Register 3, not Change Register 3 then Data Register 2). These logical pairs may be words or bytes. For example, to read all channels on the board as words, the correct sequence is:

1. read Change Registers 0 and I (as one word)
2. read Data Registers 0 and 1 (as one word)
3. read Change Registers 2 and 3 (as one word)
4. read Data Registers 2 and 3 (as one word)

During the time that the scanner is stopped, no changes in state will be detected and the Data Registers are not updated. In systems which must keep up with the fast changing inputs, the time that the scanner is stopped must be minimized. It is therefore necessary to read the Extended Status, Status/Control, or Data Registers (restarting the scanner) quickly after the Change Register is read (stopping the scanner). It is suggested that the user disable all CPU interrupts between the two reads. If an interrupt is taken after the Change Register read but before the data/status registers are read, the scanner would be off for the duration of the interrupt service routine. The following chart shows the relationship of input channel signals with respect to stopping the scanner.

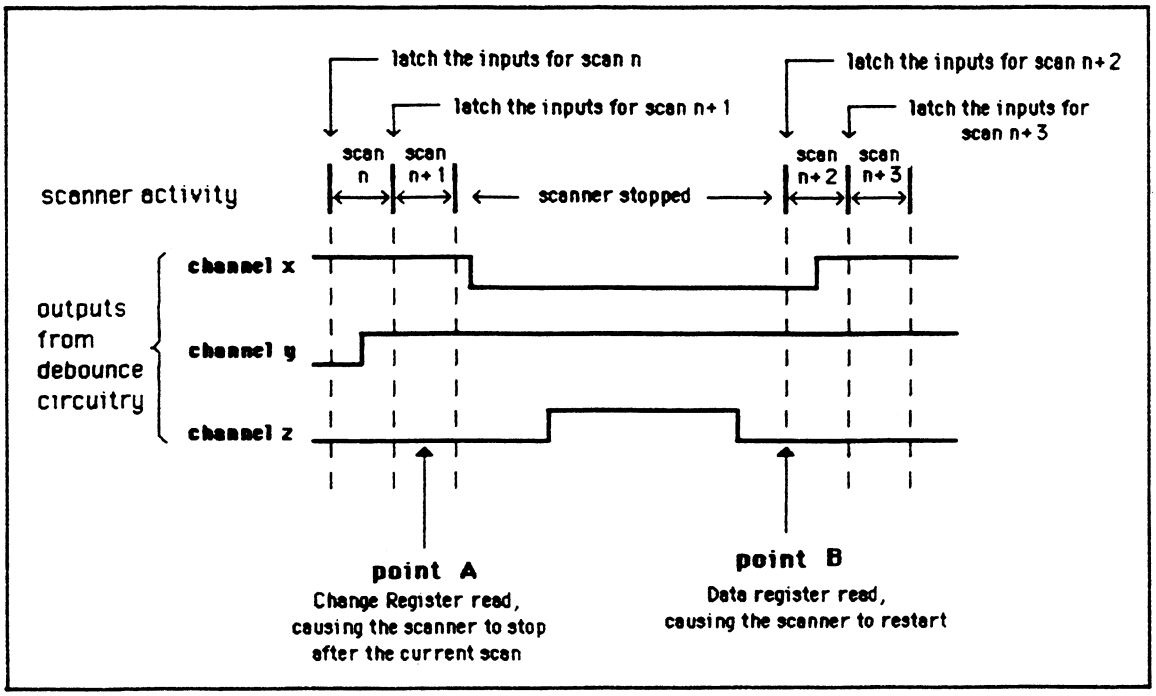


Figure 3-6. Relationship of Input Channel Signals with Respect to Stopping the Scanner

The Data and Change Registers contain the following data at the end of the designated scan:

	Change Register bits			Data Register bits		
After scan	x	y	z	x	y	z
n	0	0	0	1	0	0
n+1	0	1	0	1	1	0
n+2	1	0	0	0	1	0
n+3	1	0	0	1	1	0
Change Register read at point A	0	1	0			
Data Register read at point B				1	1	0

Please note the following:

1. The pulse on line z was undetected, because its rising AND falling edge occurred while the scanner was stopped.

2. The pulse on line x is detectable by the host, even though the line reverted to its original state during scan n+2, because Change Register bit x remained set.

3. The data read at point B was the data present at the start of scan n+l, because the data registers are not updated while the scanner is stopped.

4. The data read at point B caused Change Register bit y to clear.

Polled operation is enhanced by bits 8-11 of the Extended Status Register. These bits are set when the scanner detects any change bit set in a Change Register. These bits can be polled to quickly determine whether any of the input channels have changed state since the CPU last read the Data Registers. If bits 8-11 are zero, then no input channels have changed since the CPU last read the Data Registers and there is no need to read the Data Registers again. Polling the Extended Status Register instead of the Change Registers has two advantages. First, because the scanner is not stopped, it doesn't have to be restarted after the read. Secondly, Status Register reads are faster because the scanner does not have to be stopped before DTACK is asserted. It is therefore suggested that bits 8-11 of the Extended Status be polled instead of polling the Data or Change Registers directly.

It is not necessary to read the Change Registers at all if the user is not concerned about which individual bit in the change register is set. In these cases, the user would simply read the Data Registers when the module generated an interrupt (in interrupt driven environments) or when the status bits 8-11 indicate a change has occurred (in polled environments).

3.12 RESETTING THE MODULE

The module is reset by the assertion of the VMEbus reset signal. In response to-a reset, the module will do the following. All bits of the Extended Status and Control/Status Registers will be reset to zero. (Note that this resets all Interrupt Enable bits of the Status/Control Register so the VMEbus interrupt currently being generated by the XVME-212 will be negated, and the SYSFAIL* will be asserted on the VMEbus because bit 0 is reset to zero.) The scanner is stopped and the Data and Change Registers are reset to zero. After the reset signal is negated, the scanner will start scanning. Before the first scan, all Data and Change Registers will be zero. Therefore, after a reset, when an input channel is detected as on, its corresponding Change Register bit will be set.

Appendix A

XYCOM STANDARD I/O ARCHITECTURE

INTRODUCTION

The purpose of this appendix is to define XYCOM's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all programming for the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the XYCOM I/O Architecture are the following:

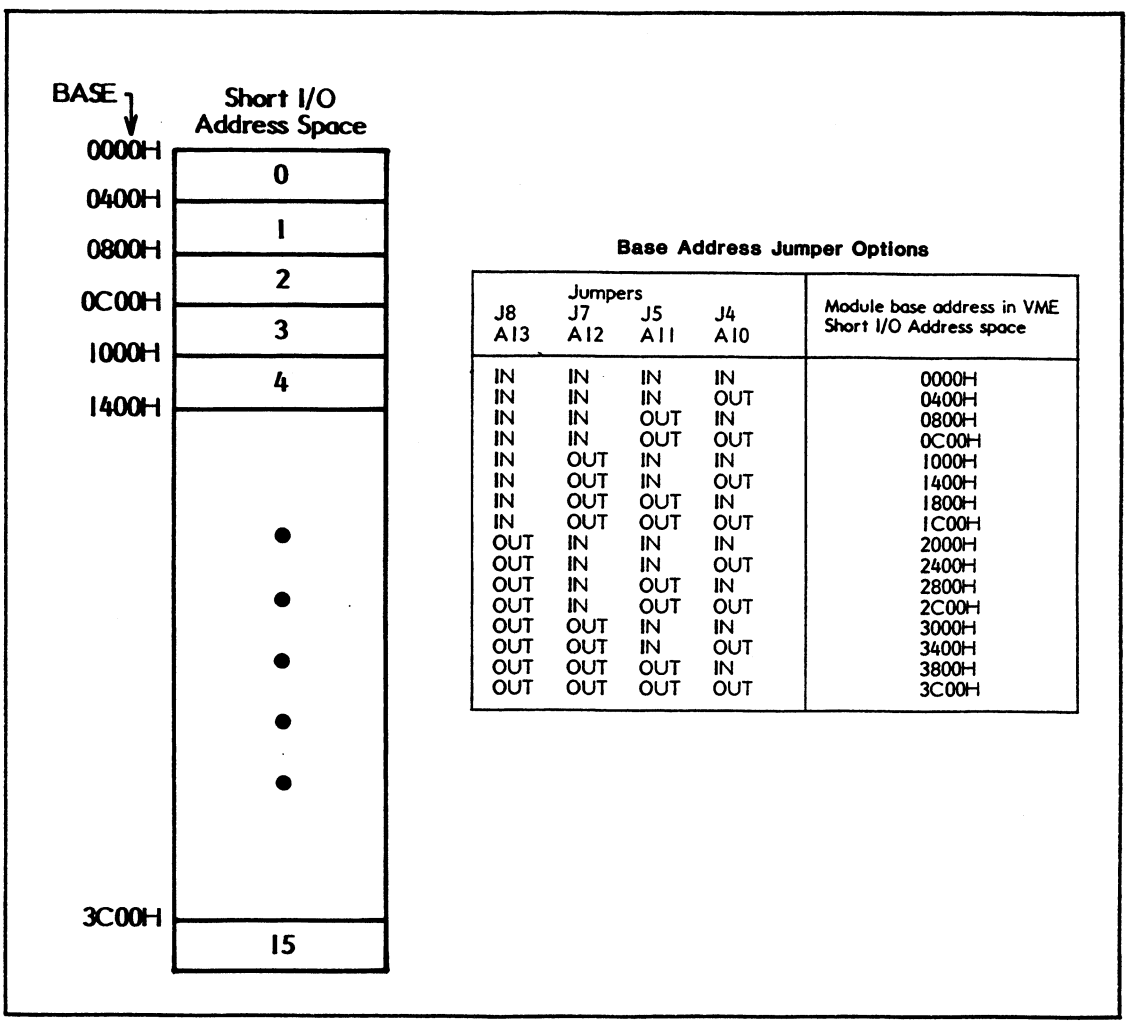
1. Module Addressing: Where a module is positioned in the I/O address space and how software can read from it or write to it
2. Module Identification: How software can identify which modules are installed in a system
3. Module Operational Status: How the operator can (through software) determine the operational condition of specific modules within the system
4. Interrupt Control: How software is able to control and monitor the capability of the module to interrupt the system
5. Communication between Modules: How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the modules
6. The I/O Kernel: How intelligent and non-intelligent "kernels" facilitate the operation of all XYCOM I/O modules

MODULE ADDRESSING

The XYCOM I/O Architecture Design Specification recommends that XVME modules should be addressed within the VMEbus-defined 64K short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while providing 64K of address space for I/O modules.

Base Addressing

Since each I/O module connected to the bus must have its own unique base address, the base-addressing scheme for XYCOM VME I/O modules has been designed to be jumper/switch selectable. Each XVME I/O module installed in the system requires at least a 1K-byte block of the short I/O Address Space. Thus, each I/O module has a base address which starts on a 1K boundary. As a result, the XYCOM I/O modules have all been implemented to decode base addresses in 1K (400H) increments. Figure A-1 shows an abbreviated view of the short I/O memory.



Base Address Jumper Options

Jumpers J8 A13	J7 A12	J5 A11	J4 A10	Module base address in VME Short I/O Address space
IN	IN	IN	IN	0000H
IN	IN	IN	OUT	0400H
IN	IN	OUT	IN	0800H
IN	IN	OUT	OUT	0C00H
IN	OUT	IN	IN	1000H
IN	OUT	IN	OUT	1400H
IN	OUT	OUT	IN	1800H
IN	OUT	OUT	OUT	1C00H
OUT	IN	IN	IN	2000H
OUT	IN	IN	OUT	2400H
OUT	IN	OUT	IN	2800H
OUT	IN	OUT	OUT	2C00H
OUT	OUT	IN	IN	3000H
OUT	OUT	IN	OUT	3400H
OUT	OUT	OUT	IN	3800H
OUT	OUT	OUT	OUT	3C00H

Figure A-1. 64K Short I/O Address Space
for Modules Occupying a 1K Block

Standardized Module I/O Map

The block of short I/O addresses (called the I/O Interface Block) allocated to each XVME module is mapped with a standardized format in order to simplify-programming and data access. The locations of frequently used registers and module-specific identification information are uniform.

For example, the module identification information is always found in the first 32 odd bytes of the module memory block. These addresses are associated with the jumpered base address (i.e., Module I.D. data address = base + odd bytes IH - 3H).

The byte located at base address + 81H on each module contains a Status/Control register which provides the results of diagnostics for verification of the module's operational condition.

The next area of the module I/O Interface Block (base address + 82H, up to FFFH) is module-specific, varying in size from one module to the next. It is in this area that the module holds specific I/O status, data, and pointer registers for use with IPC protocol.

All intelligent XVME I/O modules have an area of their I/O Interface Blocks defined as "dual access RAM." This area of memory provides the space where XVME "slave" I/O modules access their command blocks and where XVME "master" modules could access their command blocks (i.e., "master" modules can also access global system memory).

The remainder of the I/O Interface Block is then allocated to various module-specific tasks, registers, buffers, ports, etc.

Figure A-2 shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. This example shows an I/O Interface Block that occupies a 1K segment of short I/O Address Space. It should be noted that some modules (the XVME-164 MBMM for example) will occupy up to a 4K segment of short I/O Address Space. Notice that any location in the I/O Interface Block may be accessed by simply using the address formula:

Module Base Address + Relative Offset = Desired Location

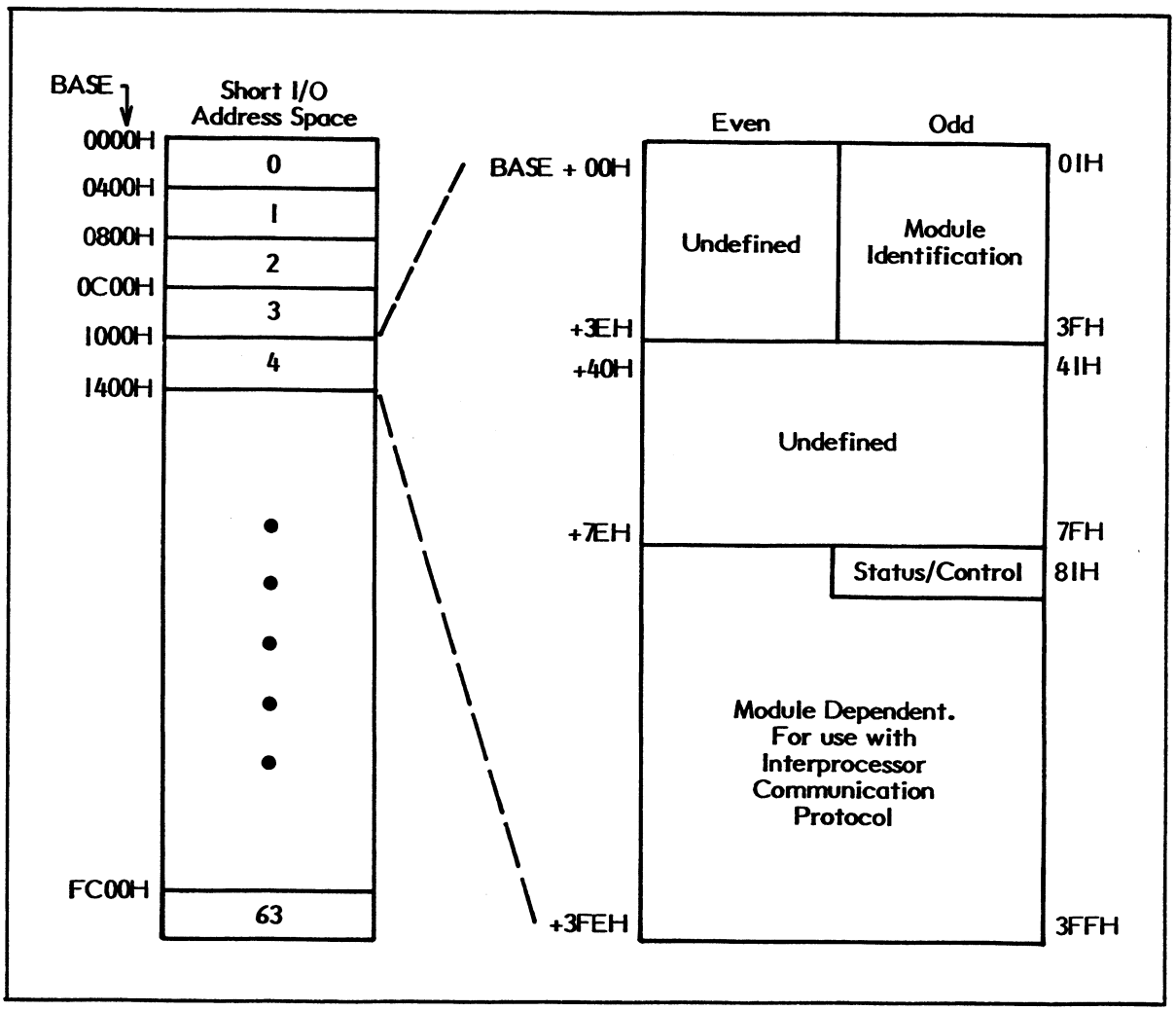


Figure A-2. XVME I/O Module Address Map

MODULE-SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module-specific information in an ASCII-encoded format. The I.D. data is provided as 32 ASCII-encoded characters consisting of board type, manufacturer identification, module model number, number of 1 Kbyte blocks occupied by the module, and model functional revision level information. This information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1 defines the identification information locations.

Table A-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier,
5	E	45	always "VMEID"
7	I	49	(5 characters)
9	D	44	
B	X	58	Manufacturer's I.D.,
D	Y	59	always "XYC" for XYCOM
F	C	43	modules (3 characters)
11	2	32	
13	1	31	Module Model Number
15	2	32	(3 characters and
17		20	4 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision
23	1	31	level with leading blank (if single digit)
25	1	30	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer
37	"		Dependent Information,
39	"		Reserved for future use
3B	"		
3D	"		
3F	"		

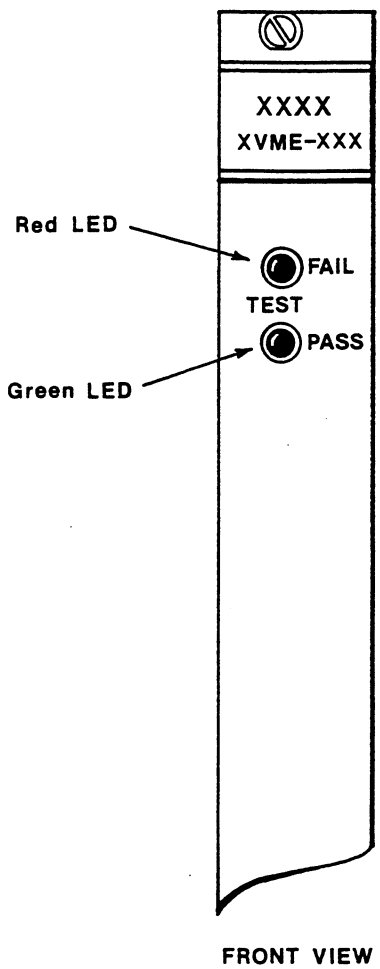
The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data has been assigned to the first 32 odd I/O Interface Block bytes (odd bytes 1H-3FH).

The I.D. information can be accessed by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H, and access to the module model number is wanted (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH): Add the offset address to each base address to read the hex-coded ASCII value at each location. In this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH (within the system's short I/O address space).

MODULE OPERATIONAL STATUS/CONTROL

All XVME intelligent I/O modules are designed to perform diagnostic self-tests on power-up or reset. For non-intelligent modules, the user must provide the diagnostic program. The self-test provision allows the user to verify the operational status of a module by either visually inspecting the two LEDs (which are mounted on the front panel, as in Figure A-3), or by reading the module status byte (located at module base address + 81H).

Figure A-3 shows the location of the status LEDs on the module front panel. The two tables included in the figure define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module passed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

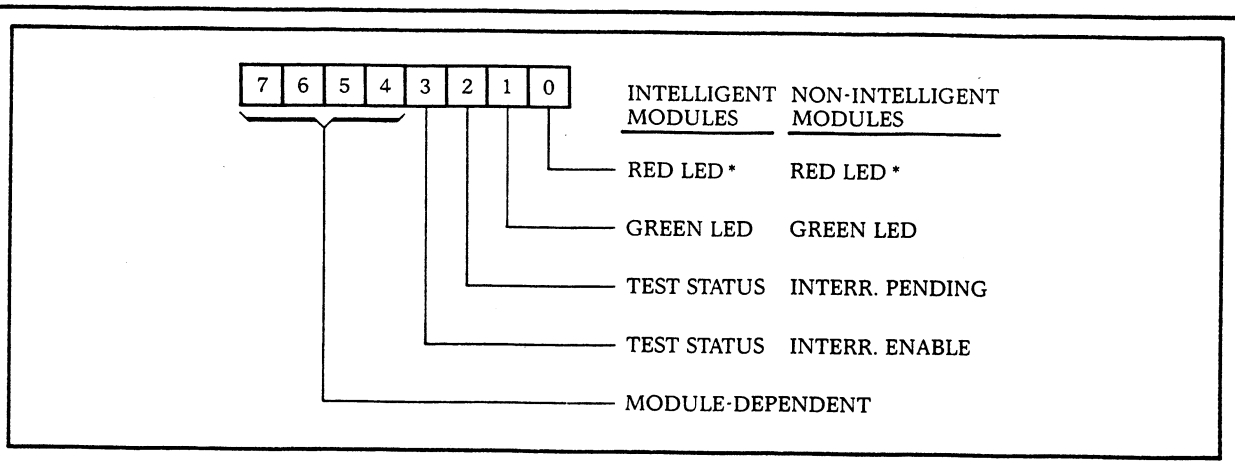
NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

The module status/control register (found at module base address + 8lH) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent modules is a "Read Only" register and it can be read by software to determine if the board is operating properly.

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module-generated interrupts. The LED status bits are "Read/Write" locations which provide the user with the indicators to accommodate diagnostic software. The Interrupt Enable bit is also a Read/Write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a "Read Only" bit indicating a module-generated pending interrupt.

Figure A-4 shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules
0	Read/Write - Red LED 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled
4	Module-dependent
5	Module-dependent
6	Module-dependent
7	Module-dependent

Bit	Intelligent Modules
0	Read Only - Red LED 0 = Red LED ON 1 = Red LED Off
1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2 & 3	Read Only - Test Status Indicators Bit 3 Bit 2 0 0 = Self-test not started 0 1 = Self-test in progress 1 0 = Self-test failed 1 1 = Self-test passed
4	Module-dependent
5	Module-dependent
6	Module-dependent
7	Module-dependent

Figure A-4. Status Register Bit Definitions

INTERRUPT CONTROL

Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status of pending on-board interrupts can also be read from this register. Interrupt control for intelligent modules **is** handled by the Interprocessor Communications Protocol.

Communications Between Processors

Communications between an intelligent 'master' and an intelligent 'slave" I/O module is governed by XYCOM's Interprocessor Communication (IPC) Protocol. This protocol involves use of 20-byte Command Block data structures -- located anywhere in the shared global RAM or dual-access RAM on an I/O module -- to exchange commands and data between a host processor and an I/O module.

THE KERNEL

To standardize its XVME I/O modules, XYCOM has designed them around "kernels' common from module to module. Each different module type consists of a standard kernel, combined with module-dependent application circuitry. Module standardization results in more efficient module design and allows the implementation of the Standard I/O Architecture. The biggest benefit of standardization for intelligent modules is that it allows the use of a common command language or protocol (Interprocessor Communication Protocol in this case).

The intelligent kernel is based around either a 68000 microprocessor or a 68B09 microprocessor (on the XVME-164 MBMM). This design provides the full complement of VMEbus Requester and Interrupter options for master/slave interfacing, as well as all of the advantages provided by the various facets of the XYCOM Standard I/O Architecture (as covered earlier in this appendix).

The non-intelligent kernel provides the circuitry required to receive and generate all of the signals for a VMEbus defined 16-bit 'slave" module. The non-intelligent kernel also employs the features of the XYCOM Standard I/O Architecture (as described earlier in this Appendix).

Appendix B

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-212 Processor Module is a double-high VMEbus compatible board. There is one 96-pin bus connector on the rear edge of the board labeled Pl (refer to Chapter 2, Figure 2-I for the location). The signals carried by connector PI are the standard address, data, and control signals required for a Pl backplane interface, as defined by the VMEbus specification. Table B-l identifies and defines the signals carried by the PI connector.

Table B-l. Pl - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	lB:3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	IA:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN and IACKOUT signals form a daisy-chained acknowledge. The IACKIN signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN and IACKOUT signals form a daisy-chained acknowledge. The IACKOUT signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 lB:16,17, 18,19 lC:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	lA:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.

Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A01-A23	1A:24-30 1C:15-30	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory 'address.
A24-A31	2B:4-11	ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B:1	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B:2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the DTB master if a higher level is requesting the bus.
BERR*	1C:11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*- BG3IN*	1B:4,6, 8,10	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*- BG3OUT*	1B:5,7, 9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.

Table B-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
BR0*-BR3*	lB:12-15	BUS REQUEST (O-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	lA:13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data buss lines (D00-D07).
DSI*	lA:12	DATA STROBE 1: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D0-D1 5).
DTACK*	lA:16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
DOO-D15	lA:l-8 lC:l-8	DATA BUS (bits 0-15): Three-state driven, b&directional data lines that provide a data path between the DTB master and slave.
GND	lA:9,11, 15,17,19, 1B:20,23, lC:9 2B:2,12, 22,3I	GROUND

Table B-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
IACK*	1 A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN in order to start the interrupt acknowledge daisy-chain.
IRQI*- IRQ7*	1B:24-30	INTERRUPT REQUEST (l-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	lC:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERV-ED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	lB:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	lA:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

Table B-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:lO	SYSTEM,FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	lC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5V	1 A:32 lB:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	1C:31	+12 VDC POWER: Used by system logic circuits.
-12v	lA:31	-12 VDC POWER: Used by system logic circuits.

Table B-l. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSFAIL*	1C:l0	SYSTEM,FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	IC:12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	lA:14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation, a low level indicates a write operation.
+5V STDBY	lB:31	+5 VDC STANDBY: This line supplies +5 VDC to devices requiring battery backup.
+5V	1 A:32 1B:32 1C:32 2B:1,13,32	+5 VDC POWER: Used by system logic circuits.
+12V	lC:31	+I2 VDC POWER: Used by system logic circuits.
-12V	lA:31	-12 VDC POWER: Used by system logic circuits.

BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

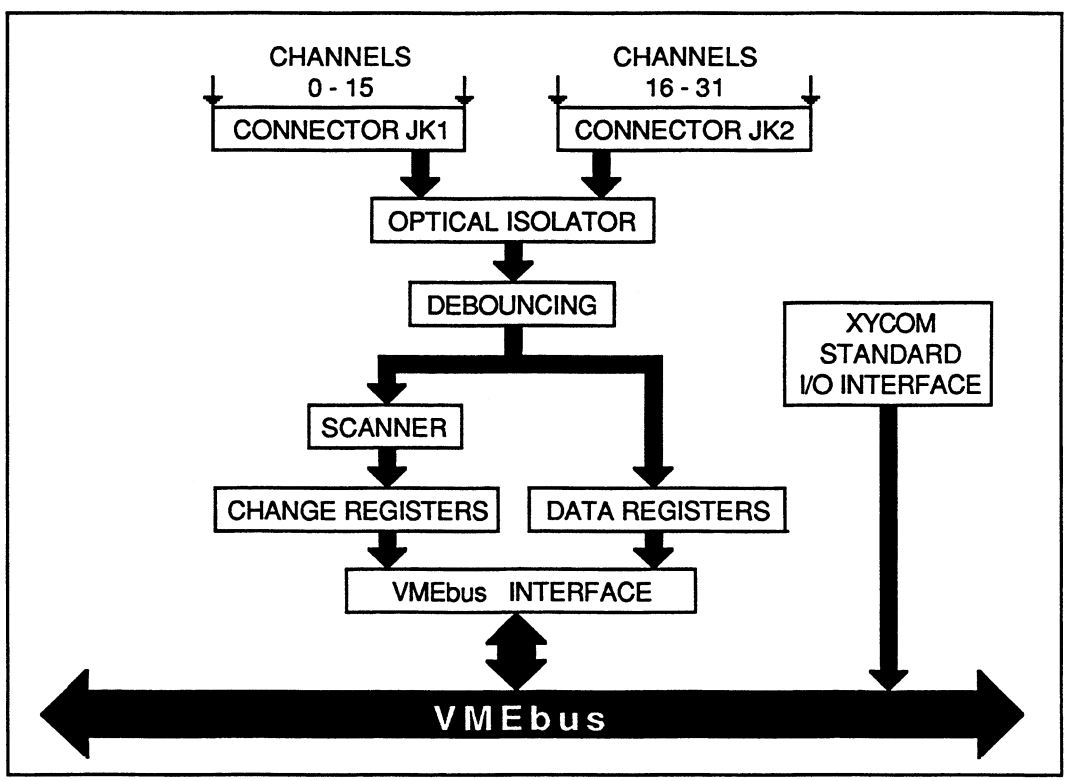
Table B-2. P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

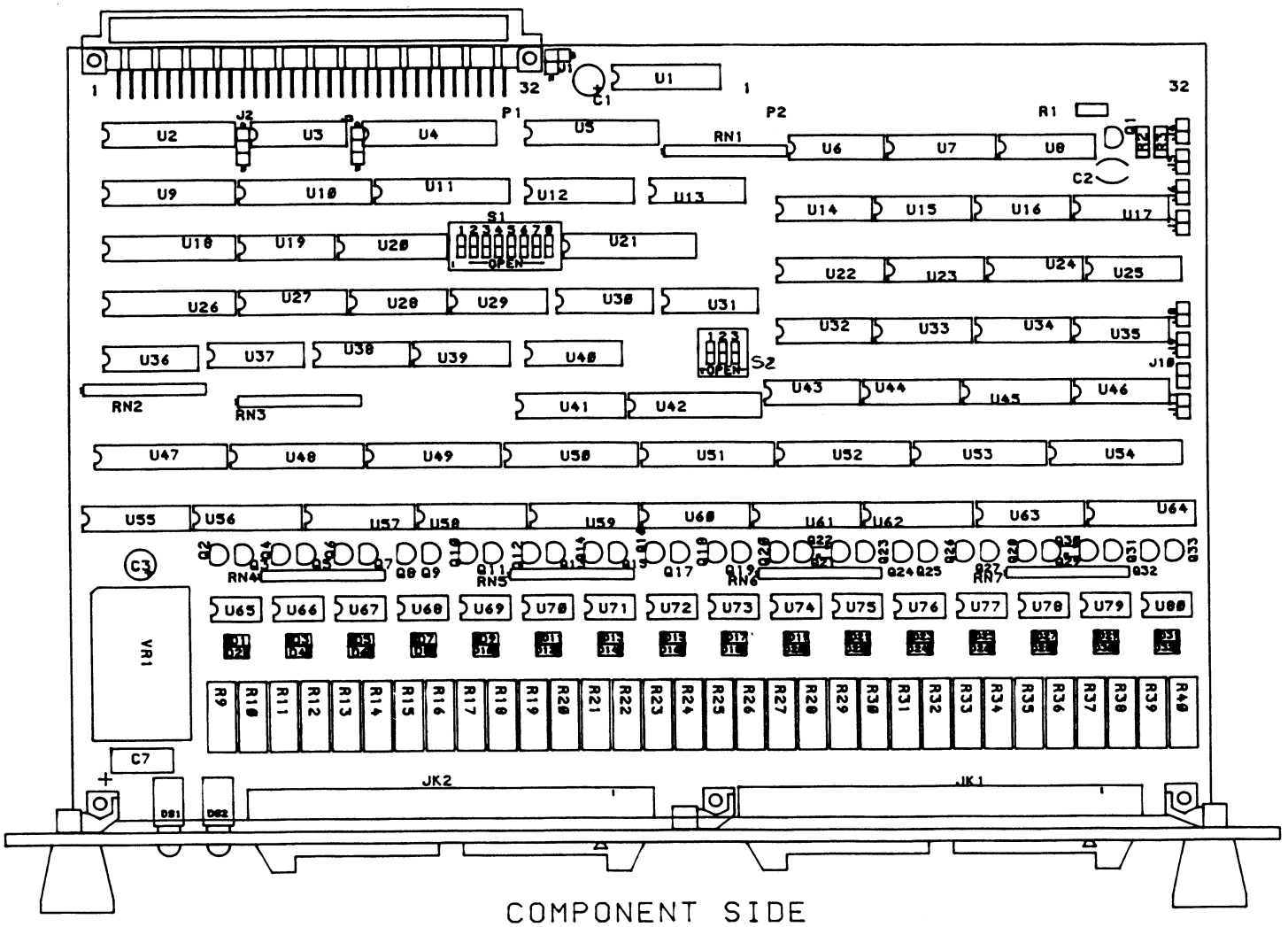
Appendix C

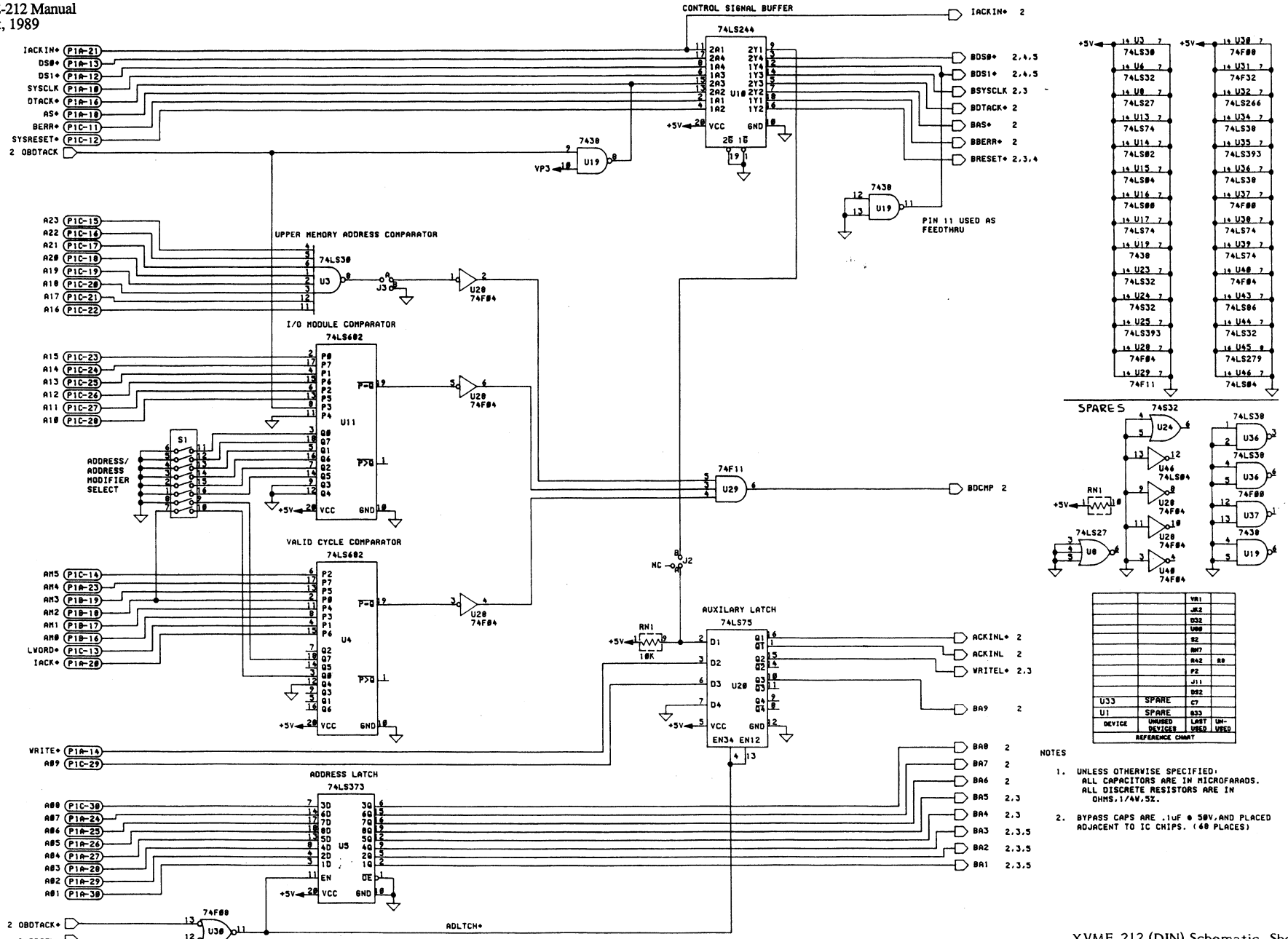
SCHEMATICS AND DIAGRAMS

Block Diagram

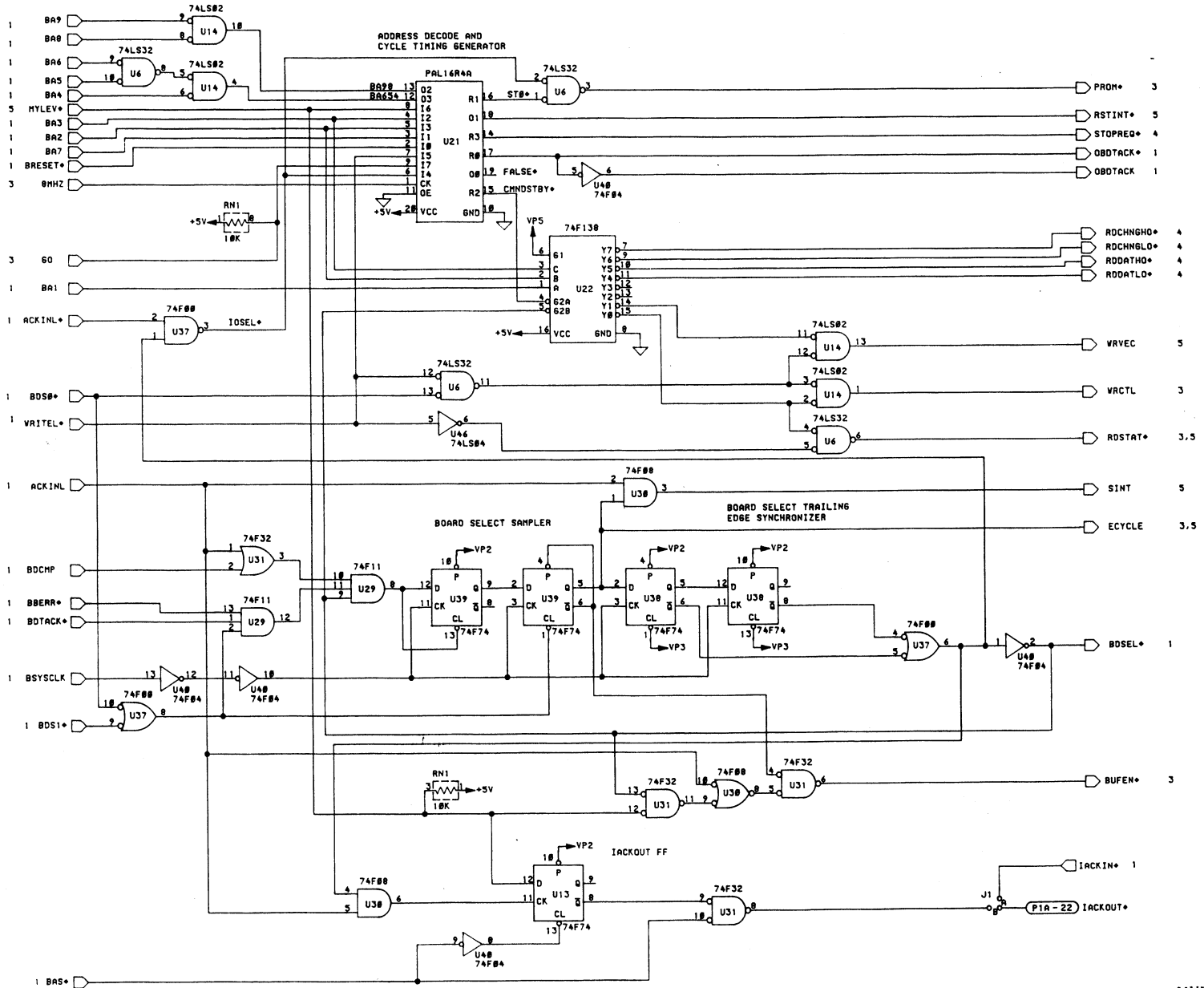


Assembly Drawing

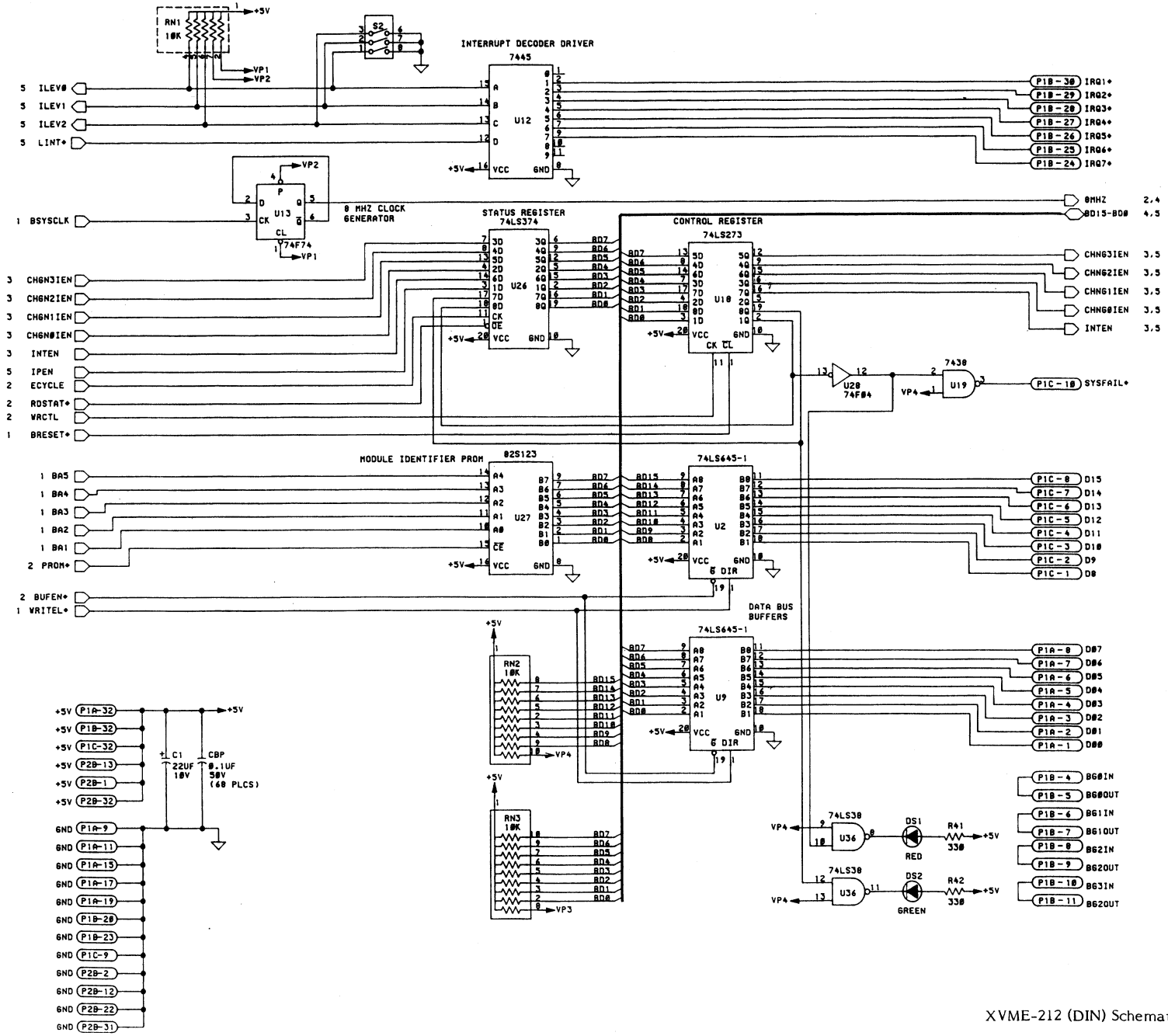




XVME-212 (DIN) Schematic, Sheet 1 of 7



XVME-212 (DIN) Schematic, Sheet 2 of 7


INTERRUPT DECODER DRIVER
7445
U12
STATUS REGISTER
74LS374
U26
CONTROL REGISTER
74LS273
U10
8 MHZ CLOCK GENERATOR
U13
74F74
MODULE IDENTIFIER PROM
82S123
U27
74LS645-1
U2
DATA BUS BUFFERS
U9
7438
U19
U20
74F04
74LS30
U36
RN1 10K
RN2 10K
RN3 10K
S2
C1 22UF 10V
CBP 0.1UF 50V (60 PLCS)
DS1
RED
DS2
GREEN
R41 330
R42 330
ILEV0
ILEV1
ILEV2
LINT*
BSYSCLK
CH6N3IEN
CH6N2IEN
CH6N1IEN
CH6N0IEN
INTEN
IPEN
ECYCLE
RDSTAT*
WRCTL
BRESET*
BA5
BA4
BA3
BA2
BA1
PROM*
BUFEN*
WRITEL*
IRQ1*
IRQ2*
IRQ3*
IRQ4*
IRQ5*
IRQ6*
IRQ7*
8MHZ
BD15-BD0
CHN3IEN
CHN2IEN
CHN1IEN
CHN0IEN
INTEN
SYSFAIL*
D15
D14
D13
D12
D11
D10
D9
D8
D07
D06
D05
D04
D03
D02
D01
D00
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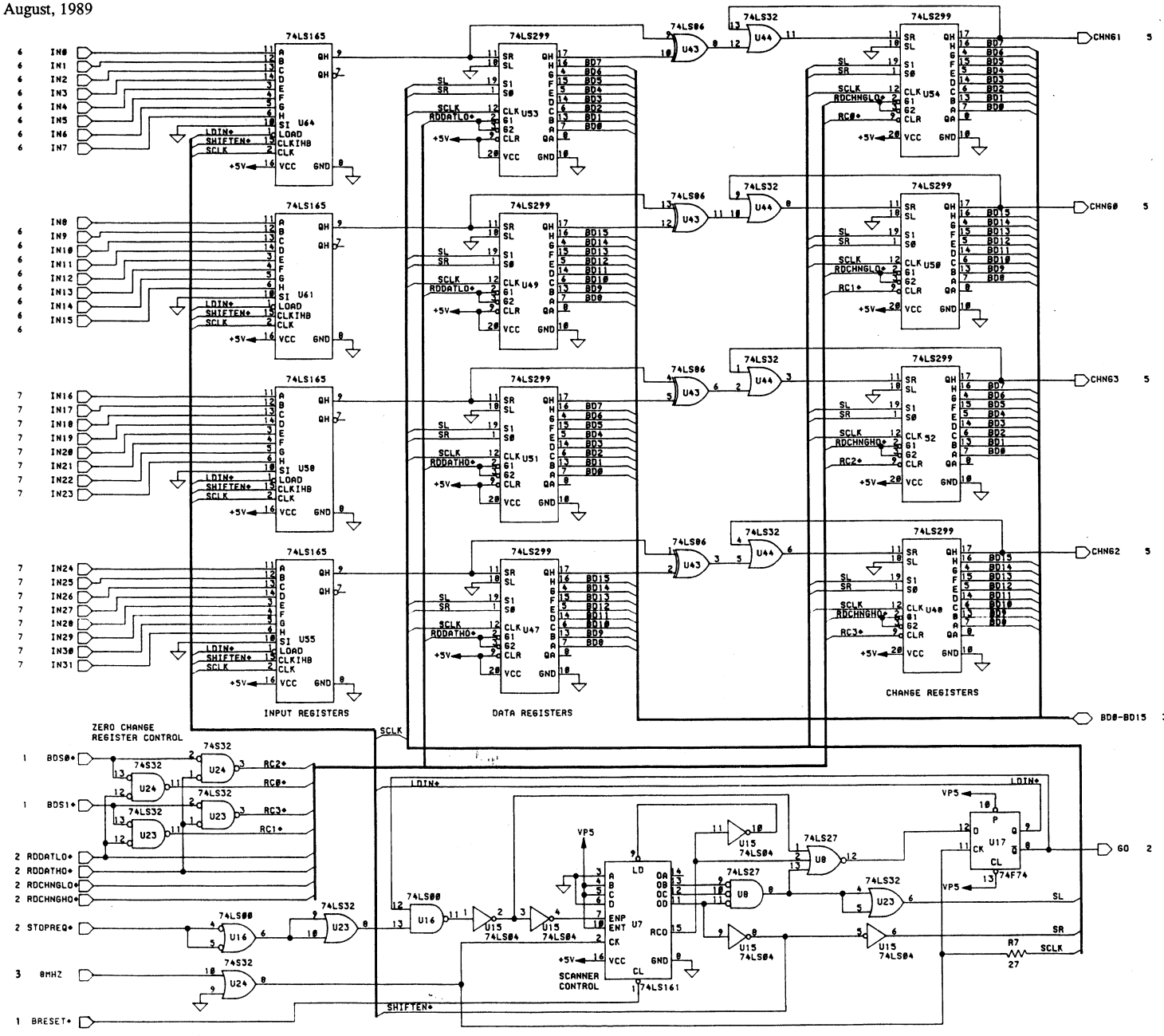
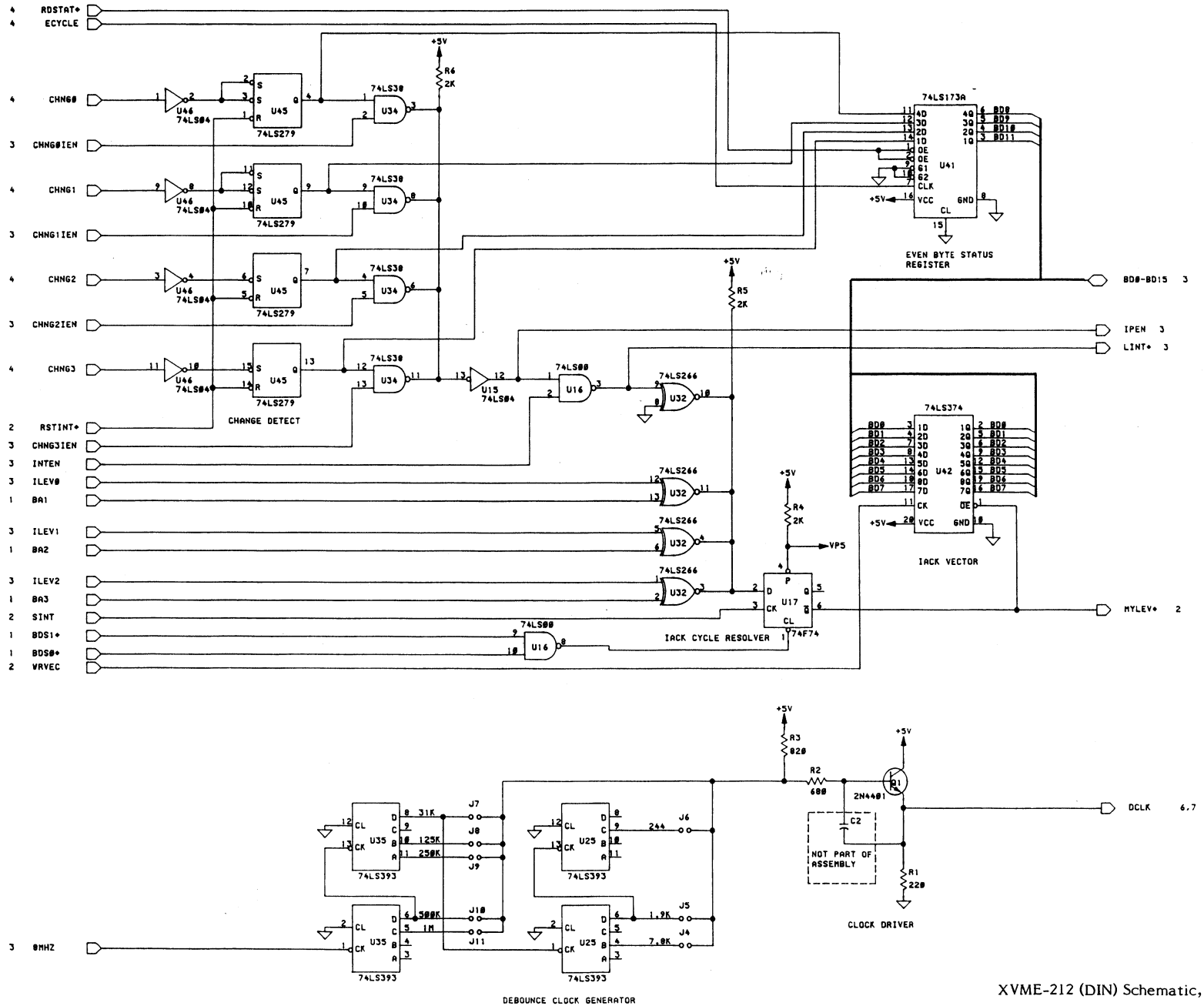
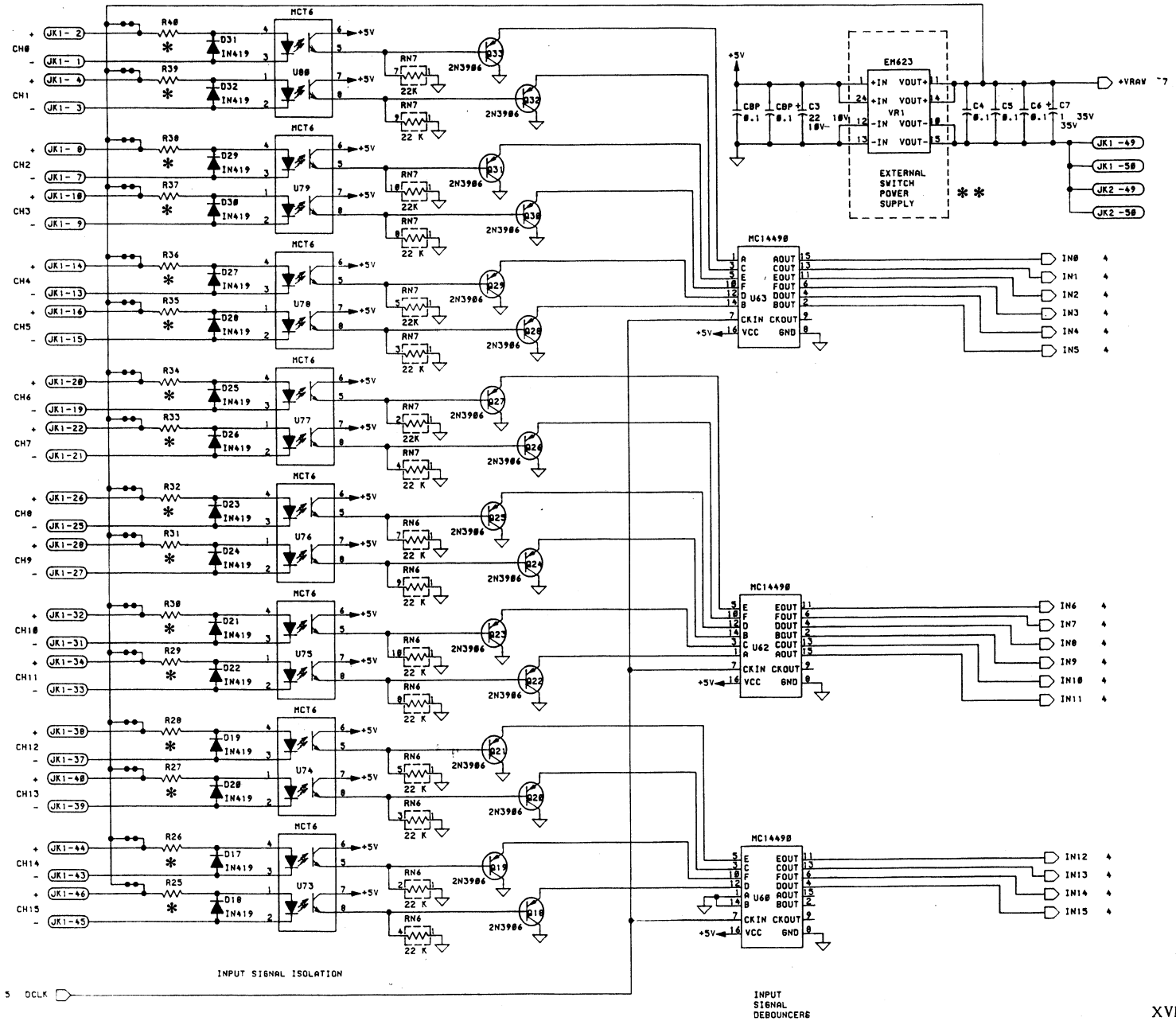
BG0OUT
BG1IN
BG1OUT
BG2IN
BG2OUT
BG3IN
BG3OUT
+5V
GND


INPUT REGISTERS
DATA REGISTERS
CHANGE REGISTERS
ZERO CHANGE REGISTER CONTROL
SCANNER CONTROL
CHN61
CHN60
CHN63
CHN62
BD0-BD15
GO
SCLK
LDIN*
SHIFTEN*
74LS165
74LS299
74LS32
74LS86
74LS27
74LS00
74LS04
74LS161
74F74



XVME-212 (DIN) Schematic, Sheet 5 of 7



* NOTE:

XVME-212/1-
Resistor values equal 3.9K Ω 1W

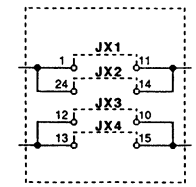
XVME-212/2-
Resistor values equal 330 Ω 1W

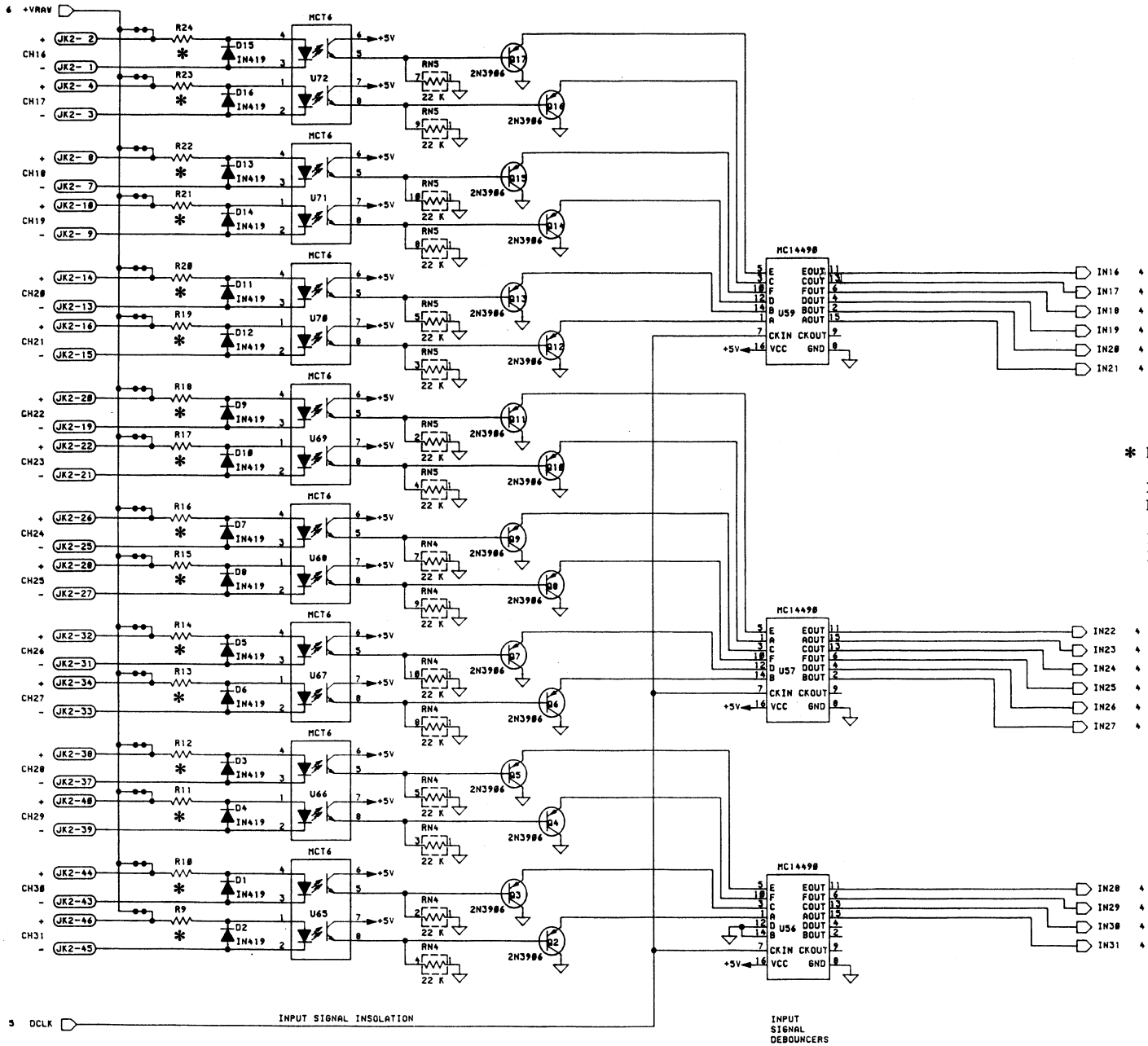
** NOTE 1:

XVME-212/1-
VR1 as shown

NOTE 2:

XVME-212/2-
VR1 not part of assembly, as shown below





* **NOTE:**

XVME-212/1-
Resistor values equal 3.9K Ω 1W

XVME-212/2-
Resistor values equal 330 Ω 1W

Appendix D

QUICK REFERENCE GUIDE

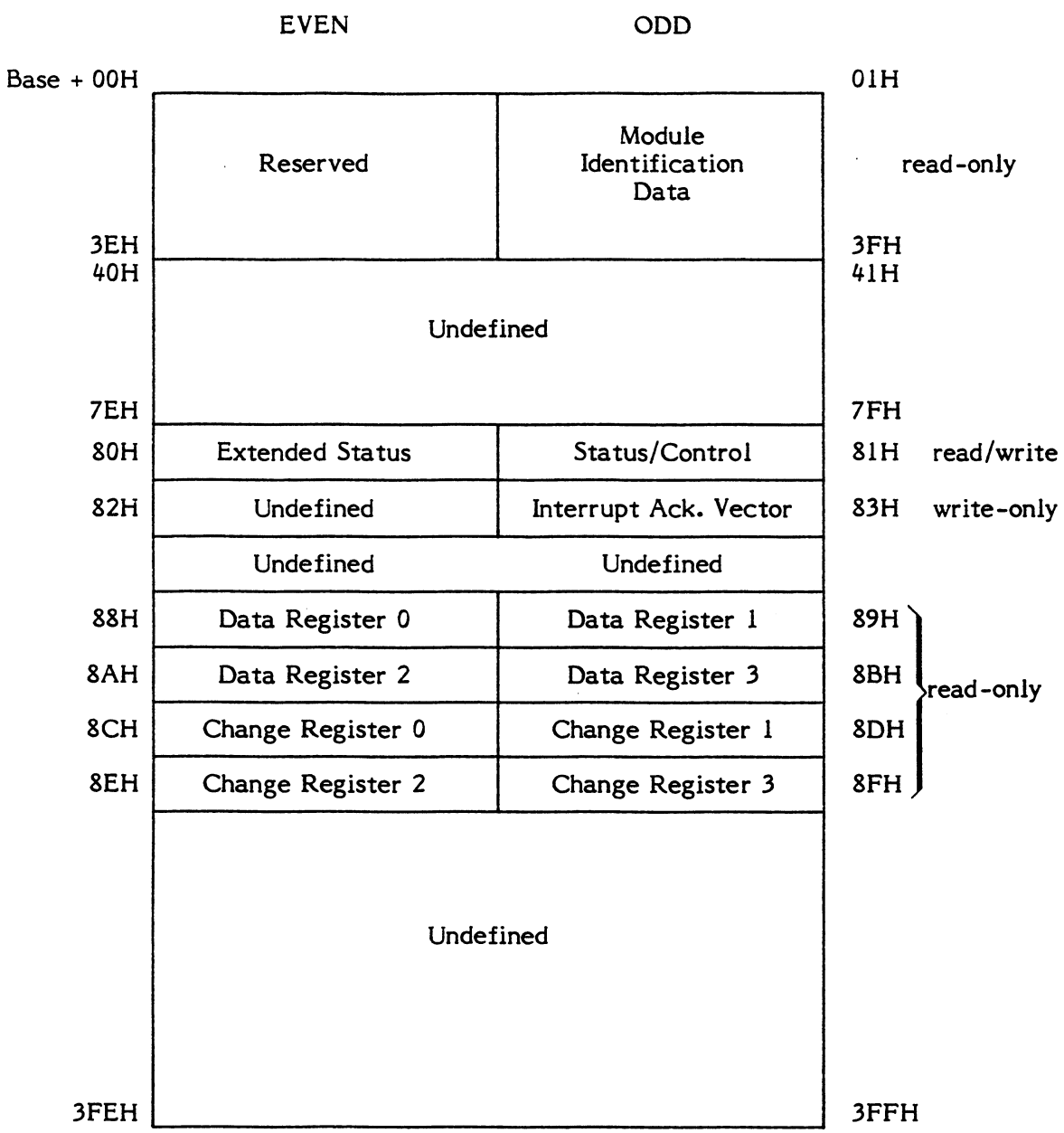


Figure D-1. XVME-212 I/O Interface Block and its Possible Locations in Short I/O Address Space

Table D-1. XVME-212 Jumper/Switch List

Address Switches (S1)

S1-8	Must be closed to select the Short I/O Address space.
S1-7	The XVME-212 will respond to one of the following AM codes, depending on the setting of this switch: OPEN = Supervisory or Non-Priveleged CLOSED = Supervisory only
S1-0 to S1-6	Sets the base address of the XVME-212: S1-6: A15 S1-5: A14 S1-4: A13 S1-3: A12 S1-2: A11 S1-1: A10

Open = Logic 1
Closed = Logic 0

Interrupt Level Switches (S2)

S2-3	S2-2	S2-1	VMEbus Interrupt Level
OPEN	OPEN	OPEN	7
OPEN	OPEN	CLOSED	6
OPEN	CLOSED	OPEN	5
OPEN	CLOSED	CLOSED	4
CLOSED	OPEN	OPEN	3
CLOSED	OPEN	CLOSED	2
CLOSED	CLOSED	OPEN	1
CLOSED	CLOSED	CLOSED	None; interrupts disabled

Jumpers / Use

Jumpers	Use
J1,J2	Use/bypass IACK daisy chain: J1 B, J2 B — Module uses IACK daisy chain J1 A, J2 A — Module bypasses chain
J3	Must be in "B" position to select the Short I/O Address space.
J4 - J11	These jumpers determine the debounce period:

		T min.	T max.
install only one	J11	3.5 us	4.5 us
	J10	7 us	9 us
	J9	14 us	18 us
	J8	28 us	36 us
	J7	112 us	144 us
	J5	448 us	576 us
	J4	1.8 ms	2.3 ms
	J6	14 ms	18 ms