MOTOROLA
Semiconductor Products Sector

Order Number: MPC857TUMAD/D
Rev. 0, 6/2001

PowerPC™

Errata to
MPC857T PowerQUICC™ User's Manual Rev. 0

This errata describes corrections to revision 0 of the *MPC857T PowerQUICC User's Manual* (order number: MPC857TUMAD/D, Rev. 0).

Digital DNA From Motorola

Section #/Page #	Changes

10.10.1, 10-28 In Figure 10-24, the reset value of the RTCSC should be replaced with the following:

0000_0000_000x_00xx.

11.1.3.1, 11-3 Add the following note:

NOTE:

The PLL loss of lock detection does not have a specification for the detection threshold. Therefore it should used solely as a debug tool and not in production systems. Characterization of the threshold value over temperature and operating voltages has shown that the threshold can be triggered when clock out to clock in phase differences is 1.8 ns. or more.

11.3.1.1, 11-9 Add BBE (boot burst enable) to bit 2, and CLES (core little endian swap) to bit 15 of Figure 11-8 and add the following description to Table 11-3:

Table 11-3. Hard Reset Configuration Word Field Descriptions

Bits	Name	Description
2	BBE	Boot Burst Enable 0 The boot device does not support bursting. 1 The boot device does support bursting.
15	CLES	Core Little Endian Swap. Defines core access operation following reset. 0 Big Endian 1 Little Endian

12.1, global Table 12-1. Add the following signals:

B7 M_CRS

H18 M_MDIO

V15 M_TXEN

H4 M_COL

W15 M_TX_CLK

For a complete listing of VDDL, VDDH, and GND, see the document MPC857T Family Hardware Specifications (MPC857TEC/D). The information provided in the Hardware Specification supersedes all information found in the MPC857T UM.

Section #/Page #	Changes

14.2.2.3, 14-8 Replace Table 14-2 with the following:

Table 14-2. XFC Capacitor Values Based on PLPRCR[MF]

MF Range	Minimum Capacitance	Recommended Capacitance	Maximum Capacitance	Unit
1 ≤ (MF+1) ≤ 4	XFC = [(MF+1) x 580] - 100	XFC = [(MF+1) x 680] - 120	XFC = [(MF+1) x 780] - 140	pF
(MF+1) > 4	XFC = (MF+1) x 830	XFC = (MF+1) X 1100	XFC = (MF+1) x 1470	pF

15.4.1,15-9 In Figure 16-5, replace the reset values of BRx with the following:

xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xx00_0000.

In Figure 16-6, replace the reset values of the first five nibbles of BR0 with xxxx_xxxx_xxxx_xxxx_xxxx, and add the following footnote:

> Since the base address values are unknown at reset, to ensure proper operation, program the base address before programming the Option Register.

15.4.2, 15-11 In Figure 16-7, replace the reset values of ORx with the following:

xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxx0.

Replace the text after Figure 16-7 with the following:

> At reset, OR0 has specific default values and is read-only, as shown in Figure 15-8. After reset, OR0 becomes R/W.

15.4.4, 15-14 In Figure 16-10, replace the reset values of the first two nibbles of MxMR with the following:

xxxx_xxxx

15.4.5, 15-15 In Figure 16-11, replace the reset values of the MCR with the following:

xx00_0000_x000_0000_xxx0_xxxx_00xx_xxxx.

15.4.6, 15-16 In Figure 16-12, replace the reset values of the MDR with the following:

xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx.

15.4.7, 15-17 In Figure 16-13, replace the reset values of the MAR with the following:

xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx_xxxx.

16.4, 16-8 Replace sections 16.4, and16.4.1 through 16.4.3 with the following:

16.4 Programming Model

This section describes the PCMCIA interface programming model. Generally, all registers are memory-mapped within the internal control register area. The registers in Table 16-7 control the PCMCIA interface.

Table 16-7 PCMCIA Registers

Name	Description
PIPR	PCMCIA interface input pins register
PSCR	PCMCIA interface status changed register
PER	PCMCIA interface enable register
PGCRA	PCMCIA interface general control register a
PGCRB	PCMCIA interface general control register b
PBR[0–7]	PCMCIA base registers 0–7 (per window)
POR[0–7]	PCMCIA option registers 0–7 (per window)

16.4.1 PCMCIA Interface Input Pins Register (PIPR)

Status of inputs from the PCMCIA card to the host (BVD, CD, RDY, VS) is reported to the PIPR, shown in Figure 16-3. PIPR is a read-only register; write operations are ignored.

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	CAVS1	CAVS2	CAWP	CACD2	CACD1	CABVD2	CABVD1	CARDY	—							
Reset	Undefined															
R/W	R															
Addr	(IMMR & 0xFFFF0000) + 0x0F0															
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	CBVS1	CBVS2	CBWP	CBCD2	CBCD1	CBBVD2	CBBVD1	CBRDY	—							
Reset	Undefined															
R/W	R															
Addr	(IMMR & 0xFFFF0000) + 0x0F2															

Figure 16-3. PCMCIA Interface Input Pins Register (PIPR)

Table 16-8 describes PIPR fields.

Table 16-8. PIPR Field Descriptions

Bits	Name	Description
0	CAVS1	Voltage sense 1 for card A
1	CAVS2	Voltage sense 2 for card A
2	CAWP	Write protect for card A
3	CACD2	Card detect 2 for card A
4	CACD1	Card detect 1 for card A
5	CABVD2	Battery voltage/$\overline{\text{SPKR\_A}}$ input for card A
6	CABVD1	Battery voltage/$\overline{\text{STSCHG\_A}}$ input for card A
7	CARDY	RDY/$\overline{\text{IRQ}}$ of card A pin
8–15	—	Reserved, should be cleared.
16	CBVS1	Voltage sense 1 for card B
17	CBVS2	Voltage sense 2 for card B
18	CBWP	Write protect for card B
19	CBCD2	Card detect 2 for card B
20	CBCD1	Card detect 1 for card B
21	CBBVD2	Battery voltage/$\overline{\text{SPKR\_B}}$ input for card B
22	CBBVD1	Battery voltage/$\overline{\text{STSCHG\_B}}$ input for card B
23	CBRDY	RDY/$\overline{\text{IRQ}}$ of card B pin
24–31	—	Reserved, should be cleared.

16.4.2 PCMCIA Interface Status Changed Register (PSCR)

The contents of PSCR, shown in Figure 16-4, are logically ANDed with the PER to generate a PCMCIA interface interrupt. Writing zeros has no effect; writing ones clears the corresponding interrupt state.

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12–15
Field	CAVS1_C	CAVS2_C	CAWP_C	CACD2_C	CACD1_C	CABVD2_C	CABVD1_C	—	CARDY_L	CARDY_H	CARDY_R	CARDY_F	—
Reset	Undefined												
R/W	R/W												
Addr	(IMMR & 0xFFFF0000) + 0x0E8												
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28–31
Field	CBVS1_C	CBVS2_C	CBWP_C	CBCD2_C	CBCD1_C	CBBVD2_C	CBBVD1_C	—	CBRDY_L	CBRDY_H	CBRDY_R	CBRDY_F	—
Reset	Undefined												
R/W	R/W												
Addr	(IMMR & 0xFFFF0000) + 0x0EA												

Figure 16-4. PCMCIA Interface Status Changed Register (PSCR)

Table 16-9 describes PSCR fields.

Table 16-9. PSCR Field Descriptions

Bits	Name	Description
0	CAVS1_C	Voltage sense 1 for card A changed
1	CAVS2_C	Voltage sense 2 for card A changed
2	CAWP_C	Write protect for card A changed
3	CACD2_C	Card detect 2 for card A changed
4	CACD1_C	Card detect 1 for card A changed
5	CABVD2_C	Battery voltage/$\overline{\text{SPKR\_A}}$ input for card A changed
6	CABVD1_C	Battery voltage/$\overline{\text{STSCHG\_A}}$ input for card A changed
7	—	Reserved, should be cleared.
8	CARDY_L	RDY/$\overline{\text{IRQ}}$ of card A pin is low. Device and socket interrupt.
9	CARDY_H	RDY/$\overline{\text{IRQ}}$ of card A pin is high. Device and socket interrupt.
10	CARDY_R	RDY/$\overline{\text{IRQ}}$ of card A pin rising edge detected. Device and socket interrupt.
11	CARDY_F	RDY/$\overline{\text{IRQ}}$ of card A pin falling edge detected. Device and socket interrupt.
12–15	—	Reserved, should be cleared.
16	CBVS1_C	Voltage sense 1 for card B changed
17	CBVS2_C	Voltage sense 2 for card B changed
18	CBWP_C	Write Protect for card B changed
19	CBCD2_C	Card detect 2 for card B changed
20	CBCD1_C	Card detect 1 for card B changed
21	CBBVD2_C	Battery voltage/$\overline{\text{SPKR\_B}}$ input for card B changed
22	CBBVD1_C	Battery voltage/$\overline{\text{STSCHG\_B}}$ input for card B changed
23	—	Reserved, should be cleared.

Table 16-9. PSCR Field Descriptions (Continued)

Bits	Name	Description
24	CBRDY_L	RDY/$\overline{\text{IRQ}}$ of card B pin is low. Device and socket interrupt.
25	CBRDY_H	RDY/$\overline{\text{IRQ}}$ of card B pin is high. Device and socket interrupt.
26	CBRDY_R	RDY/$\overline{\text{IRQ}}$ of card B pin rising edge detected. Device and socket interrupt.
27	CBRDY_F	RDY/$\overline{\text{IRQ}}$ of card B pin falling edge detected. Device and socket interrupt.
28–31	—	Reserved, should be cleared.

16.4.3 PCMCIA Interface Enable Register (PER)

Setting a bit in the PER, shown in Figure 16-5, enables the corresponding interrupt.

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12-15
Field	CA_EVS1	CA_EVS2	CA_EWP	CA_ECD2	CA_ECD1	CA_EBVD2	CA_EBVD1	—	CA_ERDY_L	CA_ERDY_H	CA_ERDY_R	CA_ERDY_F	—
Reset	0000_0000_0000_0000												
R/W	R/W												
Addr	(IMMR & 0xFFFF0000) + 0x0F8												
Bit	16	17	18	19	20	21	22	23	24	25	26	27	28-31
Field	CB_EVS1	CB_EVS2	CB_EWP	CB_ECD2	CB_ECD1	CB_EBVD2	CB_EBVD1	—	CB_ERDY_L	CB_ERDY_H	CB_ERDY_R	CB_ERDY_F	—
Reset	0000_0000_0000_0000												
R/W	R/W												
Addr	(IMMR & 0xFFFF0000) + 0x0FA												

Figure 16-5. PCMCIA Interface Enable Register (PER)

Table 16-10 describes PER fields.

Table 16-10. PER Field Descriptions

Bits	Name	Description
0	CA_EVS1	Enable for voltage sense 1 for card A changed. Setting this bit enables the interrupt on any signal change.
1	CA_EVS2	Enable for voltage sense 2 for card A changed. Setting this bit enables the interrupt on any signal change.
2	CA_EWP	Enable for write protect for card A changed. Setting this bit enables the interrupt on any signal change.
3	CA_ECD2	Enable for card detect 2 for card A changed. Setting this bit enables the interrupt on any signal change.
4	CA_ECD1	Enable for card detect 1 for card A changed. Setting this bit enables the interrupt on any signal change.

Table 16-10. PER Field Descriptions (Continued)

Bits	Name	Description
5	CA_EBVD2	Enable for battery voltage/$\overline{\text{SPKR\_A}}$ input for card A changed. Setting this bit enables the interrupt on any signal change.
6	CA_EBVD1	Enable for battery voltage/$\overline{\text{STSCHG\_A}}$ input for card A changed.
7	—	Reserved, should be 0.
8	CA_ERDY_L	Enable for RDY/$\overline{\text{IRQ}}$ of card A pin is low
9	CA_ERDY_H	Enable for RDY/$\overline{\text{IRQ}}$ card A pin is high
10	CA_ERDY_R	Enable for RDY/$\overline{\text{IRQ}}$ card A pin rising edge detected
11	CA_ERDY_F	Enable for RDY/$\overline{\text{IRQ}}$ card A pin falling edge detected
12–15	—	Reserved, should be 0.
16	CB_EVS1	Enable for voltage sense 1 for card B changed. Setting this bit enables the interrupt on any signal change.
17	CB_EVS2	Enable for voltage sense 2 for card B changed. Setting this bit enables the interrupt on any signal change.
18	CB_EWP	Enable for write protect for card B changed. Setting this bit enables the interrupt on any signal change.
19	CB_ECD2	Enable for card detect 2 for card B changed. Setting this bit enables the interrupt on any signal change.
20	CB_ECD1	Enable for card detect 1 for card B changed. Setting this bit enables the interrupt on any signal change.
21	CB_EBVD2	Enable for battery voltage/$\overline{\text{SPKR\_B}}$ input for card B changed. Setting this bit enables the interrupt on any signal change.
22	CB_EBVD1	Enable for battery voltage/$\overline{\text{STSCHG\_B}}$ input for card B changed
23	—	Reserved, should be 0.
24	CB_ERDY_L	Enable for RDY/$\overline{\text{IRQ}}$ of card B pin is low
25	CB_ERDY_H	Enable for RDY/$\overline{\text{IRQ}}$ card B pin is high
26	CB_ERDY_R	Enable for RDY/$\overline{\text{IRQ}}$ card B pin rising edge detected
27	CB_ERDY_F	Enable for RDY/$\overline{\text{IRQ}}$ card B pin falling edge detected
28–31	—	Reserved, should be 0.

33.5.1.3, 33-21 The final sentence in this section should be replaced with the following:

> The Fast Ethernet Controller is described in Part VII, Chapter 43, “Fast Ethernet Controller (FEC).”

35, 35-1 Remove this sentence:

> When not in ESAR mode, the MPC857T remains backwards compatible to the classic SAR ATM operation of the MPC860SAR.

Section #/Page #	Changes
42.1,42-1	Remove this from the feature list: Back compatible with MPC860SAR UTOPIA muxed bus.
Ch. 43, global	FEC (Fast Ethernet Controller) R_FSTART should show bits 16-31 as address 0xED2 X_WMRK should show bits 0-15 as address 0xEE4 X_WMRK should show bits 16-31 as address 0xEE6 R_CNTRL should show bits 0-15 as address 0xF44 R_CNTRL should show bits 16-31 as address 0xF46

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