QSEVEN Design Guide

For Designing QSEVEN Carrier boards

Revision 2.0

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Revision History

Rev.	Date	Author	Changes
0.1	2009/3/1	Darwin	Initial Release
2.0	2014/08/20	Ian	Update to Rev. 2,0, Update PQ7-M106 Design info Update Input Power Sequencing info

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1. Q$_{SEVEN}$™ Specification

PQ7 series Specification defines requirements for highly integrated compact moduleswith standard I/O interfaces and connections. Key capabilities defined in the PQ7 specification include support for:

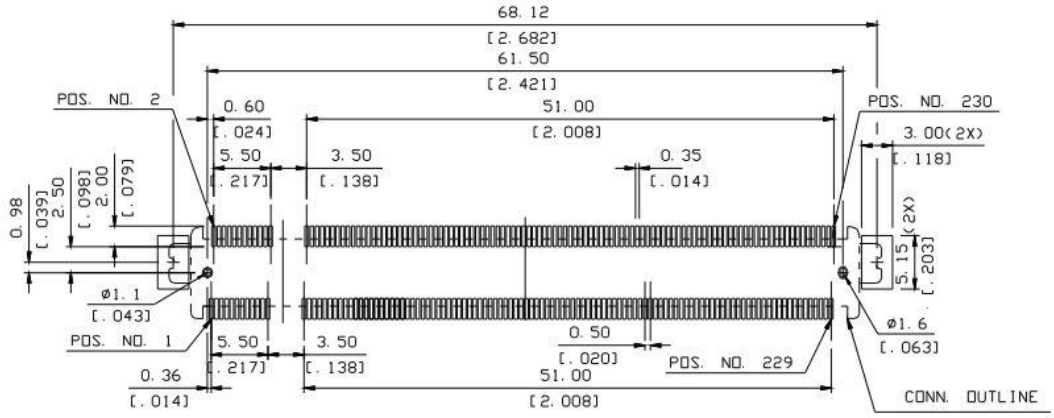
- PCI Express
- Serial ATA
- USB 2.0
- USB 3.0
- DisplayPort™, TMDS
- Secure Digital I/O interface
- LPC interface
- Gigabit Ethernet
- LVDS Display Interface
- High Definition Digital Audio (HDA)
- Intergrated Interchip Sound (I2S)

PQ7 series have a standardized form factor of 70mm x 70mm and have specified pin outs based on the high speed MXM system connector.

2. Q$_{SEVEN}$™ Connector

PQ7 series utilizes a 230-pin card-edge connector. The MXM connector accommodates various connector heights for different carrier board application needs.
This specification suggests two connector heights, 7.8mm and 7.5mm.

Figure 2-1 MXM connector.



The connectors mentioned in Table 2-1 are only a partial list of what is offered by the manufacturers.

Table 2-1 MXM Connector.

Manufacturer	Part Number	Specification	Resulting height between carrier board and Qseven® module	Overall height of the MXM Connector
Aces	88882-2Dxx	88882-2Dxx	5.0mm	7.5mm
Yamaichi	BEC05230S9xFREDC	BEC05230S9xFREDC	5.0 mm	7.8 mm
Foxconn	AS0B32x-S78N-xH	AS0B32x-S78N-xH	5.0 mm	7.8 mm

The components located on the top side of the module are up to 5.5mm high. The bottom components have a maximum height of 2.5mm while the standard distance between the standard MXM connector on the carrier board and the PQ7 series module is 2.7mm. When using the standard MXM connector, with an overall height of 5.5mm, carrier board component placement below the PQ7 series module is not permitted.

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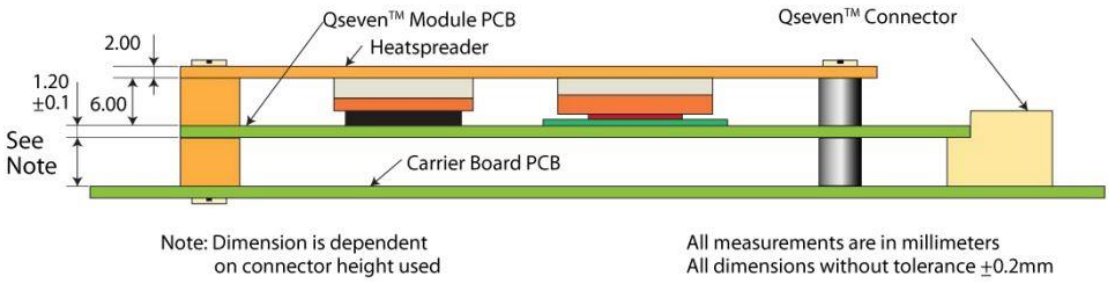
If it is necessary to place carrier board components below the PQ7 series module, then a MXM connector with an overall height of 7.8mm must be used and no carrier board component can exceed a maximum height of 2.5mm.

The heatspreader offered for PQ7 series modules acts as a thermal coupling device and is not heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heat spreader. The dissipation of heat will fluctuate between different CPU boards. Refer to the PQ7 series module user's manual for heat spreader dimensions and specifications.

The standoff for the heat spreader and carrier board must not exceed 5.6 mm overall external diameters. It ensures that the standoff contact-area does not exceed the defined mounting hole footprint on the PQ7 series module. The screw that is to be used for mounting must be a metric thread M2.5 DIN7985 / ISO7045.
PQ7 series modules are defined to feature ultra low power CPU and chipset solutions with an ultra low "Thermal Design Power" (TDP). The modules power consumption not exceeds 12W.

Figure 2-2 Overall Height including Heat-spreader of the Qseven® Module.



3. QSEVEN™ Feature Overview

The Qseven mandatory and optional feature as Table 3-1 shows the minimum、maximum and PQ7 series configuration of the feature set.

Table 3-1 QSEVEN™ Supported Features.

System I/O Interface	ARM/RISC Based Minimum Configuration	X86 Based Maximum Configuration	M100 Series Configuration
PCI Express	0	1 (x1 link)	4
Serial ATA	0	0	2
USB 2.0 ports	3	4	8
USB 3.0 ports	0	0	2
LVDS channels embadded	0 0	0 0	Dual Channel 24bits
DisplayPort TMDS	0	0	1
High Definition Audio / AC'97 /	1	0	1
Ethernet 10/100 Mbit/Gigabit	0	0	1 (Gigabit Ethernet)
UART	0	0	1
Low Pin Count	0	0	1
Secure Digital I/O 8-bit for SD/MMC	0	0	1
System	0	1	1
I2C Bus	1	1	1
SPI Bus	0	0	1
CAN Bus	0	0	1
Watchdog Trigger	1	1	1
Power Button	1	1	1
Power Good	1	1	1
Reset Button	1	1	1
LID Button	0	0	1
Sleep Button	0	0	1
Suspend To	0	0	1
Wake	0	0	1
Battery low alarm	0	0	1
Thermal control	0	0	1
FAN control	0	0	1

Note: Please refer to PQ7 series modules' user manual for detail information.

4. Q$_{SEVEN}$™ Connector Pin out

Figure 4-1 Connectors Pin out Description.

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Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	LPC_AD0
9	GBE_LINK1000#	10	GBE_LINK1000#
11	GBE_MDI1-	12	GBE_MDI0-
13	GBE_MDI1+	14	GBE_MDI0+
15	GBE_LINK#	16	SUS_S5#
17	GBE_CTREF	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	RSVD
57	GND	58	GND
59	HAD_SYNC / I2S_WS	60	SMB_CLK / GP1_I2C_CLK
61	HAD_RST# / I2S_RST#	62	SMB_DAT / GP1_I2C_DAT
63	HAD_BITCLK# / I2S_CLK	64	SMB_ALERT#
65	HAD_SDI / I2S_SDI	66	GP0_I2C_CLK
67	HAD_SDO / I2S_SDO	68	GP0_I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7- / USB_SSTX0-	76	USB_P6- / USB_SSRX0-
77	USB_P7+ / USB_SSTX0+	78	USB_P6+ / USB_SSRX0+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX1-	82	USB_P4- / USB_SSRX1-
83	USB_P5+ / USB_SSTX1+	84	USB_P4+ / USB_SSRX1+

Pin	Signal	Pin	Signal
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CC	92	USB_ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	eDP0_TX0+ / LVDS_A0+	100	eDP1_TX0+ / LVDS_B0+
101	eDP0_TX0- / LVDS_A0-	102	eDP1_TX0- / LVDS_B0-
103	eDP0_TX1+ / LVDS_A1+	104	eDP1_TX1+ / LVDS_B1+
105	eDP0_TX1- / LVDS_A1-	106	eDP1_TX1- / LVDS_B1-
107	eDP0_TX2+ / LVDS_A2+	108	eDP1_TX2+ / LVDS_B2+
109	eDP0_TX2- / LVDS_A2-	110	eDP1_TX2- / LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+ / LVDS_A3+	114	eDP1_TX3+ / LVDS_B3+
115	eDP0_TX3- / LVDS_A3-	116	eDP1_TX3- / LVDS_B3-
117	GND	118	GND
119	eDP0_AUX+ / LVDS_A_CLK+	120	eDP1_AUX+ / LVDS_B_CLK+
121	eDP0_AUX- / LVDS_A_CLK-	122	eDP1_AUX- / LVDS_B_CLK-
123	LVDS_BLT_CTRL/ GP_PWM_OUT0	124	GP_1-Wire_Bus
125	GP2_I2C_DAT / LVDS_DID_DAT	126	eDP0_HPD# / LVDS_BLC_DAT
127	GP2_I2C_CLK / LVDS_DID_CLK	128	eDP0_HPD# / LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	DP_LANE3+ / TMDS_CLK+	132	RSVD
133	DP_LANE3- / TMDS_CLK-	134	RSVD
135	GND	136	GND
137	DP_LANE1+ / TMDS_LANE1+	138	DP_AUX+
139	DP_LANE1- / TMDS_LANE1-	140	DP_AUX-
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+	144	RSVD
145	DP_LANE2- / TMDS_LANE0-	146	RSVD
147	GND	148	GND
149	DP_LANE0+ / TMDS_LANE2+	150	HDMI_CTRL_DAT
151	DP_LANE0- / TMDS_LANE2-	152	HDMI_CTRL_CLK
153	DP_HDMI_HPD#	154	RSVD
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND

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Pin	Signal	Pin	Signal
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0 / GPIO0	186	LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2	188	LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4	190	LPC_FRAME# / GPIO5
191	SERIRQ / GPIO6	192	LPC_LDRQ# / GPIO7
193	VCCRTC	194	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

Note: Please refer to PQ7 series modules' user manual for detail information.

5. QSEVEN™ Carrier Board Design

5-1. PCB Design Rules

The PQ7 series Specification provides a rich set of modern, high-speed differential serial interfaces. Designing PQ7 series Carrier Boards must be followed the certain design rules.

The most important design rule is route high-speed serial interfaces as differential pairs.The two lines in the pair must be length-matched and should have uniform edge-to-edge spacing. They should have a minimum of layer changes. If they do change layers, both lines in the pair should change. The preferred reference plane for the high-speed pairs is a single, continuous GND plane. If the differential pair is referenced to a power plane, avoid routing the pair across a power-plane split.

5-2. Trace-Impedance Considerations

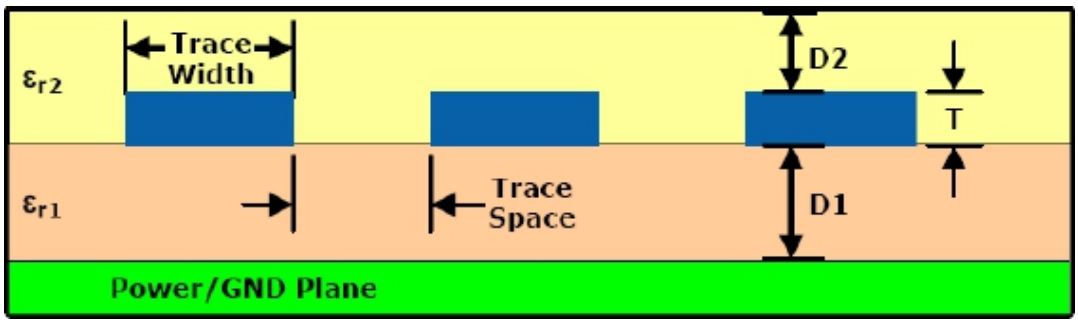
Most high-speed interfaces used in a Q_{SEVEN}™ design for a Carrier Board are differential pairs that need a well-defined and consistent differential and single-ended impedance. he differential pairs should be edge-coupled

There are two basic structures used for high-speed differential and single-ended signals. The first is “microstrip”, in which a trace or trace pair is referenced to a single ground or power plane. The outer layers of multi-layer PCBs are microstrips. A diagram of a microstrip cross section is shown in Figure 5-1 below.

The second structure is “stripline” in which a trace or pair of traces is sandwiched between two reference planes, as shown in Figure 5-2 below. If the traces are exactly halfway between the reference planes, then the stripline is said to be symmetric or balanced. Usually the traces are a lot closer to one of the planes than the other. Inner layer traces on multi-layer PCBs are usually asymmetric striplines.

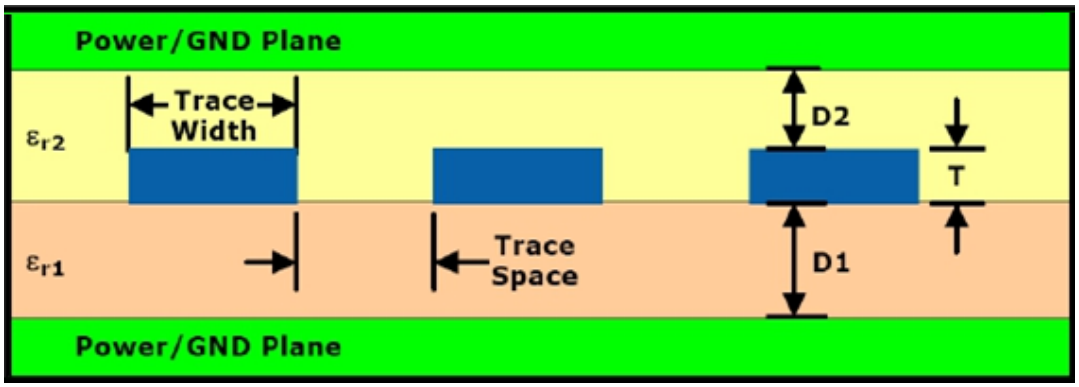
Before proceeding with a Carrier Board layout, designers should decide on a PCB stack-up and on trace parameters, primarily the trace-width and differential-pair spacing. It is quite harder to change the differential impedance of a trace pair after layout work is done than it is to change the impedance of a single-ended signal. It is more important for the PCB designer and the Project Engineer to determine the routing parameters for differential pairs ahead of time.

Figure 5-1 Microstrip Diagram.



NOTE: The trace spacing vary from one signal group to the other. Each signal group's values are specified in their respective sections within this design guide.

Figure 5-2 Stripline Diagram.



NOTE: The trace spacing vary from one signal group to the other. Each signal group's values are specified in their respective sections within this design guide.

Figure 5-3 Differential Trace Dimension Terminology.

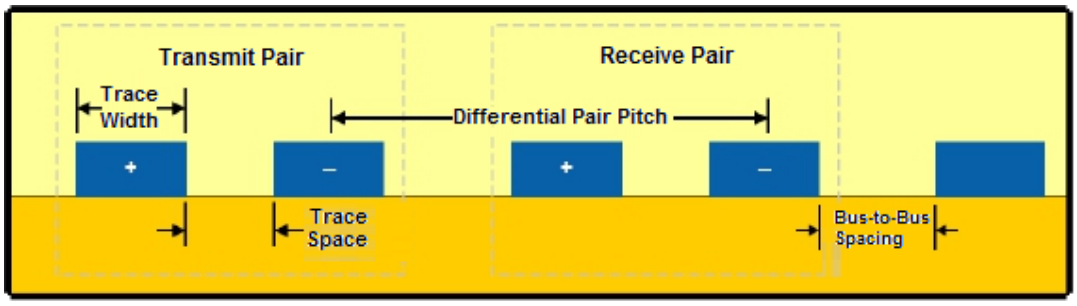


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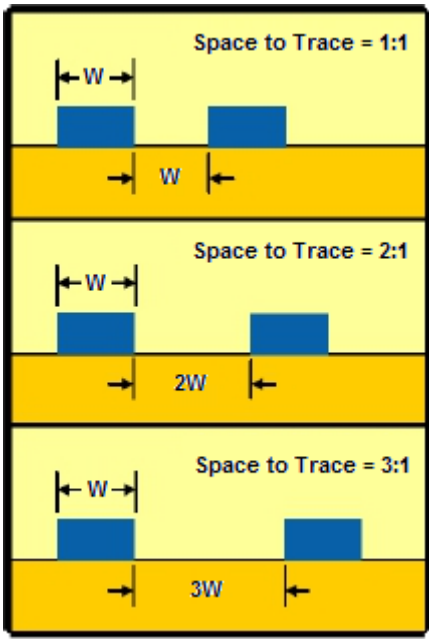
Figure 5-4 Trace Spacing vs Trace Width Examples.



6. Signal Descriptions

The "#" symbol at the end of the signal name indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level. Differential pairs are indicated by trailing'＋' and '－' signs for the positive or negative signal.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Table 6-1 Signal Terminology.

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
I_{OL}	Output low current The I_{OL} is the maximum output low current the module must be able to drive to an external circuitry.
I_{IL}	Input low current The I_{IL} is the maximum input low current that must be provided to the Qseven® module via external circuitry in order to guarantee a proper logic low level of the signal.
P	Power Input
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.1.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

6-1. PCI Express Interface Signal

According to the PCI Express Base Specification Revision 1.1, a total available interconnect loss budget of 13.2 dB is allowed between the PCI Express host device on the Qseven® CPU module and the PCI Express device on the carrier board, ExpressCard or PCI Express add-in card.
The specifications contained herein apply to all high-speed signals of each interface width definition.
The signaling rate for encoded data is 2.5 Gigabit transfers/s and the signaling is point-to-point.

PCI Express (PCIe) signals are high-speed differential pairs with a nominal 85Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

Table 6-2 Signal Definition PCI Express.

Signal	Description	I/O Type	I_{OL}/I_{IIL}	I/O
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	PCIE		I
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	PCIE		O
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	PCIE		I
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	PCIE		O
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	PCIE		I
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	PCIE		O
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	PCIE		I
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	PCIE		O
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	PCIE		O
PCIE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	CMOS 3.3V Suspend	≥ 5 mA	I
PCIE_RST#	Reset Signal for external devices.	CMOS 3.3V	max 1 mA	O

PCIe pairs need to be length-matched within a given pair, but the different pairs do not need to be matched. The transmit pairs are designated as PCIE0_TX+ and PCIE0_TX- thru PCIE1_TX+ and PCIE1_TX-. Transmit in this context means that the signals are transmitted out of the Module. No coupling capacitors are needed on Carrier Board PCIe transmit lines. The coupling caps are located on the Module. The receive pairs are designated PCIE0_RX+ and PCIE0_RX- thru PCIE1_RX+ and PCIE1_RX-. Receive in this context means that the signals are received by the Module. Coupling capacitors are needed on the Carrier Board on these lines if the PCIe target device is down on the Carrier Board. Locate the coupling capacitors near the transmit pins of the Carrier Board's PCIe target device. If the PCIe target device is on a slot card, then no coupling caps are needed on the lines on the Carrier Board because the coupling caps will be on the slot card.

6-1-1. PCI Express Insertion Loss Budget

Figure 6-1 PCI Express Link Topology 1.

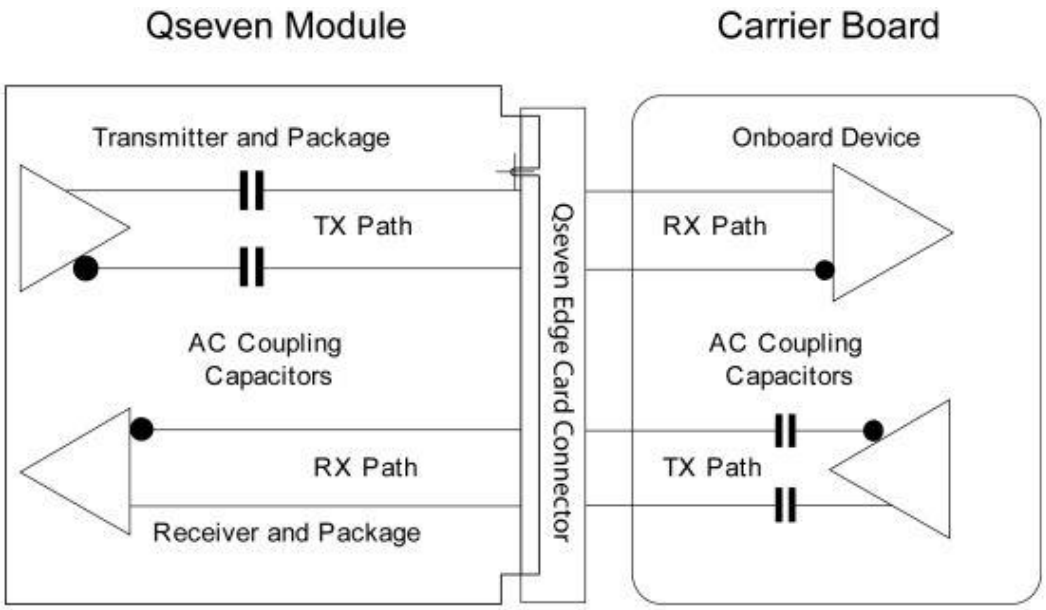


Figure 6-2 PCI Express Link Topology 2.

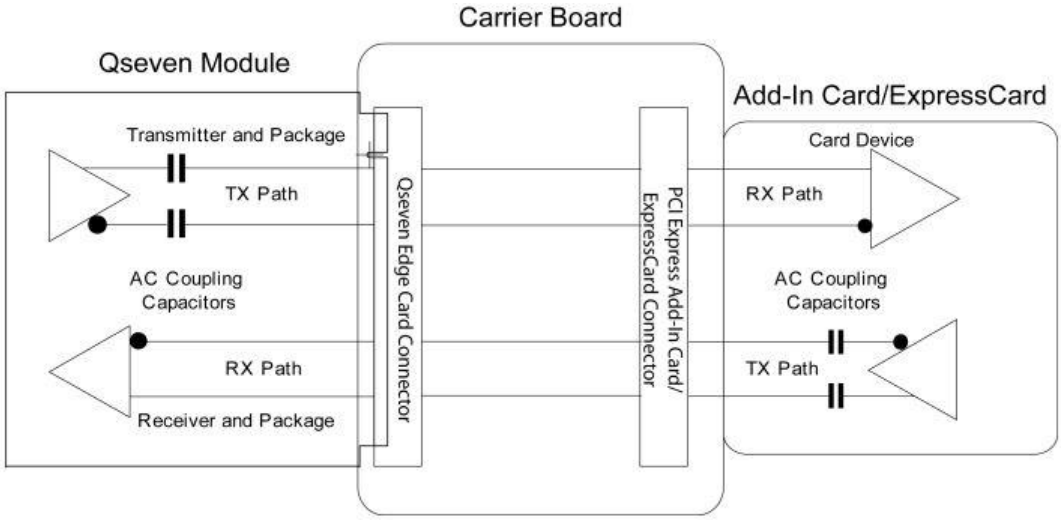


Table 6-3 Carrier Board PCI Express Insertion Loss Budget.

Segment	Loss Budget Value at 1.25 GHz (dB)	Max. Trace Length	Comments
Carrier Board Topology 1 (TX path)	5.5dB	14.5 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 1 (RX path)	5.9dB	15.7 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 2 (TX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard
Carrier Board Topology 2 (RX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard

The trace lengths presented in Table are based on the following assumptions：

- Typical damping of the PCB trace of 0.35dB/inch @ 1,25GHz (common value for FR-4 based material)
- The RX path budget includes the additional damping of the DC decoupling capacitors and 2 additional vias for connecting the decoupling capacitors
- Maximum 2 vias per trace for a RX path and maximum 4 vias per trace for a TX path on the connection from the the Qseven ® connector on the Qseven ® carrier board to an onboard device
- Maximum 2 vias per trace for a RX path and maximum 2 vias per trace for a TX path on the connection from the Qseven ® connector on the Qseven ® carrier board to a PCI Express extension socket that is compliant to the properties defined in the PCI Express Card Electromechanical

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Specification (this includes standard PCI Express cards as well as ExpressCards).

- Trace routing is implemented according to the design rules for high speed differential traces.

The values in Table above are derived from a signal integrity simulation and reflect a worst case scenario. Designers that face the necessity to deviate from the given values have to conduct a suitable signal integrity simulation to guarantee compliance to the PQ7 series specification and the underlying PCI Express specification.

For USB3.0, HDMI and DisplayPort interface signals the description offered in this section is also applicable.

6-2. Gigabit Ethernet Signals

The LAN port defines to support a 10/100 Megabits per second or Gigabit Ethernet. The Module Specification specifies that LAN magnetics must reside on the Carrier Board, not on the Module. The LAN interface consists of four differential pair signals, designated as GBE_MDI0+/- thru GBE_MDI3+/-. Additionally, there are four single-ended signals that provide link-status information, along with a reference voltage for the magnetics center tap.

Route LAN differential pairs with 100Ω differential impedance and 50Ω, single-end impedance.

Table 6-4 Signal Definition Ethernet.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
GBE_MDI0+ GBE_MDI0-	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI1+ GBE_MDI1-	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI2+ GBE_MDI2-	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_MDI3+ GBE_MDI3-	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_CTREF	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shouldbe current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		
GBE_LINK#	Ethernet controller 0 link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK100#	Ethernet controller 0 100Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK1000#	Ethernet controller 0 1000Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_ACT#	Ethernet controller 0 activity indicator, active low.	CMOS 3.3V PP	max 10 mA	O

6-2-1. Gigabit Ethernet Insertion Loss Budget

Figure 6-3 Gigabit Ethernet Link Topology.

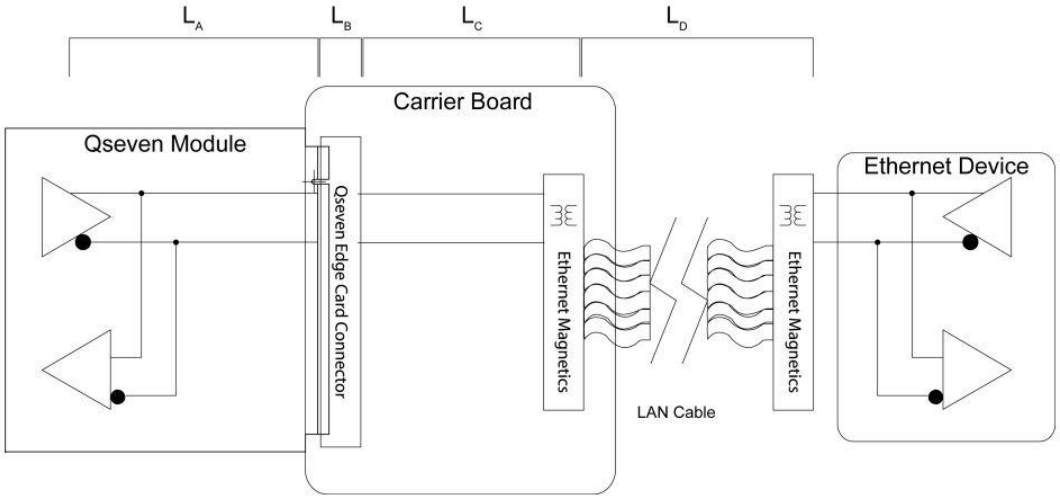


Table 6-5 Signal Definition Ethernet.

Segment	Loss Budget Value at 100 MHz	max. Trace Length	Comments
L_A	0.08 dB	2 inches	Module trace @ 0.28 dB / GHz / inch
L_B	0.02 dB		MXM connector at 100 MHz
L_C	0.15 dB	4 inches	Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00 dB		Cable and cable connectors, integrated magnetics, per source spec
Total	24.25 dB		

Qseven® Ethernet implementations should conform to insertion loss values less than or equal to those shown in Table above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gigabit Ethernet specification. “Device Down” implementations, in which the Ethernet target device is implemented on the carrier board (for instance, an Ethernet switch), may add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the carrier board budget. This insertion loss value is typically 1 dB. The carrier board insertion loss budget then becomes LC + 1 dB, or 1.15 dB.

6-2-2. LAN Component Placement

When using RJ45 connectors without integrated magnetics, the discrete magnetics module has to be placed as close as possible to the RJ45 connector. The distance between the magnetics module and RJ45 connector must be less than 1 inch. This distance mequirement must be observed during the carrier board layout when implementing LAN.

6-3. Serial ATA Interface Signals

Serial ATA（SATA）signals are high-speed differential pairs with a nominal 85Ω differential impedance. Route them as differential pairs, preferably referenced to a continuous GND plane with a minimum of via transitions.

Maintain parallelism between SATA differential signals with the trace spacing needed to achieve same differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Ensure minimum deviations in length.

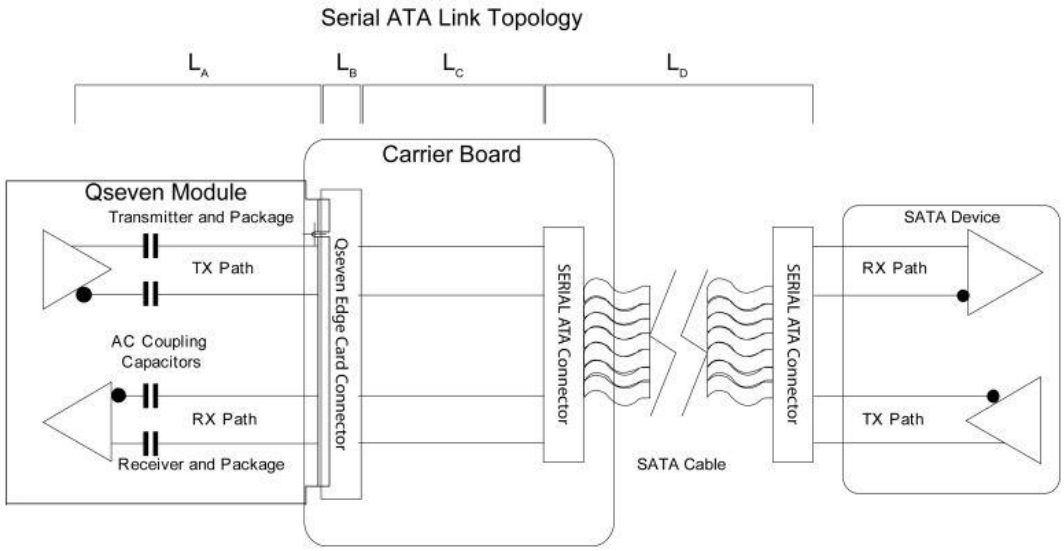
Table 6-6 Signal Definition SATA.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	SATA		I
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	SATA		O
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	SATA		I
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	SATA		O
SATA_ACT#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	max. 10mA	O

6-3-1. Serial ATA Insertion Loss Budget

The Serial ATA source specification provides insertion loss figures only for the SATA cable.

Figure 6-4 Serial ATA Link Topology.



SATA specification 3.1 defines the signal budget from chip to mated connector.

The trace lengths presented in Table 6-X are based on the following assumptions:

- Typical damping of the PCB trace of 0.42dB/inch @ 1,5GHz (common value for FR-4 based material)
- The budget includes the additional damping of the DC decoupling and the Qseven ® connector losses.
- Trace routing is implemented according to the design rules for high speed differential traces.

Table 6-7 SATA Gen 1 Loss Budget Allocation.

Segment	Loss Budget Value at 0.75 GHz (dB)	Max. Trace Length	Comments
L_A	0.5 dB	2.5 inches	Module Trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40 dB		
L_B	0.40 dB		MXM Connector @ 0.75 GHz
L_C	1.55 dB	7.2	Carrier Board Trace @ 0.28 dB / GHz / inch
Total	2.85 dB		

Table 6-8 SATA Gen2 Loss Budget Allocation.

Segment	Loss Budget Value at 1.5 GHz (dB)	Max. Trace Length	Comments
L_A	1.05 dB	2.5 inches	Module Trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40 dB		
L_B	0.50 dB		MXM Connector @ 1.5 GHz
L_C	1,05 dB	2.5 inches	Carrier Board Trace @ 0.28 dB / GHz / inch
Total	3.00 dB		

6-4. USB Interface Signals

A common mode choke is advisable if USB pairs on the Carrier Board are routed to a connector for use with an external cable.
PQ7 SERIES can support up to 8 USB 2.0 ports and 2 USB SuperSpeed.

Signals USB_0_1_OC#, USB_2_3_OC#, USB_4_5_OC# and USB_6_7_OC# are used to flag a USB over-current situation.
Carrier Board USB current monitors may may pull these lines to GND with open drain drivers to indicate that the monitor's current limit has been exceeded.
Do not pull up these lines to 3.3V on the Carrier Board. These pins are already pull high to VSB3 at PQ7 series.

Carrier Boards that supply power to external USB devices over a USB cable should implement current-limiting hardware and should drive the appropriate over-current line.
If the USB target device is on the Carrier Board, then it is not necessary to implement the current-limiting and to drive the over-current line for that port. The over-current line may be left open.

Route USB signals as differential pairs, with a 85Ω differential impedance and a 50Ω, single-ended impedance. Ideally, a USB pair is routed on a single layer adjacent to a ground plane. USB pairs should not cross plane split. Keep layer transitions to a minimum. If the differentialpair is referenced to a power plane, avoid routing the pair across a power-plane split and should be well-bypassed.

Table 6-9 Signal Definition USB.

Signal	Description	I/O Type	I_{OL} /I_{IL}	I/O
USB_P0+ USB_P0-	Universal Serial Bus Port 0 differential pair.	USB		I/O
USB_P1+ USB_P1-	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	USB		I/O
USB_P2+ USB_P2-	Universal Serial Bus Port 2 differential pair.	USB		I/O
USB_P3+ USB_P3-	Universal Serial Bus Port 3 differential pair.	USB		I/O
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	USB		I/O I
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path.	USB		I/O O
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	USB		I/O I
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path.	USB		I/O O
USB_0_1_OC#	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_2_3_OC#	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_4_5_OC#	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_6_7_OC#	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_ID	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	CMOS 3.3V Suspend		I
USB_CC	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	CMOS 3.3V Suspend		I

Figure 6-5 USB 2.0 Link Topology

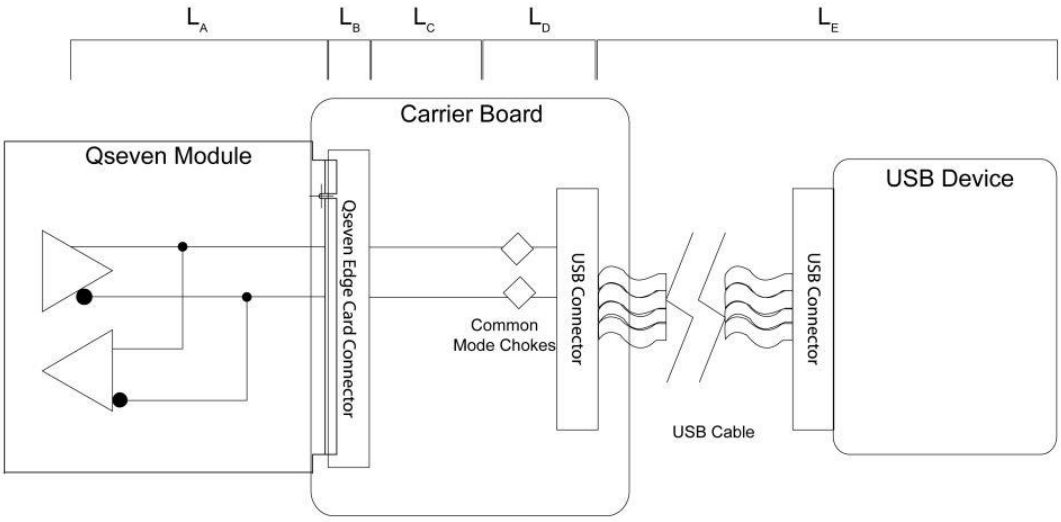


Table 6-10 Signal Definition Ethernet

Segment	Loss Budget Value at 240 MHz	max. Trace Length	Comments
L_A	0.4 dB	6 inches	Module Trace @ 0.28 dB / GHz / inch
L_B	0.05 dB		MXM Connector at 240 MHz
L_C	1 dB	14 inches	Carrier Board Trace @ 0.28 dB / GHz / inch
L_D	1.00 dB		USB Connector and Ferrite Loss
L_E	3,6 dB		USB cable and far end connector loss, per source specification.
Total	6.05 dB		

Qseven® USB implementations should conform to insertion loss values less than or equal to those shown in Table 6-10 above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

“Device Down” implementations, in which the USB target device is implemented on the carrier board, may add the ferrite and USB connector insertion loss values to the carrier board budget.

The carrier board insertion loss budget then becomes LC + LD, or 2.68 dB.

6.4.2 USB 3.0 Clint

PQ7-M106-IL-ZR1don't have USB 3.0 Clint Signal，If want to use USB 3.0 Clint Signal need to modify schematic.

Q seven Pin81~84

Table 16-139.USB 3.0 Interface Client (Device) Signals

Signal Name	Direction	Description
USB3DEV_RXP/N[0]	I USB 3.0 V1P0A	**Data In:** High speed serialized data inputs
USB3DEV_TXP/N[0]	O USB 3.0 V1P0A	**Data Out:** High speed serialized data outputs.
USB3DEV_REXT[0]	I V1P0A	**Resistor Compensation:** An external resistor 1.24K +/-1% Ohm must be connected between this pin and package ground.

79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX1-	82	USB_P4- / USB_SSRX1-
83	USB_P5+ / USB_SSTX1+	84	USB_P4+ / USB_SSRX1+
85	USB_2_3_OC#	86	USB_0_1_OC#

6-5. SDIO Interface Signals

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories.

Table 6-11 Signal Definition SDIO.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	CMOS 3.3V		I/O
SDIO_CLK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	CMOS 3.3V		O
SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	CMOS 3.3V OD/PP		I/O
SDIO_LED	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	CMOS 3.3V	max 1 mA	O
SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	CMOS 3.3V		I/O
SDIO_PWR#	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	CMOS 3.3V		O
SDIO_DAT0-7	SDIO Data lines. These signals operate in push-pull mode.	CMOS 3.3V PP		I/O

~~PQ7-SERIES-SD/SDIO/MMC inside controller—is based on the standards outlined in these specifications:~~

- MultiMediaCard System Specification, Version 4.1
- SDIO Specification, Version 1.1

The SD/SDIO/MMC controller is connected to SD, SDIO, or MMC card devices, but there are limitations to which device type installs into which socket type. See Table 5-9 for information on sockets and devices supported by the SD/SDIO/MMC controller.

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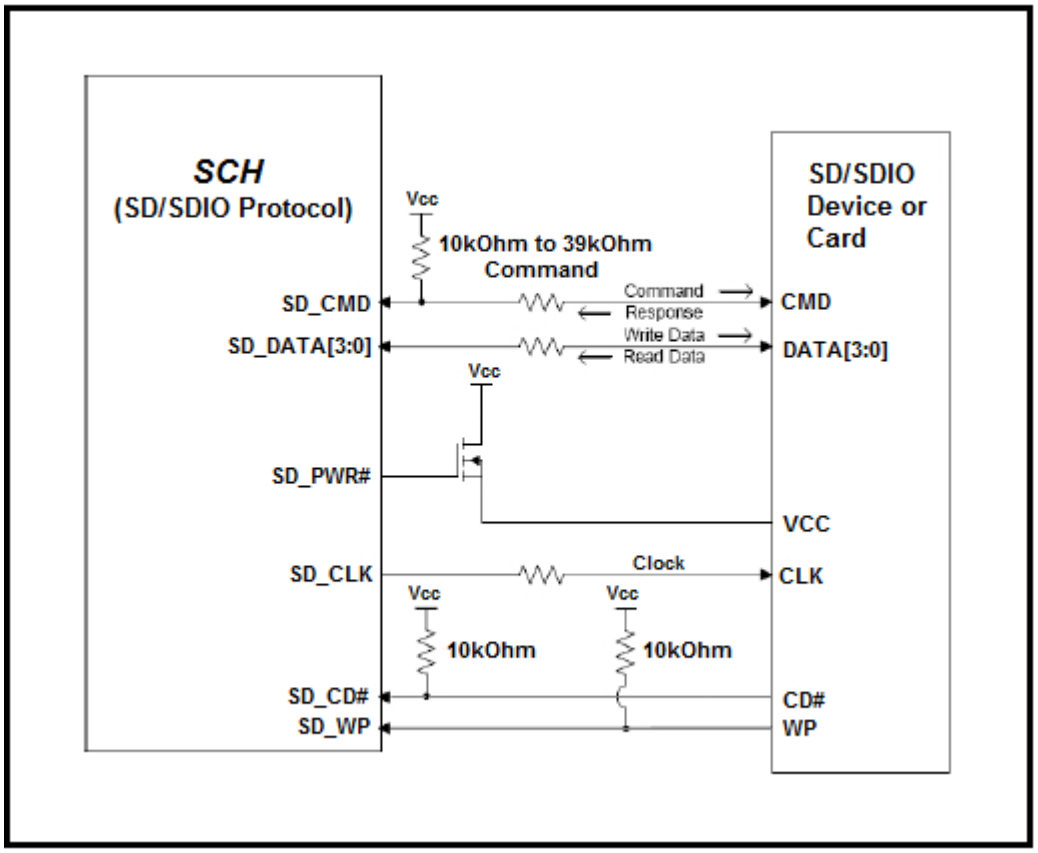
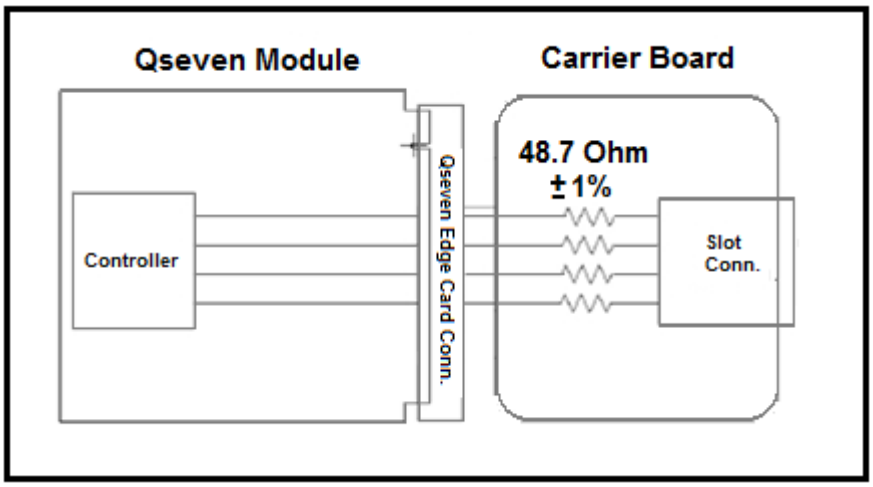
Figure 6-6 SD and SDIO Protocol Interface Block Diagram.



NOTES:

1. A 10-kΩ to 39-kΩ ±5% pull-up resistor to VCC is required for SD_CMD.
2. The Intel® SCH has integrated the required pull-up resistors on the DATA[3:0] signals.
3. A 10-kΩ ±5% pull-up resistor to VCC is recommended for both SD_CD# and SD_WP.

Figure 6-7 SD/SDIO Protocol Clock/DATA/CMD Routing Topology.



NOTE: SDIO signal include SD_CLK, SD_CMD, SD_DATA[3:0]. Trace length at carrier side limit at 2.8 inch.

PQ7-M106 SDIO Design

PQ7-M106-IL Use SD card 3.0 Interface

PQ7-M106-IE Use SD card 3.0 Interface、eMMC 4.5 Interface

The Storage Control Cluster (SCC) consists of SDIO, SD Card and eMMC controllers to support mass storage and IO devices.

- One eMMC 4.5 interface
- One SD Card 3.0 interface
- One SDIO 3.0 interface for SDIO-based WIFI

Note: All units in the SCC support both PCI mode and ACPI mode of operation. A level shifter may be needed on the platform for SDIO 3.0 compliance. An eMMC 4.41 controller also exists but shouldn't be used.

16.2 Features

16.2.1 eMMC Interface Features

- eMMC 4.5 controller supported
- Transfers the data in 1 bit, 4 bit and 8 bit modes.
- Transfers data in the following speed classes: Baseline (1, 4, 8 bit up to 25Mhz), HS SDR/DDR (4, 8 bit up to 50Mhz) and HS200 (4, 8 bit up to 200MHz - 4.5 controller only)
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Supports MMC Plus and MMC mobile.
- Supports both round-robin and priority-based arbitration for transmit operation.
- Run-time configurabilty of channel ID bits.

Table 184. eMMC Signals

Signal Name	Direction Power	Description
MMC1_CLK	O V1P8S	**eMMC Clock** The frequency may vary between 26 and 52 MHz.
MMC1_D[7:0]	I/O V1P8S	**eMMC Port Data bits 0 to 7** Bidirectional port used to transfer data to and from eMMC device. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using either D[0]-D[3] or D[0]-D[7], by the MultiMedia Card controller. The MultiMedia Card includes internal pull-ups for data lines D[1]-D[7]. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines D[1], D[2], and D[3]. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines D[1]-D[7].
MMC1_CMD	I/O V1P8S	**eMMC Port Command** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.
MMC1_RCOMP	-	**eMMC RCOMP** This signal is used for pre-driver slew rate compensation.
MMC1_RST#	O V1P8S	**eMMC Reset Signals** Active low to reset.

Table 186. SD Card Signals

Signal Name	Direction Power	Description
SD3_CLK	O VSDIO	**SD Card Clock** The frequency may vary between 24 and 50 MHz.
SD3_D[3:0]	I/O VSDIO	**SD Card Data bits 0 to 3** Bidirectional port used to transfer data to and from SD card. By default, after power up or reset, only D[0] is used for data transfer. A wider data bus can be configured for data transfer, using D[0]-D[3].
SD3_CD#	I/O V1P8S	**SD Card Detect** Active low when a card is present. Floating (pulled high with internal PU) when a card is not present.
SD3_CMD	I/O VSDIO	**SD Card Command** This signal is used for card initialization and transfer of commands. It has two modes—open-drain for initialization, and push-pull for fast command transfer.
SD3_1P8EN	O V1P8S	**SD Card 1.8V Enable** Indicates the voltage of the SD Card to the power delivery subsystem. The default voltage (3.3 V) is requested when this signal is driven low. 1.8 V is requested when this signal is high. This voltage change applies to the SD3_V1P8V3P3_S3 (VSDIO) rail on the SoC.
SD3_RCOMP	-	**SD Card RCOMP** This signal is used for pre-driver slew rate compensation.
SD3_PWREN#	O V1P8S	**SD Card Power Enable** This signal is used to enable power on a SD device.

16.2.2 SDIO/SD Card Interface Features

- Up to 832Mbits per second data rate using 4 parallel data lines.
- Transfers the data in 1 bit and 4 bit SD modes.
- Transfers the data in following UHS-I modes: HS and DDR50.
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity.
- Designed to work with I/O cards, Read-only cards and Read/Write cards.
- Supports Read wait Control.
- SDIO only validated with WIFI devices.

16.2.3 Storage Interfaces Overview

This section provides a very high level overview of the SD, SDIO, eMMC 4.5 specification. Refer to the SD and eMMC specifications for complete details.

16.2.3.1 SD Card 3.0 Bus Interface

The SD Card bus has a single master, single slaves (card), synchronous topology (refer to Figure 105). During initialization process commands are sent to the card, allowing the application to detect the card and assign logical addresses to the physical slot. All data communication in the Card Identification Mode uses the command line (CMD) only.

SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Card will use only SD3_D[0] for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between hardware cost and system performance. Note that while DAT1-SD3_D[3:1] are not in use, the SoC will tri-state those signals.

Figure 105.SD Memory Card Bus Topology

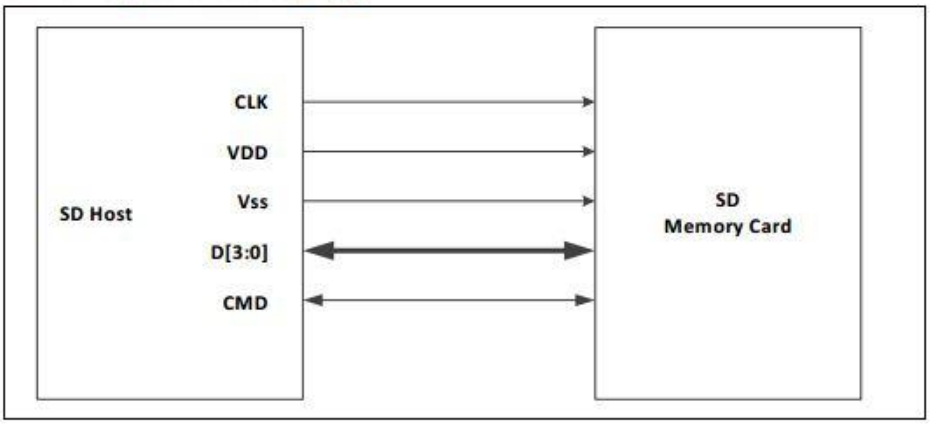
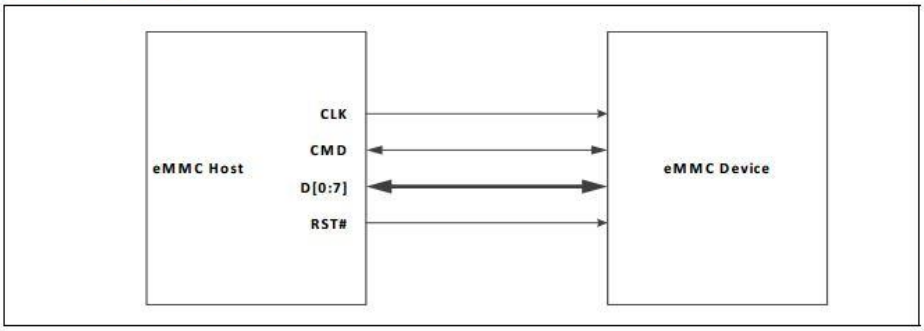


Figure 107.eMMC Interface



High Definition Audio Signals

The High Definition Audio or AC'97 or I2S interface are features that are platform dependent and therefore may not be available in all cases.

Table 6-12 Signal Definition HAD.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
HDA_RST# I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset.	CMOS 3.3V		O
HDA_SYNC I2S_WS	Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	CMOS 3.3V		O
HDA_BCLK I2S_CLK	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	CMOS 3.3V		O
HDA_SDO I2S_SDO	HD Audio/AC'97 Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	CMOS 3.3V		O
HDA_SDI I2S_SDI	HD Audio/AC'97 Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	CMOS 3.3V		I

6-5-1. HDA Placement and Routing Guidelines

HDA_RST# is the reset signal to external Codec. This signal should have a series termination of 33Ω±5%

HDA_SDO is a serial TDM data output to the Codec. The serial output is double pumped for a bit rate of 48 Mb/s for HD Audio. This signal should have a series termination of 33 Ω±5%. A non-stuffed resistor site for a 1kΩ ±5% pull-up to 3.3V should be provided.

HDA_SYNC is 48-kHz fixed rate sample sync to the Codec. It is also used to encode the stream number. This signal should have a series termination of 33Ω±5%. It has a weak internal pull-down and should not be pulled high.

Ground return paths for the analog signals must be given special consideration.

Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.

Partition the carrier board with all analog components grouped together in one area and all digital components in another.

Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.

Route analog power and signal traces over the analog ground plane.

Route digital power and signal traces over the digital ground plane.

Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.

Place the crystal or oscillator as close as possible to the codec

6-6. LVDS Flat Panel Signal

LVDS is a high speed, low power data transmission standard used for display connections to LCD panels.

The Intel SCH supports a Low-Voltage Differential Signaling interface that allows the Intel Graphics Media Adapter to communicate directly to an on-board flat-panel display. The LVDS interface supports pixel color depths of 18 and 24 bits.

Route LVDS differential pairs with 100Ω differential impedance and 50Ω, single-end impedance. Keep traces as short as possible.

The LVDS flat panel configuration within the BIOS of the Qseven ® module shall be implemented in accordance to the DisplayID specification that is under development within the Video Electronics Standards Association (VESA). For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA).
The LVDS interface can be used either as a single channel or as a dual channel,
depending on the properties of the platform used for the Qseven®/µQseven module. It is also possible to use the LVDS interface as two independent single LVDS channels. To do this, it is recommended to set the configuration of the LVDS display with an external EEPROM.

Table 6-13 Signal Definition LVDS.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
LVDS_PPEN	Controls panel power enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLEN	Controls panel backlight enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLT_CTRL /GP_PWM_OUT0	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
LVDS_A0+ LVDS_A0-	LVDS primary channel differential pair 0.	LVDS		O
eDP0_TX0+ eDP0_TX0-	Display Port primary channel differential pair 0.	LVDS		O
LVDS_A1+ LVDS_A1-	LVDS primary channel differential pair 1.	LVDS		O
eDP0_TX1+ eDP0_TX1-	Display Port primary channel differential pair 1.	LVDS		O
LVDS_A2+ LVDS_A2-	LVDS primary channel differential pair 2.	LVDS		O
eDP0_TX2+ eDP0_TX2-	Display Port primary channel differential pair 2.	LVDS		O
LVDS_A3+ LVDS_A3-	LVDS primary channel differential pair 3.	LVDS		O
eDP0_TX3+ eDP0_TX3-	Display Port primary channel differential pair 3.	LVDS		O
LVDS_A_CLK+ LVDS_A_CLK-	LVDS primary channel differential pair clock lines.	LVDS		O
eDP0_AUX+ eDP0_AUX-	Display Port primary auxiliary channel.	LVDS		O
LVDS_B0+ LVDS_B0-	LVDS secondary channel differential pair 0.	LVDS		O
eDP1_TX0+ eDP1_TX0-	Display Port secondary channel differential pair 0.	LVDS		O
LVDS_B1+ LVDS_B1-	LVDS secondary channel differential pair 1.	LVDS		O
eDP1_TX1+ eDP1_TX1-	Display Port secondary channel differential pair 1.	LVDS		O
LVDS_B2+ LVDS_B2-	LVDS secondary channel differential pair 2.	LVDS		O
eDP1_TX2+ eDP1_TX2-	Display Port secondary channel differential pair 2.	LVDS		O
LVDS_B3+ LVDS_B3-	LVDS secondary channel differential pair 3.	LVDS		O
eDP1_TX3+ eDP1_TX3-	Display Port secondary channel differential pair 3.	LVDS		O
LVDS_B_CLK+ LVDS_B_CLK-	LVDS secondary channel differential pair clock lines.	LVDS		O
eDP1_AUX+ eDP1_AUX-	Display Port secondary auxiliary channel.	LVDS		O
LVDS_DID_CLK GP2_I2C_CLK	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I²C bus clock line.	CMOS 3.3V OD		I/O
LVDS_DID_DAT GP2_I2C_DAT	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I²C bus data line.	CMOS 3.3V OD		I/O
LVDS_BLC_CLK eDP1_HPD#	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort secondary Hotplug detection.	CMOS 3.3V OD		I/O
LVDS_BLC_DAT eDP0_HPD#	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort primary Hotplug detection.	CMOS 3.3V OD		I/O

PQ7-M106 VGA Connector Design:

	PQ7-M106-IL	PQ7-M106-IE
VGA_RED	204	204
VGA_GREEN	210	208
VGA_BLUE	208	210
VGA_VSYNC	209	207
VGA_HSYNC	207	209
VGA_DDC_CLK	144	N/A
VGA_DDC_DATA	146	N/A

6-6-1. LVDS Implementation Guidelines

Many carrier board designs do not need the full range of LVDS performance offered by PQ7 series modules. It depends on the flat panel configuration of the PQ7 SERIES, as well as the carrier board design, as to how many LVDS signal pairs are supported.

If the LVDS display interface of the PQ7 series is not implemented, all signals associated with this interface should be left open.

This display port is normally used in conjunction with the pipe functions of panel up scaling and 6-to 8- bit dithers. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not being used. While disabled, individual or sets of pairs will enter a low power state. When the port is disabled, all pairs enter a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

A maximum pixel clock of 112 MHz is supported for the LVDS interface. And maximum supported cable length is 7 inches.

6-7. DisplayPort Interface Signals

DisplayPort(DP) is an open, industry standard digital display interface, that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

Route DP differential pairs with 85Ω differential impedance and 50Ω, single-end impedance.

Table 6-14 Signal Definition DisplayPort.

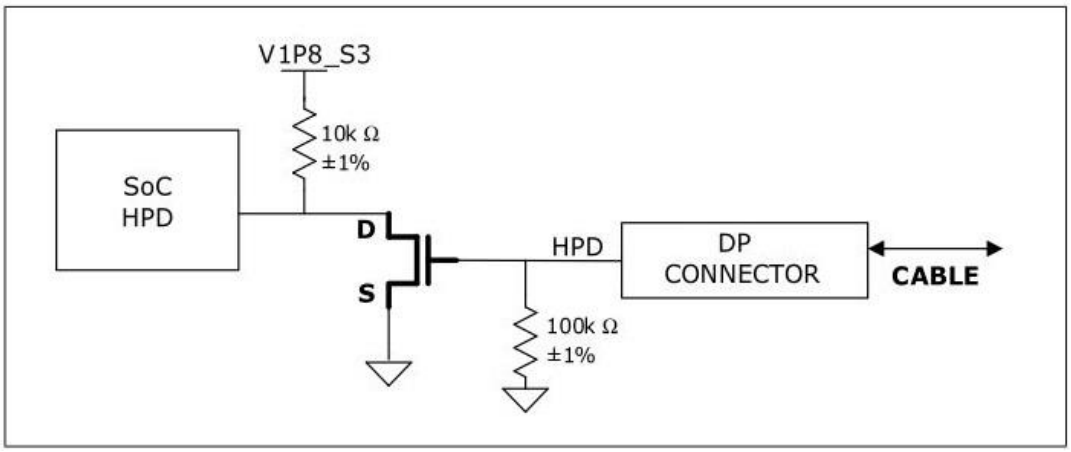
Signal	Shared With	Description	I/O Type	I_{OL}/I_{IL}	I/O
DP_LANE3- DP_LANE3+	TMDS_CLK- TMDS_CLK+	DisplayPort differential pair lines lane 3.	PCIE		O
DP_LANE2- DP_LANE2+	TMDS_LANE0- TMDS_LANE0+	DisplayPort differential pair lines lane 2.	PCIE		O
DP_LANE1- DP_LANE1+	TMDS_LANE1- TMDS_LANE1+	DisplayPort differential pair lines lane 1.	PCIE		O
DP_LANE0- DP_LANE0+	TMDS_LANE2- TMDS_LANE2+	DisplayPort differential pair lines lane 0.	PCIE		O
DP_AUX- DP_AUX+		Auxiliary channel used for link management and device control. Differential pair lines.	PCIE		I/O
DPHDMI_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Support of the DisplayPort interface is chipset dependent and therefore may not be available on all Qseven® modules. The DisplayPort interface signals are shared with the signals for the TMDS interface.

The hot-plug detect(HPD) output from DisplayPort sink device is a 3.3 V active high signal.

For example as below, a logic invertion circuit is required on the motherboard since the input on the SOC is a 1.8 V active low signal.

Figure 6-8 HPD Passgate Design Recommendation.



6-8. HDMI Interface Signals

High-Definition Multimedia Interface(HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Both HDMI and DVI were pioneered by Silicon Image and are based on TMDS ® , Silicon Image's powerful, high-speed, serial link technology. The HDMI specification requires the receiver to be terminated to AVCC (nominally 3.3 V) through Rt (nominally 50 Ω). The HDMI receiver requirements require the native HDMI signals from the SOC to be level shifted.

Route HDMI/DVI differential pairs with 85Ω differential impedance and 50Ω, single-end impedance.

Table 6-15 Signal Definition HDMI.

Signal	Shared With	Description	I/O Type	I_{OL}/I_{IL}	I/O
TMDS_CLK- TMDS_CLK+	DP_LANE3- DP_LANE3+	TMDS differential pair clock lines.	TMDS		O
TMDS_LANE0- TMDS_LANE0+	DP_LANE2- DP_LANE2+	TMDS differential pair lines lane 0.	TMDS		O
TMDS_LANE1- TMDS_LANE1+	DP_LANE1- DP_LANE1+	TMDS differential pair lines lane 1.	TMDS		O
TMDS_LANE2- TMDS_LANE2+	DP_LANE0- DP_LANE0+	TMDS differential pair lines lane 2.	TMDS		O
HDMI_CTRL_CLK		DDC based control signal (clock) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	CMOS 3.3V OD		I/O
HDMI_CTRL_DAT		DDC based control signal (data) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	CMOS 3.3V OD		I/O
DP_HDMI_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

6-9. LPC interface Signal

The Intel SCH implements an LPC interface as described in the LPC 1.1 Specification. The LPC bridge function of the Intel SCH resides in PCI Device 31: Function 0. The LPC_CLKOUT signals support two loads with no external buffering.

Table 6-16 Signal Definition LPC.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
LPC_AD[0..3] GPIO[0..3]	Multiplexed Command, Address and Data. General purpose input/output [0..3]	CMOS 3.3V		I/O
LPC_FRAME# GPIO5	LPC frame indicates the start of a new cycle or the termination of a broken cycle. General purpose input/output 5.	CMOS 3.3V		I/O
LPC_LDRQ# GPIO7	LPC DMA request. General purpose input/output 7.	CMOS 3.3V		I/O
LPC_CLK GPIO4	LPC clock. General purpose input/output 4.	CMOS 3.3V		I/O
SERIRQ GPIO6	Serialized Interrupt. General purpose input/output 6.	CMOS 3.3V		I/O

6-10. CAN Bus Interface Signals

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but now is also used in other areas such as industrial automation and medical equipment.

Table 6-17 Signal Definition CAN Bus.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
CAN0_TX	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		O
CAN0_RX	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		I

If the CAN Bus interface is not used, and/or the Qseven ® module's chipset does not support CAN Bus, then these pins shall be left unconnected.

6-11. SPI Interface Signals

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system devices such as EEPROM and flash components.

Table 6-18 Signal Definition SPI.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SPI_MOSI	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	CMOS 3.3V		O
SPI_MISO	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	CMOS 3.3V		I
SPI_SCK	SPI clock output.	CMOS 3.3V		O
SPI_CS0#	SPI chip select 0 output.	CMOS 3.3V		O
SPI_CS1#	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	CMOS 3.3V		O

6-12. UART Interface Signals

Table 6-19 Signal Definition of UART.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
UART0_TX	Serial Data Transmitter	CMOS 3.3V	max 1 mA	O
UART0_RX	Serial Data Reciever	CMOS 3.3V	≥ 5 mA	I
UART0_CTS#	Handshake signal, ready to send data	CMOS 3.3V	≥ 5 mA	I
UART0_RTS#	Handshake signal, ready to receive data	CMOS 3.3V	max. 1 mA	O

6-13. Input power pin

The PQ7 series operate entirely from 5-volt input power. All other necessary voltages are generated on the PQ7 SERIES using onboard power supplies.

Table 6-20 Signal Definition Input Power.

Signal	Description	I/O
VCC	Power Supply +5VDC ±5%.	P
VCC_5V_SB	Standby Power Supply +5VDC ±5%.	P
VCC_RTC	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P
GND	Power Ground.	P

6-14. Power control signal

Table 6-21 Signal Definition Power Control.

Signal	Description of Power Control signals	I/O Type	I_{OL}/I_{IL}	I/O
PWGIN	High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.	CMOS 5V	≥ 4 mA	I
PWRBTN#	Power Button: Low active power button input. This signal is triggered on the falling edge.	CMOS 3.3V Standby	≥ 10 mA	I

6-15. Power Management signals

It must be guaranteed that all the carrier board power rails, that are generated out of the VCC power rail, will be enabled by the SUS_S3# signal.

Table 6-22 Signal Definition Power Management.

Signal	Description of Power Management signals	I/O Type	I_{OL}/I_{IL}	I/O
RSTBTN#	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	CMOS 3.3V	≥ 10 mA	I
BATLOW#	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	CMOS 3.3V Suspend	≥ 10 mA	I
WAKE#	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	CMOS 3.3V Suspend	≥ 10 mA	I
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S3#	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S5#	S5 State: This signal indicates S4 or S5 (Soft Off) state.	CMOS 3.3V Suspend	max. 1 mA	O
SLP_BTN#	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	CMOS 3.3V Suspend	≥ 10 mA	I
LID_BTN#	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.	CMOS 3.3V Suspend	≥ 10 mA	I

6-16. Miscellaneous Signals

Table 6-23 Signal Definition Miscellaneous.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
WDTRIG#	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	CMOS 3.3V	≥ 10 mA	I
WDOUT	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	CMOS 3.3V	max. 5 mA	O
GP0_I2C_CLK	General Purpose I²C bus #0 clock line.	CMOS 3.3V OD		I/O
GP0_I2C_DAT	General Purpose I²C bus #0 data line.	CMOS 3.3V OD		I/O
SMB_CLK GP1_I2C_CLK	Clock line of System Management Bus. Multiplexed with General Purpose I²C bus #1 clock line.	CMOS 3.3V OD Suspend		I/O
SMB_DAT GP1_I2C_DAT	Data line of System Management Bus. Multiplexed with General Purpose I²C bus #1 data line.	CMOS 3.3V OD Suspend		I/O
SMB_ALERT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	CMOS 3.3V OD Suspend		I/O
SPKR GP_PWM_OUT2	Primary functionality is output for audio enunciator, the "speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
BIOS_DISABLE# /BOOT_ALT#	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.	CMOS 3.3V		I
RSVD	Do not connect.			NC
GP_1-Wire_Bus	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI	CMOS 3.3V		I/O

6-17. Manufacturing Signals

The MFG_NC[4:0] pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board.

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC[4:0] are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qseven ® Design Guide.

For more information about vendor specific functionality of MFG_NC[4:0], refer to the vendor's module documentation.

Table 6-24 Signal Definition Manufacturing.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
MFG_NC0	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC1	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC2	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC3	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC4	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	n.a.	n.a.	n.a.

6-18. Thermal Management Signals

PQ7 SERIES provides the 'THRM#' and 'THRMTRIP#' signals, which are used for system thermal management. In most current system platforms thermal management is closely associated with system power management.

Table 6-25 Signal Definition Miscellaneous.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
THRM#	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	CMOS 3.3V		I
THRMTRIP#	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	CMOS 3.3V		O

6-19. Fan Control Implementation

Table 6-26 Signal Definition Fan Control.

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
FAN_PWMOUT /GP_PWM_OUT1	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V OC		O
FAN_TACHOIN /GP_TIMER_IN	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	CMOS 3.3V		I

7. Input Power Requirements

PQ7 series modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by QSEVEN™ to provide a +5V standby voltage on the PQ7 series module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. The same applies to the +3V RTC battery voltage. If no RTC/CMOS backup functionality is required by the system, then the +3V RTC supply battery voltage can be omitted.

If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then the VCC_5V_SB pins (pins 205-206) of the Qseven ® module must be connected with the main VCC power rail pins (pins 211-230).

Table 7-1 Input Power Characteristics.

Power Rail	Nominal Input	Input Range	Max Input Ripple
VCC	+5V	+4.75V - +5.25V	±50 mV
VCC_5V_SB	+5V	+4.75V - +5.25V	±50 mV
VCC_RTC	+3V	+2.0V - +3.3V	±20 mV

NOTE: If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then all pins must be connected together with the standard 5V power rail 'VCC'.

7-1. Input Power Sequencing

PQ7 series input power sequencing requirements are as follows:

ATX Mode：

Start Sequence:

- VCC_RTC must come up at the same time or before VCC_5V_SB comes up.
- VCC_5V_SB must come up at the same time or before VCC comes up.
- PWGIN must be active at the same time or after VCC comes up.

Stop Sequence:

- PWGIN must be inactive at the same time or before VCC goes down
- VCC must go down at the same time or before VCC_5V_SB goes down.
- VCC_5V_SB must go down at the same time or before VCC_RTC goes down

Figure 7-1 Input Power Sequencing.

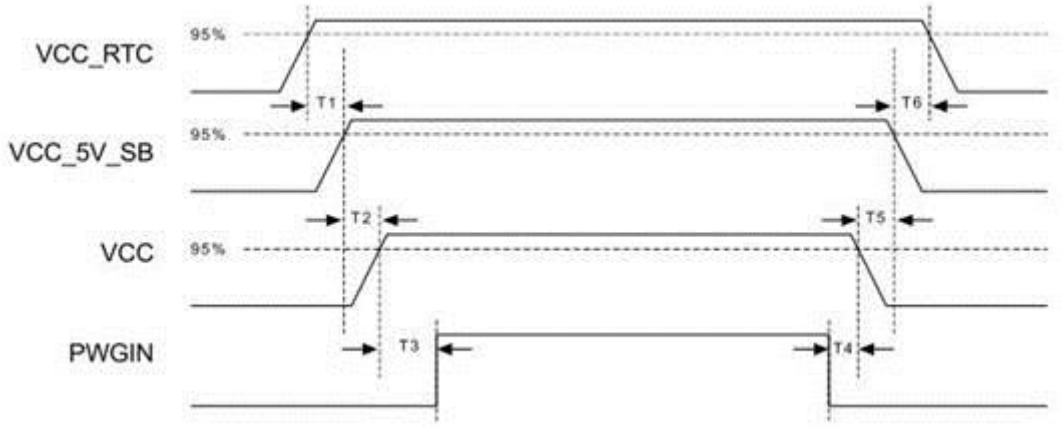


Table 7-2 Input Power Sequencing.

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms
T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

AT Mode：

AT mode only provides main voltage VCC. ***ATX Detect pin*** shall pull low then power button control by EC on PQ7 series module.

The sequence VCC and PWGIN are the same as ATX.

Table 7-2 Input Power Sequencing.

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms
T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

8. General Considerations for Differential Signal

The following is a list of suggestions for designing with high-speed differential signals. This should help implement these interfaces while providing maximum PQ7 SERIES carrier board performance.

- Use controlled impedance PCB traces that match the specified differential impedance.
- Keep the trace lengths as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and corners. This will reduce signal eflections and impedance changes. Use GND stitching vias when changing layers.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate, clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal

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reflections and affect signal quality.

- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50mil.

- Use a minimum of 20mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (split planes) increases inductance and radiation levels by forcing a greater loop area.

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Figure 8-1 Symmetrical and Non-Symmetrical Routing.

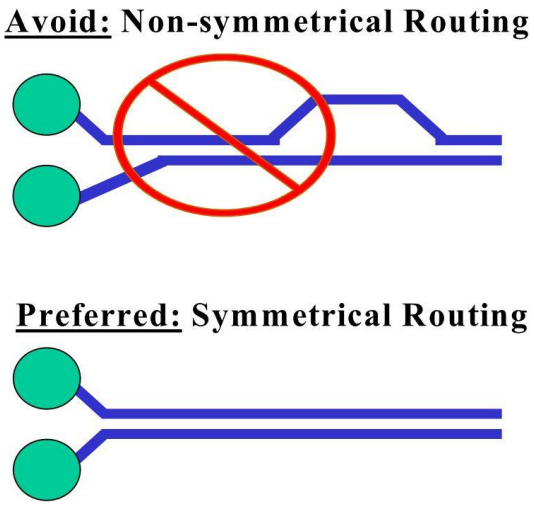
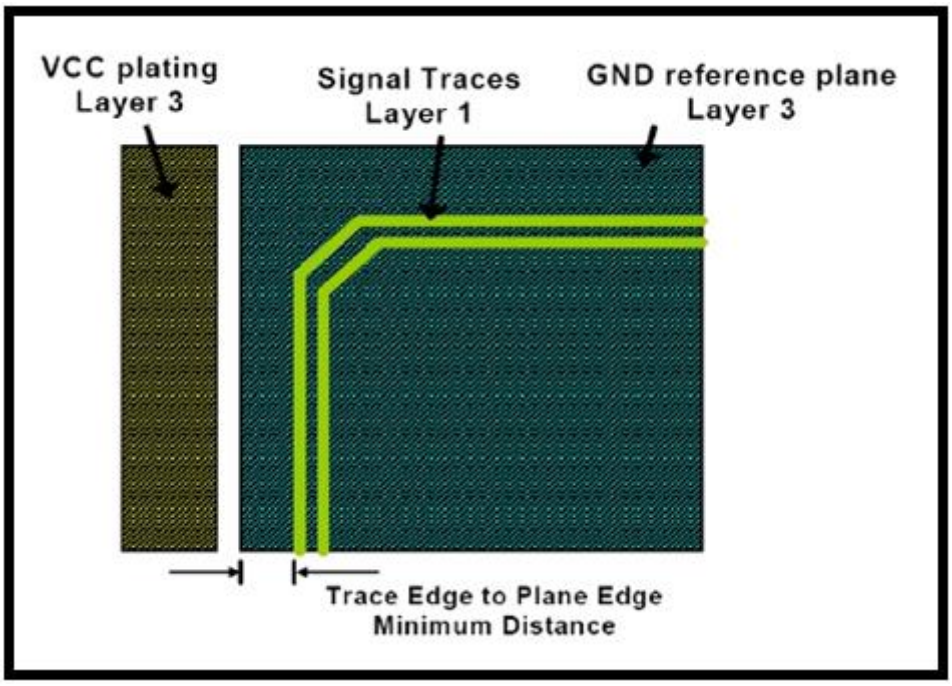
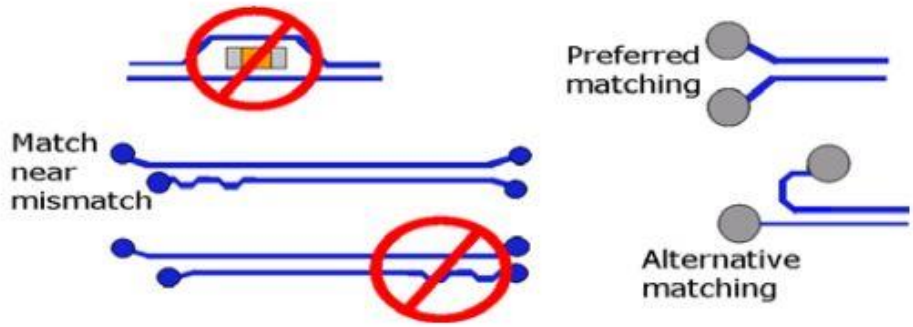


Figure 8-2 Trace Edge to Reference Plane Guidance.



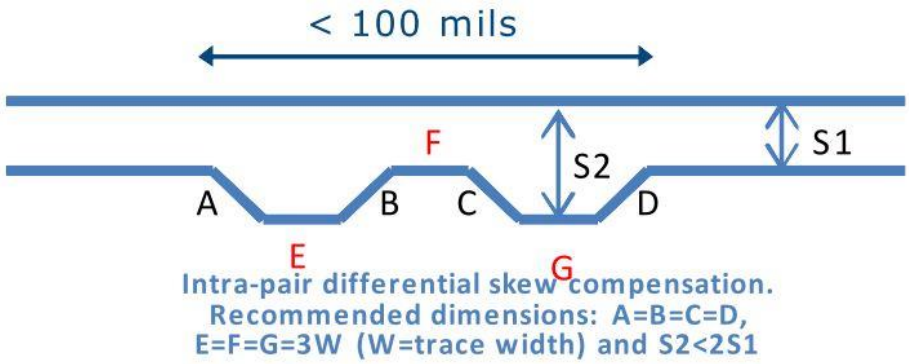
- When trace length matching occurs, the matching should be made as close as possible to the point where the length variation occurs, as shown in Figure 8-3, so the discontinuity won't propagate across the channel. For example, length matching in a chipset breakout area or connector pin field should occur within the first 125 mils (3.175 mm) of the structure that causes the length mismatch.
-

Figure 8-3 Length Matching Example.



- Serpentine layout introduces discontinuity to the channel and should be minimized so as to make it transparent to the signal. This is done by making its electrical length shorter than the signal rise time. In general, keeping serpentine routing length <100 mils is adequate. Trace spacing should not become greater than two times the original spacing. See Figure 8-4.

Figure 8-4 Serpentining Example.



- Keep bends to a minimum. Bends can introduce common mode noise into the system, which can affect the signal integrity of the differential signal pair.

- If bends are required, they should be at a 135-degree angle or greater; there should be no 90-degree bends or turns. An adequate air gap should be maintained between the inside traces of a bend. The gap should be four times the trace width or greater. The lengths of the segments in a bend should be 1.5 times the trace width or greater. See
- Figure 8-5 and Figure 8-6 for examples.

Figure 8-5 Acceptable Bends vs. Tight Bends Example.

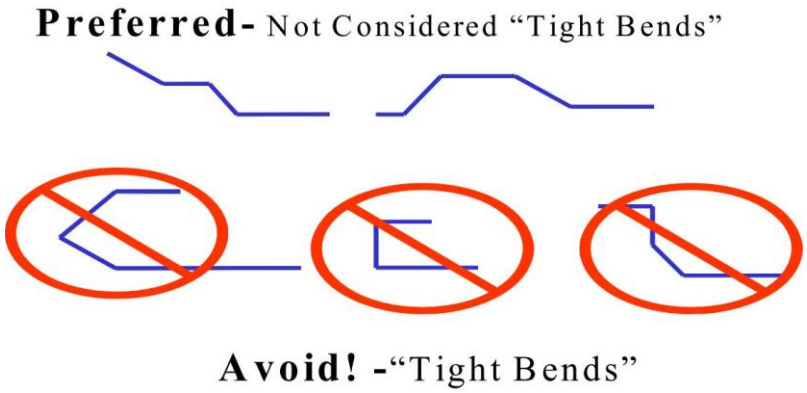
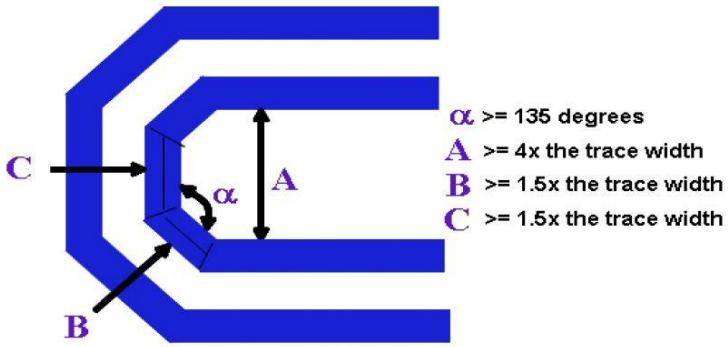


Figure 8-6 Via Pair Placement.



- The via count can be reduced but not increased from the maximum interface via requirements given in this document. Remove pads from unused internal layers to minimize excess via capacitance. The differential-pair via placement must be symmetrical. Vias on the differential-pair should not only match in number but also in relative location.

Figure 8-7 Via Pair Placement.