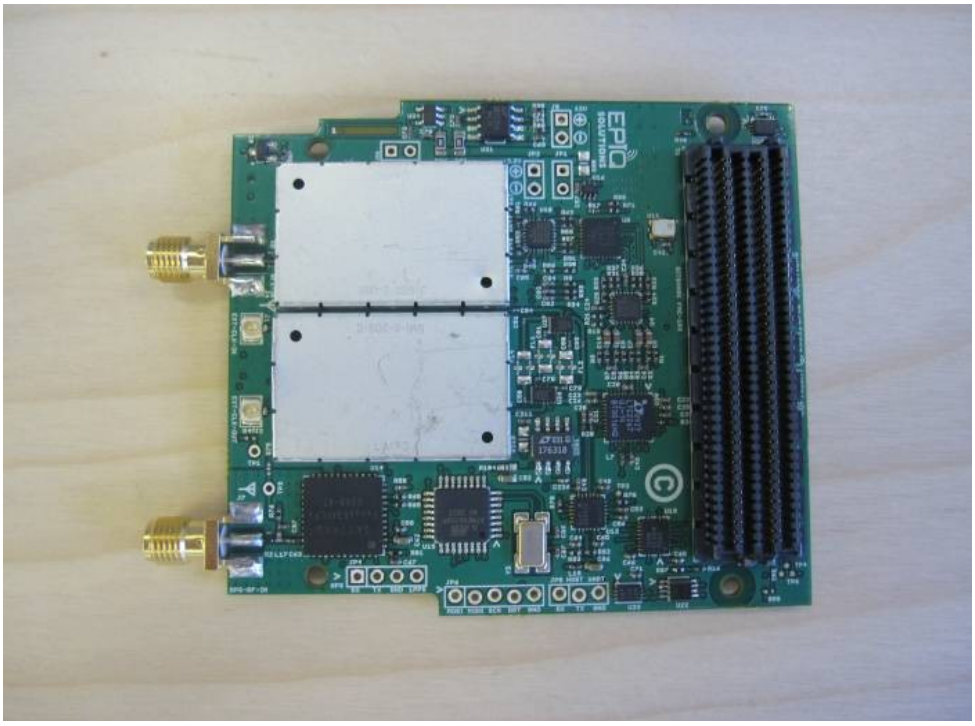
Bitshark FMC-1RX Rev C
User's Manual

Version 2.0



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Revision History

Date	Revision	Description
1.0	1/3/2011	Official public release
2.0	12/11/2011	Re-worked document for rev C of hardware: -Added SYS_PWR_EN line to allow the FPGA to control whether or not the card's power supplies are enabled -Improved I/Q imbalance by adding LO harmonic rejection filters between the LO and the quadrature demodulator (leading to significant improvements in quadrature balance below 600 MHz) -Migrated from the LTC2174-14 quad A/D converter to the LTC2267-14 dual A/D converter since there are no plans to use the other two channels in the near future -Updated the pinout for the LVDS pairs carrying the A/D signals

1 About this Document

This document provides the necessary details for interfacing to and using the Bitshark FMC-1RX RF receiver card, developed by Epiq Solutions [1]. It includes the specification of all the relevant signals supported by the card to allow an end user to integrate the FMC-1RX card into an FMC-compliant carrier platform. The Bitshark FMC-1RX is electrically compatible with any FMC-compliant carrier supporting the low-pin count (LPC) interface, as specified by the VITA 57 specification [2]. However, it is up to the end user to ensure that the FMC-1RX is compatible with the carrier, in terms of both electrical interconnect as well as mechanical fit.

In addition, the complete specification for the Bitshark FMC-1RX Command Protocol is provided.

2 Legal Considerations

The Bitshark FMC-1RX card is distributed all over the world. Each country has its own laws governing reception of radio frequencies. The user of the Bitshark FMC-1RX card and associated software is solely responsible for insuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used. Many countries, including the United States, prohibit the reception of certain frequency bands, or receiving certain transmissions without proper authorization. Again, the user is solely responsible for the user's own actions.

3 Proper Care and Handling

The Bitshark FMC-1RX card is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the FMC-1RX can easily cause it to become non-functional, so Epiq Solutions cannot make any guarantees as to its function over time. In particular, a list of actions that are very likely to cause damage to the card include the following:

- Adding or removing the card to a host system while the host system is powered up
- Allowing metal objects to touch the circuit board (on either side) while it is powered up
- Connecting a transmitter into the FMC-1RX card without proper attenuation
- Handling the FMC-1RX card without proper static precautions (ESD protection)
- Connecting a cable to either the external clock out or external clock in signal ports while the FMC-1RX is powered up

The above list is not comprehensive, and experience with the appropriate measures for handling unhoused electronic devices is required.

4 References

[1] Epiq Solutions Website:
http://www.epiq-solutions.com

[2] VITA 57 Specification:
http://www.vita.com/specifications.html

[3] Linear Technology LTC2267-14 dual A/D converter datasheet:
http://cds.linear.com/docs/Datasheet/22687614fa.pdf

[4] Skytraq VENUS634SMD GPS receiver datasheet:
http://www.sparkfun.com/datasheets/GPS/Modules/Skytraq-Venus634FLPx_DS_v051.pdf

[5] Ellingson, S.W. “Correcting I-Q Imbalance in Direct Conversion Receivers ” 2003
http://argus.naapo.org/~rchilders/swe_argus_pubs/iqbal.pdf

[6] Bitshark FMC-1RX Reference Design User's Manual
http://www.epiq-solutions.com

5 Overview

The Bitshark FMC-1RX card is a broadband, high performance, single tuner RF receiver card that is compliant with the FPGA Mezzanine Card (FMC/VITA 57) digital interface standard [2]. It supports a tuning range between 300 MHz and 4 GHz, while supporting user-defined channel bandwidths up to 50 MHz. Digitized baseband I/Q samples are provided by dual A/D converters, and are accessible on the FMC interface for use by the host system. The FMC-1RX card is targeted at commercial wireless radio applications, supporting a variety of common RF frequency bands.

The Bitshark FMC-1RX provides unprecedented radio functionality in a small form factor, allowing an end user to concentrate on their signal processing tasks instead of the challenges of configuring and interfacing to an RF front end. The key features of the FMC-1RX card include the following:

- FMC/VITA 57 digital interface for integration with a variety of FPGA development platforms
- Direct conversion (zero-IF) architecture
- Single RF tuner covering 300 MHz to 4 GHz
- Configurable baseband channel filtering supporting RF bandwidths up to 50 MHz
- Integrated high stability 26 MHz TCVCXO
- Dual 14-bit 105 Msample/sec A/D converters
- Low jitter programmable A/D sample clock with 1 Hertz resolution
- Integrated GPS receiver with 1 PPS signal
- UART configuration interface using an ASCII-based command protocol
- Phase-coherent reception with multiple FMC-1RX cards
- Low power consumption (typically consumes 500 mA from a 4V supply)

A block diagram of the Bitshark FMC-1RX is shown in Figure 1.

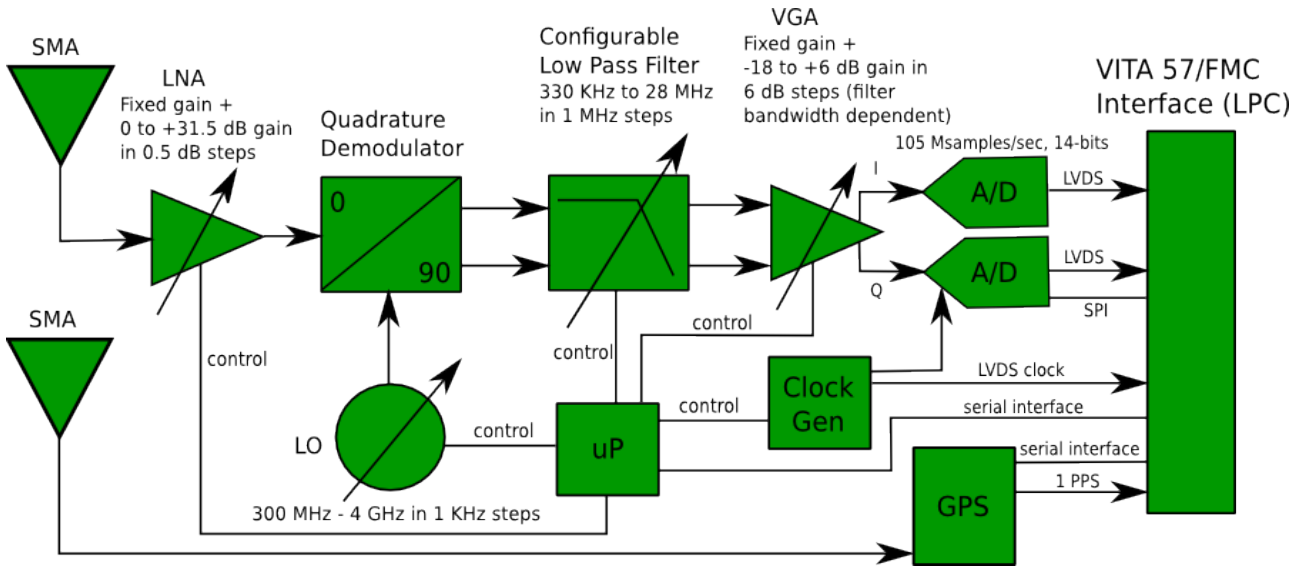

Figure 1: Block diagram of the Bitshark FMC-1RX card

6 FMC-1RX Interfaces

The Bitshark FMC-1RX utilizes the VITA 57/FPGA Mezzanine Card (FMC) digital interface to communicate with a host carrier card.. This standardized interface provides pin assignments for single-ended I/O, differential I/O, gigabit serial I/O, clock I/O, and power rails which can be utilized by an FMC card.

The FMC-1RX card utilizes single-ended I/O, differential I/O, clock I/O, and the available power rails provided by the FMC specification. Additional user I/O signals are also accessible on the FMC-1RX card. A complete description of both the FMC pin assignments as well as the available user I/O signals is presented in the following sections.

6.1 RF Input Interface

The FMC-1RX card has a single RF input port for receiving RF signals. This port is provided by the SMA connector located on the front panel I/O of the card (see Image 1). An external passive antenna can be connected to this interface. This input port presents a 50 ohm RF interface.

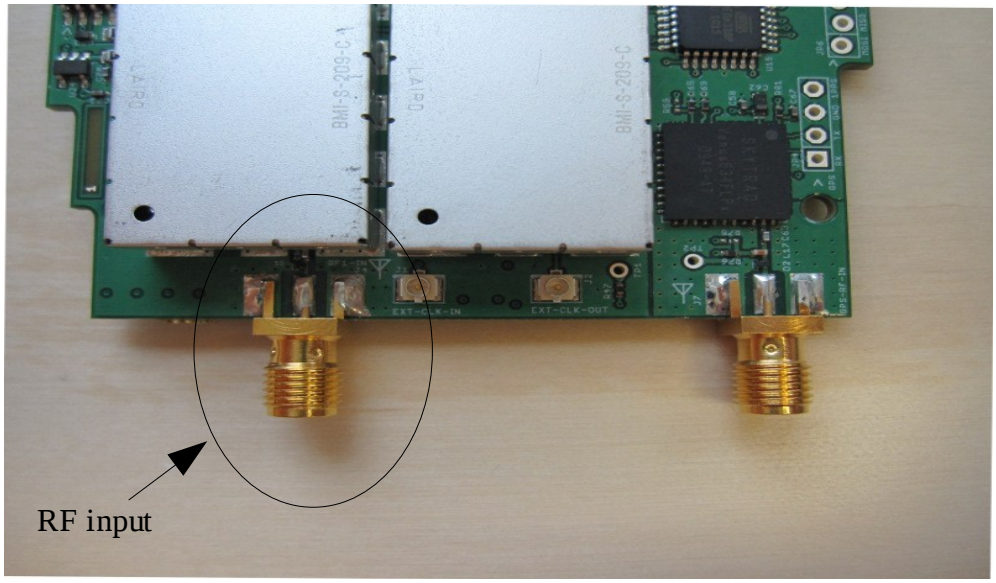

Image 1: RF input for receiving RF signals

6.2 Serial Port Interface

The FMC-1RX card provides a serial port (UART) interface for configuring the operation of the board. All RF and baseband parameters can be configured through this interface using the Bitshark FMC-1RX Command Protocol, a simple ASCII-based command set. The complete specification of this command protocol can be found in Section 8.

The serial port interface is accessible through single-ended I/O pins on the FMC connector. The following table

provides the pin assignments for the serial port interface.

Signal Name	Signal Type	FMC Pin Location	FMC Pin Name	Voltage Ref	Description
HOST_UART_TX	Single-ended	D27	LA26_N	Vadj	UART transmit line for sending data to the FMC-1RX card
HOST_UART_RX	Single-ended	C26	LA27_P	Vadj	UART receive line for receiving data from the FMC-1RX card

Table 1: Serial port interface signals accessible to the host through the FMC interface

The UART signals associated with this serial port interface are also available on 0.1" header pins on the FMC-1RX. This provides a means for a user to interact with the board directly using a an external terminal emulator (such as HyperTerminal or Minicom). These signals use 3V logic, but are 3.3V tolerant. The location of these header pins is shown in Image 2. Warning: driving this serial interface from an external terminal while simultaneously driving these pins from the host FMC interface may damage the board.

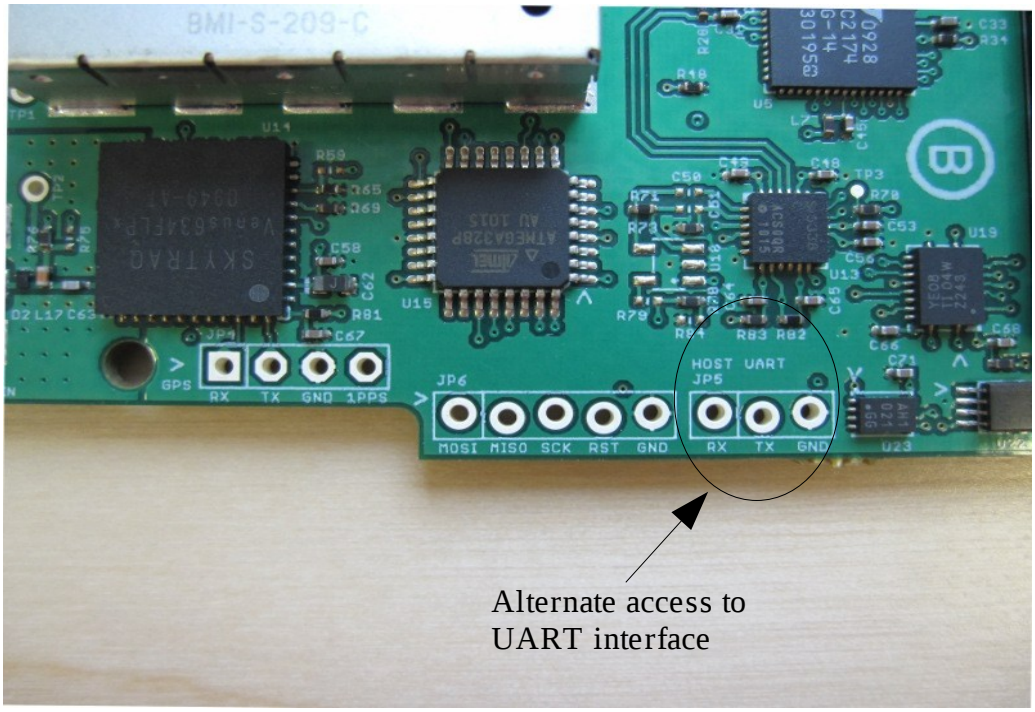

Image 2: Host UART signals available for external access

6.3 A/D Interface

The FMC-1RX card provides an interface to the on-board A/D converters (Linear Technology LTC2267-14) to allow digitized baseband samples to be transferred to the host system. These samples are transferred to the host system using multiple LVDS signal pairs. In addition, a SPI bus control interface is used to configure the A/D

converters. A complete description of the LVDS signals, as well as the SPI bus control interface, can be found in the datasheet for the LTC2267-14 [3]. The following table provides the pin assignments for the A/D interface.

Signal Name	Signal Type	FMC Pin Location	FMC Pin Name	Voltage Ref	Description
AD_FR+	LVDS (clock)	G6	LA00_P_CC	2.5V LVDS	Positive side of the LVDS frame clock indicating the start of a new sample
AD_FR-	LVDS (clock)	G7	LA00_N_CC	2.5V LVDS	Negative side of the LVDS frame clock indicating the start of a new sample
AD_DCO+	LVDS (clock)	D8	LA01_P_CC	2.5V LVDS	Positive side of the LVDS bit clock for each digital sample
AD_DCO-	LVDS (clock)	D9	LA01_N_CC	2.5V LVDS	Negative side of the LVDS bit clock for each digital sample
AD_DIG_I_1A+	LVDS	G15	LA12_P	2.5V LVDS	Positive side of the LVDS pair used to transfer lane A of the 'I' channel
AD_DIG_I_1A-	LVDS	G16	LA12_N	2.5V LVDS	Negative side of the LVDS pair used to transfer lane A of the 'I' channel
AD_DIG_I_1B+	LVDS	G12	LA08_P	2.5V LVDS	Positive side of the LVDS pair used to transfer lane B of the 'I' channel
AD_DIG_I_1B-	LVDS	G13	LA08_N	2.5V LVDS	Negative side of the LVDS pair used to transfer lane B of the 'I' channel
AD_DIG_Q_2A+	LVDS	H19	LA15_P	2.5V LVDS	Positive side of the LVDS pair used to transfer lane A of the 'Q' channel
AD_DIG_Q_2A-	LVDS	H20	LA15_N	2.5V LVDS	Negative side of the LVDS pair used to transfer lane A of the 'Q' channel
AD_DIG_Q_2B+	LVDS	H16	LA11_P	2.5V LVDS	Positive side of the LVDS pair used to transfer lane B of the 'Q' channel
AD_DIG_Q_2B-	LVDS	H17	LA11_N	2.5V LVDS	Negative side of the LVDS pair used to transfer lane B of the 'Q' channel
AD_CS_BAR	Single-ended	G24	LA22_P	Vadj	SPI chip select
AD_SCK	Single-ended	G25	LA22_N	Vadj	SPI clock
AD_SDI	Single-ended	D23	LA23_P	Vadj	SPI data in
AD_SDO	Single-ended	D24	LA23_N	Vadj	SPI data out

Table 2: A/D converter signals accessible to the host through the FMC interface

6.4 GPS Interface

The FMC-1RX card contains a complete GPS receiver for providing both timing and position information during operation. The GPS receiver utilized on the card is the Skytraq Venus634SMD [4]. An SMA connector is provided on the front panel I/O interface which accepts an external GPS antenna (see Image 3). By default, a 3V DC bias signal is provided on the RF input line to support active GPS antennas. An active GPS antenna is recommended for optimal operation. This bias voltage can also be provided by an external power, as well as disabled if required. Contact Epiq Solutions for details on alternate bias voltage options.

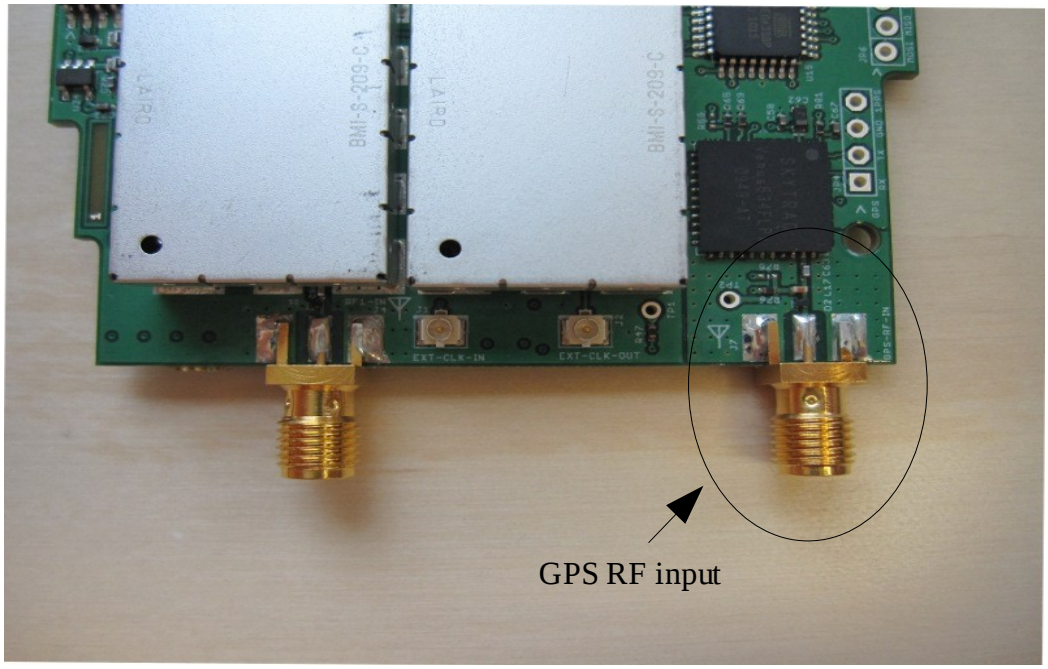

Image 3: GPS RF input for external GPS antenna

The GPS receiver provides a data interface through a standard UART. By default, NMEA sentences are sent from the FMC-1RX card to the FMC host through this interface at 9600 baud, N-8-1 using single-ended I/O. In addition, the 1PPS signal and a soft reset signal from the GPS receiver are made available to the FMC host. The following table provides the pin assignments for the GPS interface.

Signal Name	Signal Type	FMC Pin Location	FMC Pin Name	Voltage Ref	Description
GPS_UART_TX	Single-ended	D26	LA26_P	Vadj	UART transmit line for sending data from the GPS receiver to the FPGA host
GPS_UART_RX	Single-ended	G28	LA25_N	Vadj	UART receive line for receiving serial commands from the FPGA host
GPS_1PPS	Single-ended	G27	LA25_P	Vadj	One Pulse Per Second signal (only active after a GPS fix has been acquired)
GPS_RESET_BAR	Single-ended	C27	LA27_N	Vadj	Active-low reset signal to allow the FMC host to perform a soft reset of the GPS receiver

Table 3: GPS signals accessible to the host through the FMC interface

The UART and 1PPS signals associated with the GPS interface are also available on 0.1" header pins on the FMC-1RX. This provides an alternate means for a user to access the data provided by the GPS receiver. These signals use 3V logic, but are 3.3V tolerant. The location of these header pins is shown in Image 4. Warning: driving this GPS interface while simultaneously driving these pins from the host FMC interface may damage the board.

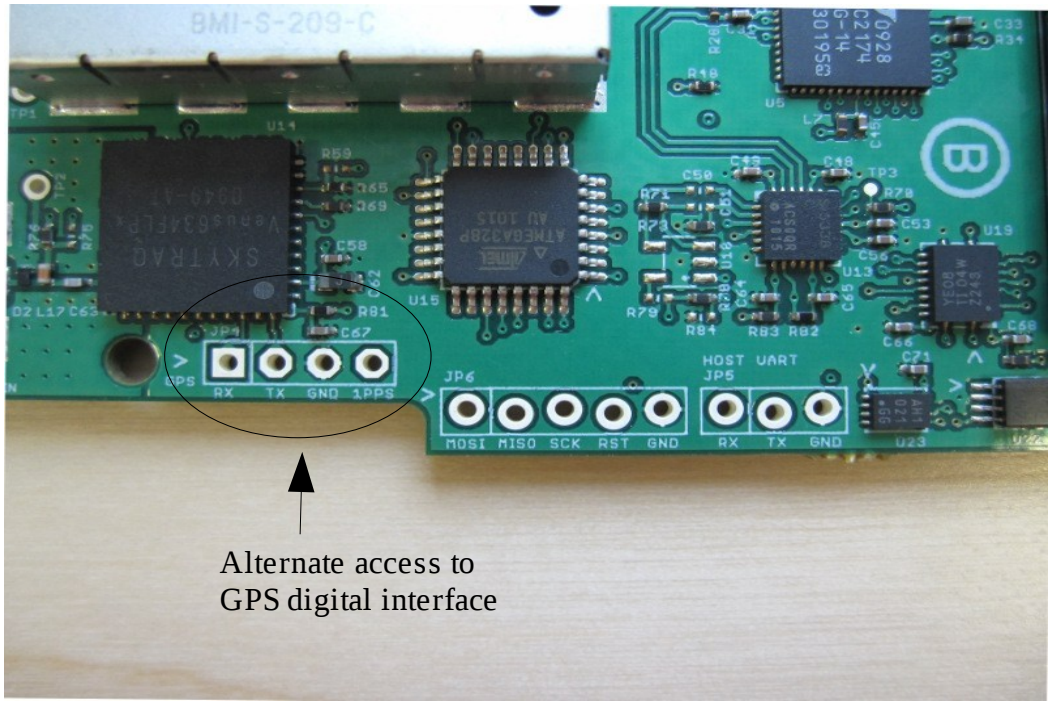

Image 4: External access to GPS digital interface signals

An LED indicator (D201, shown in Image 5) is provided by the FMC-1RX to indicate the status of the GPS receiver. This LED is illuminated (100% duty cycle "on") while searching for a GPS fix. Once a GPS fix has

been acquired, D201 will blink at a rate of 1 Hz, with a 50% duty cycle.

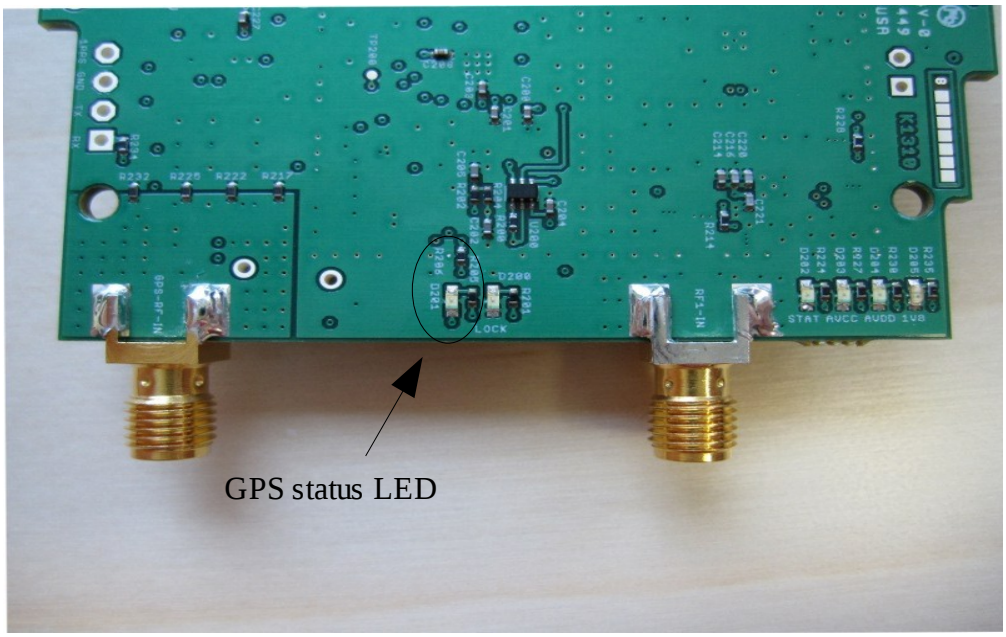

Image 5: Location of GPS status LED

6.5 Clock Interface

The FMC-1RX card contains an on-board 26 MHz temperature compensated, voltage controlled crystal oscillator (TCVCXO) which provides the default reference clock for both the RF front end as well as the A/D converters. It also serves as the reference for an additional user programmable clock that is accessible on the FMC digital interface. An on-board DAC provides a warp voltage to the TCVCXO to allow for fine-grained steps in the reference clock frequency. Warping the reference clock is accomplished through commands sent over the serial port interface. For more information on these commands, see the Bitshark FMC-1RX Command Protocol specification in Section 8.

A complete clock tree for the FMC-1RX is shown in Figure 2.

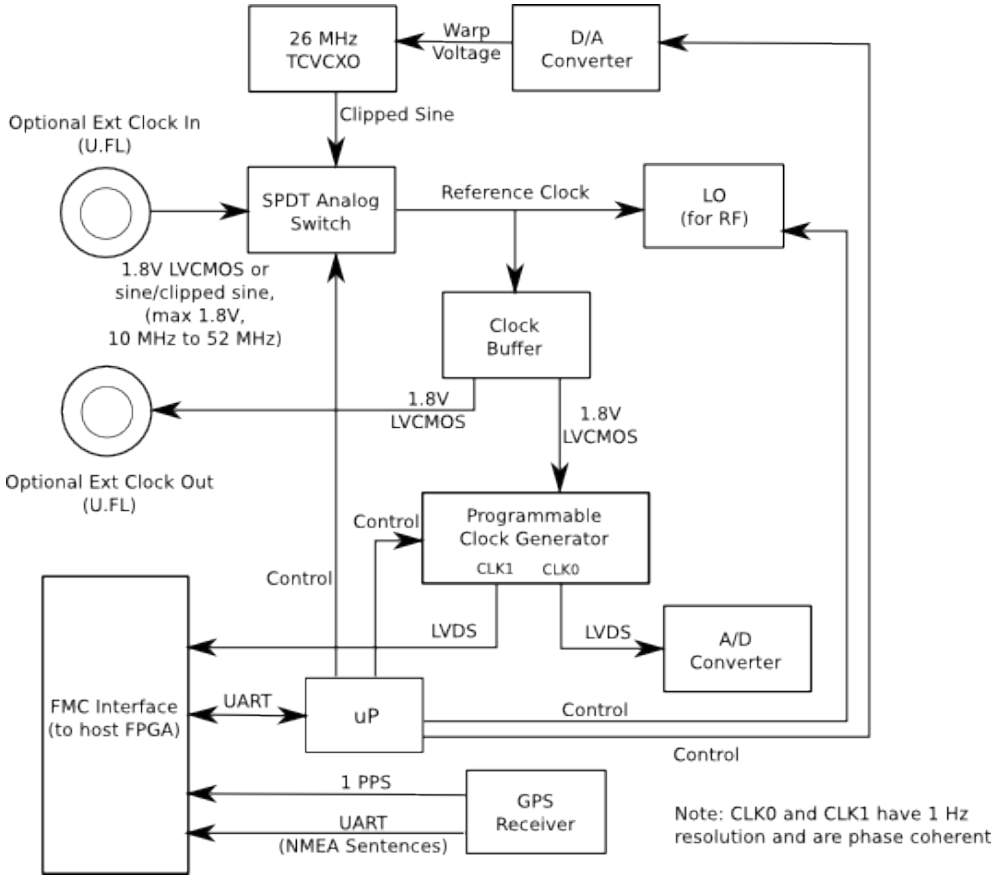

Figure 2: Clock tree of the Bitshark FMC-1RX card

The FMC-1RX provides external access to the reference clock used by the card on a U.FL connector (EXT_CLK_OUT) located near the front panel I/O (see Image 6). This signal is buffered from the actual reference clock used by the card, and can drive a maximum load of 50 pF capacitance.

By default, the FMC-1RX utilizes the on-board 26 MHz TCVCXO. However, an external clock signal can also be provided to serve as the reference clock for the card. This requires the user to supply this external clock signal to the U.FL connector (EXT_CLK_IN) located near the front panel I/O (see Image 6), as well as setting the proper "clock scheme" through the Bitshark FMC-1RX Command Protocol. The requirements of this external reference clock signal are listed below:

- Minimum Frequency: 10 MHz
- Maximum Frequency: 52 MHz
- Signal Type: Sine Wave, Clipped Sine Wave, or 1.8V LVCMOS, single-ended, DC coupled
- Max Input Voltage: 1.8V
- Clock input impedance: 6K Ω
- Clock input capacitance: 4.75 pF

The EXT_CLK_OUT signal from one FMC-1RX card can drive the EXT_CLK_IN from another FMC-1RX

card to allow fully phase coherent operation between receivers. Multiple cards can be daisy-chained together in this manner to extend the number of receivers based on application requirements. In this configuration, one card utilizes the default reference clock configuration (on-board 26 MHz TCVCXO), while all other cards in the chain are configured for using an external reference clock.

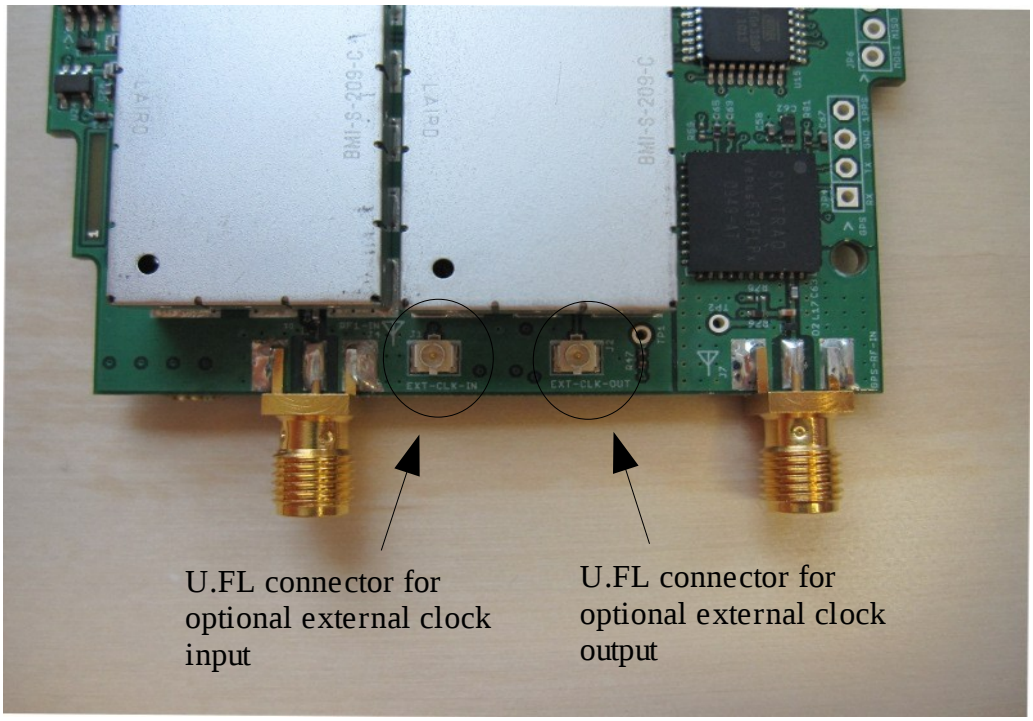

Image 6: Location of "external clock out" and "external clock in" U.FL connectors

Lastly, the FMC interface provides access to a user programmable clock signal generated from the on-board programmable clock generator. This programmable clock generator provides an LVDS clock signal to the FMC connector for use by the host FPGA. This clock is phase coherent to the reference clock driving the RF front end, as well as the A/D sample clock. The minimum frequency of this clock is 5 MHz, and the maximum frequency of this clock is 200 MHz, with a resolution of 1 Hz. This clock signal is an optional output and can be turned off. The following table provides the pin assignments for the user programmable clock interface.

Signal Name	Signal Type	FMC Pin Location	FMC Pin Name	Voltage Ref	Description
PROG_CLK1_+	LVDS	H4	CLK0_M2C_P	2.5V LVDS	Positive side of the LVDS pair used for the programmable clock
PROG_CLK1_-	LVDS	H5	CLK0_M2C_N	2.5V LDVS	Negative side of the LVDS pair used for the programmable clock

Table 4: User programmable clock signal accessible to the host through the FMC interface

For details on the for configuring this user programmable clock, see the Bitshark FMC-1RX Command Protocol specification in Section 8.

6.6 General Purpose I/O Interface

The FMC-1RX card provides an interface to three single-ended GPIO signals originating from the FMC host. These signals are accessible through test pads on the top side of the card (see Image 7). The following table provides the pin assignments for the general purpose I/O pins.

Signal Name	Signal Type	FMC Pin Location	FMC Pin Name	Voltage Ref	Description
GPIO_1 (TB4)	Single-ended	C11	LA06_N	Vadj	GPIO line for end user application
GPIO_2 (TP5)	Single-ended	C10	LA06_P	Vadj	GPIO line for end user application
GPIO_3 (TP6)	Single-ended	D12	LA05_N	Vadj	GPIO line for end user application

Table 5: General purpose I/O signals accessible to the host through the FMC interface

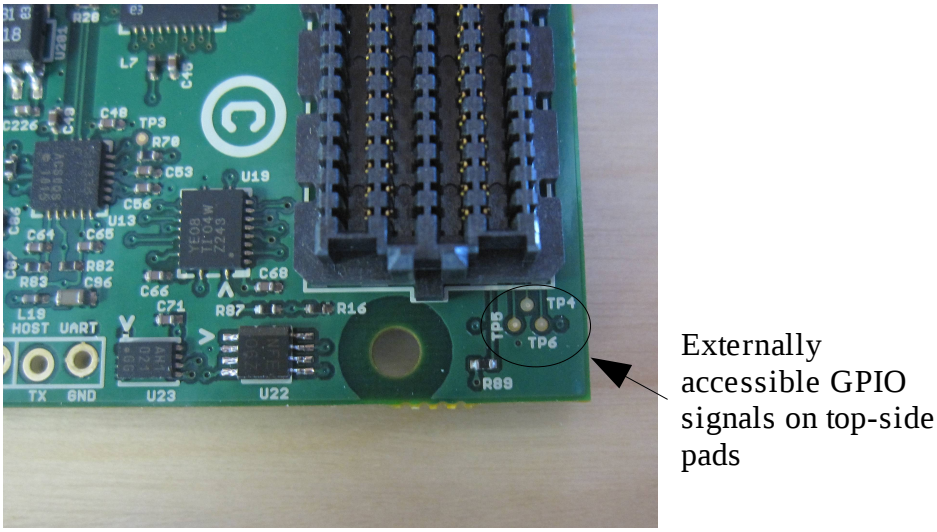

Image 7: Location of GPIO signals

6.7 LED Interface

The FMC-1RX card provides multiple status LEDs that can be used to determine the state of the card. These signals are not routed to the FMC interface, but are useful to an end user to provide immediate feedback regarding the state of the card. Table 6 provides a description of the available LEDs. An image showing the placement of the LEDs can be found in Image 8.

LED Name	Designator	Description
LO synthesizer PLL lock	D200	Indicates if the PLL within the LO synthesizer has locked: Off: PLL has not locked On: PLL has locked
GPS Fix State	D201	Indication of GPS fix: 100% duty cycle on: GPS is searching for a fix 50% duty cycle: GPS has acquired a fix and is tracking
<Reserved>	D202	Reserved for future use
AVcc power ready	D203	Indicates if the 3V AVcc rail is available or not: Off: 3V AVcc rail is not available On: 3V AVcc rail is available
AVdd power ready	D204	Indicates if the 3V AVdd rail is available or not: Off: 3V AVdd rail is not available On: 3V AVdd rail is available
1.8V power ready	D205	Indicates if the 1.8V rail is available or not (Note: this LED will typically be very dimly lit in the “On” state): Off: 1.8V rail is not available On: 1.8V rail is available

Table 6: Description of LED signals

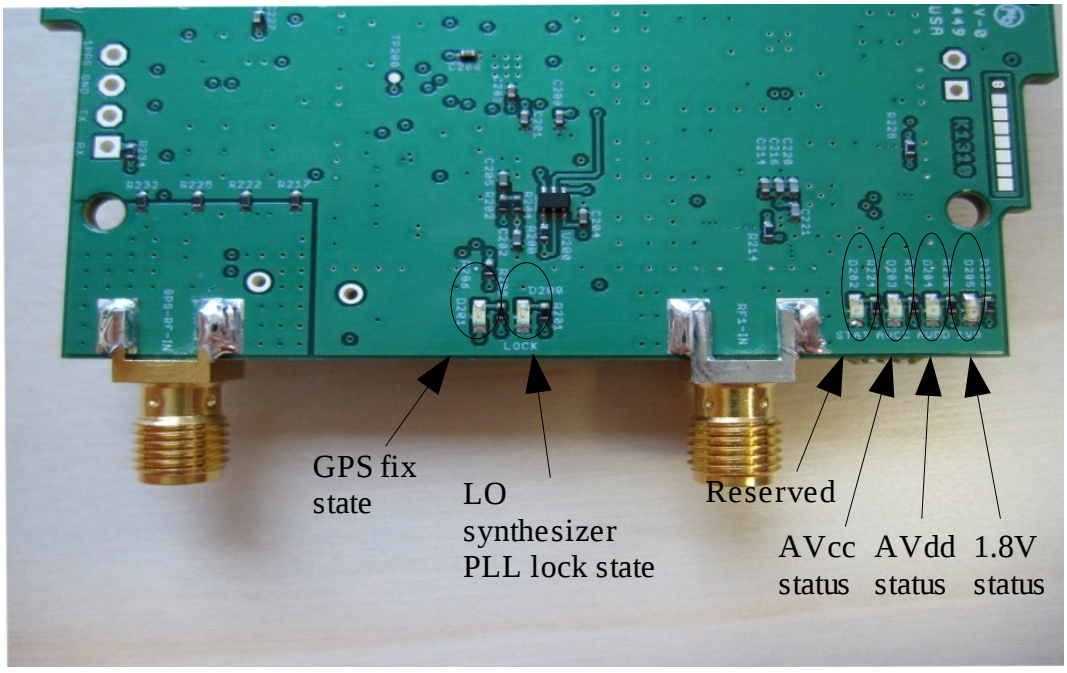

Image 8: Location of all available LED signals

6.8 Power Interface

The FMC-1RX card derives its power from the voltage rails provided through the FMC interface. The card utilizes the standard 12VDC rail available on the FMC interface to generate the voltages necessary to drive the various on-board circuitry. A single control line (SYS_PWR_EN) from the FPGA provides a means to control whether or not the power supplies on the card are enabled or not. In addition, the Vadj rail is used to drive an I/O voltage translator on the card to allow the FMC-1RX to work with FMC carrier boards supporting Vadj voltages from 1.2V up to 3.0V. Typical current consumption on this 12VDC rail provided by the FMC interface is 0.250 mA. Note: the FMC-1RX provides its own on-board power regulation, converting the 12 VDC down to 4VDC using a switching power supply, followed by additional regulation using low-dropout (LDO) linear regulators for the noise sensitive portions of the card.

Signal Name	**Signal Type**	**FMC Pin Location**	**FMC Pin Name**	**Voltage Ref**	**Description**
SYS_PWR_EN	Single-ended	D11	LA06_N	Vadj	Active-high enable line from the FPGA to control whether or not the power supplies on the FMC-1RX card are enabled
+12V	Voltage Rail	C35, C37	12P0V	N/A	12V DC rail
Vadj	Voltage Rail	E39, F40, G39, H40	VADJ	N/A	Adjustable voltage rail for I/O
GND	Ground	(multiple)	(multiple)	N/A	Ground reference

Table 7: Power signals provided by the host through the FMC interface

7 Mechanical

The complete specification for the mechanical dimensions of an FMC card can be found in [2]. The Bitshark FMC-1RX is compliant with a subset of the VITA 57 mechanical requirements. The form factor of the card meets all requirements of the specification with the exception of the maximum Z dimension of the "IO Area" as specified by VITA 57. This is due to the inclusion of RF shields used to prevent EMI. The RF shields extend approximately 5 mm past the specified depth of the "IO Area". It is important for an end user to verify that there are no components on the host carrier card that will make contact with the RF shielding. The FMC-1RX card can be purchased without shields to be fully compliant with the VITA 57 specification. Please contact Epiq Solutions [1] for details.

A parts placement diagram of the top side of the FMC-1RX is shown in Image 9. A parts placement diagram of the bottom side of the FMC-1RX is shown in Image 10.

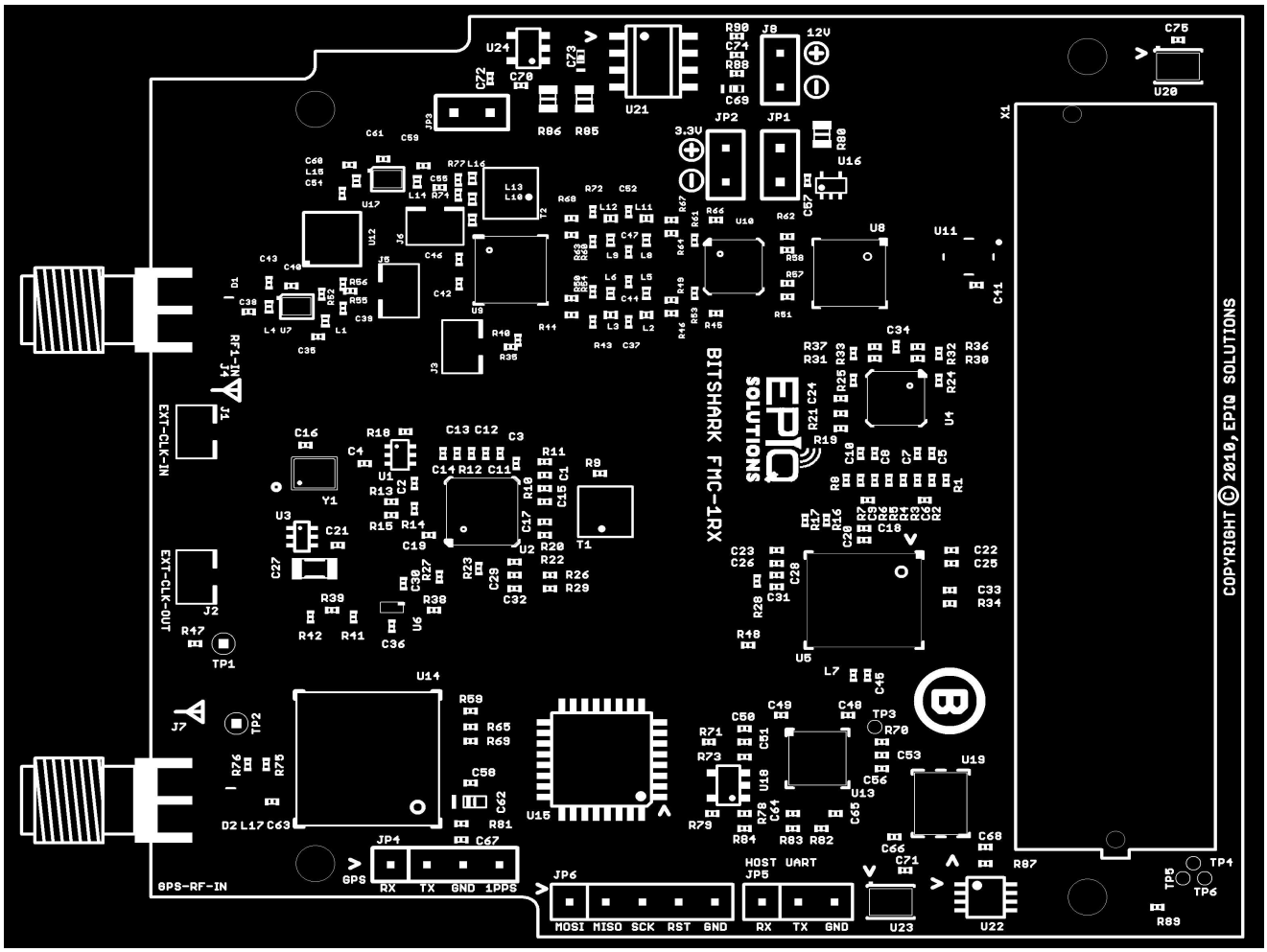

Image 9: Top side parts placement diagram

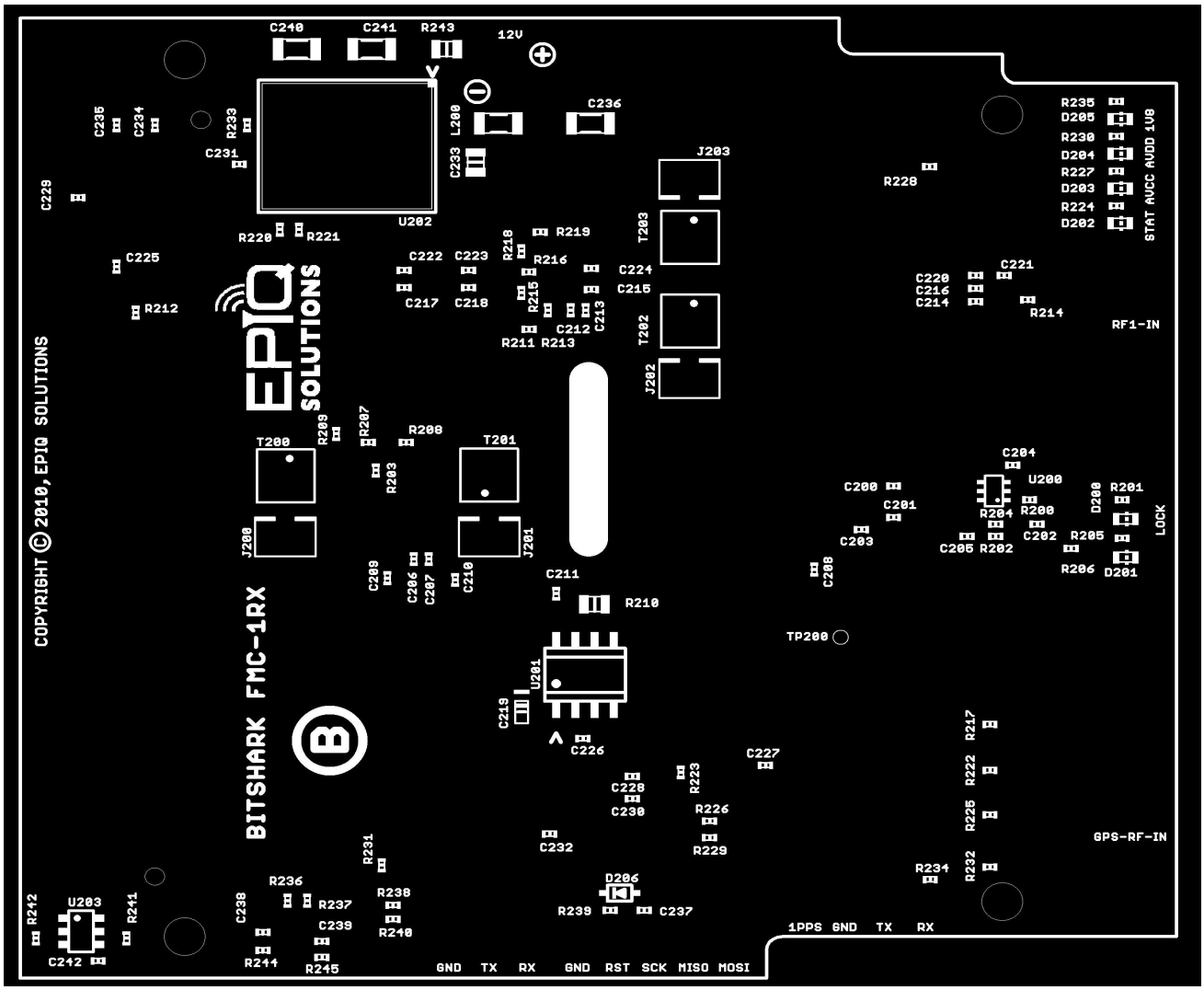

Image 10: Bottom side parts placement diagram

8 Command Protocol Specification

8.1 Overview

The Bitshark FMC-1RX utilizes a UART control interface to allow a user to configure the operation of the card. There are three electrical signals associated with this UART: transmit (HOST_UART_TX), receive (HOST_UART_RX), and ground (GND). All signals are referenced with respect to the FMC host (i.e., the HOST_UART_TX signal is a transmit signal from the FMC host to the FMC-1RX card). The high-level requirements of this interface are listed below:

- The UART interface operates at 9600 baud, with 8 data bits, 1 stop bit, no parity, and no flow control.
- Commands are sent and received from the FMC-1RX card as simple human-readable ASCII text.
- The ASCII text command interface is case-insensitive, as all commands are converted to uppercase by the FMC-1RX upon reception.
- The FMC-1RX card immediately echos all received characters back over its UART interface to confirm reception.
- All commands must be terminated with either a '\r' (carriage return) character or a '\n' (newline) character.
- Upon reception of either the '\r' or '\n' terminating character, the FMC-1RX card will echo back “\r\n”. This is the only case where the echo is not exactly what is received.
- Responses from the FMC-1RX consist of one or more lines that are terminated with a “\r\n” character sequence.
- All commands result in a response that contains, at minimum, an ACK or NCK indicating the command was acknowledged or not acknowledged.
- Information messages may be sent by the FMC-1RX as part of a response (in addition to the actual contents of the response). These messages begin with “I:”, contain non-critical details of the response, and terminate in “\r\n”.
- Error messages may be sent by the FMC-1RX as part of a response. These messages begin with “E:”, contain an error message and terminate in “\r\n”.
- All commands, regardless of success or failure, result in a '>' character (without a terminating “\r\n”) being sent by the FMC-1RX card as the final character in a response to indicate that it is ready for a new command.

8.2 Command Specification

8.2.1 Read

Name	read
Format	read <parameter>
Description	The “read” command is used to read the currently set value for a specific parameter on the FMC-1RX card.
Example	>read freq

Usage:	ACK 1972.5 MHz >

8.2.2 Write

Name	write
Format	write <parameter> <value> <optional value 1> <optional value 2> <...>
Description	The “write” command is used to update the currently set value for a specific parameter on the FMC-1RX card.
Example Usage:	>write freq 2400.020 ACK >

8.2.3 Help

Name	help
Format	help
Description	The “help” command is used to provide a description of all supported commands and parameters for the FMC-1RX, along with a brief set of examples.
Example Usage:	>help ACK <text describing supported commands and parameters, along with examples> >

8.3 Parameter Specification

8.3.1 Frequency

Name	freq
Format	read freq write freq <desired frequency in MHz>
Description	The freq parameter defines the currently tuned RF frequency in MHz. This parameter has a range from 300 MHz to 4000 MHz, with a resolution of 1 KHz. The default value of this parameter is 2000.0 MHz.
Example Usage:	>read freq ACK 1972.5 MHz > >write freq 2400.032 ACK >

8.3.2 RF Gain

Name	rfgain
Format	read rfgain write rfgain <desired gain in dB>
Description	The rfgain parameter provides control over the amount of gain used in the RF front end, measured in dB. This gain is in addition to fixed RF gain in the front end. This parameter has a range from 0 dB to 31.5 dB, in 0.5 dB steps. The default value of this parameter is 15 dB.
Example Usage:	>read rfgain ACK 20.5 dB > >write rfgain 31.5 ACK >

8.3.3 Baseband Gain

Name	bbgain
Format	read bbgain write bbgain <desired gain in dB>
Description	The bbgain parameter provides control over the amount of gain used in the baseband, measured in dB. This gain is in addition to fixed baseband gain in the front end. The range of this

	parameter is dependent on the currently set chanbw parameter. The following bbgain values are available: • 660 KHz <= chanbw < 8000 KHz: 0 dB, 6 dB • 8000 KHz <= chanbw < 16000 KHz: -6 dB, 0 dB, 6 dB • 16000 KHz <= chanbw < 32000 KHz: -12 dB, -6 dB, 0 dB, 6 dB • 32000 KHz <= chanbw <= 56000 KHz: -18 dB, -12 dB, -6 dB, 0 dB, 6 dB The default value of this parameter is 6 dB.
Example Usage:	>read bbgain ACK 0 dB > >write bbgain -12 E: gain not supported for current chanbw NCK > >write bbgain 6 ACK >

8.3.4 Channel Bandwidth

Name	chanbw
Format	read chanbw write chanbw <desired channel bandwidth in KHz>
Description	The chanbw parameter provides control of the corner frequency of the baseband analog low-pass filter. Typically, the RF signal of interest is downconverted and centered at 0 Hz (zero-IF). The baseband low-pass filter is used to attenuate additional signals outside of the channel bandwidth of interest. In the standard zero-IF usage, the chanbw parameter defines 2x the value of the low-pass filter corner frequency. This parameter supports the following range of values: 660 KHz, 1320 KHz, 2000 KHz to 56000 KHz in 1000 KHz steps. The default value of this parameter is 56000 KHz.
Example Usage:	>read chanbw ACK 4000 KHz > >write chanbw 8000 KHz ACK >

8.3.5 A/D Sample Clock

Name	adclk
Format	read adclk write adclk <desired sample rate in hertz>
Description	The adclk parameter provides control over the sample rate clock used to digitize samples in the A/D converter. This parameter has a range of 5000000 Hz to 105000000 Hz, with a resolution of 1 Hz. The default value of this parameter is 5000000 Hz.
Example Usage:	>read adclk ACK 7680000 Hz > >write adclk 104000000 ACK >

8.3.6 IQ Imbalance Calibration

Name	iqcal
Format	read iqcal <RF frequency in MHz> write iqcal <RF frequency in MHz> <16-bit 'C' parameter> <16-bit 'D' parameter>
Description	The iqcal parameters provide calibration values to optimize the I/Q imbalance of the received signal, and thus improving the sideband suppression. These parameters are used in conjunction with the IQ imbalance correction block in the host FPGA to provide the desired balancing operation. The algorithm used for this imbalance correction can be found in [5]. Each FMC-1RX card is calibrated at production time from 300 MHz to 4 GHz in 50 MHz increments to determine the the 'C' and 'D' parameters (see [5] for details on these parameters]. The 'C' and 'D' parameters are then stored in EEPROM on the FMC-1RX card. A typical end-user application would read these parameters out at start-up, and would write these calibration parameters to the associated IQ imbalance correction block in the host FPGA as each RF frequency of interest is tuned. Additional details of how this correction block in the FPGA operates can be found in [6]. Note: under normal operating conditions, it shouldn't be necessary to perform a write operation on the iqcal data. The only time this would be necessary is in the case where an end-user would want to perform an update to the calibration table.
Example Usage:	>read iqcal 830.0 ACK 0x03F4 0x0001 > >write iqcal 1972.5 0x0002 0x0001 ACK

	>

8.3.7 Temperature Sensor

Name	temp
Format	read temp (write operation is not allowed)
Description	The temp parameters provides a current temperature reading of the FMC-1RX card in degrees Celsius.
Example Usage:	>read temp ACK 35 deg C >

8.3.8 User Programmable Clock

Name	userclk
Format	read userclk write userclk <desired clock rate in hertz>
Description	The userclk parameter provides control over a user programmable clock that is accessible on the FMC interface for use by the host FPGA. This clock is phase coherent with the reference clock used on the FMC-1RX. This parameter has a range of 5000000 Hz to 200000000 Hz, with a resolution of 1 Hz. The userclock can be disabled by setting the parameter to 0 Hz. The default value of this parameter is 0 Hz (disabled).
Example Usage:	>read userclk ACK 43600000 Hz > >write userclk 156000000 ACK > >write userclk 0 ACK >

8.3.9 Clock

Name	clock
Format	read clock write clock <ref clock source> <ref clock frequency in MHz>
Description	The clock parameter is used to control the source and frequency of the reference clock used by

	the FMC-1RX. The <ref clock source> field allows for selection between the on-board 26 MHz TCVCXO and the external clock input. The following range of values are supported for <ref clock source>: • 0: external clock input • 1: on-board 26 MHz TCVCXO (default) The <ref clock frequency in MHz> field allows for definition of the reference clock frequency. By default, the FMC-1RX uses the on-board TCVCXO, which operates at 26 MHz. When the <ref clock source> field is set to 0, the <ref clock frequency in MHz> parameter can range from 10 MHz to 52 MHz.
Example Usage:	>read clock ACK 1 26.0 MHz > >write clock 0 52.0 ACK >

8.3.10 Clock Warp Voltage

Name	clkwarp
Format	read clkwarp write clkwarp <warp voltage in DAC steps>
Description	The clkwarp parameter is used to control the value of the voltage used to warp the on-board TCVCXO reference clock. This provides fine-grained control of the reference clock frequency over a limited range. The warp voltage is generated by a 12-bit DAC which is capable of outputting voltages between 0V and 3.3V. The warp voltage for the TCVCXO can be between 0.5 V and 2.5V, which corresponds to DAC values of 683 and 3413. Note: modifications to the warp voltage will effect all clocks derived from the reference clock, which include the RF center frequency, the A/D sample clock, and the user programmable clock. The resultant modification in frequency to the derived clock will depend on the current value of the derived clock.
Example Usage:	>read clkwarp ACK 2430 > >write clkwarp 35 E: warp value out of range NCK > >write clkwarp 988 ACK

	>