

EVB8700 User Manual



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1 Introduction

The LAN8700 is a low-power, small form factor, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN8700 requires only a single +3.3v supply, and has an integrated +1.8v supply to run the core digital logic.

The EVB8700 is a customer evaluation board that interfaces a standard 40 pin MII connector from an existing MAC controller to the SMSC LAN8700 Ethernet PHY, and out to an RJ-45 Ethernet Jack for 10/100 connectivity.

1.1 References

Concepts and material available in the following documents may be helpful when reading this document.

Table 1.1 References

DOCUMENT	LOCATION
<ul style="list-style-type: none">■ SMSC LAN8700 Datasheet■ SMSC LAN8187 Datasheet	http://www.smSC.com/main/datasheet.html
<ul style="list-style-type: none">■ AN13-9 Migrating from the LAN83C183 10/100 PHY to the LAN83C185 10/100 PHY■ AN13-2 Scalable Reference Design for Migrating from the SMSC LAN83C185 Non Auto MDIX to a Future SMSC LAN8187 HP Auto MDIX Configuration■ AN8-13 Suggested Magnetics	http://www.smSC.com/main/appnotes.html

2 Details

The EVB8700 shown in [Figure 2.1](#) is a Daughter Card designed to plug into a user's test system, using the 40 pin MII connector. The MII connector is an AMP 40 pin Right Angle through hole MII connector, PN AMP-174218-2, reference designator P1. The mating connector is PN AMP 174217-2. The pinout for the plug is shown in [Table 2.8](#).

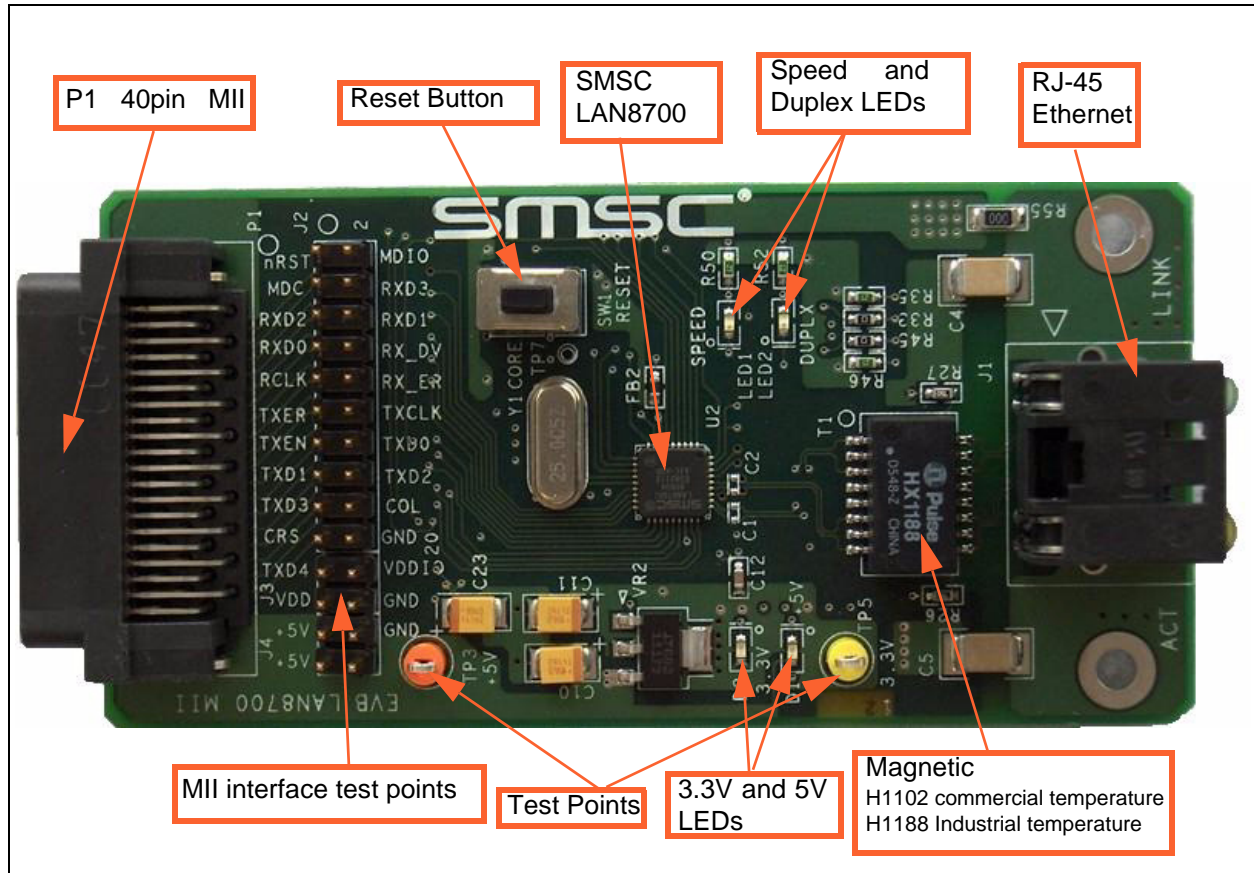


Figure 2.1 Top View of the EVB8700

Note: Actual board may vary.

2.1 Power

Power is provided to the on board +3.3v regulator by the +5v power coming from the MII connector P1. Standby power of +5v can be supplied externally by the test point loop at TP3 with ground connected to pin 20 of header J2.

2.1.1 +3.3 Volt Power Supply

The EVB8700 has an on-board step down DC-DC +3.3v power supply regulator and uses the +5v input from the MII.

2.2 Configuration

This section documents the configuration options available on the SMSC EVB8700.

2.2.1 PHY Address and LEDs

Resistors R50, R51, R45, R46, R44, R47, R33, R35, R34, R36, R52, and R53 are used to set the PHY address according to [Table 2.8](#).

Table 2.1 PHY address and LED configuration

NET NAME	PHY ADDRESS		LED OUTPUT	DESCRIPTION
SPEED100LED	LSB PHYAD0 = 1 LSB PHYAD0 = 0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Depopulate [R37, R51] Populate [R50] LED1 orient up Populate [R37, R51] Depopulate [R50] LED1 orient down
LINKLED	PHYAD1=1 PHYAD1=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Depopulate [R38, R44, R47] Populate [R45, R46] Populate [R38, R44, R47] Depopulate [R45, R46]
ACTIVITYLED	PHYAD2=1 PHYAD2=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Depopulate [R34,R36, R39] Populate [R33, R35] Populate [R34, R36, R39] Depopulate [R33, R35]
FULLDUPLEXLED	PHYAD3=1 PHYAD3=0	DEFAULT	ACTIVE LOW ACTIVE HIGH	Depopulate [R53, R40] Populate [R52] LED4 orient up Populate [R53, R40] Depopulate [R52] LED4 orient down
CRS/PHYAD4	MSB PHYAD4 = 1 MSB PHYAD4=0	DEFAULT		Depopulate [R49] Populate [R49]

The address lines are strapped as defined in the diagram below. The LED outputs will automatically change polarity based on the presence of an external pull-down resistor.

- If the LED pin is pulled high, by the **internal** 100K pull-up resistor, the LED output will be active low.
- If the LED pin is pulled low, by an **external** 10K pull-down resistor, the LED output will be active high.

To set the PHY address on the PHYAD pins, float the pin to set the address high or pull-down the pin with an **external** 10K resistor to GND to set the address low. See the [Figure 2.2](#) below:

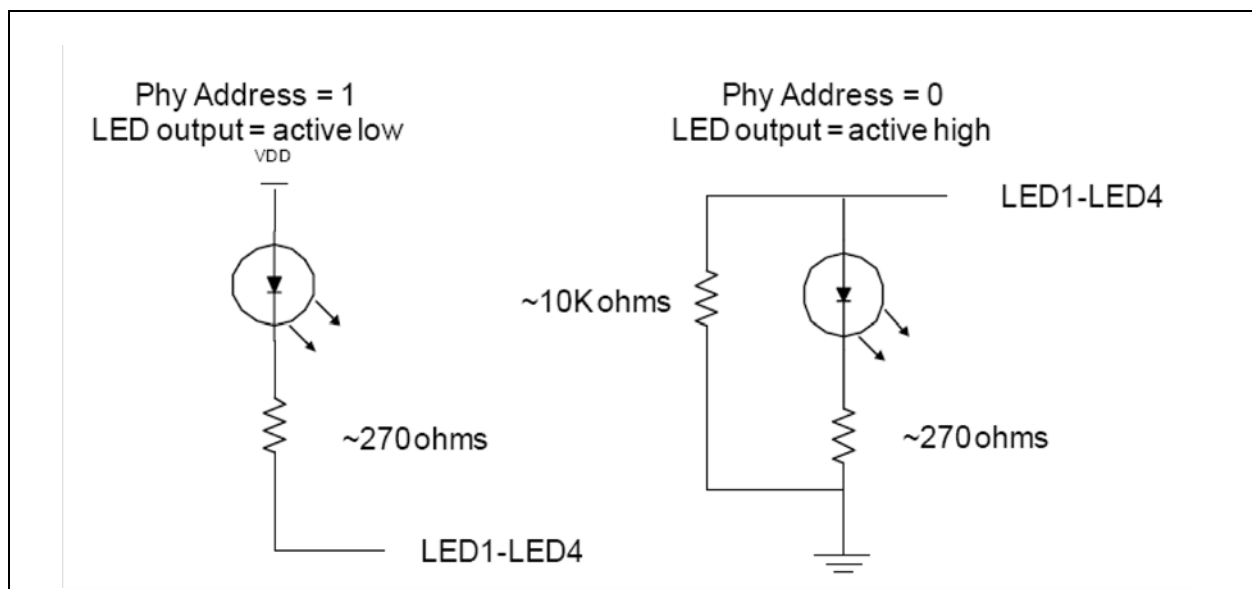


Figure 2.2 PHY Address Strapping with the LED pins.

2.2.2 Boot Mode Configuration Options

There are three resistors used to bootstrap the PHY into a specific mode. [Table 2.2](#) below shows how to populate the resistor to configure the PHY into different modes upon bootup (after reset).

Table 2.2 PHY Address Configuration Resistors

MODE2 R32	MODE1 R15	MODE0 R16	BOOT MODE DESCRIPTION	MODE REGISTER BITS MODE [2:0]
Empty	Empty	Empty	All Capable Auto Negotiate Enable [Default]	111
Empty	Empty	Populated	Powerdown mode startup (Note 2.1)	110
Empty	Populated	Empty	Repeater Mode (Note 2.2): 100Base-TX Half Duplex is advertised Auto-negotiate enabled CRS is active during Receive	101
Empty	Populated	Populated	100Base-TX Half Duplex is Advertised. Auto-negotiation is enabled. CRS is active during Transmit and Receive.	100
Populated	Empty	Empty	100Base-TX Full Duplex. Auto-negotiate disabled. CRS is active during receive.	011
Populated	Empty	Populated	100Base-TX Half Duplex. Auto-negotiation disabled. CRS is active during transmit and receive.	010
Populated	Populated	Empty	10Base-T Full Duplex. Auto-negotiation disabled.	001
Populated	Populated	Populated	10Base-T Half Duplex. Auto-negotiation disabled.	000

Note 2.1 Please refer to the datasheet section 5.4 for more information on Powerdown mode.

Note 2.2 Please refer to the datasheet section 5.4 for more information on Repeater mode.

Note: An Empty resistor means an internal pull-up will bootstrap the Mode pin high to a logic 1. A Populated resistor will bootstrap the Mode pin low to a logic 0.

2.2.3 Pin 1 mode configuration

Pin 1 can either be configured to drive nINT (Active low output interrupt pin) or to drive TXER/TXD4 (Transmit Error pin or Transmit Data 4). This bootstrapping option is controlled by R25 on the board, which is a 10k pull-down to ground on RXD3/nINTSEL. Normally this resistor is empty and the pin is pulled high internally. This default is to configure pin 1 option as nINT. To change this to a TXER pin, the user needs to populate R25. Refer to the LAN8700 datasheet for instructions on changing the TXER pin to a TXD4 pin.

2.2.4 Digital Communications Mode

Resistor R7 will change the digital communications mode of the LAN8700 PHY. By default this resistor is empty. An empty resistor defaults the pin to low at bootup and configures the PHY for MII communication.

If R7 is populated with a 10k resistor, then the device will boot up in RMII mode. See [Chapter 3](#) for more details.

2.2.5 MDIO pullup

Resistor R1 is used to give a pullup to the MDIO pin. Normally the resistor is not needed because the MAC that the PHY is interfacing to has a pull-up built into its system.

2.3 HP Auto-MDIX options

The LAN8700 supports Auto-MDIX on the analog output pins.

The EVB8700 supports disabling the Auto-MDIX through the MDIO interface to the Internal registers. Setting bit 15 of register 27 to a 1 will disable Auto-MDIX switching function. Please refer to the SMSC LAN8700 datasheet for more information.

2.4 LED indicators

There are 6 LEDs on the board, 4 placed on the board as discrete components, and 2 on the RJ-45 connector.

Table 2.3 LED indicators

SCHEMATIC REFERENCE	SILK SCREEN NAME	DESCRIPTION
LED1	SPEED 100	This LED indicates when the PHY is communicating in 100Base-TX mode. This LED will only come on when the PHY has a link established.
LED2e	LED2	This LED indicates that the link is communicating in Full Duplex.
Green(link)	LINK	This LED indicates that a link to the other host has been made.
Yellow(Act)	ACT	This LED indicates that there is communication activity on the Ethernet Link.
D1	+5V	This LED indicates that there is +5v power to the board
D2	+3.3V	This LED indicates that there is +3.3v power to the board.

2.5 Test Points

[Table 2.4](#) and [Table 2.5](#) below identify the test points for debug purposes.

Table 2.4 Test Points

TEST POINTS	DESCRIPTION	TEST POINTS	DESCRIPTION
TP3	+5v power	TP5	+3.3v power supply output.
TP7	VDDCORE (Note 2.3)		

Note 2.3 VDDCORE is the internal +1.8v regulated output, that needs a 4.7uF and a 0.1uF capacitor to decouple the voltage.

Table 2.5 Test Points From Header J2

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	nRST: active low reset signal from the MII plug or the on board reset button SW1	11	TX_ER: Transmit Error
2	MDIO: Management Data Input Output.	12	TX_CLK: Transmit clock
3	MDC: Management Clock	13	TX_EN: Transmit Enable
4	RXD3: Receive Data Bit 3	14	TXD0: Transmit Data Bit 0.
5	RXD2: Receive Data Bit 2	15	TXD1: Transmit Data Bit 1
6	RXD1: Receive Data Bit 1	16	TXD2: Transmit Data Bit 2
7	RXD0: Receive Data Bit 0	17	TXD3: Transmit Data Bit 3
8	RX_DV: Receive Data Valid	18	COL: Collision Detected.
9	RX_CLK: Receive Clock	19	CRS: Carrier Sense.
10	RX_ER: Receive Error	20	Digital Ground

Table 2.6 Test Points From Header J3

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	nINT/TX_ER/TXD4: Multi-use pin.	2	VDDIO: I/O voltage test pin (Note 2.4)
3	VDD: Core VDD voltage.	4	Digital Ground

Note 2.4 This pin can be used to drive a separate IO voltage, when the ferrite bead FB5 is Depopulated

Table 2.7 Test Points From Header J4

HEADER PIN	DESCRIPTION	HEADER PIN	DESCRIPTION
1	+5V from MII plug	2	Digital Ground
3	+5V from MII plug	4	Digital Ground

2.6 Connector Pin-outs

2.6.1 MII Connector

The MII connector supplies +5v power to the board, as well as the digital control signals. The pinout for the connector is shown below in [Table 2.8](#).

Table 2.8 AMP MII Connector Pinout RA (P1)

1	+5V[3]	11	TX_ER (Note 2.5)	21	+5V[2]	31	GND[9]
2	MDIO	12	TX_CLK	22	GND[18]	32	GND[8]
3	MDC	13	TX_EN	23	GND[17]	33	GND[7]
4	RXD3	14	TXD0	24	GND[16]	34	GND[6]
5	RXD2	15	TXD1	25	GND[15]	35	GND[5]
6	RXD1	16	TXD2	26	GND[14]	36	GND[4]
7	RXD0	17	TXD3	27	GND[13]	37	GND[3]
8	RX_DV	18	COL	28	GND[12]	38	GND[2]
9	RX_CLK	19	CRS	29	GND[11]	39	GND[1]
10	RX_ER	20	+5V[4]	30	GND[10]	40	+5V[1]

Note 2.5 TX_ER from the MII is not used on the EVB8700, but can be monitored on the test header J2.

2.6.2 MII Pin Description

The signals are defined in [Table 2.9](#) with a description relative to the EVB8700

Table 2.9 MII 40 Pin Description

NAME	DIRECTION RELATIVE TO EVB8700	ACTIVE LEVEL	DESCRIPTION
GND[18-1]	Power	n/a	Ground Plane.
+5V[4-1]]	Power	n/a	+5v supply from the MII connector. Converted to +3.3v on the EVB and used to power the LAN8700 PHY and +3.3v rail.
RXD[3-0]	Output	TBA	Receive data bits 0 to 3 that are sent by the PHY to the receive path of the MII connector to the MAC controller.
TXD[3-0]	Input	TBA	Transmit data bits 0 to 3 that are accepted by the PHY in the receive path from the MAC controller.
MDIO	Input/Output	TBA	Management Data Input Output: serial management data input/output.
MDC	Input	TBA	Management Data Clock: clock signal for the above MDIO signal.

Table 2.9 MII 40 Pin Description

NAME	DIRECTION RELATIVE TO EVB8700	ACTIVE LEVEL	DESCRIPTION
RX_DV	Output	TBA	Receive data valid: this signal indicates that recovered and decoded data nibbles are being presented on RXD[3:0].
RX_CLK	Output	TBA	Receive Clock: 25MHz in 100base-TX mode. 2.5MHz in 10base-T mode.
RX_ER	Output	TBA	Receive Error: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY.
TX_ER	Input/Output	TBA	Transmit Error or Transmit data 4: This bit is set by the RXD3/nIntsel pin.
TX_CLK	Output	TBA	Transmit Clock: 25MHz in 100base-TX mode. 2.5MHz in 10base-T mode.
TX_EN	Input	TBA	Transmit Enable: Indicates that valid data is present on the TXD[3:0] signals, for transmission.
COL	Output	TBA	MI1 Collision detection: Assertion to indicate detection of collision.
CRS	Output	TBA	Carrier Sense: Assertion indicates detection of carrier.

2.6.3 RJ-45 Ethernet Jack

The pinout for the RJ-45 Jack is described in [Table 2.10](#) below.

Table 2.10 RJ-45 Ethernet Jack Pin-Out

PIN	DESCRIPTION
1	TXP: Transmit Positive
2	TXN: Transmit Negative
3	RXP: Receive Positive
4	Analog Reference to ground
5	Analog Reference to ground
6	RXN: Receive Negative
7	Analog Reference to ground
8	Analog Reference to ground

2.7 Clocking

2.7.1 Crystal Oscillator

The 25 MHz crystal Y1 is connected to the internal oscillator of the LAN8700. A PLL circuit in the LAN8700 generates all the timing needed by the PHY.

2.7.2 External Clock

The board can be configured to use an external clock if the crystal Y1 is removed and a 25MHz +2.0v signal is injected onto pin Y1.1 which is connected to pin 14 of the LAN8700. Y1.2 (pin 13 of the LAN8700) is left floating.

3 RMII Configuration

The first section of this chapter provides detailed instructions to modify an existing EVB8700 rev E board to make it operate in RMII mode. The second section describes using the RMII modified EVB board in a customer's application.

3.1 Modifications to the EVB8700

There are four modifications needed to the EVB8700 to make it run in RMII mode.

1. Crystal Circuit - Remove crystal Y1 and resistor R48.
2. RMII mode pin - Add resistor R7.
3. 50MHz clock - The system must supply a 50MHz clock.

3.1.1 Crystal circuit

Remove Y1 and R48 from the crystal circuit as the 25MHz crystal is not needed. Also the 1Meg ohm resistor is not needed.

3.1.2 RMII mode pin

Populate resistor R7 with a 10k ohm 0603 resistor. This will boot strap the EVB8700 into RMII digital communications mode.

3.1.3 50MHz Clock Source

The digital communication between the LAN8700 and the MAC requires a single 50MHz clock source for both devices. This can be added in several ways. The easiest is to add a crystal oscillator chip (ECS Inc PN:ECS-3963-500-BN-TR) to the EVB module as shown in [Figure 3.1](#). A footprint is not provided on the board. The 50MHz source also needs to go into the MAC clock control circuit. This can easily be accommodated by using the RX_CLK pin, since its not used in RMII mode.

To use the RX_CLK pin, remove resistor R21, then using a wire, make a connection from the 50MHz clock source, to pin 9 of J2.

This will provide 50MHz clock to the PHY at X1, and 50MHz clock to the MAC through the MII plug RX_CLK pin. If the customers board doesn't have an MII plug, then the customer can add a wire to the EVB into the header plug at J2. The 50MHz clock source for the MAC would come from the RX_CLK on the header.

The alternative solution is to add a 50MHz source from the system. The RX_CLK pin can also be used, just remove R21, and connect a wire from the MII plug side of R21 to the CLKIN side of the Y1 crystal.

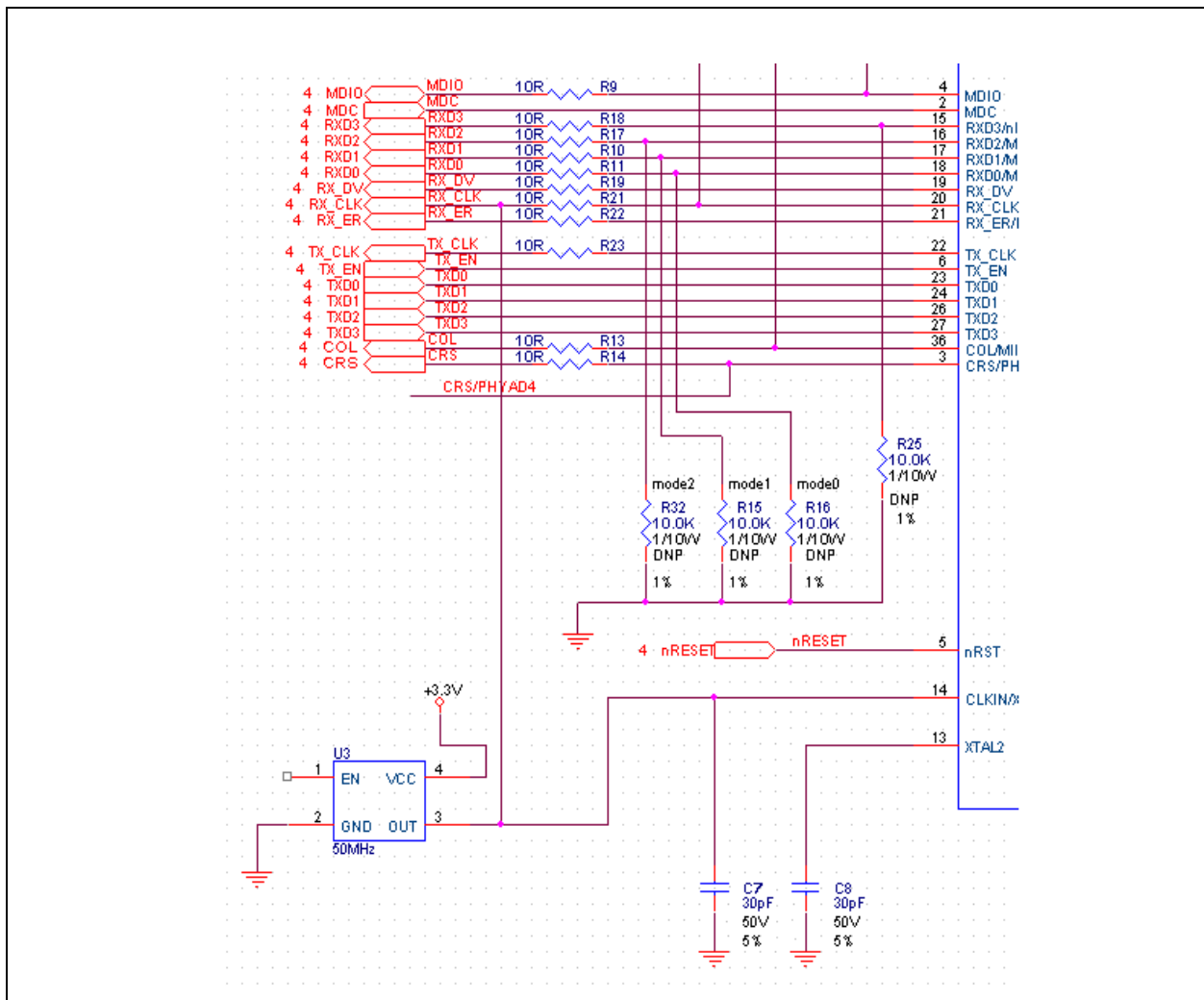


Figure 3.1 Add a 50MHz Oscillator to the EVB8700 for RMII Mode

Table 3.1 RMII Connections Using the Debug Header J2 of the EVB8700

EVB8700 SILK SCREEN HEADER J2 NAME	J2 PIN NUMBER	RMII NAME	MAC NAME	COMMENT
nRST	1	nRST	nRST	This signal is used to reset the PHY on the EVB
MDIO	2	MDIO	MDIO	Optional, used to read/write the internal registers of the PHY.
MDC	3	MDC	MDC	Optional. clock signal used to read/write the registers of the PHY
RXD3	4			Not used in RMII mode
RXD2	5			Not used in RMII mode

Table 3.1 RMII Connections Using the Debug Header J2 of the EVB8700 (continued)

EVB8700 SILK SCREEN HEADER J2 NAME	J2 PIN NUMBER	RMII NAME	MAC NAME	COMMENT
RXD1	6	RXD1	RXD1	Receive data 1
RXD0	7	RXD0	RXD0	Receive data 0
RX_DV	8			Not used in RMII mode
RCLK	9	CLKIN	REFclk	This header pin and MII plug pin can be used as the 50MHz port between the PHY and the MAC. (Note 3.1)
RX_ER	10	RX_ER	RXER	Optional for the MAC. Required by the PHY. The MAC can choose to ignore this signal.
TXER	11			Not used.
TXCLK	12			Not used.
TX_EN	13	TX_EN	TX_EN	Transmit enable.
TXD0	14	TXD0	TXD0	Transmit data bit 0
TXD1	15	TXD1	TXD1	Transmit data bit 1
TXD2	16			Not used in RMII mode, these can be tied directly to GND.
TXD3	17			Not used in RMII mode, these can be tied directly to GND.
COL	18	CRS_DV	CRSDV	Carrier Sense and Data Valid
CRS	19			This pin is not used in RMII mode.
GND	20	GND	GND	Ground connection to VSS.
J3 extension of J2				
TXD4	1			Not used in RMII mode.
VDDIO	2	VDDIO	VDDIO	Variable Voltage IO (+1.8V to +3.6V) to match IO voltage of MAC. (Note 3.2)
VDD	3	VDD	+3.3V	+3.3V power to drive analog and core
GND	4	GND	GND	Ground connection to VSS.
J4 extension of J2				
+5	1	+5V	+5V	+5V power.
GND	2	GND	GND	Ground connection to VSS.
+5	3	+5V	+5V	+5V power.
	4	GND	GND	Ground connection to VSS.

Note 3.1 By Default this is connected to +3.3V on the EVB8700. To isolate this power and drive separately, remove FB5.

Note 3.2 By Default this is connected to +3.3V on the EVB8700. To isolate this power and drive separately, remove FB5.

3.2 How to use the RMII configured EVB8700

The easiest way to use the EVB8700 configured for RMII mode, is to have an MII plug designed into your system so that the EVB8700 can plug directly in. The pinout is shown below in [Figure 3.2](#)

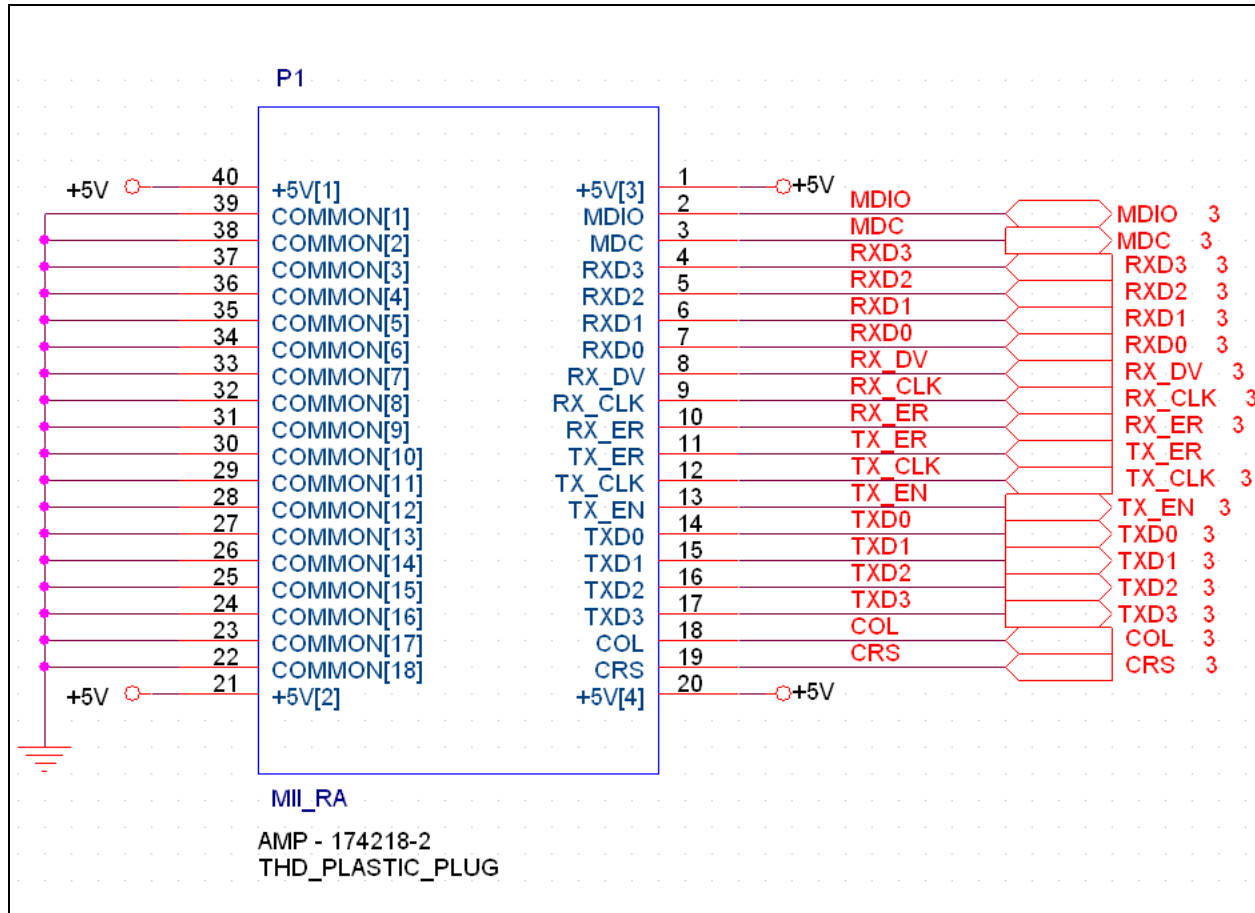


Figure 3.2 MII Plug Pinout

If the system doesn't have an MII plug, then the EVB8700 has a debug header J2 which can be used to wire in the EVB to the system, using the RMII pins identified in column 3 of [Table 3.1](#).

EVB-LAN8700

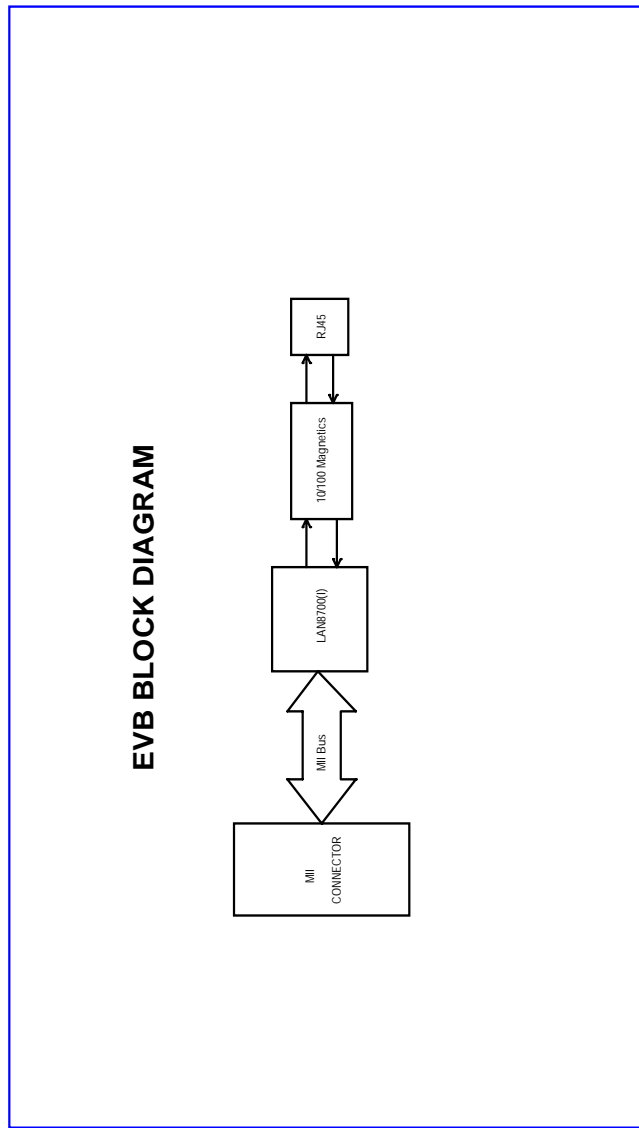
LAN8700(I) MII Customer Evaluation Board +3.3V I/O VDDIO Operation Schematic Revision E0

Design Details

Board: PCB-7054AZ-E0
Chip: LAN8700(I)

Board Form Factor:
Assembly:

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications. Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Provided. It Is The Responsibility Of The User To Verify That All Components Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.



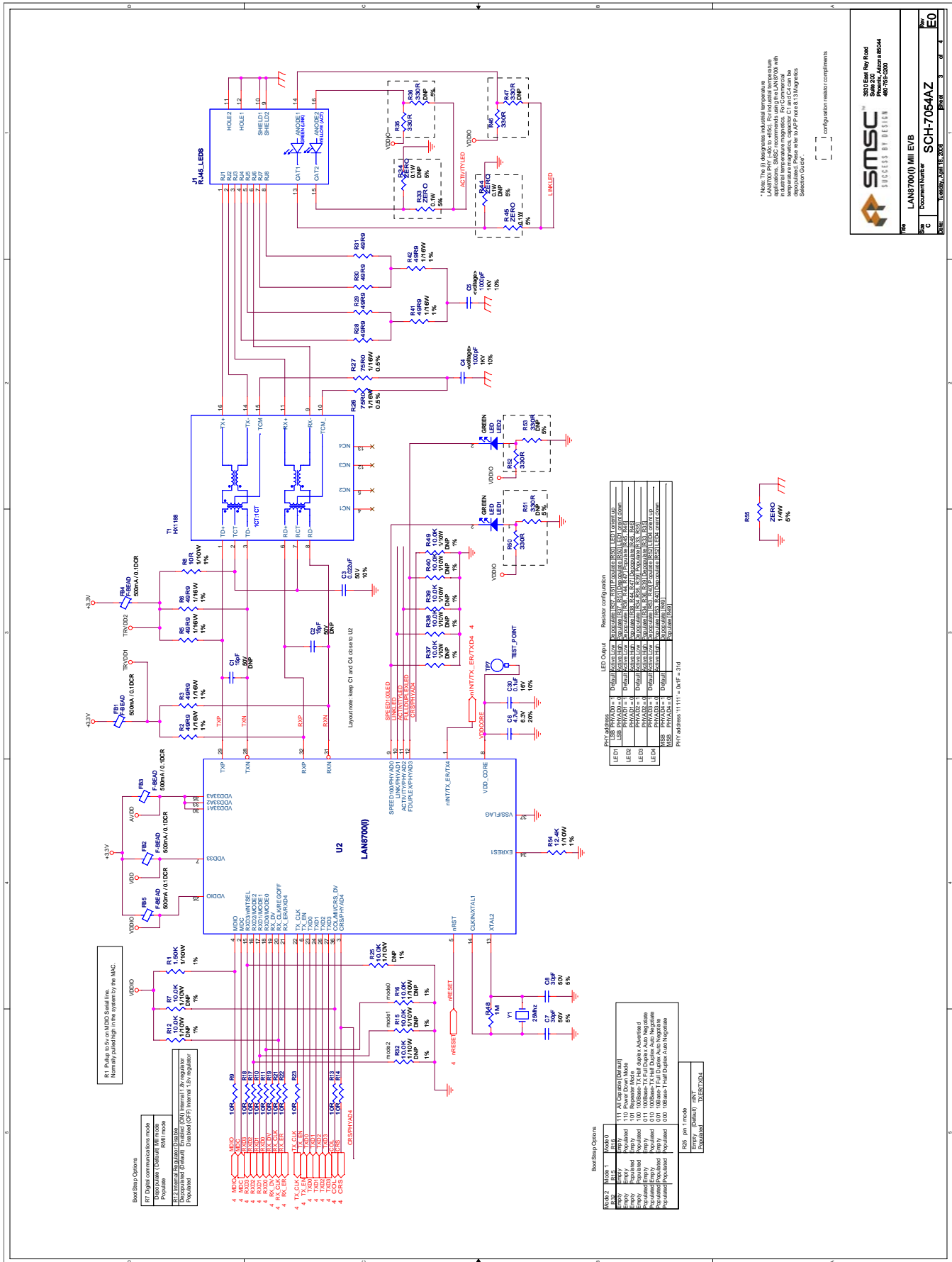
ITEM	REV	DESCRIPTION
1	1	Initial Release
2	2	LAN8700(I) Magnetics
3	3	Board Form Factor
4	4	Assembly

Revisions

Rev D1 12/05/05 Customer Mark; we are revised from D1
Rev D2 12/05/05 Customer Mark; we are revised from D1
Rev D3 12/15/06 Customer Mark; we are revised from D3
Rev D4 12/15/06 Customer Mark; we are revised from D4
Rev E0 02/24/08 Customer Mark; we are revised from E0

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SUCCESS THROUGH INNOVATION

Part No. LAN8700(I) MII EVB
Doc No. SCH-7054AZ
Rev. E0



*Note: This EVB is not recommended for industrial applications. SMSC recommends using the LAN8700 with industrial grade components. For industrial applications, SMSC recommends using the LAN8700 with industrial grade components. For industrial applications, SMSC recommends using the LAN8700 with industrial grade components.

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 SUCCESS BY DESIGN

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Part Number: LAN8700(0) MII EVB

 Document Number: SCH-7054AZ

 Rev: 0

 Date: 07-24-07

Resistor configuration table:

Part	Value	Notes
R1	100k	100k
R2	100k	100k
R3	100k	100k
R4	100k	100k
R5	100k	100k
R6	100k	100k
R7	100k	100k
R8	100k	100k
R9	100k	100k
R10	100k	100k
R11	100k	100k
R12	100k	100k
R13	100k	100k
R14	100k	100k
R15	100k	100k
R16	100k	100k
R17	100k	100k
R18	100k	100k
R19	100k	100k
R20	100k	100k
R21	100k	100k
R22	100k	100k
R23	100k	100k
R24	100k	100k
R25	100k	100k
R26	100k	100k
R27	100k	100k
R28	100k	100k
R29	100k	100k
R30	100k	100k
R31	100k	100k
R32	100k	100k
R33	100k	100k
R34	100k	100k
R35	100k	100k
R36	100k	100k
R37	100k	100k
R38	100k	100k
R39	100k	100k
R40	100k	100k
R41	100k	100k
R42	100k	100k
R43	100k	100k
R44	100k	100k
R45	100k	100k



