electronicdesign
UNCOVERED
ISSUE 08
February 2015
newark.com

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Benchmarking Low-Power

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In this article we will discuss the common methodology and various benchmarks that are frequently used in the industry to show microcontroller (MCU) power performance. In the MCU market space power requirements vary greatly. Some applications will need a MCU device that performs best (current consumption and wakeup time) when off or mostly in the lowest possible power mode – think pulse oximeter or glucose meters. On the other hand there are applications where devices need really efficient active current for an 'always on' type application such as listening for sensor data. The focus of this article will be on the segment of MCUs that need active current consumption and how these are measured and benchmarked.

Microcontroller datasheets are a wonderful source for good ole' factual reliable engineering information, like peripheral interface timing, Vih, Vil threshold levels and all that malarkey! But all datasheets have caveats as well. For example 'equivalent to CoreMark code' does not mean 'CoreMark' code or maybe more obvious - "current consumed while executing from internal SRAM" is not the same as "from Flash" – so make sure that you are comparing apples to apples! Pay attention to footnotes and other subtle hints on the true source of the data being presented. Probably best to read it at least twice.

Benchmark Tools

While(1) One could argue that this is not a benchmark at all due to the simplicity and lack of code/algorithm. It is the most basic datasheets active current consumption number. Some vendors quote running from Flash and/or SRAM with various permutations of clocks on or off, PLL and so on. Can it really tell you something? Maybe or maybe not! Since it is not a 'standard' vendors will quote this number with conditions that 'massage' the result.

Fibonacci Fibonacci code is executed on the MCU and the active current consumed is measured – simple! Atmel and recently NXP are using this 'algorithm' to benchmark active current performance. What does this code do exactly? Simply it adds the 2 previous numbers together to get the next number. And so on. 1. 1. 2. 3. 5. 8. 13. 21. 34. 55. 89. 144… This is not a very sophisticated routine and probably not something that exercises much of the core instruction set and hardware that other benchmarks accomplish. Nevertheless it is a bit better than a While(1). Of course when comparing devices with the same core it has some comparison merit.

Dhrystone Dhrystone was developed back in the 80s to benchmark CPUs. It is older and has somewhat been superseded by the newer CoreMark Benchmark. The common metric report for Dhrystone is DMIPS.

Dhrystone does not support any floating point operations in the test suite – this is covered by Whetstone benchmark. Dhrystone has some weaknesses that are widely published. Major portions of Dhrystone are susceptible to a compiler's ability to optimize the work away. That said CoreMark can also be subject to Compiler trickery!

Dhrystone is still commonly seen in MCU promotional literature. ARM frequently use it to show their core performance – but do not expect to always match ARMs Core Dhrystone numbers with MCUs using the same ARM core! Also the compiler settings and compiler used when creating this Benchmark code will greatly influence the results.

CoreMark This has become an Industry standard for benchmarking MCU active current. NXP has been one of the advocates of the CoreMark benchmark. In all the recent DS releases CoreMark performance and the way it was achieved is detailed. On the recent LPC54102 launch an Application note with step by step instructions is available that helps customers recreate the excellent CoreMark numbers the part can truly achieve. CoreMark benchmark also supports a Floating point option for those devices that have such hardware support.

Some would argue that CoreMark is now the subject of compiler wars, this may be true, however if a customer uses the same IDE and compiler version for benchmark they can compare two competing devices – this assumes the IDE vendor does not show a preference to a particular device! The CoreMark rules state that the compiler and settings should be disclosed with the number.

Results for 32-bit ARM Cortex-M4F/M0+ microcontroller

CoreMark Score

Conditions	Typ	Parameters
ARM Cortex-M4F in active mode; ARM Cortex-M0+ in sleep mode, CoreMark code executed from SRAM, Tamb = 25°C, VDD = 3.3V		
CCLK = 12 MHz	2.6 Iterations/MHz	[1] [3] [4] [5]
CCLK = 48 MHz	2.6 Iterations/MHz	[2] [3] [4] [5]
CCLK = 84 MHz	2.6 Iterations/MHz	[2] [3] [4] [5]
CCLK = 100 MHz	2.6 Iterations/MHz	[2] [3] [4] [5]
ARM Cortex-M4F in active mode; ARM Cortex-M0+ in sleep mode, CoreMark code executed from flash, Tamb = 25°C, VDD = 3.3V		
CCLK = 12 MHz, 1 system clock	2.6 Iterations/MHz	[1] [3] [4] [6]
CCLK = 48 MHz, 3 system clock	2.4 Iterations/MHz	[2] [3] [4] [6]
CCLK = 84 MHz, 4 system clock	2.3 Iterations/MHz	[2] [3] [4] [6]
CCLK = 100 MHz, 5 system clock	2.2 Iterations/MHz	[2] [3] [4] [6]

Parameters Detail

[1] Clock source 12 MHz IRC. PLL disabled.

[2] Clock source 12 MHz IRC. PLL enabled.

[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision v.5.12, optimization level 3, optimized for time on.

[5] SRAM0 and SRAM1 powered, SRAM2 powered down.

[6] See the FLASHCFG register in the LPC5410x User Manual for system clock flash access time settings.

Current Consumption

Conditions	Typ	Parameters
ARM Cortex-M4F in active mode,ARM Cortex-M0+ in sleep mode, CoreMark code executed from SRAM, Tamb = -40 °C to +105 °C, Unless otherwise specified: 1.62 V <= V_{DD} <= 3.6 V, I_{DD}, supply current		
CCLK = 12 MHz	1.5 mA	[2] [4] [6]
CCLK = 48 MHz	4.8 mA	[3] [4] [6]
CCLK = 84 MHz	7.9 mA	[3] [4] [6]
CCLK = 100 MHz	9.9 mA	[3] [4] [6]
ARM Cortex-M4F in active mode,ARM Cortex-M0+ in sleep mode, CoreMark code executed from flash, Tamb = -40 °C to +105 °C, Unless otherwise specified: 1.62 V <= V_{DD} <= 3.6 V, I_{DD}, supply current		
CCLK = 12 MHz, 1 system clock	1.9 mA	[2] [4] [6]
CCLK = 48 MHz, 3 system clock	5.7 mA	[3] [4] [6]
CCLK = 84 MHz, 6 system clock	8.8 mA	[3] [4] [6]
CCLK = 100 MHz, 7 system clock	10.7 mA	[3] [4] [6]

Current Consumption Running Fibonacci

Conditions	Typ	Parameters
ARM Cortex-M4F in active mode, Cortex-M0+ in sleep mode, CoreMark code executed from SRAM, Tamb = -40 °C to +105 °C, Unless otherwise specified: 1.62 V <= V_{DD} <= 3.6 V, I_{DD}, supply current		
CCLK = 12 MHz	1.7 mA	[2] [4] [5]
CCLK = 84 MHz	8.0 mA	[3] [4] [5]
CCLK = 96 MHz	9.4 mA	[3] [4] [5]
ARM Cortex-M0+ in active mode, Cortex-M4F+ in sleep mode, CoreMark code executed from flash, Tamb = -40 °C to +105 °C, Unless otherwise specified: 1.62 V <= V_{DD} <= 3.6 V, I_{DD}, supply current		
CCLK = 12 MHz, 1 system clock	1.5 mA	[2] [4] [5]
CCLK = 48 MHz, 3 system clock	6.2 mA	[3] [4] [5]
CCLK = 84 MHz, 6 system clock	7.2 mA	[3] [4] [5]

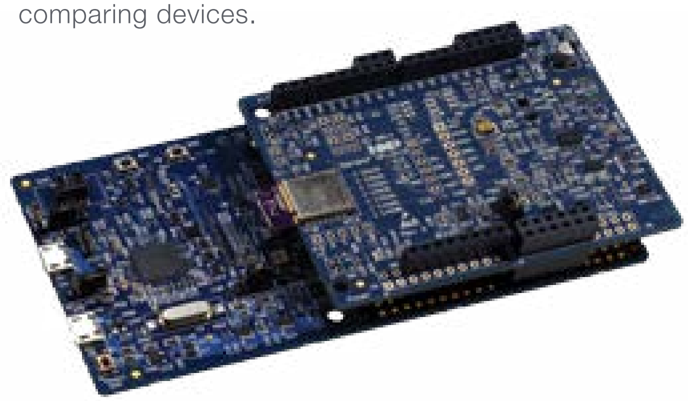
The CoreMark benchmark and the EEMBC consortium address some of the aforementioned Dhrystone weaknesses. It is simple, yet sophisticated, easily ported in minutes, comes with comprehensive documentation and run rules. The C code is hosted and downloadable for free from EEMBC website.

Care should be taken, optimum settings, code partition and scattering loading and MCU architecture can greatly influence the CoreMark number. For example on the LPC54102 device there is an AHB Matrix with various masters and slaves. The SRAM blocks are slaves as is the Flash. Code and data can be scattered loaded in such a manner to reduce contention. This could be viewed as cheating but really it is not. It is the best utilization of the hardware memory architecture to optimize performance, which can also be applied to real world applications.

It should be also mentioned that the best CoreMark number does not occur at the same time as the best uA/MHz – some specmanship! Flash wait states, prefetch and Flash on/off also have an influence and these items can be adjusted to suit the particular application and power requirements.

Conclusion

The best way to determine if a particular MCU fits the bill with respect to performance (current consumption and processing) is to write your own application code, debug, optimize and then measure! MCU vendors use many ways to report active current on their datasheets, each method has some advantages and some disadvantages, simplicity versus complexity. Reviewing a combination of these Benchmarks data points is a good approach. Engineers should pay attention to the finer details when comparing devices.



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PIC18F13K22-I/P	07P9664
PIC18F13K50-I/P	77M3098
PIC18F14K22-E/ML	07P9670
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AT32UC3C-EK	68T4564
AT32UC3A0256-ALUT	68T4474
AT32UC3A0512-ALUT	68T4481
AT32UC3A1128-AUT	68T4486
AT32UC3A1512-AUT	68T4491
AT32UC3A3256-ALUT	68T4503
AT32UC3A3256-CTUT	68T4505
AT32UC3B0256-A2UT	68T4538
AT32UC3B0512-A2UT	68T4542
AT32UC3B064-A2UT	68T4547
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AT32UC3C0512C-ALZR	87W8129

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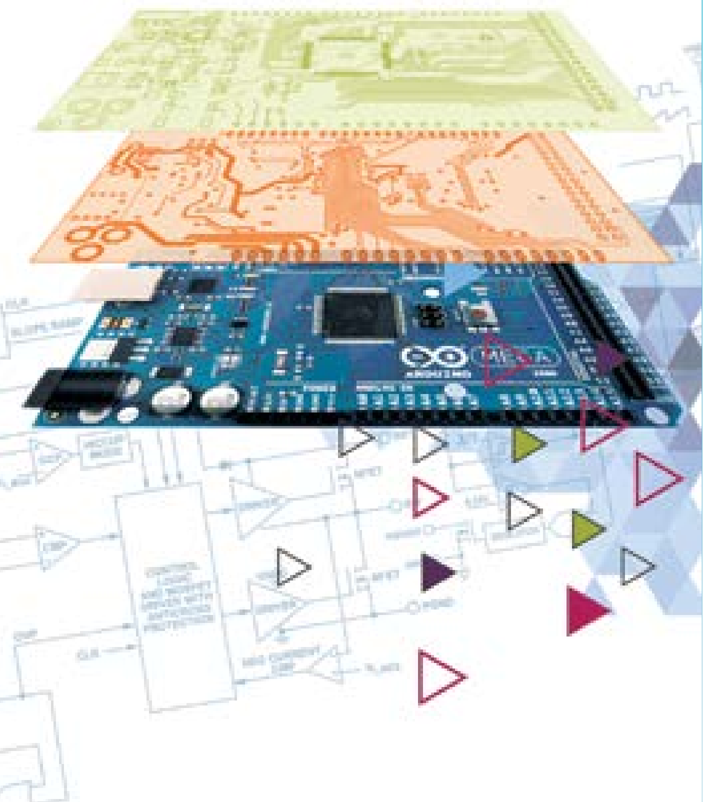

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88981106	83X6185
88981107	83X6186
88981113	83X6187
88981114	83X6188
88981116	83X6189
88981117	83X6190
88981153	83X6191
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TM221C16R	84X5870
TM221C24R	84X5872
TM221CE16R	84X5864
TM221CE16T	84X5865
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FT1A-H24RC	72W3985
FT1A-B24RC	72W3971
FT1A-H24RA	72W3984
FT1A-PC1	73W9261
FT1A-PC2	73W9262
FT1A-PM1	73W9264
FT9Z-1D3PN05	73W9267
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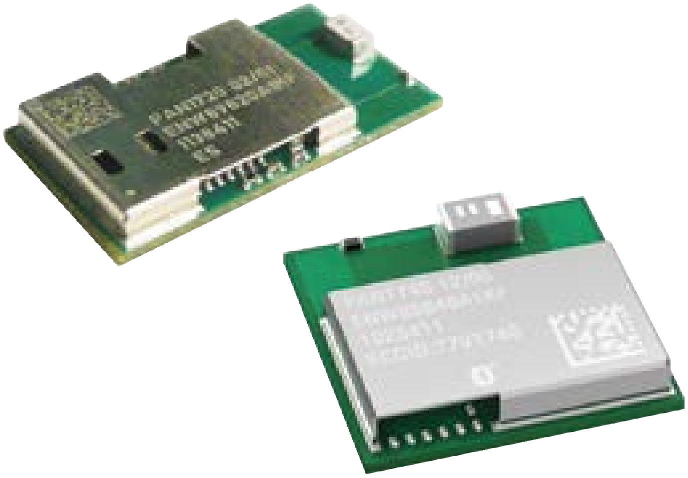
ENW-89829C2KF	49W8296
ENW-89829A2KF	49W8295
EVAL_PAN1555-SPP/HDP	62W4322
EVAL_PAN1322	62W4319
ENW-89815A3KF	64W2462
ENW-89829C2KF	64W2467



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ENW-89823C2KF	49W8293
ENW-89837A3KF	64W2471
EVAL_PAN1323ETU	62W4321
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ENW-89820A3KF	43W5821
ENW-89820A1KF	49W8291
ENW-89835A3KF	64W2469
EVAL_PAN1720BR	62W4324
EVAL_PAN1720	62W4323
EVAL_PAN1740	49X8755
ENW-89820A1KF	01X1611
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2SEPC560MZ+TSS	98W0401
16SVP82M	98W0240
6SVPC220M	98W0933
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Panasonic POSCAP Tantalum-Polymer Solid Capacitors use a sintered tantalum anode and a proprietary high conductivity polymer for a cathode. This innovative construction and processing offer stable capacitance at high frequency and temperature, with the lowest ESR level in polymer tantalum technology. The POSCAP product line spans several series of Solid Electrolyte Chip Capacitors which include the TPE, TQC, TPF, TPSF, TPB, TPC, TPG, and TPU Series. This product line is ideal Chip Capacitor for digital, high-frequency devices and more.

Manufacturer Part No.	Newark Part No.
2R5TPE330M7	98W0348
6TPE470MAZU	98W1014
10TPE68M	97W9297
12TPC15M	97W9305
20TQC47MYF	98W0470

SP-CAP™ POLYMER ALUMINUM CAPACITORS ▶

Panasonic SP-Cap Polymer Aluminum Capacitors are surface mount (SMT) capacitors that utilize a conductive polymer as their electrolyte material in a layered aluminum design. SP-Cap™ capacitors are primarily used as input and output capacitors for DC/DC converters due to ultra-low ESR values, high voltage options, and the ability to withstand high reflow temperatures. Panasonic SP-Cap™ Polymer Aluminum Capacitors offer capacitance values up to 560µF, voltage values ranging from 2V to 25V, and are free from temperature drift.

Manufacturer Part No.	Newark Part No.
EEF-CX0E331R	54W2535
EEF-GX0E471R	95W5408
EEF-GX0E471L	95W5406
EEF-GX0D471R	53W8322
EEF-CS1C150R	17X9818

HYBRID SURFACE MOUNT ALUMINUM ELECTROLYTIC CAPACITORS ▶

Panasonic Electronic Components, new EEH-ZA and EEH-ZC Series Hybrid Surface Mount Aluminum Electrolytic Capacitors take the benefits of both electrolytic and polymer capacitor technologies and combine them, producing a capacitor with low ESR, low leakage current, high ripple current and smaller case sizes. These combined benefits save valuable board space, enhance overall board performance and lower design costs.

Manufacturer Part No.	Newark Part No.
EEH-ZA1E330R	91T4887
EEH-ZC1E560P	91T4905
EEH-ZC1H100R	91T4906
EEH-ZC1H220P	91T4908
EEH-ZC1E330R	91T4903

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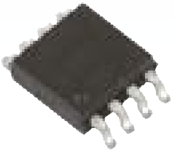

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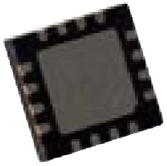

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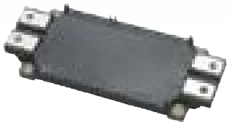

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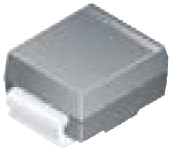

ZENER DIODES IN SMD AND AXIAL PACKAGES

These diodes feature wide power handling capabilities, voltages and reverse currents and promote efficient use of power in DC-to-DC converters, PC motherboards, power supplies, consumer products, and communications systems.

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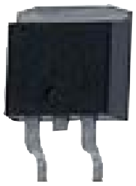

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