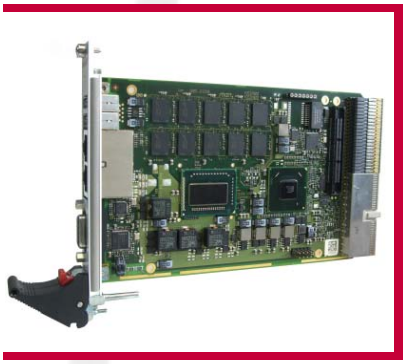
User Manual

F21P – 3U CompactPCI® PlusIO Intel® Core™ i7 CPU Board



F21P - 3U CompactPCI® PlusIO Intel® Core™ i7 CPU Board

The F21P versatile 4HP/3U single-board computer is a continuation of MEN's proven range of Intel® CPU boards. It is equipped with the high-performance second generation Intel® Core™ i7 processor running at 2.1 GHz and offering the latest quad core processor architecture from Intel® with full 64-bit support. The CPU card delivers an excellent graphics performance and is designed especially for embedded systems which require high computing performance with low power consumption.

The F21P offers a 32-bit/33-MHz CompactPCI® bus interface and can also be used without a bus system. 4 USB 2.0 ports, 4 PCI Express® x1 links, 2 SATA 3 Gb/s and 2 SATA 6 Gb/s interfaces as well as one Gigabit Ethernet are led to the J2 rear I/O connector which is compatible with the PICMG 2.30 CompactPCI® PlusIO specification.

The F21P is equipped with fast DDR3 DRAM which is soldered to the F21P to guarantee optimum shock and vibration resistance. An mSATA disk and a microSD™ card device which are connected via a USB interface and a SATA channel offer nearly unlimited space for user applications.

The standard I/O available at the front panel of F21P includes graphics on a VGA connector, two PCIe®-driven Gigabit Ethernet as well as two USB 2.0 ports.

The F21P can be extended by different side cards. Additional functions include a digital video interface for flat panel connection via DVI (multimedia), a variety of different UARTs or another four USBs, SATA for hard disk connection and HD audio.

Thermal supervision of the processor and a watchdog for the operating system complete the functionality of the F21P. As an option, a TPM (Trusted Platform Module) chip can be assembled.

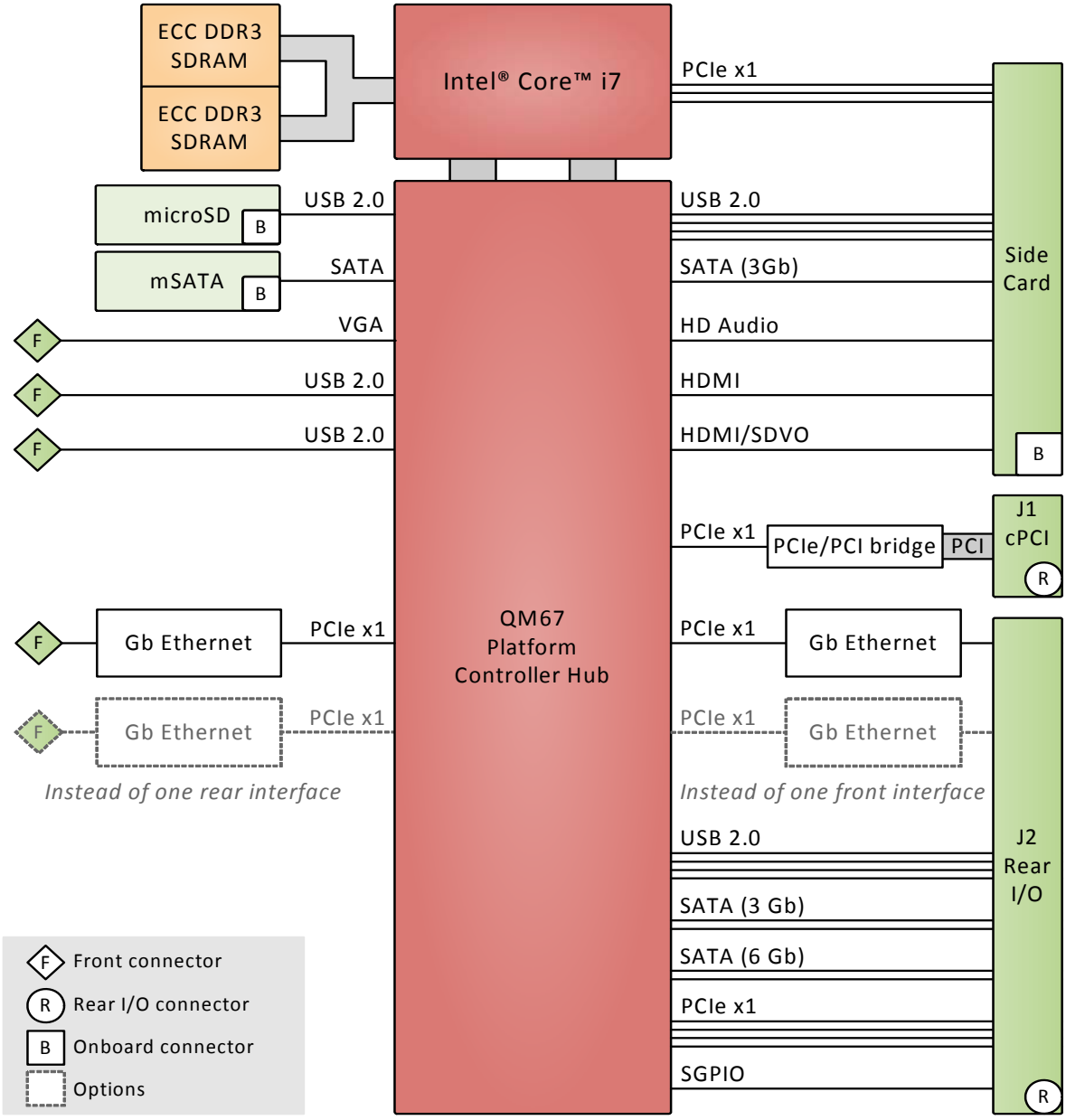
The F21P operates in Windows® and Linux environments as well as under real-time operating systems that support Intel®'s multi-core architecture. The InsydeH2O™ EFI BIOS was specially designed for embedded system applications.

Equipped with Intel® components exclusively from the Intel® Embedded Line, the F21P has a guaranteed minimum standard availability of 7 years.

The F21P is suited for a wide range of industrial applications, e.g. for monitoring, vision and control systems as well as test and measurement. Main target markets comprise industrial automation, multimedia, traffic and transportation, aerospace, shipbuilding, medical engineering and robotics.

The F21P comes with a tailored passive heat sink within 4 HP height. The robust design of the F21P make the board especially suited for use in rugged environments with regard to shock and vibration according to applicable DIN, EN or IEC industry standards. The F21P is also ready for coating so that it can be used in humid and dusty environments.

Diagram


ECC DDR3 SDRAM
ECC DDR3 SDRAM
Intel® Core™ i7
PCIe x1
microSD
B
USB 2.0
USB 2.0
mSATA
B
SATA
SATA (3Gb)
Side Card
VGA
HD Audio
F
USB 2.0
HDMI
F
USB 2.0
HDMI/SDVO
F
B
J1 cPCI
PCIe x1
PCIe/PCI bridge
PCI
R
F
Gb Ethernet
PCIe x1
QM67 Platform Controller Hub
PCIe x1
Gb Ethernet
F
Gb Ethernet
PCIe x1
PCIe x1
Gb Ethernet
Instead of one rear interface
Instead of one front interface
USB 2.0
J2 Rear I/O
SATA (3 Gb)
SATA (6 Gb)
PCIe x1
SGPIO
R
F Front connector
R Rear I/O connector
B Onboard connector
Options

Technical Data

CPU

- Intel® Core™ i7-2715QE
  - Up to 2.1 GHz processor core frequency
  - 3 GHz maximum turbo frequency
- Chipset
  - Intel® QM67 Platform Controller Hub (PCH)

Memory

- Up to 6 MB last level cache integrated in i7
- Up to 16 GB SDRAM system memory
  - Soldered
  - DDR3 with ECC support
  - 1066/1333/1600 MHz memory bus frequency
- 64 Mbits boot Flash
- Serial EEPROM 2kbits for factory settings

Mass Storage

- microSD™ card interface
  - Connected via one USB port
- mSATA disk slot
  - Connected via one SATA channel
- Serial ATA (SATA)
  - Four channels via rear I/O, one channel via side-card connector, one channel for mSATA disk
  - 4 SATA 3 Gbit/s interfaces, 2 SATA 6 Gbit/s interfaces (rear I/O)
  - RAID level 0/1/5/10 support

Graphics

- Integrated in QM67 chipset
  - 650 MHz graphics base frequency
  - 1.2 GHz graphics maximum dynamic frequency
- VGA connector at front panel
- Two digital display interface ports available via side-card connector
  - DisplayPort®, HDMI and SDVO (SDVO only on one interface)
  - One additional DVI connector at front panel optional via side card
  - Simultaneous connection of two monitors

I/O

- USB
  - Two USB 2.0 ports via Series A connectors at front panel
  - Four USB 2.0 ports via side-card connector
  - Four USB 2.0 ports via rear I/O
  - One USB for connection of microSD
  - UHCI implementation
  - Data rates up to 480 Mbit/s
- Ethernet
  - Two 10/100/1000Base-T Ethernet channels at the front
  - RJ45 connectors at front panel
  - Ethernet controllers are connected by two x1 PCIe® links
  - Onboard LEDs to signal activity status and connection speed
  - One 10/100/1000Base-T Ethernet channel via rear I/O
  - Ethernet controller is connected by one x1 PCIe® link
- High Definition (HD) audio
  - Accessible via side-card connector

Front Connections (Standard)

- VGA
- Two USB 2.0 (Series A)
- Two Ethernet (RJ45)

Rear I/O (PICMG 2.30)

- Four SATA
- Four USB
- One Gigabit Ethernet (second rear interface instead of one front interface as an assembly option)
- Four PCI Express® x1 links
- Compatible with PICMG 2.30 CompactPCI® PlusIO
  - 1PCI33/4PCIE5/2SATA3/2SATA6/4USB2/1(2)ETH1G

Miscellaneous

- Board controller
- Real-time clock, buffered by a GoldCap or alternatively a battery (5 years life cycle)
- Watchdog timer
- Temperature measurement
- One user LED
- Reset button

PCI Express

- Three x1 links to connect local 1000Base-T Ethernet controllers
  - Data rate 250 MB/s in each direction (2.5 Gbit/s per lane)
- Four x1 links via rear I/O
  - Data rate up to 500 MB/s in each direction (5 Gbit/s per lane)
- Three x1 links for extension through side-card connector
  - Data rate up to 500 MB/s in each direction (5 Gbit/s per lane)

CompactPCI® Bus

- Connection via PCI Express® link from processor using PCI-Express-to-PCI-Bridge
- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- System slot
- 32-bit/33-MHz CompactPCI® bus
- V(I/O): +3.3V (+5V tolerant)

Busless Operation

- Board can be supplied with +5V only, all other voltages are generated on the board
- Backplane connectors used only for power supply

Electrical Specifications

- Supply voltage/power consumption (board versions with i7-2715QE processor)
  - +5V (-3%/+5%), 9.6 A typ., 14.4 A max.
  - +3.3V (-3%/+5%), 1.8 A (3 Gb Ethernet), 1.4 A (2 Gb Ethernet), 1 A (1 Gb Ethernet)
  - +12V (-10%/+10%), approx. 10 mA
  - If the board is supplied with 5V only (typically without a bus connection), the 3.3V are generated on the board and fed to the backplane (3A max.) No external 3.3 V voltage may be applied in that case!

Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Front panel: 4HP with ejector
- Weight: 204 g (w/o heat sink)

Environmental Specifications

- Temperature range (operation):
  - Depends on system configuration (CPU, hard disk, heat sink...)
  - Maximum: +85°C
  - Minimum: -40°C (all processors)
  - Conditions: airflow 1.5m/s, typical power dissipation: 12 W (board versions with i7-2715QE processor) with Windows® XP operating system and 1 Gb Ethernet connection
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 2,000m
- Shock: 50 m/s², 30 ms
- Vibration (Function): 1 m/s², 5 Hz – 150 Hz
- Vibration (Lifetime): 7.9 m/s², 5 Hz – 150 Hz
- Conformal coating on request

MTBF

- 417,879 h @ 40×C according to IEC/TR 62380 (RDF2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC

- Tested according to EN 55022 (radio disturbance), IEC 61000-4-3 (electromagnetic field immunity), IEC 61000-4-4 (burst) and IEC 61000-4-6 (conducted disturbances)

BIOS

- InsydeH2O™ UEFI Framework

Intel® Active Management Technology

- Manageability Engine in Chipset
- Network Filters in Chipset
- Dedicated Flash Storage Area
- Out of Band (OOB) Access
  - Power off Access
  - Independent of OS status
  - Power status control
  - Keyboard-Video-Mouse (KVM) Viewer (VNC-compatible)
  - IDE-Redirect
  - Serial-over-LAN

Software Support

- Note that 64-bit hardware technology can be used in an optimal way with 64-bit operating system support
- Windows
- Linux
- VxWorks® (on request)
- QNX® (on request)
- Intel® Virtualization Technology, allows a platform to run multiple operating systems and applications in independent partitions; one computer system can function as multiple "virtual" systems

For more information on supported operating system versions and drivers see Downloads.

Configuration Options

CPU

- Intel® Core™ i7-2715QE, 2.1 GHz, 6 MB Cache, 45 W
- Intel® Core™ i7-2655LE, 2.2 GHz, 4 MB Cache, 25 W
- Intel® Core™ i7-2610UE, 1.5 GHz, 4 MB Cache, 17 W
- Intel® Core™ i5-2515E, 2.5 GHz, 3 MB Cache, 35 W
- Intel® Core™ i3-2340UE, 1.3 GHz, 3 MB Cache, 17 W, no AMT
- Intel® Core™ i3-2310E, 2.1 GHz, 3 MB Cache, 35 W, no AMT
- Intel® Celeron® B810E, 1.6 GHz, 2 MB Cache, 35 W, no AMT
- Intel® Celeron® 847E, 1.1 GHz, 2 MB Cache, 17 W, no AMT
- Intel® Celeron® 827E, 1.4 GHz, 1.5 MB Cache, 17 W, no AMT

Memory

- System RAM
  - Up to 16 GB
- microSD™ card
  - 0 MB up to maximum available
- mSATA disk
  - 0 MB up to maximum available

Graphics

- One DVI-D connector at front via side card
  - Simultaneous connection of two monitors

I/O

- Ethernet
  - 9-pin D-Sub connector with one or two 10/100Base-T ports instead of two RJ45 connectors
  - Second Ethernet at rear I/O connector J2 instead of one interface at the front
- Rear I/O
  - VGA on CompactPCI® J2 connector as an assembly option for the conduction-cooled board version
  - VBATT on CompactPCI® J1 connector as an assembly option for the conduction-cooled board version

Miscellaneous

- TPM (Trusted Platform Module) chip assembled as an option

Mechanical

- Side card can be added at left or right side of CPU

Operating Temperature

- Depends on system configuration (CPU, hard disk, heat sink...)
- Maximum: +85°C
- Minimum: -40°C (all processors)

Cooling Concept

- Also available with conduction cooling in MEN CCA frame

Please note that some of these options may only be available for large volumes.

For more information on available standard versions, see the online data sheet.

Product Safety

Lithium Battery

This board contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced! See Chapter 4 Maintenance on page 78

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Only store the board in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Issue	Comments	Date
E1	First issue	2011-12-21
E2	Description of new board revision R02: PCIe lanes on side-card connector from PEG interface, VGA and battery voltage via rear I/O	2012-08-31
E3	Added TPM option, extended AMT description, minor restructuring of chapters, cosmetics	2013-05-23
E4	Corrected options and minor errors, added RTC accuracy, reworked block diagram, cosmetics	2014-01-13

Conventions

Indicates important information or warnings concerning proper functionality of the product described in this document.

The globe icon indicates a hyperlink that links directly to the Internet, where the latest updated information is available.
When no globe icon is present, the hyperlink links to specific elements and information within this document.

italics	Folder, file and function names are printed in *italics*.
bold	**Bold** type is used for emphasis.
`mono`	A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by `"0x"`.
comment	Comments embedded into coding examples are shown in green text.
IRQ# /IRQ	Signal names followed by a hashtag "#" or preceded by a forward slash "/" indicate that this signal is either active low or that it becomes active at a falling edge.
in/out	Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "from it the board or component".

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RoHS

Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.

WEEE Application

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.

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Tables

Figures

1 Getting Started

This chapter gives an overview of the board and some hints for first installation in a system.

1.1 Map of the Board

Figure 1. *Map of the board – front view*

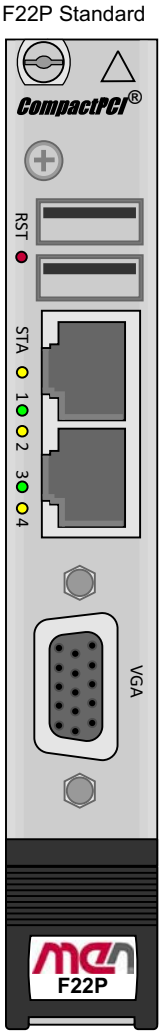
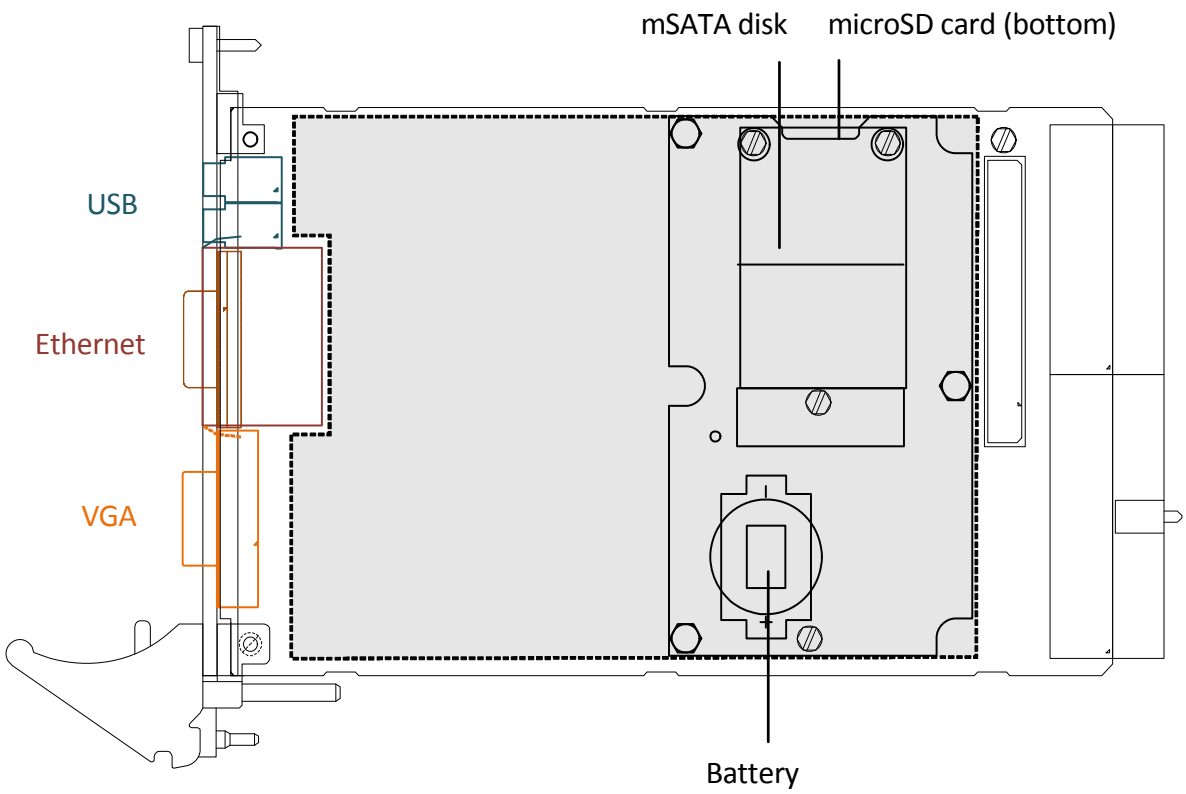


Figure 2. *Map of the board – top view*



1.2 Configuring the Hardware

You should check your hardware requirements before installing the board in a system, since most modifications are difficult or even impossible to do when the board is mounted in a system.

The following check list gives an overview on what you might want to configure.

☑ microSD

The board is shipped without a microSD card. You should check your needs and install a suitable microSD card.

> Refer to Chapter 2.9 Mass Storage on page 29 for more information on installation of the card.

☑ mSATA disk

The board is shipped without an mSATA disk. You should check your needs and install a suitable disk.

> Refer to Chapter 2.9.3 mSATA Disk on page 31 for more information on installation of the card.

☑ Expansion by a side card

The board offers the option of adding one side card. Side cards come in standard 3U format and can be attached directly to F21P at the heat sink side. Every side card has dedicated functions, e.g. legacy COM interfaces, SATA hard disk or DVI front connectors.

> Refer to Chapter 2.14 Side-Card Interface on page 40 for further information on side cards.

The MEN sales staff will be glad to help you find the right extension and front panel solution. See also MEN's website for ordering information and standard products.

1.3 Integrating the Board into a System

You can use the following check list when installing the F21P in a system for the first time and with minimum configuration.

- ☑ Power-down the system.
- ☑ Remove all boards from the CompactPCI system.
- ☑ Insert the F21P into the system slot of your CompactPCI system, making sure that the CompactPCI connectors are properly aligned.

  Note: The system slot of every CompactPCI system is marked by a △ triangle on the backplane and/or at the front panel. It also has red guide rails.
- ☑ Connect a USB keyboard and mouse to the USB connectors at the front panel.
- ☑ Connect a CRT or flat-panel display to the VGA connector at the front panel.
- ☑ Power-up the system.
- ☑ You can start up the BIOS setup menu by hitting the <F2> key.
- ☑ Now you can make configurations in BIOS.

For more Information on the BIOS see Chapter 3 BIOS on page 56

- ☑ Observe the installation instructions for the respective software.

1.4 Troubleshooting at Start-up

If you have any problems at start-up of the F21P, you can start the board with EFI default settings for troubleshooting.

For more Information on the BIOS see Chapter 3 BIOS on page 56

1.5 Configuring BIOS

The F21P is equipped with an InsydeH2O UEFI framework. Normally you won't need to make any changes in the BIOS setup.

If you do, however, you find further details on the F21P's BIOS in Chapter 3 BIOS on page 56.

1.6 Installing Operating System Software

The board supports Windows, Linux, VxWorks (on request) and QNX (on request).

You can find any software available on MEN's website.

By standard, no operating system is installed on the board. Refer to the respective manufacturer's documentation on how to install operating system software.

1.6.1 Installing Windows XP or Windows 7 on USB Devices

The microSD card of the F21P is connected via USB. A standard Windows operating system (like Windows XP Professional or Windows 7 Ultimate) does not support direct installation on USB memory devices.

There are three possible solutions:

- Install the operating system on the mSATA disk of the F21P.
- Add a hard drive (SATA, mSATA) on a peripheral board or side card
- Switch to an Embedded Windows (like Windows Embedded Standard or Windows Embedded Standard 7). These Embedded Windows operating systems support being installed on and booted from a USB device.

Linux supports booting from a USB device without problems.

1.7 Installing Driver Software

For a detailed description on how to install driver software refer to the respective documentation.

You can find any driver software and documentation available for download on MEN's website.

2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU.

More information on the individual controller chips and the CPU can be obtained from the data sheets or data books of the semiconductor manufacturer concerned, see Chapter 5.1 Literature and Web Resources on page 79.

2.1 Power Supply

The power sequence is compliant to the ATX Power Supply Design Guide.

There are only two possible ways to power the F21P:

- +5V, +3.3V **and** +12V via CompactPCI connector J1
- +5V **only** via CompactPCI connector J1

To supply the board with 3.3V and 5V is not allowed and may cause serious damage. If +3.3V are supplied via CompactPCI connector J1, the +12V supply always has to be present.

If the +12V are not present, the board automatically generates +3.3V and also feeds them to the backplane, which would cause a conflict with the external +3.3V supply.

2.2 Board Supervision

The F21P provides an intelligent board management controller (BMC) with the following main features:

- Board power sequencing control
- Voltage supervision
- System watchdog
- Software reset functionality
- Error state logging
- Power mode settings
- SMBus communication with main CPU

The watchdog device monitors the board on operating system level. If enabled, the watchdog must be triggered by application software. If the trigger is overdue, the watchdog initiates a board reset and this way can put the system back into operation when the software hangs.

The watchdog uses a configurable time interval or is disabled. Settings are made through BIOS or via an MEN software driver.

In addition, the F21P uses a temperature device to measure the local board temperature.

MEN provides dedicated software drivers for the board controller and the temperature device. For a detailed description of the functionality of the driver software refer to the drivers' documentation.

You can find any driver software and documentation available for download on MEN's website.

2.3 Intel Active Management Technology (AMT)

F21P boards equipped with an Intel Core i7 or i5 processor support Intel Active Management Technology (AMT 7.0). Intel AMT is powered by a separate hardware engine in Intel chipsets which enables e.g. out-of-band (OOB) diagnostics, remote control, IDE-Redirect, Serial-over-LAN (SOL), agent presence checking and network traffic filtering.

AMT is supported on the lower front Ethernet interface (ETH2) of the F21P. For information on how to enable the AMT BIOS extension see Chapter 3 BIOS.

MEN provides an application note on how to switch on the AMT functionality and log onto the CPU board via VNC afterwards.

If the supercapacitor and/or the battery is empty, the F21P loses its complete AMT settings due to Intel's security standards.

As an option, a BIOS setting can be implemented which makes it possible to switch the AMT interface to the backplane via the Ethernet rear I/O card. In this case, there is only one Ethernet interface (ETH1) available at the front panel.

Contact MEN's sales team for further information.

2.4 Trusted Platform Module

As an assembly option, a trusted platform module to protect the content of the SATA storage devices can be implemented on the F21P. A TPM module compliant to the TPM v1.2 specification can be used.

Contact MEN's sales team for further information.

2.5 Reset Behavior and Power States

The F21P can be reset using the reset button on the front panel or the *PBRST#* signal on the backplane. It supports the S5, S4, S3, S0 and Mx power states. All voltages which are not required are deactivated while the board is into a lower power state.

See also Chapter 2.17 Reset Button and Status LED on page 55.

2.6 Real-Time Clock

The board includes a real-time clock connected to the chipset. For data retention during power off the RTC is backed up by a supercapacitor. The supercapacitor gives an autonomy of approx. 14 hours when fully loaded. Under normal conditions, replacement should be superfluous during lifetime of the board. The RTC can generate interrupt requests to the chipset.

The RTC has an accuracy of approximately 1.7 seconds/day (11 minutes/year) at 25°C.

For retention of time/date data after a power off of more than 8-10 hours the RTC is also backed by a battery.

For ordering options see MEN's website.

2.7 Processor Core

The F21P can be equipped with different types of Intel i7, i5 or Celeron processors. The following table gives a performance overview:

Table 1. *Processor core options on F21P*

Processor Type	Core Frequency	Cores/ Threads	Power Consumption	Cache	AMT Support
Intel Core i7-2715QE	2.1 GHz	4/8	45 W	6 MB	yes
Intel Core i7-2655LE	2.2 GHz	2/4	25 W	4 MB	yes
Intel Core i7-2610UE	1.5 GHz	2/4	17 W	4 MB	yes
Intel Core i5-2515E	2.5 GHz	2/4	35 W	3 MB	yes
Intel Core i3-2340UE	1.3 GHz	2/4	17 W	3 MB	no
Intel Core i3-2310E	2.1 GHz	2/4	35 W	3 MB	no
Intel Celeron B810E	1.6 GHz	2/2	35 W	2 MB	no
Intel Celeron 847E	1.1 GHz	2/2	17 W	2 MB	no
Intel Celeron 827E	1.4 GHz	1/1	17 W	1.5 MB	no

2.7.1 Thermal Considerations

A suitable heat sink is provided to meet thermal requirements. For special requirements a larger heat sink is also available on request.

Note that if you use any other heat sink than that supplied by MEN, or no heat sink at all, warranty on functionality and reliability of the F21P may cease. If you have any questions or problems regarding thermal behavior, contact MEN.

Contact MEN sales for more information on this topic.

2.8 Memory

The standard board versions provide a memory configuration suitable for many applications. However, memory on the F21P can also be configured for your needs.

For standard memory sizes and ordering options see MEN's website.

2.8.1 DRAM System Memory

The board provides up to 16 GB onboard, soldered DDR3 (double data rate) SDRAM. The memory bus is 2x72 bits wide (dual channel) and operates with up to 1066 MHz.

2.8.2 Boot Flash

The F21P has a 64-Mbit SPI Serial Flash implemented as onboard Flash for BIOS data.

2.9 Mass Storage

The F21P offers six SATA lines on the J2 rear I/O connector and the side card connector. In addition, the board offers the possibility to connect an mSATA disk and a microSD card on a small adapter card in the heat sink area which is assembled by standard.

See Chapter 2.9.1 Serial ATA (SATA) for details on the Serial ATA interface, Chapter 2.9.3 mSATA Disk for details on the mSATA interface and also Chapter 2.9.2 microSD Card for more information on the microSD card.

2.9.1 Serial ATA (SATA)

The serial ATA (SATA) interface is controlled by the platform controller hub and provides six SATA channels.

In compliance with the CompactPCI PlusIO standard PICMG 2.30 four of these interfaces are led to the J2 rear I/O connector.

One SATA channel is led to the side-card connector. The device can be connected through the use of a side card. The sixth channel is used for the mSATA disk.

Four interfaces are compliant to SATA revision 2.x (3.0 Gb/s). Two of the interfaces on the J2 rear I/O connector are compliant to SATA revision 3.x (6.0 Gb/s). The interfaces can be run in AHCI and RAID mode. RAID 0, 1, 5 and 10 are supported.

See Chapter 2.14 Side-Card Interface on page 40 for details on the side-card interface, and also Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 50 for details on the rear I/O.

2.9.2 microSD Card

The F21P provides an onboard microSD card slot on the bottom side of the mSATA adapter card in the heat sink area. The slot is ready-to-use. The F21P is shipped without a microSD card installed.

See MEN's website for ordering options.

2.9.2.1 Inserting and Extracting a microSD Card

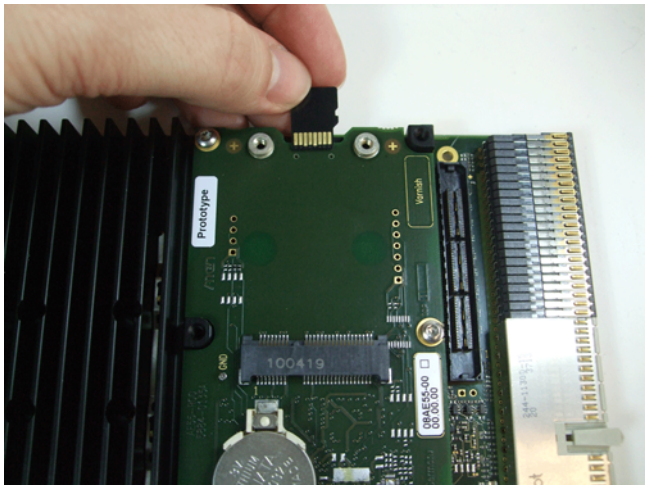
The microSD card has to be installed before the mSATA disk as it is difficult to access it afterwards.

To install a microSD card, stick to the following procedure.

☑ Power down your system and remove the F21P from the system.

☑ Put the board on a flat surface.

☑ Insert the microSD card into the slot with the contacts at the top.



☑ Make sure that it clicks into place properly.

☑ For extracting the card push it down and pull it out.

2.9.3 mSATA Disk

The mSATA disk is controlled via a SATA channel from the chipset. The F21P is shipped without an mSATA disk installed.

See MEN's website for ordering options.

2.9.3.1 Installing an mSATA Disk

To install an mSATA disk, stick to the following procedure.

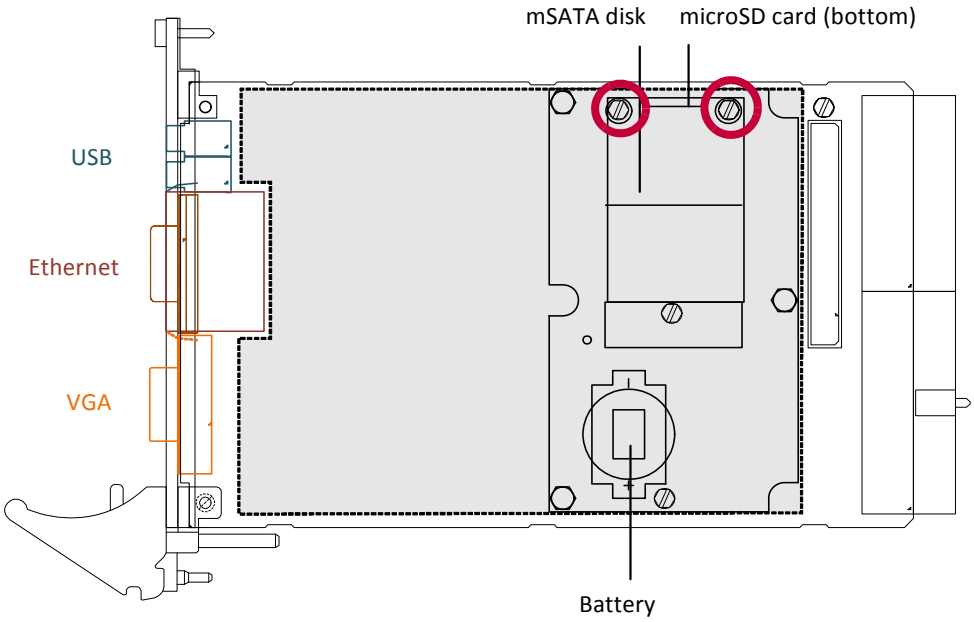
☑ Power down your system and remove the F21P from the system.

☑ Put the board on a flat surface.

☑ Insert the mSATA disk carefully in a 30° angle.

☑ Make sure that all the contacts are aligned properly and the card is firmly connected with the card connector.

☑ Fix the card using two M2.5 x4 screws and two spacers (highlighted in red).



2.10 Graphics

The graphics subsystem is part of the Intel QM67 Platform Controller Hub and supports VGA as well as different digital display interfaces (HDMI, DisplayPort and SDVO).

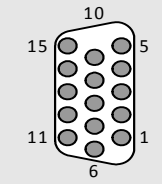
2.10.1 VGA Front Connection

You can connect a VGA monitor directly at the F21P's front panel. The pinout of the 15-pin HD-Sub connector is standard VGA.

Connector types:

- 15-pin HD-Sub receptacle according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  15-pin HD-Sub plug according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

Table 2. *Pin assignment of 15-pin HD-Sub VGA receptacle connector*



15	SCL	10	GND	5	GND
14	VSYNC	9	-	4	-
13	HSYNC	8	GND	3	B
12	SDA	7	GND	2	G
11	-	6	GND	1	R

Table 3. *Signal mnemonics of 15-pin HD-Sub VGA connector*

Signal	Direction	Function
GND	-	Ground
HSYNC	out	Horizontal synchronization
R, G, B	out	Analog monitor interface (red, green, blue)
SCL	out	Monitor I²C interface
SDA	in/out	
VSYNC	out	Vertical synchronization

2.10.2 VGA Rear Connection

For conduction-cooled versions of the F21P, there is the possibility to lead a display data channel to the backplane via the J1 CompactPCI connector.

2.10.3 Connection via Digital Display Interface

The F21P provides two digital display interfaces on the side-card connector. One supports SDVO, DisplayPort and HDMI, the other only DisplayPort and HDMI. Embedded audio is also supported on DisplayPort and HDMI.

One DVI interface can be implemented using the SDVO interface on an MEN side card.

See Chapter 2.14 Side-Card Interface on page 40 for further details on the side-card interface.

See MEN's website for available side cards. For possibilities to implement DisplayPort or HDMI using a side card please contact MEN's sales team.

2.11 USB Interfaces

The F21P provides eleven USB 2.0 ports controlled by the chipset. Two USB interfaces are routed to standard front-panel connectors, four are led to the side-card connector, and another four can be accessed on the CompactPCI J2 rear I/O connector (compliant to the CompactPCI PlusIO standard). The remaining interface is used for connection of the microSD card. The USB interfaces support UHCI.

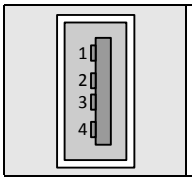
2.11.1 Front-Panel Connection

Two USB interfaces are accessible at the front panel.

Connector types:

- 4-pin USB Series A receptacle according to Universal Serial Bus Specification Revision 1.0
- Mating connector:
  4-pin USB Series A plug according to Universal Serial Bus Specification Revision 1.0

Table 4. *Pin assignment of USB front-panel connectors*



1	+5V
2	USB_D-
3	USB_D+
4	GND

Table 5. *Signal mnemonics of USB front-panel connectors*

Signal	Direction	Function
+5V	out	+5 V power supply
GND	-	Digital ground
USB_D+, USB_D-	in/out	USB lines, differential pair

2.11.2 Side-Card Connection

Four USB interfaces are accessible via a side card.

See Chapter 2.14 Side-Card Interface on page 40 for further details on the side-card interface.

See MEN's website for available side cards and board versions.

2.11.3 Rear I/O Connection (CompactPCI PlusIO)

Four USB interfaces are accessible via rear I/O in compliance to the CompactPCI PlusIO standard PICMG 2.30.

See Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 50 for information on J2 rear I/O pin assignments.

2.12 Ethernet Interfaces

The F21P has three Ethernet interfaces connected to the processor and the PCH via three x1 PCI Express (PCIe) links. They are controlled by two Intel 82574L Ethernet controllers and one Intel 82579LM Ethernet PHY. They support 10 Mbits/s up to 1000 Mbits/s as well as full-duplex operation and autonegotiation. The lower front interface supports AMT.

The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable.

The naming of the interfaces may differ depending on the operating system. The MAC addresses on F21P are:

- LAN1 (upper front interface):
  - 0x 00 C0 3A AE 80 00 - 0x 00 C0 3A AE FF FF
- LAN2 (lower front interface):
  - 0x 00 C0 3A AF 00 00 - 0x 00 C0 3A AF 7F FF
- LAN3 (rear I/O) :
  - 0x 00 C0 3A AF 80 00 - 0x 00 C0 3A AF FF FF

where "00 C0 3A" is the MEN vendor code. The last six digits describe the range from which the addresses for the board are taken. The serial number is added to the first number in the range:

- Serial number 0042 (0x2A): 0x 80 00 + 0x 00 2A = 0x 80 2A.

Also see Chapter 5.2 Finding out the Product's Article Number, Revision and Serial Number on page 81.

2.12.1 Front-Panel Connection

Two standard RJ45 connectors are available at the front panel. There are two status LEDs for each channel at the front panel.

The pin assignment corresponds to the Ethernet specification IEEE802.3.

Table 6. *Signal mnemonics of Ethernet 10/100/1000Base-T connectors*

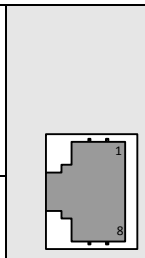
Signal	Direction	Function
BI_Dx+/-	in/out	Differential pairs of data lines for 1000Base-T
RX+/-	in	Differential pair of receive data lines for 10/100Base-T
TX+/-	out	Differential pair of transmit data lines for 10/100Base-T

Connection via RJ45 Connectors

Connector types:

- Modular 8/8-pin mounting jack according to FCC68
- Mating connector:
  Modular 8/8-pin plug according to FCC68

Table 7. *Pin assignment and status LEDs of 8-pin RJ45 Ethernet 10/100/1000Base-T connectors (LAN1/LAN2)*

On: Link up Off: Link down	L		1	BI_DA+
			2	BI_DA-
			3	BI_DB+
			4	BI_DC+
On: Transmit or receive activity Off: No transmit or receive activity Blinking: Transmit or receive activity	A		5	BI_DC-
			6	BI_DB-
			7	BI_DD+
			8	BI_DD-

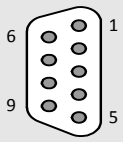
Connection via 9-pin D-Sub Connector (optional)

A D-Sub connector can be implemented as an option. In this case, only 10Base-T and 100Base-TX are supported, no Gigabit Ethernet connection. The two interfaces are routed to one D-Sub connector.

Connector types:

- 9-pin D-Sub plug according to DIN41652/MIL-C-24308, with thread bolt UNC 4-40
- Mating connector:
  9-pin D-Sub receptacle according to DIN41652/MIL-C-24308, available for ribbon cable (insulation piercing connection), hand-soldering connection or crimp connection

Table 8. *Pin assignment of 9-pin D-Sub 10Base-T/100Base-TX plug connector (LAN1/LAN2)*

			1	LAN2_TX+
	6	LAN2_TX-	2	LAN1_TX+
	7	LAN1_TX-	3	-
	8	LAN1_RX-	4	LAN1_RX+
	9	LAN2_RX-	5	LAN2_RX+

2.12.2 Rear I/O Connection

The third Ethernet interface is controlled via a PCI Express x1 link from the processor and available at the J2 rear I/O connector in compliance with CompactPCI PlusIO standard PICMG 2.30.

As an option, one of the front Ethernet interfaces can be led to the J2 connector. A special board version is required for this. On this board version the lower front Ethernet interface with AMT functionality cannot be used.

For the J2 rear I/O pin assignments see Chapter 2.16.1 CompactPCI PlusIO Rear I/O on page 50.

Contact MEN's sales staff for further information.

2.13 High Definition (HD) Audio Interface

The F21P provides an HD audio interface accessible via a side card. Embedded audio on DisplayPort and HDMI is supported.

Also see Chapter 2.14 Side-Card Interface on page 40 for further details on the side-card interface.

See MEN's website for available side cards.

Also see Chapter 5.1 Literature and Web Resources on page 79 for literature on HD audio.

2.14 Side-Card Interface

MEN offers a number of side cards for F21P, featuring different I/O functionality. The side cards are all standard 3U Eurocards in 4 HP (single) width. Access to I/O connectors is given directly from the front panel.

The side-card connector is located at the top side of the board, so that one side card can be attached to the right side of the F21P. As an option, the F21P can also be supplied with the side-card connector at the bottom side, so that the side card may be attached to the left side of the CPU.

The side-card connector on F21P supports the following interfaces:

- One SATA channel (switchable to port A or B via BIOS)
- Four USB interfaces
- Three PCI Express x1 links
- HD audio interface
- One digital video output supporting SDVO, DisplayPort and HDMI (Port B)
- One digital video output supporting DisplayPort and HDMI (Port C)

Neither the +3.3V nor the +5V pins of the expansion interface connector are protected against a short-circuit situation! This connector therefore should be used exclusively for attachment of a side card.

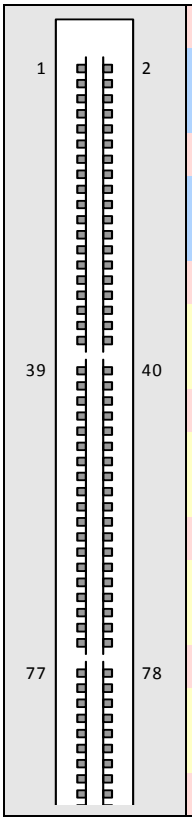
See MEN's website for available side cards and board versions.

2.14.1 Connection

Connector types:

- 114-pin matched impedance receptacle connector, MICTOR 0.64 mm grid
- Mating connector:
  114-pin matched impedance plug connector, MICTOR 0.64 mm grid

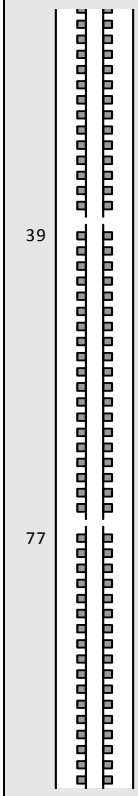
Table 9. *Pin assignment of 114-pin side-card connector, pins 1..38*



1	GND		2	GND
3	SATA_A_TX+		4	SATA_B_TX+
5	SATA_A_TX-		6	SATA_B_TX-
7	GND		8	GND
9	SATA_A_RX+		10	SATA_B_RX+
11	SATA_A_RX-		12	SATA_B_RX-
13	GND		14	GND
15	PCIE1_TX+		16	PCIE3_TX+
17	PCIE1_TX-		18	PCIE3_TX-
19	GND	GND	20	GND
21	PCIE1_RX+		22	PCIE3_RX+
23	PCIE1_RX-		24	PCIE3_RX-
25	GND		26	GND
27	PCIE0_TX+		28	PCIE2_TX+
29	PCIE0_TX-		30	PCIE2_TX-
31	GND		32	GND
33	PCIE0_RX+		34	PCIE2_RX+
35	PCIE0_RX-		36	PCIE2_RX-
37	GND		38	GND

Note: There is one SATA port on the side-card connector which can be switched to Port A or Port B via the BIOS. PCI Express port 3 can be implemented on a special board version instead of port 1.

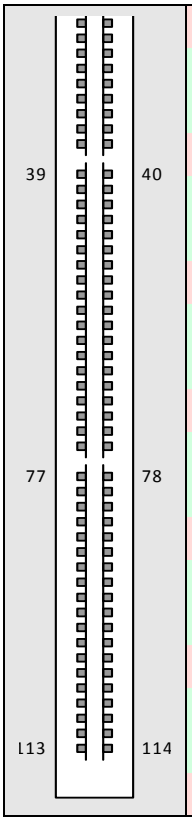
Table 10. *Pin assignment of 114-pin side-card connector, pins 39..76*



		39	+3.3V		40	+3.3V
		41	USB_1_2_OC#		42	HDA_SYNC
		43	USB_3_4_OC#		44	HDA_BIT_CLK
		45	GND		46	HDA_RST#
		47	USB_D3-		48	HDA_SDOUT
		49	USB_D3+		50	HDA_SDIN
39	40	51	GND		52	GND
		53	USB_D1-		54	PCIE_WAKE#
		55	USB_D1+		56	PLT_RST#
		57	GND		58	-
		59	USB_D5-	+5V	60	SMB_CLK
		61	USB_D5+		62	SMB_DATA
		63	GND		64	GND
77	78	65	USB_D4-		66	DPB_OB_AUX_p/ SDVO_CTRLCLK
		67	USB_D4+		68	DPB_OB_AUX_n/ SDVO_CTRLDATA
		69	GND		70	GND
		71	PCIE_CLK_A_REF+		72	PCIE_CLK_B_REF+
		73	PCIE_CLK_A_REF-		74	PCIE_CLK_B_REF-
		75	GND		76	GND

Note: The signals marked in gray are multiplexed.

Table 11. *Pin assignment of 114-pin side-card connector, pins 77..114*



77	GND		78	GND
79	SDVO_TVCLKIN-		80	SDVO_FLDSTALL-
81	SDVO_TVCLKIN+		82	SDVO_FLDSTALL+
83	GND		84	GND
85	DDPB_[2]_n		86	DDPC_[2]_n
87	DDPB_[2]_p		88	DDPC_[2]_p
89	GND		90	GND
91	DDPB_[1]_n		92	DDPC_[1]_n
93	DDPB_[1]_p		94	DDPC_[1]_p
95	GND	GND	96	GND
97	DDPB_[0]_n		98	DDPC_[0]_n
99	DDPB_[0]_p		100	DDPC_[0]_p
101	GND		102	GND
103	DDPB_[3]_n		104	DDPC_[3]_n
105	DDPB_[3]_p		106	DDPC_[3]_p
107	GND		108	GND
109	SDVO_INT-		110	DDP_CTRDATA
111	SDVO_INT+		112	DDP_CTRLCLK
113	GND		114	DDPC_HPD

Table 12. *Signal mnemonics of 114-pin side-card connector*

	Signal	Direction	Function
Power	+3.3V	out	+3.3 V power supply
	+5V	out	+5 V power supply
	GND	-	Digital ground of respective interface
SATA (Port A or B depending on BIOS setting)	SATA_A_RX+, SATA_A_RX-	in	Differential pair of SATA receive lines, port A
	SATA_A_TX+, SATA_A_TX-	out	Differential pair of SATA transmit lines, port A
	SATA_B_RX+, SATA_B_RX-	in	Differential pair of SATA receive lines, port B
	SATA_B_TX+, SATA_B_TX-	out	Differential pair of SATA transmit lines, port B
PCI Express	PCIE_CLK_A_REF+, PCIE_CLK_A_REF-	out	Reference clock A 100 MHz
	PCIE_CLK_B_REF+, PCIE_CLK_B_REF-	out	Reference clock B 100 MHz
	PCIE0_RX+, PCIE0_RX-	in	Differential pair of PCIe receive lines, port 0
	PCIE0_TX+, PCIE0_TX-	out	Differential pair of PCIe transmit lines, port 0
	PCIE1_RX+, PCIE1_RX-	in	Differential pair of PCIe receive lines, port 1
	PCIE1_TX+, PCIE1_TX-	out	Differential pair of PCIe transmit lines, port 1
	PCIE2_RX+, PCIE2_RX-	in	Differential pair of PCIe receive lines, port 2
	PCIE2_TX+, PCIE2_TX-	out	Differential pair of PCIe transmit lines, port 3
	PCIE3_RX+, PCIE3_RX-	in	Differential pair of PCIe receive lines, port 3 (optional, can be implemented on a special board version instead of port 1)
	PCIE3_TX+, PCIE3_TX-	out	Differential pair of PCIe transmit lines, port 3
	PCIE_WAKE#	in	Wake signal from PCIe device to wake F21P from sleep state
USB	USB_D[1]+, USB_D[1]-	in/out	Differential pair of USB lines, port 2
	USB_D[2]+, USB_D[2]-	in/out	Differential pair of USB lines, port 3
	USB_D[3]+, USB_D[3]-	in/out	Differential pair of USB lines, port 4
	USB_D[4]+, USB_D[4]-	in/out	Differential pair of USB lines, port 5
	USB_OC12#	in	USB overcurrent, ports 1and 2
	USB_OC34#	in	USB overcurrent, ports 3 and 4

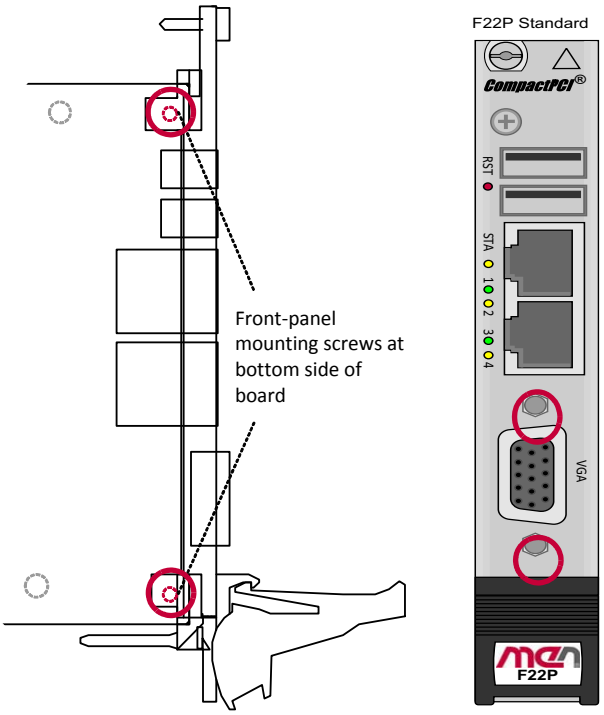
	Signal	Direction	Function
HD Audio	HDA_BIT_CLK	in/out	HD Audio serial data clock
	HDA_RST#	out	HD Audio reset
	HDA_SDIN	in	HD Audio serial data in
	HDA_SDOUT	out	HD Audio serial data out
	HDA_SYNC	out	HD Audio synchronization
Digital Display Interface (DDP)	DDPB_[x]_n, DDPB_[x]_p,	out	Digital display interface B data, differential pair
	DDPC_[x]_n, DDPC_[x]_p,	out	Digital display interface C data, differential pair
	DDP_CTRDATA	in/out	Digital display interface control data
	DDP_CTRLCLK	in/out	Digital display interface control clock
	DDPC_HPD	in	Digital display interface hot plug detect
	DPB_OB_AUX_n, DPB_OB_AUX_p (shared with SDVOCTRL_CLK and SDVOCTRL_DATA	in/out	Digital display interface auxiliary lines, needed when interface B is used as DisplayPort or HDMI
	SDVOB_INT+, SDVOB_INT-	in	Serial digital video input interrupt, differential pair
	SDVO_FLDSTALL+, SDVO_FLDSTALL-	in	Serial digital video field stall, differential pair
	SDVO_TVCLKIN+, SDVO_TVCLKIN-	in	Serial digital video TVOUT synchronization clock, differential pair
	SDVOCTRL_CLK (shared with DPB_OB_AUX_p)	in/out	I2C based control signal (clock) for SDVO device, needed when interface B is used as SDVO
	SDVOCTRL_DATA (shared with DPB_OB_AUX_n)	in/out	I2C based control signal (data) for SDVO device, needed when interface B is used as SDVO
Other	PLT_RST#	out	Platform reset (global reset)
	SMB_CLK	out	System Management Bus clock
	SMB_DATA	in/out	System Management Bus data

2.14.2 Installing a Side Card

Perform the following steps to install a side card:

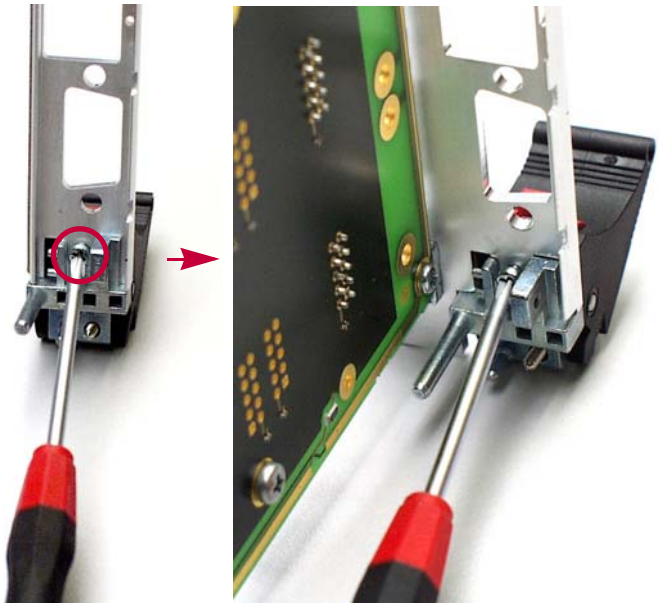
☑ Power-down your system and remove the F21P from the system.

☑ Remove the front panel: Loosen and remove the screws highlighted in red.

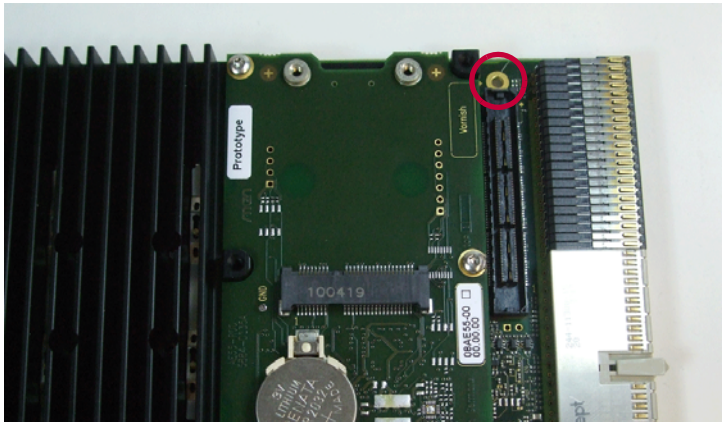


☑ Remove the front-panel ejector from the F21P front panel: Loosen the ejector screw at the back of the front panel.

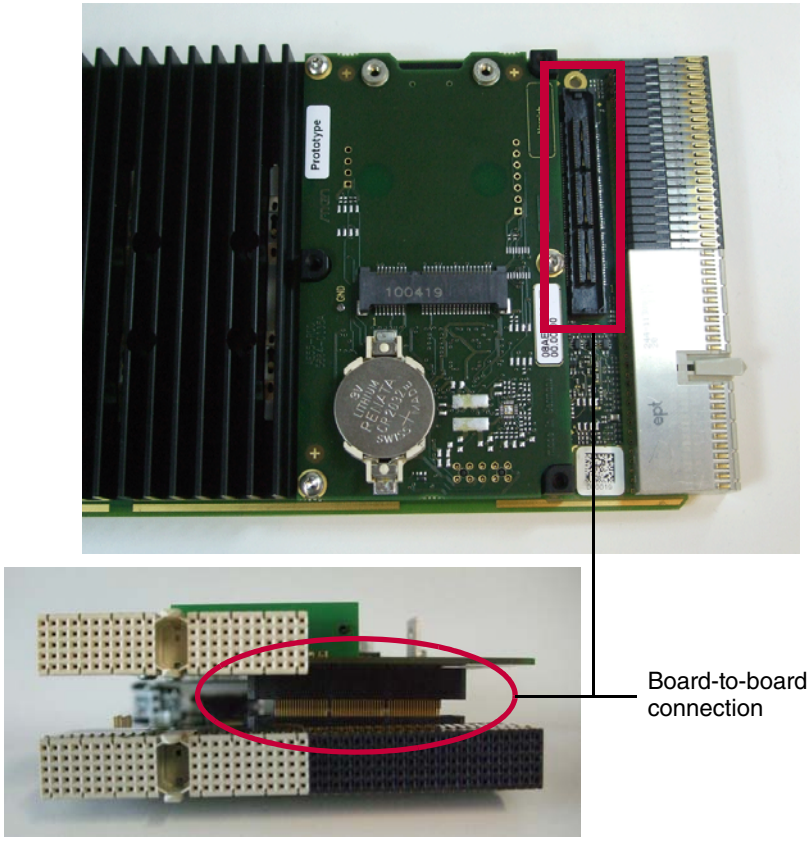
☑ Install the ejector on the side card's front panel.



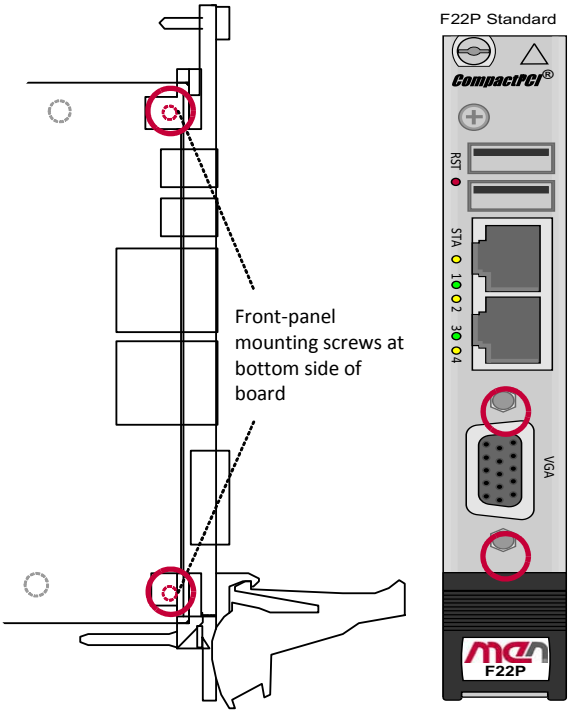
☑ Install the side card standoff supplied with the side card in the mounting hole indicated in red in the following picture. Note that two different standoffs are supplied with the side card. For the F21P the longer standoff (M2x18,72 I/I) is required.



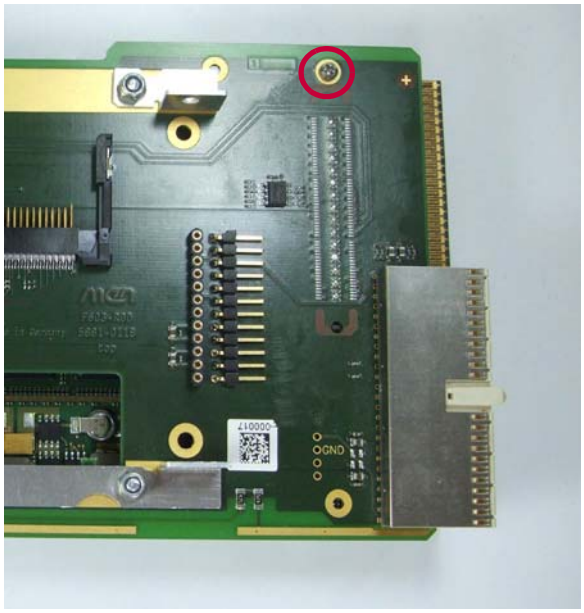
☑ Each side card comes with a dedicated one-piece, two-slot front panel. Align the F21P's front panel connectors with the side card's front panel, and align the board-to-board connector of the side card with the side-card connector of F21P. Press the board-to-board connectors together.



☑ Fasten the front panel: Install the screws removed before as highlighted in red.



☑ Fasten the side-card standoff using the spring and screw provided with the side card at the top of the side card.



☑ Reinsert the board into your system.

2.15 PCI Express

2.15.1 General

PCI Express (PCIe) succeeds PCI and AGP and offers higher data transfer rates.

As opposed to the PCI bus, PCIe is no parallel bus but a serial point-to-point connection. Data is transferred using so-called lanes, with each lane consisting of a line pair for transmission and a second pair for reception. Individual components are connected using switches.

At the electrical level, each lane consists of two unidirectional LVDS (Low Voltage Differential Signaling) pairs. Transmit and receive are separate differential pairs, for a total of 4 data wires per lane.

PCIe supports full-duplex operation and uses a clock rate of 1.25 GHz. This results in a data rate of max. 250 MB/s per lane in each direction. (The standard PCI bus with 32 bits/33 MHz only allows a maximum of 133 MB/s.)

If you use only one lane, you speak of a PCIe x1 link. You can couple several lanes to increase the data rate, e.g. x2 with 2 lanes up to a x32 link using 32 lanes.

In addition, PCIe supports hot plug, for instance to exchange defect expansion boards during operation.

In terms of software, most operating systems can handle PCI Express boards just as well as the old PCI.

2.15.2 Implementation on F21P

On F21P the three Gigabit Ethernet channels are permanently connected via PCIe x1 links. Another three x1 links are available for use over a side card. This means that the side card implementation determines the usage of these three links.

Four PCIe x1 links are led to the J2 rear I/O connector in compliance with the CompactPCI PlusIO standard PICMG 2.30. The interfaces on the J2 connector and the side-card connector support the PCI Express specification 2.x with a data transfer rate of 5 Gbits/s per lane.

2.16 CompactPCI Interface

The F21P is a 3U CompactPCI system slot board. It implements a 32-bit PCI interface to the CompactPCI backplane which uses a +3.3 V signaling voltage. It also tolerates +5 V.

The CompactPCI bus connects to the processor via a PCI-Express-to-PCI-Bridge. The board supports seven external PCI bus devices.

In combination with a specific side card the F21P can also perform system-slot functionality in a CompactPCI Express system.

2.16.1 CompactPCI PlusIO Rear I/O

The F21P is also compliant to the CompactPCI PlusIO standard PICMG 2.30. This means that it offers a fixed pin assignment of one Gigabit Ethernet, 4 SATA, 4 PCI Express and 4 USB interfaces at the J2 connector. A second Gigabit Ethernet interface can be implemented by switching one front interface to the rear.

As a result, the pin assignment of the F21P rear I/O connector J2 is not compliant anymore to the rear I/O of the F14, F15, F17 and F18.

MEN offers a rear I/O transition module on which all interfaces from the J2 connector can be accessed, the CT12.

Note: The F21P supports one Gigabit Ethernet interface at the rear whereas the PICMG 2.30 CompactPCI PlusIO standard supports up to two.

See MEN's website for further information.

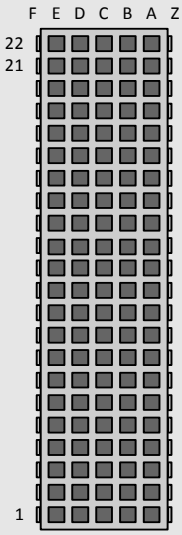
2.16.2 CompactPCI Connector J1

The pin assignment of connector J1 as defined in the CompactPCI specification will not be repeated here. The voltage supply for the battery can optionally be made available on the A4 pin on the conduction-cooled board version.

2.16.3 CompactPCI Connector J2

The table below shows the fixed pinout of the J2 connector as defined in the PICMG 2.30 CompactPCI PlusIO standard.

Table 13. *Pin assignment of CompactPCI connector J2*



	F	E	D	C	B	A	Z
22	GND	GA0	GA1	GA2	GA3	GA4	GND
21	GND	1_ETH_B+	1_ETH_D+	2_ETH_B+	GND	CLK6	GND
20	GND	1_ETH_B-	1_ETH_D-	2_ETH_B-	GND	CLK5	GND
19	GND	1_ETH_A+	1_ETH_C+	2_ETH_A+	GND	GND	GND
18	GND	1_ETH_A-	1_ETH_C-	2_ETH_A-	2_ETH_C+	2_ETH_D+	GND
17	GND	GNT6#	REQ6#	PBRST#	2_ETH_C-	2_ETH_D-	GND
16	GND	CRT_R_D-DC_CLK	GND	DEG#	2_PE_CLK+	4_PE_CLK-	GND
15	GND	GNT5#	REQ5#	FAIL#	2_PE_CLK-	4_PE_CLK+	GND
14	GND	PWRBTN#	SATA_SCL	4_PE_CLKE#	1_PE_CLK+	3_PE_CLK-	GND
13	GND	SATA_SL	SATA_SDO	3_PE_CLKE#	1_PE_CLK-	3_PE_CLK+	GND
12	GND	4_SATA_Rx+	SATA_SDI	2_PE_CLKE#	1_PE_CLKE#	4_PE_Rx00+	GND
11	GND	4_SATA_Rx-	4_SATA_Tx+	4_USB2+	4_PE_Tx00+	4_PE_Rx00-	GND
10	GND	3_SATA_Rx+	4_SATA_Tx-	4_USB2-	4_PE_Tx00-	3_PE_Rx00+	GND
9	GND	3_SATA_Rx-	3_SATA_Tx+	3_USB2+	3_PE_Tx00+	3_PE_Rx00-	GND
8	GND	2_SATA_Rx+	3_SATA_Tx-	3_USB2-	3_PE_Tx00-	2_PE_Rx00+	GND
7	GND	2_SATA_Rx-	2_SATA_Tx+	2_USB2+	2_PE_Tx00+	2_PE_Rx00-	GND
6	GND	1_SATA_Rx+	2_SATA_Tx-	2_USB2-	2_PE_Tx00-	1_PE_Rx00+	GND
5	GND	1_SATA_Rx-	1_SATA_Tx+	1_USB2+	1_PE_Tx00+	1_PE_Rx00-	GND
4	GND	CRT_R_D-DC_DATA	1_SATA_Tx-	1_USB2-	1_PE_Tx00-	V_IO	GND
3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4	GND
2	GND	REQ3#	GNT2#	-	CLK3	CLK2	GND
1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1	GND

Note: SATA ports 3 and 4 support SATA revision 3.x (6.0 Gb/s). The second Ethernet interface (marked in gray) can be implemented as an option on a special board version.

Table 14. *Signal mnemonics of CompactPCI connector J2 – CompactPCI and CompactPCI PlusIO rear I/O*

	Signal	Direction	Function
CompactPCI	CLK[6:1]	out	Clocks 1 to 6
	PBRST#	in	Push button reset
	DEG#	in	Power supply degenerate
	FAIL#	in	Power supply fail
	PWRBTN#	in	Power button
	REQ#/GNT#[6:1]	in/out	Request/grant pairs 1 to 6
Ethernet	1_ETH_A+, 1_ETH_A-	in/out	Differential data pair 0, Ethernet port 1
	1_ETH_B+, 1_ETH_B-	in/out	Differential data pair 1, Ethernet port 1
	1_ETH_C+, 1_ETH_C-	in/out	Differential data pair 2, Ethernet port 1
	1_ETH_D+, 1_ETH_D-	in/out	Differential data pair 3, Ethernet port 1
	2_ETH_A+, 2_ETH_A-	in/out	Differential data pair 0, Ethernet port 2 (instead of one interface at the front)
	2_ETH_B+, 2_ETH_B-	in/out	Differential data pair 1, Ethernet port 2 (instead of one interface at the front)
	2_ETH_C+, 2_ETH_C-	in/out	Differential data pair 2, Ethernet port 2 (instead of one interface at the front)
	2_ETH_D+, 2_ETH_D-	in/out	Differential data pair 3, Ethernet port 2 (instead of one interface at the front)

	Signal	Direction	Function
SATA	1_SATA_Rx+, 1_SATA_Rx-	in	Differential pair of SATA receive lines, port 1
	1_SATA_Tx+, 1_SATA_Tx-	out	Differential pair of SATA transmit lines, port 1
	2_SATA_Rx+, 2_SATA_Rx-	in	Differential pair of SATA receive lines, port 2
	2_SATA_Tx+, 2_SATA_Tx-	out	Differential pair of SATA transmit lines, port 2
	3_SATA_Rx+, 3_SATA_Rx-	in	Differential pair of SATA receive lines, port 3 (SATA revision 3.x support)
	3_SATA_Tx+, 3_SATA_Tx-	out	Differential pair of SATA transmit lines, port 3 (SATA revision 3.x support)
	4_SATA_Rx+, 4_SATA_Rx-	in	Differential pair of SATA receive lines, port 4 (SATA revision 3.x support)
	4_SATA_Tx+, 4_SATA_Tx-	out	Differential pair of SATA transmit lines, port 4 (SATA revision 3.x support)
SGPIO	SATA_SC	out	Clock signal
	SATA_SL	out	Last clock of a bit stream; begin a new bit stream on the next clock
	SATA_SDO	out	Serial data output bit stream
	SATA_SDI	in	Serial data input bit stream (may not be supported by all SGPIO devices)
USB	1_USB2+, 1_USB2-	in/out	Differential pair of USB lines, port 1
	2_USB2+, 2_USB2-	in/out	Differential pair of USB lines, port 2
	3_USB2+, 3_USB2-	in/out	Differential pair of USB lines, port 3
	4_USB2+, 4_USB2-	in/out	Differential pair of USB lines, port 4

	Signal	Direction	Function
PCI Express	1_PE_Rx00+, 1_PE_Rx00-	in	Differential PCIe receive lines, lane 1
	1_PE_Tx00+, 1_PE_Tx00-	out	Differential PCIe transmit lines, lane 1
	2_PE_Rx00+, 2_PE_Rx00-	in	Differential PCIe receive lines, lane 2
	2_PE_Tx00+, 2_PE_Tx00-	out	Differential PCIe transmit lines, lane 2
	3_PE_Rx00+, 3_PE_Rx00-	in	Differential PCIe receive lines, lane 3
	3_PE_Tx00+, 3_PE_Tx00-	out	Differential PCIe transmit lines, lane 3
	4_PE_Rx00+, 4_PE_Rx00-	in	Differential PCIe receive lines, lane 4
	4_PE_Tx00+, 4_PE_Tx00-	out	Differential PCIe transmit lines, lane 4
	[1:4]_PE_CLKE#	in	Presence detect, PCIe lane 1..4
	[1:4]_PE_CLK-, [1:4]_PE_CLK+	out	Differential 100 MHz Reference Clock, PCIe lane 1:4
VGA (optional on special conduction -cooled board version)	CRT_R_DDC_CLK		Display Data Channel clock
	CRT_R_DDC_DATA		Display Data Channel data lines

2.16.4 Power Supply Status (*DEG#*, *FAIL#*)

Power supply failures may be detected before the system crashes down by monitoring the signals *DEG#* or *FAIL#*. These active-low lines are additions of the CompactPCI specification and may be driven by the power supply. *DEG#* signals the degrading of the supply voltages, *FAIL#* their possible failure.

2.17 Reset Button and Status LED

The F21P has a reset button and one status LED at the front panel. The reset button is recessed within the front panel and requires a tool, e.g. paper clip to be pressed, preventing the button from being inadvertently activated.

The yellow status LED shows board status messages. The LED is controlled by the board controller. It is switched on when the BIOS starts, switched off when the board is switched off and flashing slowly when the board is in stand-by (S3) status.

During normal operation the LED can be switched on and off using the MEN driver for the board controller.

See MEN's website for further information.

In case of a board failure, the LED displays the following error messages:

Table 15. *Error codes signaled by board management controller via LED flashes*

Number of Flashes	Error	Description
0	*CPUBCI_ERR_NONE*	No error
1	*CPUBCI_ERR_33V*	3.3 V failure
2	*CPUBCI_ERR_INP*	Input voltage failure
3	*CPUBCI_ERR_NO_EXT_PWR_OK*	External power supply failure
4	*CPUBCI_ERR_CPU_TOO_HOT*	CPU temperature too high
5	*CPUBCI_ERR_BIOS_TIMEOUT*	BIOS startup failure
>5		Internal error

2.18 SMBus Devices

Table 16. *SMBus devices*

Address[1]	Function
0x9A / 0x9B	Board controller
0xA0	Memory channel A
0x60	Protected register
0x30	Temperature sensor A
0xA4	Memory channel B
0x64	Protected register
0x34	Temperature sensor B
0xAE	Board EEPROM
0x6E	Protected register
0x3E	Temperature sensor B

[1] The first address is for write command, the second for read command

3 BIOS

The F21P is equipped with an InsydeH2O setup utility from Insyde Software. InsydeH2O is Insyde Software's firmware product line designed to replace traditional PC BIOS. It is an implementation of the Intel's Platform Innovation Framework for UEFI /EFI. The UEFI/EFI specification defines a new model for the interface between operating systems and platform firmware. This interface consists of data tables that contain platform-related information, plus boot and runtime service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running pre-boot applications. This product line is the next generation of PC BIOS technology.

The ">" character in front of a menu item means that a sub-menu is available. An "x" in front of a menu item means that there is a configuration option which needs to be activated through a higher configuration option before being accessible.

The F21P BIOS has two configuration modes. One mode shows only a selection of the most important items and hides items where normally no changes in the settings are required. This manual only describes the short mode. You can easily switch between the two modes via a menu item.

For more details see Chapter Full Configuration Mode on page 58

3.1 Main

InsydeH2O Setup Utility					Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit
InsydeH2O Version			MEN F21P V1.00		
Processor Type			Intel(R) Core(TM) i7-2715QE CPU @ 2.10GHz		
System Bus Speed			1333 MHz		
System Memory Speed			1333 MHz		
Cache RAM			256 kB		
Total Memory			4096 MB		
Channel A					
SODIMM 0			2048 MB		
SODIMM 1			[Not Installed]		
Channel B					
SODIMM 0			2048 MB		
SODIMM 1			[Not Installed]		
Intel ME Version			7.0.4.1197		
Language			<English>		
System Time			[hh:mm:ss]		
System Date			[mm/dd/yyyy]		
Full Configuration Mode			[no]		
F1 Help		↑↓ Select Item		F5/F6 Change Values	F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Submenu	F10 Save and Exit

InsydeH2O Version / MEN Board / Processor Type / System Bus Speed / System Memory Speed / Cache RAM/ Total Memory / Intel ME Version/ MEN EC Version/ SODIMM 0 / SODIMM 1

Description	You cannot change any values in these fields. They are only for information.

Language

Description	Select the default language	
Options	*English*	

System Time

Description	Change the internal clock.	
Options	*hh*	Hours (Valid range from 0 to 23)
	mm	Minutes (Valid range from 0 to 59)
	ss	Seconds (Valid range from 0 to 59)

System Date

Description	Change the date	
Options	*mm*	Month (Valid range from 1 to 12)
	dd	Day (Valid range from 1 to 31)
	yyyy	Year (Valid range from 2000 to 2099)

Full Configuration Mode

Description	The F21P BIOS has two configuration modes. One mode shows only a selection of the most important items and hides items where normally no changes in the settings are required.	
Options	*Yes*	Enable full configuration mode
	No	Disable full configuration mode

3.2 Advanced

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
>Boot Configuration						
>Peripheral Configuration						
>IDE Configuration						
>Thermal Configuration						
>Video Configuration						
>USB Configuration						
>Chipset Configuration						
>ACPI Table/Features Control						
>Active Management Technology Support						
>PCI Express Configuration						
>Platform Configuration						
>Extended ICC						
F1 Help	↑↓ Select Item			F5/F6 Change Values		F9 Setup Defaults
Esc Exit	← → Select Menu			Enter Select > Submenu		F10 Save and Exit

Boot Configuration — Sub-menu

```
SATA Port on Sidecard                    [Port B]
```

SATA Port on Sidecard

Description	Selects the SATA port on the sidecard.	
Options	*Port A*	*Port B*

Peripheral Configuration — Sub-menu

```
HD Audio              [Disabled]
LAN-1                 [Enabled]
LAN-2                 [Enabled]
LAN-3                 [Enabled]
```

HD Audio

Description	Enable or disable the HD Audio controller.	
Options	*Auto*	The controller is enabled if a codec is found.
	Disabled	The controller is disabled even when there is an audio codec.
	Enabled	The controller is enabled independent of the presence of a codec.

LAN-1/LAN-2/LAN-3

Description	Enables or disables the LAN interfaces.	
Options	*Enabled*	*Disabled*

IDE Configuration — Sub-menu IDE Mode

```
IDE Controller           [Enabled]
HDC Configure as         [IDE]

>Serial ATA Port 0       [Not Installed]
>Serial ATA Port 1       [Not Installed]
>Serial ATA Port 2       [Not Installed]
>Serial ATA Port 3       [Not Installed]
>Serial ATA Port 4       [Not Installed]
>Serial ATA Port 5       [Not Installed]
```

IDE Controller

Description	Enables or disables the IDE controllers.	
Options	*Enabled*	*Disabled*

HDC Configure as

Description	Set hard disk controller configure type.	
Options	*IDE*	*RAID*
	AHCI	

Serial ATA Port 0/1/2/3/4/5

Description	Not installed. You can make no changes here.

IDE Configuration — Sub-menu AHCI Mode

```
IDE Controller                  [Enabled]
HDC Configure as                [AHCI]
>Software Feature Mask Configuration
Aggressive LPM Support          [Enabled]
SATA Port 0  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 1  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 2  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 3  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 4  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 5  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]

>Serial ATA Port 0       [Not Installed]
>Serial ATA Port 1       [Not Installed]
>Serial ATA Port 2       [Not Installed]
>Serial ATA Port 3       [Not Installed]
>Serial ATA Port 4       [Not Installed]
>Serial ATA Port 5       [Not Installed]
```

IDE Controller

Description	Enables or disables the IDE controllers.	
Options	*Enabled*	*Disabled*

HDC Configure as

Description	Set hard disk controller configure type.	
Options	*IDE*	*RAID*
	AHCI	

Software Feature Mask Configuration

Description	The RAID OROM/RST driver will refer to the SWFM configuration to enable/disable the storage feature.

Aggressive LPM Support

Description	Enable /disable the aggressive link power management (SALP) support.	
Options	*Enabled*	*Disabled*

SATA Port 0/1/2/3 Hot Plug

Description	Enable/disable Hot Plug. Not supported on SATA ports 4 and 5.	
Options	*Enabled*	*Disabled*

SATA Port 0/1/2/3/4/5 Spin Up Device		
Description	Enable/disable support of staggered spin up (SSS).	
Options	*Enabled*	*Disabled*
SATA Port 0/1/2/3/4/5 Port Multiplier		
Description	Enable/disable support of port multiplier (PMS).	
Options	*Enabled*	*Disabled*
Serial ATA Port 0/1/2/3/4/5		
Description	Not installed. You can make no changes here.	

IDE Configuration — Sub-menu RAID Mode

```
IDE Controller                  [Enabled]
HDC Configure as                [RAID]
>Software Feature Mask Configuration
Aggressive LPM Support          [Enabled]
Alternate ID                    [Disabled]
SATA Port 0  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 1  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 2  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 3  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 4  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]
SATA Port 5  - HotPlug          [Disabled]
             - Spin Up Device   [Disabled]
             - Port Multiplier  [Disabled]

>Serial ATA Port 0       [Not Installed]
>Serial ATA Port 1       [Not Installed]
>Serial ATA Port 2       [Not Installed]
>Serial ATA Port 3       [Not Installed]
>Serial ATA Port 4       [Not Installed]
>Serial ATA Port 5       [Not Installed]
```

IDE Controller

Description	Enables or disables the IDE controllers.	
Options	*Enabled*	*Disabled*

HDC Configure as

Description	Set hard disk controller configure type.	
Options	*IDE*	*RAID*
	AHCI	

Software Feature Mask Configuration

Description	The RAID OROM/RST driver will refer to the SWFM configuration to enable/disable the storage feature.

Aggressive LPM Support

Description	Enable /disable the aggressive link power management (SALP) support.	
Options	*Enabled*	*Disabled*

Alternate ID

Description	Report alternate device ID.

Options	*Enabled*	*Disabled*
SATA Port 0/1/2/3 Hot Plug		
Description	Enable/disable Hot Plug. Not supported on SATA ports 4 and 5.	
Options	*Enabled*	*Disabled*
SATA Port 0/1/2/3/4/5 Spin Up Device		
Description	Enable/disable support of staggered spin up (SSS).	
Options	*Enabled*	*Disabled*
SATA Port 0/1/2/3/4/5 Port Multiplier		
Description	Enable/disable support of port multiplier (PMS).	
Options	*Enabled*	*Disabled*
Serial ATA Port 0/1/2/3/4/5		
Description	Not installed. You can make no changes here.	

Thermal Configuration — Sub-menu

```
>Platform Thermal Configuration

    Shut Down Temperature      [100°C]
    Throttle on Temperature    [85°C]
```

Shut Down Temperature		
Description	ACPI Active Trip Point - the point at which the OS will shut down the system.	
Options	*70°C*	*75°C*
	80°C	*85°C*
	90°C	*100°C*
	110°C	*120°C*

Throttle on Temperature		
Description	Set the CPU temperature point of Throttle on.	
Options	*40°C*	*45°C*
	50°C	*55°C*
	60°C	*65°C*
	70°C	*75°C*
	80°C	*85°C*
	90°C	

Video Configuration — Sub-menu

```
Primary Display              [Auto]
>Internal Graphic Device

   Internal Graphic Device    [Auto]
   IGD - DVMT Pre-Allocated   [32 MB]
   IGD - Gfx Low Power Mode   [Disabled]
```

Primary Display

Description	Set the primary display. For an external graphic device, PEG or PCI has to be set.	
Options	*Auto*	*Scans and activates the graphics devices with the following priority:* *- IGFX (integrated graphics)* *- PEG (PCI Express graphics)* *- PCI (graphics card at the PCI bus)*
	PEG	
	IGFX	
	PCI	

Internal Graphic Device

Description	Enable internal graphic device.	
Options	*Enabled*	*Disabled*
	Auto	

IGD - DVMT Pre-Allocated

Description	Select DVMT5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.	
Options	*32 MB*	*64 MB*
	96 MB	*128 MB*

IGD - Gfx Low Power Mode

Description	Applicable for SFF only	
Options	*Enabled*	*Disabled*

USB Configuration — Sub-menu

```
Setup Warning:
Disabling USB devices or ports may cause your system to not enter setup
and to prevent reenabling of USB devices or ports

USB Legacy              [Enabled]
EHCI 1                  [Enabled]
EHCI 2                  [Enabled]
Per-Port Control        [Disabled]
USB RMH Mode            [Enabled]
```

USB Legacy

Description	If this menu item is enabled it is possible to boot from USB devices and use a USB keyboard under DOS. Cannot be changed.
Options	*Enabled*

EHCI 1/2

Description	Enable/Disable EHCI 1/2.	
Options	*Enabled*	*Disabled*

Per-Port Control

Description	Enable/Disable the per port disable control override.	
Options	*Enabled*	*Disabled*

USB RMH Mode

Description	Enable/Disable the PCH USB Rate Matching Hubs Mode. Cannot be changed.
Options	*Enabled*

Chipset Configuration

```
Setup warning
Setting items on this screen to incorrect values may cause your system
to malfunction!

VT-d                    [Disabled]
```

VT-d

Description	Check to enable VT-d function on MCH	
Options	*Enabled*	*Disabled*

ACPI Table/Feature Control

```
APIC - IO APIC Mode      [Enabled]
Watchdog ACPI Table      [Enabled]
```

APIC - IO APIC Mode

Description	This item is valid only for WIN2k and WINXP.Also, a fresh install of the OS must occur when APIC Mode is desired.Test the IO ACPI by setting item to Enable.The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in ICH4M.	
Options	*Enabled*	*Disabled*

Watchdog ACPI Table

Description	Enable/disable to support watchdog ACPI Table (WDAT).	
Options	*Enabled*	*Disabled*

Active Management Technology Support

```
Intel AMT Support              [Enabled]
Watchdog Support               [Disabled]
   OS Timer                    [0]
   BIOS Timer                  [0]
```

Intel AMT Support

Description	Enable/disable Intel Active Management Technology BIOS extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution.	
Options	*Enabled*	*Disabled*

Watchdog Support

Description	Enable or disable Watchdog timer.	
Options	*Enabled*	*Disabled*

OS Timer/BIOS Timer

Description	Set OS/BIOS watchdog timer.

PCI Express Configuration

```
>PCI Express Root Port 1
  PCI Express Root Port 1       [Enabled]
>PCI Express Root Port 2
  PCI Express Root Port 2       [Enabled]
>PCI Express Root Port 3
  PCI Express Root Port 3       [Enabled]
>PCI Express Root Port 4
  PCI Express Root Port 4       [Enabled]
>PCI Express Root Port 5
  PCI Express Root Port 5       [Enabled]
>PCI Express Root Port 6
  PCI Express Root Port 6       [Enabled]
>PCI Express Root Port 7
  PCI Express Root Port 7       [Enabled]
>PCI Express Root Port 8
  PCI Express Root Port 8       [Enabled]
```

PCI Express Root Port 1/2/3/4/5/6

Description	Enable/disable PCI Express Root Ports. If PCI Express Root Port 1 is disabled, PCI Express Root Ports 2 to 6 will also be disabled.	
Options	*Enabled*	*Disabled*

Platform Configuration

```
VBIOS Ver: 2117
EC Ver: N/A
CPUID: 206A5
PCH Rev: 0x03
SA Rev: 0x07
Microcode Rev: 0x07
Number of Core: 4
Number of Thread per Core: 2
VT-d: Supported
VMX: Supported
SMX/TXT: Supported
```

Platform Configuration

Description	In this menu fixed system values are listed. No changes can be made here.

Extended ICC

```
ICC Overclocking Lib     7.0.1.51
```

ICC Overclocking Lib

Description	Integrated clock control for overclocking operations and dynamic ICC control. For information only.

3.3 Security

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
TPM Status			Not Installed			
TPM Operation			[No Operation]			
Supervisor Password			[Installed/Not Installed]			
User Password			[Installed/Not Installed]			
Set Supervisor Password						
Power on password			[Disabled]			
User Access level			[View Only]			
Set User Password						
Clear User Password						
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Submenu		F10 Save and Exit

TPM Status

Description	TPM (Trusted Platform Module) Status. Not supported on the F21P.
Options	*Not installed*

TPM Operation

Description	TPM (Trusted Platform Module) Operation. Not supported on the F21P.
Options	*No operation*

Supervisor Password

Description	Shows whether a supervisor password has been entered.

User Password

Description	Shows whether a user password has been entered.

Set Supervisor Password

Description	Enter and confirm the supervisor password under this menu item. To delete the password enter an empty password.

Power On Password

Description	Select when the password has to be entered.	
Options	*Enabled*	The password has to be entered when the system starts.
	Disabled	The password has to be entered when changing to the setup menu.

User Access Level

Description	Set the User Access Level.	
Options	*View Only*	Access to InsydeH2O Setup allowed but the fields cannot be changed.
	Full	Any field can be changed except the Supervisor password.
	Limited	Only limited fields can be changed.

Set User Password

Description	Enter and confirm the user password under this menu item.

Clear User Password

Description	Clear the user password. Only possible for a supervisor or user in the access levels full or limited.

3.4 Power

InsydeH2O Setup Utility						Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit	
>Advanced CPU Control						
Wake on Lan			[Enabled]			
F1 Help		↑↓ Select Item		F5/F6 Change Values		F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Submenu		F10 Save and Exit

Advanced CPU Control – Sub-Menu

```
TXT                              [Disable]
Active Processor Cores           [All Core]
HT Support                       [Auto]
VT Support                       [Enabled]
Hardware Prefetcher              [Enabled]
Adjacent CacheLine Prefetch      [Enabled]
Max CPUID value limit            [Disabled]
C-States                         [Enabled]

Turbo Mode                       [Enabled]
```

TXT

Description	Enables utilization of additional hardware capabilities provided by Intel Trusted Execution Technology; changes require a full power cycle to take effect.	
Options	*Enabled*	*Disabled*

Active Processor Cores

Description	Numbers of cores to enable in each processor package	
Options	*All Core*	*1 Core*

	2 Core	*3 Core*
	4 Core	*5 Core*
	6 Core	*7 Core*
HT Support		
Description	Enable or disable Hyper Threading.	
Options	*Auto*	*Disabled*
VT Support		
Description	Enable or disable Vanderpool technology.	
Options	*Enabled*	*Disabled*
Hardware Prefetcher		
Description	Enable/disable MLC (Mid level cache, L2 cache) streamer prefetcher.	
Options	*Enabled*	*Disabled*
Adjacent CacheLine Prefetch		
Description	Enable/disable MLC (Mid level cache, L2 cache) spatial prefetcher.	
Options	*Enabled*	*Disabled*
Max CPUID value limit		
Description	Limit CPUID max value to 3 (if max CPUID value > 3). This setting is useless for windows OS.	
Options	*Enabled*	*Disabled*
C-States		
Description	Enable processor idle power saving states (C-States).	
Options	*Enabled*	*Disabled*
Turbo Mode		
Description	Enable processor Turbo Mode (requires EMTTM enabled too).	
Options	*Enabled*	*Disabled*

Wake on Lan

Description	Determines the action taken when the system power is off and a Wake on Lan event occurs.	
Options	*Enabled*	*Disabled*

3.5 Boot

InsydeH2O Setup Utility					Rev. 3.5
Main	Advanced	Security	Power	Boot	Exit
UEFI Boot			[Enabled]		
Quick Boot			[Enabled]		
Quiet Boot			[Enabled]		
PXE Boot to LAN			[Disabled]		
ACPI Selection			[ACPI 3.0]		
USB Boot			[Enabled]		
EFI Device First			[Disabled]		
>EFI					
F1 Help		↑↓ Select Item		F5/F6 Change Values	F9 Setup Defaults
Esc Exit		← → Select Menu		Enter Select > Submenu	F10 Save and Exit

UEFI Boot

Description	Enable/Disable UEFI Boot Function	
Options	*Enabled*	*Disabled*

Quick Boot

Description	Allows InsydeH2O to skip certain tests while booting. This will decrease the time needed to boot the system.	
Options	*Enabled*	*Disabled*

Quiet Boot

Description	Disables or enables booting in Text Mode	
Options	*Enabled*	*Disabled*

PXE Boot to LAN

Description	Disables or enables PXE boot to LAN.	
Options	*Enabled*	*Disabled*

ACPI Selection

Description	Select booting to Acpi3.0/Acpi1.0B	
Options	Acpi3.0/	Acpi1.0B

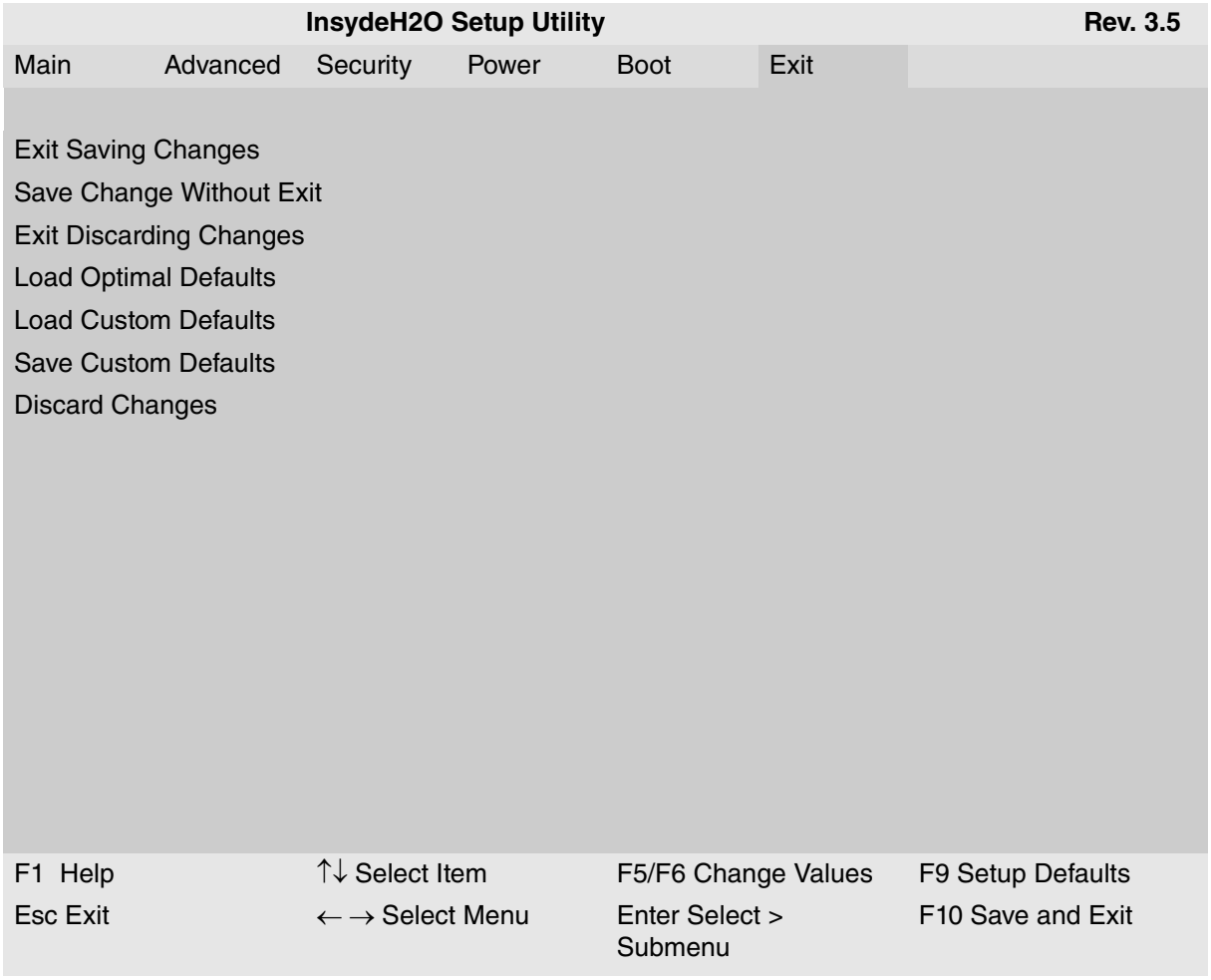
USB Boot

Description	Disables or enables booting to USB boot devices.	
Options	*Enabled*	*Disabled*

EFI Device First

Description	Determines whether the EFI device or the legacy device is booted first. If enabled, the EFI device is booted first. If disabled, the legacy device is booted first.	
Options	*Enabled*	*Disabled*

3.6 Exit



3.6.1 Exit Saving Changes

Exit system setup and save your changes.

3.6.2 Save Change Without Exit

Save your changes without exiting the system.

3.6.3 Exit Discarding Changes

Exit system setup without saving your changes.

3.6.4 Load Optimal Defaults

If this option is selected, a verified factory setup is loaded.

On the first BIOS setup configuration, this loads safe values for setup, which make the board boot up.

3.6.5 Load Custom Defaults

If this option is selected the custom defaults that have been saved in a former session with Save Custom Defaults are loaded.

For details see Chapter 3.6.6 Save Custom Defaults

3.6.6 Save Custom Defaults

Save custom defaults.

3.6.7 Discard Changes

Discard changes.

4 Maintenance

4.1 Lithium Battery

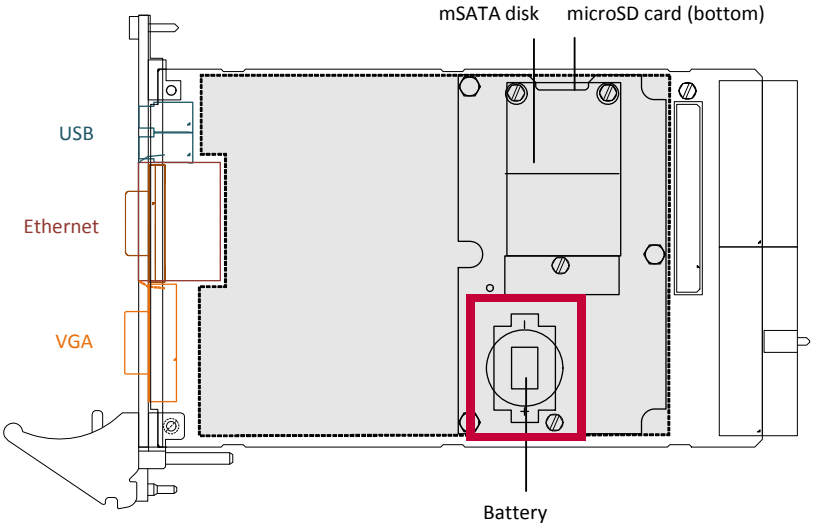
The board contains a lithium battery. There is a danger of explosion if the battery is incorrectly replaced!

Replace only with the same or equivalent type.

- Manufacturer: Renata
- Type: CR2032
- Capacity: 235 mAh

Dispose of used batteries according to the manufacturer's instructions.

Figure 3. *Position of battery on the mass storage adapter on the F21P*



5 Appendix

5.1 Literature and Web Resources

F21P data sheet with up-to-date information and documentation.

5.1.1 CPU

Intel Embedded Processors

5.1.2 SATA

Serial ATA International Organization (SATA-IO)

5.1.3 USB

USB Implementers Forum, Inc.

5.1.4 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE

ANSI/IEEE 802.3-1996

- Charles Spurgeon's Ethernet Web Site

Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.

- InterOperability Laboratory, University of New Hampshire

General Ethernet technology.

5.1.5 HD Audio

Intel High Definition Audio

5.1.6 PCI Express

PCI Special Interest Group

5.1.7 CompactPCI

CompactPCI PlusIO Specification PICMG 2.0 R3.0:
1999; PCI Industrial Computers Manufacturers Group (PICMG)

PCI Local Bus Specification Revision 2.2:
1995; PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214, USA

5.1.8 CompactPCI PlusIO

CompactPCI PlusIO Specification PICMG 2.30 R1.0:
1999; PCI Industrial Computers Manufacturers Group (PICMG)

Introduction to CompactPCI PlusIO on Wikipedia

5.2 Finding out the Product's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or design revisions of the F21P. You can find information on the article number, the design revision and the serial number on a label attached to the board.

- **Article number:** Gives the product's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the design revision of the product.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 4. *Labels giving the product's article number, revision and serial number*