To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

User's Manual

Multimedia Processor for Mobile Applications

Timer

EMMA Mobile^{TM}1

Document No. S19266EJ3V0UM00 (3rd edition)
Date Published September 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

PREFACE

Readers	This manual is intended for hardware/software application system designers who wish to understand and use the timer module (ATIM) functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.
Purpose	This manual is intended to explain to users the hardware and software functions of the timer module (ATIM) of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Registers
- Chapter 3 Description of functions
- Chapter 4 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the timer module (ATIM) of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	This manual
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

LIST OF FIGURES

CHAPTER 1 OVERVIEW

1.1 General

The timer module (ATIM) is a programmable timer counter that enables 32-bit counting (1 to FFFF_FFFFH).

1.2 Features

(1) When a timer counts out (counts up to the user-set count value), the timer count value returns to 0 (0000_0000H) and the timer starts counting again (free-run counting).

(2) The TOUT signal is asserted each time a timer counts out and the TOUT signal is output for two TIN clock cycles.

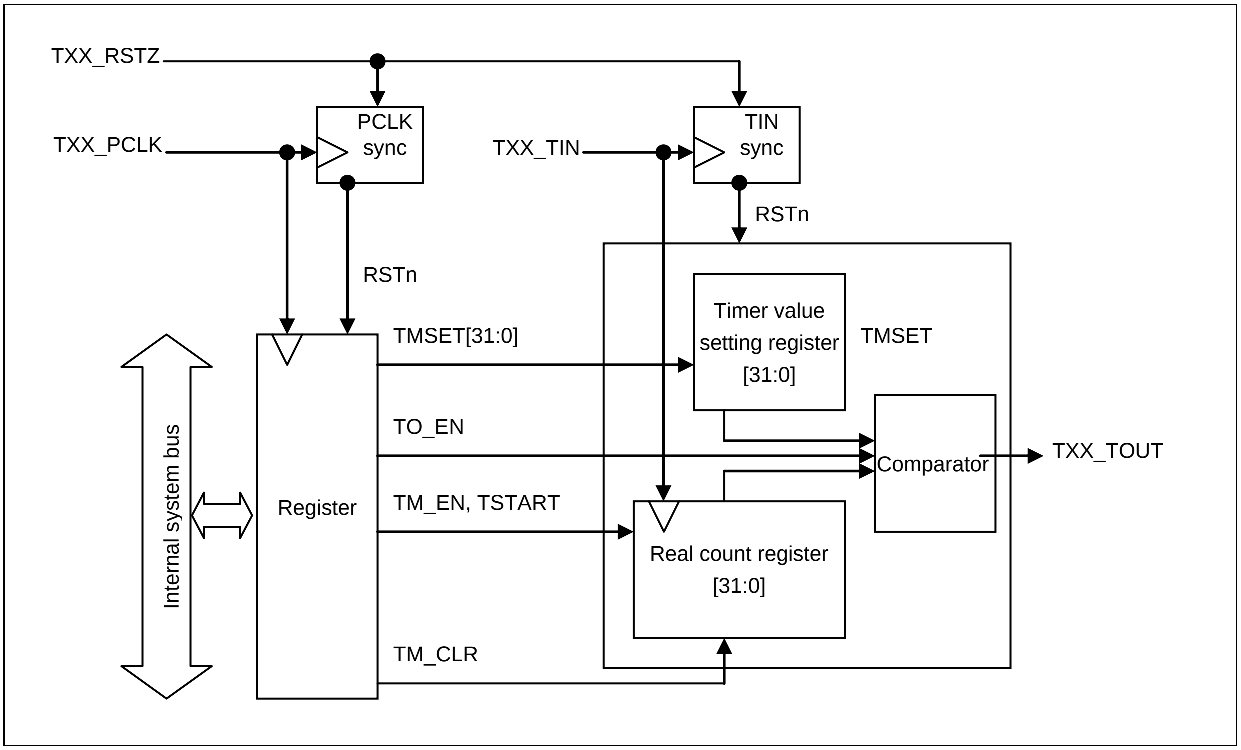
(3) Once the ATIM registers are set up and the timer starts counting, the ATIM continues counting as described in (1) as long as the TIN clock is supplied, even if the APB bus clock (PCLK) is stopped.

(4) The timer count set value can be changed while the timer is counting.

(5) ATIM has 14 functionally equivalent timer modules (TI0 to TI3, TW0 to TW3, and TG0 to TG5).

1.3 Timer Module Block Diagram

Figure 1-1. ATIM_Txx Block Diagram



CHAPTER 2 REGISTERS

ATIM has 256-byte register spaces for each module (TI0 to TI3, TW0 to TW3, and TG0 to TG5), which have different offset addresses.

2.1 Offset Address

PB1_PADDR[31:0]	Module
C000_0000H	TI0
C000_0100H	TI1
C000_0200H	TI2
C000_0300H	TI3
C000_1000H	TW0
C000_1100H	TW1
C000_1200H	TW2
C000_1300H	TW3
C000_2000H	TG0
C000_2100H	TG1
C000_2200H	TG2
C000_2300H	TG3
C000_2400H	TG4
C000_2500H	TG5

2.2 Registers

Each ATIM register consists of 32 bits.

Address	Register Name	Symbol	R/W	After Reset
0000H	Timer operation register	xxx_OP	R/W	0000_0000H
0004H	Timer clear register	xxx_CLR	W	0000_0000H
0008H	Timer value setting register	xxx_SET	R/W	0000_0000H
000CH	Real count read register	xxx_RCR	R	0000_0000H
0010H	Reserved	–	–	–
0014H	Timer value setting monitor register	xxx_SCLR	R/W	0000_0000H
0018H to 00FCH	Reserved	–	–	–

(xxx = TI0/TI1/TI2/TI3/TW0/TW1/TW2/TW3/TG0/TG1/TG2/TG3/TG4/TG5)

Operation when a reserved area is accessed:

Write: Ignored (invalid)

Read: Zeros are returned.

2.2.1 Timer operation register

This register (xxx_OP: xxxx_0000H) control the timer operations.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved					TO_EN	TSTART	TM_EN

Name	R/W	Bit	After Reset	Function
Reserved	–	31:3	0	Reserved.
TO_EN	R/W	2	0	Specifies whether to assert the TOUT signal. 0: Does not assert the TOUT signal even if timer counting times out. 1: Asserts the TOUT signal when timer counting times out.
TSTART	R/W	1	0	Starts timer counting (valid when TM_EN = 1) 0: Does not start timer counting. (The internal timer count register retains the current value.) 1: Starts timer counting. (The internal timer count register is incremented per TIN clock cycle).
TM_EN	R/W	0	0	Specifies whether to enable the timer operation. 0: Disables the timer operation. The internal timer count register value is reset to 0. 1: Enables the timer operation.

Caution Make sure that the interrupt enable period is at least five internal clock cycles + four TIN clock cycles, because the register value is output in synchronization with PCLK and TOUT is output in synchronization with the TIN clock.

2.2.2 Timer clear register

This register (xxx_CLR: xxxx_0004H) clears the internal timer count registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						TCR_CLR	Reserved

Name	R/W	Bit	After Reset	Function
Reserved	–	31:2	0	Reserved.
TCR_CLR	W	1	0	Clears the internal timer count registers. 0: No operation 1: Clears the internal timer count registers. This bit is automatically cleared to “0”. (Re-setting “0” is unnecessary). For details, see **4.4 Timer count value clear operation**.
Reserved	–	0	0	Reserved.

2.2.3 Timer value setting register

This register (xxx_SET: xxxx_0008H) specifies the value at which the timer counts out.

31	30	29	28	27	26	25	24
TMSET_31	TMSET_30	TMSET_29	TMSET_28	TMSET_27	TMSET_26	TMSET_25	TMSET_24

23	22	21	20	19	18	17	16
TMSET_23	TMSET_22	TMSET_21	TMSET_20	TMSET_19	TMSET_18	TMSET_17	TMSET_16

15	14	13	12	11	10	9	8
TMSET_15	TMSET_14	TMSET_13	TMSET_12	TMSET_11	TMSET_10	TMSET_9	TMSET_8

7	6	5	4	3	2	1	0
TMSET_7	TMSET_6	TMSET_5	TMSET_4	TMSET_3	TMSET_2	TMSET_1	TMSET_0

Name	R/W	Bit	After Reset	Function
TMSET_[31:0]	R/W	31:0	0	Specifies the value at which the timer counts out. Set a desired value minus 1. Specify a value greater than or equal to 2. When a timer counts out, the TOUT signal is asserted (when TO_EN = 1) and the real count register is reset to 0. For details, see **4.5 Rewriting the Timer Count Value**.

Caution Before setting values in this register, read the TM_SCLR bit of the timer value setting monitor register (xxx_SCLR: xxxx_xx14H), confirm that the LSB of the read value is "0", and then wait for at least two or three TIN clock cycles.

2.2.4 Real count read register

This register (xxx_RCR: xxxx_000CH) is used to read the real count registers (current timer value).

31	30	29	28	27	26	25	24
RCR_31	RCR_30	RCR_29	RCR_28	RCR_27	RCR_26	RCR_25	RCR_24

23	22	21	20	19	18	17	16
RCR_23	RCR_22	RCR_21	RCR_20	RCR_19	RCR_18	RCR_17	RCR_16

15	14	13	12	11	10	9	8
RCR_15	RCR_14	RCR_13	RCR_12	RCR_11	RCR_10	RCR_9	RCR_8

7	6	5	4	3	2	1	0
RCR_7	RCR_6	RCR_5	RCR_4	RCR_3	RCR_2	RCR_1	RCR_0

Name	R/W	Bit	After Reset	Function
RCR_[31:0]	R	31:0	0	Used to read the real count register values.

2.2.5 Timer value setting monitor register

This register (xxx_SCLR: xxxx_0014H) is used to monitor the timer value setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							TM_SCLR

Name	R/W	Bit	After Reset	Function
Reserved	–	31:1	0	Reserved.
TM_SCLR	R/W	0	0	Monitors the timer value setting. This bit holds 1H until a count value is set to the timer value setting register. After a value is set, this bit is automatically reset to 0H.

Remarks 1. This bit is not automatically reset to 0 when the TM_EN bit of the timer operation register is set to 0.

2. If the timer value is set in the timer value setting register (TMSET bits) while the TM_SCLR bit is set to 1, the TM_SCLR bit is fixed to “1”. In this case, reset this bit.

CHAPTER 3 DESCRIPTION OF FUNCTIONS

3.1 Status After Reset

ATIM is set as follows after reset.

- TOUT signal polarity: 0
- Timer count: Stop
- Timer setting register: 0x0000_0000
- Internal timer count register: 0x0000_0000

3.2 Calculation of Timer Count

A wide range of counting is possible by using a combination of input frequency and timer count settings. The following table shows setting examples. The term [seconds] in this table refers to the interval at which the TOUT signal is asserted.

TIN (Input Frequency)	Timer Count Setting Value		
	0000_0000H	0000_FFFFH	FFFF_FFFFH
32.768 kHz	30.52×10^{-6} [seconds]	2 [seconds]	131072 [seconds]
15.616 MHz	64.04×10^{-9} [seconds]	4.20×10^{-3} [seconds]	275.04 [seconds]

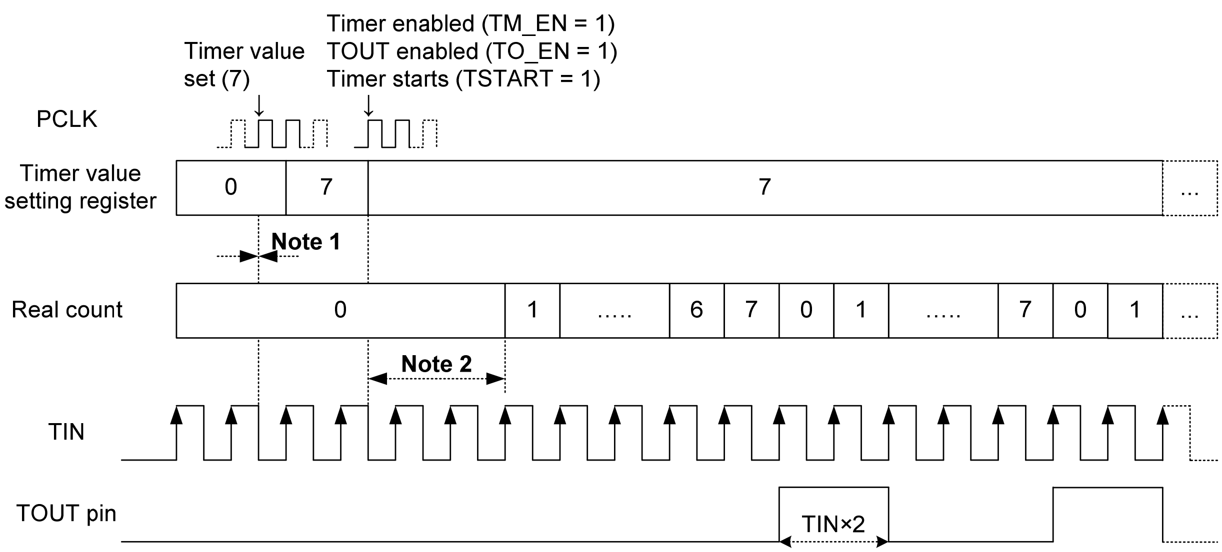
Expression: (1/TIN) $\times$ (Count setting value + 1)

Example: 1/32.768 kHz $\times$ (0000_FFFFH + 1) = $30.52 \times 10^{E-6} \times 65536$ = 2 [seconds]

4.1 Starting the Timer

(1) Set up the timer value setting register: TMSET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)

Figure 4-1. Starting the Timer



(Example: When the timer value is set to 7)

<1> Steps (2) to (4) can be performed with a single write.

<2> The TOUT signal is asserted under the following conditions.

(1) The timer value setting register (TMSET) is set to a value other than “0”

(2) Asserting the TOUT signal is enabled (TO_EN = 1)

(3) The timer is counting (TM_EN = 1, TSTART = 1).

With these settings, the TOUT signal is asserted every 8 TIN clock cycles.
To set the TOUT signal assertion cycle to 8, set the timer value setting register to 7 (8 − 1).

<3> The internal timer count register operates even if the system clock (PCLK) is stopped after the timer starts, as long as the TIN clock is supplied.

The TOUT signal is asserted according to the timer value setting (every 8 clock cycles in this example).

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

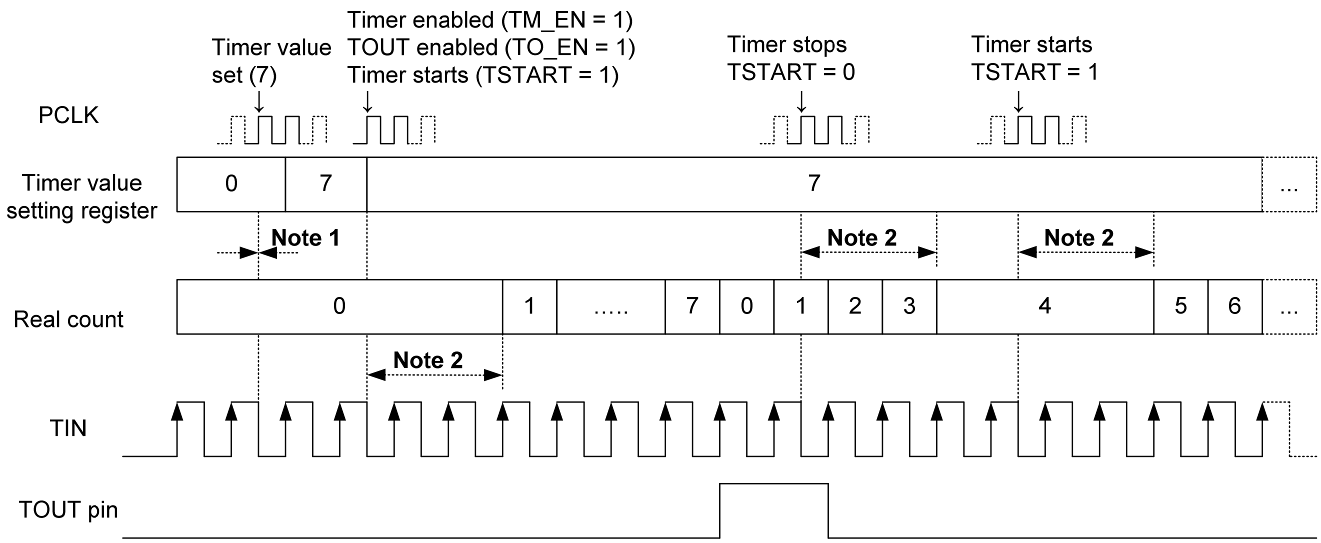
2. The TSTART, TO_EN, TM_EN, and TMSET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TMSET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.2 Pausing the Timer

(1) Stop timer counting (with count values retained): TM_EN = 1, TSTART = 0 (pause for a certain period)

(2) Restart timer counting: TM_EN = 1, TSTART = 1

Figure 4-2. Pausing the Timer



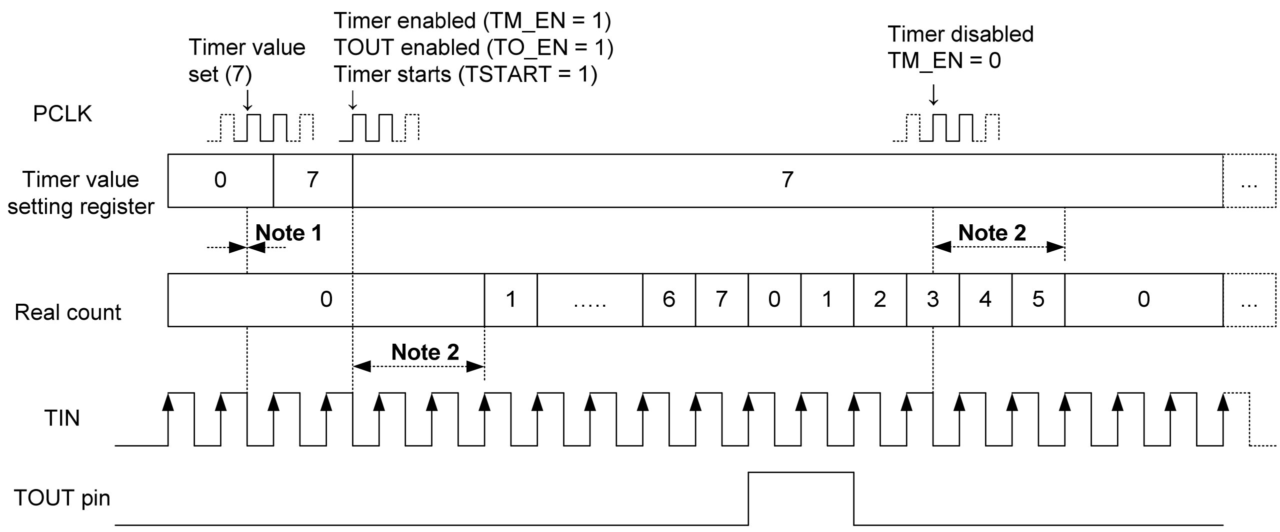
Notes 1. Registers are set in synchronization with APBCLK, and real counting occurs in synchronization with TIN. APBCLK and TIN are asynchronous.

2. The TSTART and TM_EN bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART and TM_EN bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.3 Stopping the Timer

(1) Stop timer counting (internal count value returns to 0): TM_EN = 0, TSTART = *

Figure 4-3. Stopping the Timer



Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

2. The TSTART and TM_EN bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART and TM_EN bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

4.4 Clearing the Timer Count Value Timer

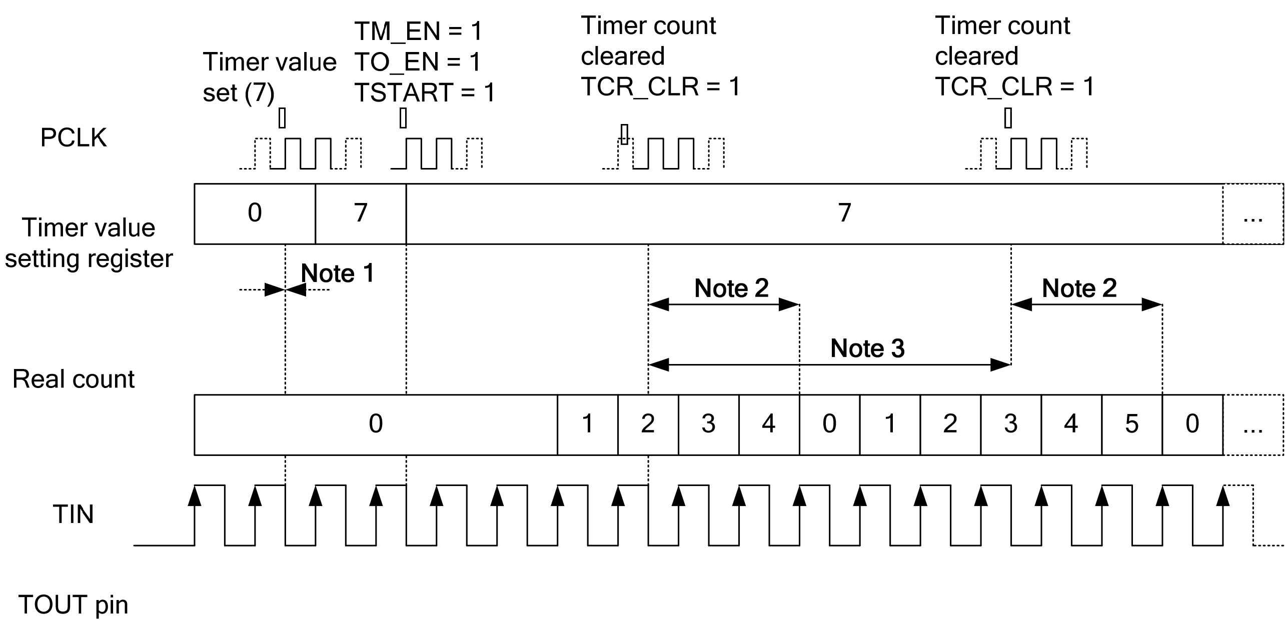
The values of the internal timer count register can be cleared to 0 with a single write operation during counting.

This operation can be used during clearing of the watchdog timer. (The TOUT signal is not asserted if writing is performed at least once before the timer counts out.)

(It's used as Watchdog timer: **Multimedia Processor for Mobile Applications System Control/General-Purpose I/O Interface User's Manual chapter 3.2.8).**

(1) Clears the timer count: TCR_CLR = 1 (bit 1 of xxx_CLR register)

Figure 4-4. Clearing the Timer Count Value Timer



<1> This bit is automatically cleared to "0" after the timer count value is cleared (TCR_CLR = 1).

Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

2. After the timer count value is cleared, the timer count is actually cleared one PCLK cycle + two or three TIN cycles later because the value is specified to be cleared in synchronization with PCLK, but is actually cleared in synchronization with TIN.

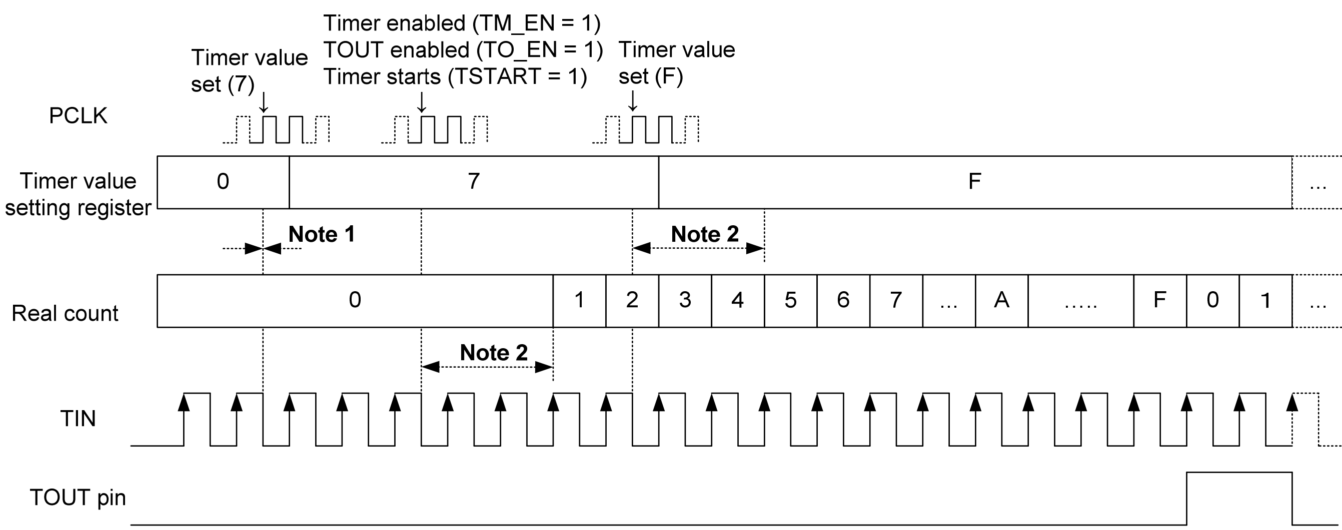
3. When the timer count value is cleared, the signal is output from the register for one PCLK cycle, and clearing takes effect in synchronization with TIN (this takes three cycles). Next, a clear signal in synchronization with TIN is output for one cycle and is synchronized with PCLK again (this takes four cycles). The timer clear register is then cleared to 0, and the clear operation is complete. Therefore, a timer count that is cleared within five PCLK cycles + four TIN cycles is ignored. For the watchdog timer, set the timer value setting register (TMSET bits) to a value of at least (5 PCLK cycles) + (4 TIN cycles).

4.5 Rewriting the Timer Count Value

The maximum value of real counting can be changed by changing the values of the relevant timer value setting register (TMSET) while the timer is counting.

(1) Set up the timer value setting register: TMSET = count value
(2) Enable the timer: TM_EN = 1 (bit 0 of xxx_OP register)
(3) Enable TOUT signal assertion: TO_EN = 1 (bit 2 of xxx_OP register)
(4) Start timer counting: TSTART = 1 (bit 1 of xxx_OP register)
(5) Set up the timer value setting register: TMSET = count value (count value different from that of (1))

Figure 4-5. Rewriting the Timer Count Value



Notes 1. Registers are set in synchronization with PCLK, and real counting occurs in synchronization with TIN. PCLK and TIN are asynchronous.

2. The TSTART, TO_EN, TM_EN, and TMSET bits are set in synchronization with PCLK. However, because real counting occurs in synchronization with TIN, the setting of the TSTART, TO_EN, TM_EN, and TMSET bits will not be applied for 2 or 3 TIN cycles. This is the case regardless of whether the timer is set again while it is counting or when it is stopped.

3. If a value smaller than the real count value is set in the timer value setting register during counting, the timer counts up to FFFF_FFFFH, and then counts up to the preset count value. If this operation causes any problems, read the real count read register and set a value larger than the read value in the timer value setting register.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	−
April 27, 2009	2.0	Incremental update from comments to the 1.0..
September 30, 2009	3.0	Incremental update from comments to the 2.0..

For further information, please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

Shanghai Branch
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai, P.R.China P.C:200120
Tel:021-5888-5400
http://www.cn.necel.com/

Shenzhen Branch
Unit 01, 39/F, Excellence Times Square Building,
No. 4068 Yi Tian Road, Futian District, Shenzhen,
P.R.China P.C:518048
Tel:0755-8282-9800
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2, Grand Century Place,
193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

G0706