TASKING C166/ST10 Tool Chain v8.5r1 patch 5 RELEASE NOTE

This patch updates the C166/ST10 v8.5r1 product. It includes all fixes and updates released in previous patches for v8.5r1.

Overview of changes:

v8.5r1 patch 5:

- Added support for ST10F296
- Updated flash register segment for the 252-series (251,252,271,272) of the 27X family
- Solved register definition file problems: PR34066, PR33771, PR33747, PR33746
- Solved EDE problems PR33992 and PR33888
- Solved CrossView Pro problems PR33997, PR34010 and PR34063
- All of v8.5r1 patch 4

v8.5r1 patch 4:

- Correction to fix of PR34018: DIVL now has the correct behavior
- All of v8.5r1 patch 3

v8.5r1 patch 3:

- Solved Simulator PR34018
- All of v8.5r1 patch 2

v8.5r1 patch 2:

- Solved several problems in CrossView Pro: PR33879, PR33924, PR33753, PR33761, PR33837, PR33880, PR33931, PR31994, PR33198, PR33878
- Moved instruction DISWDT to top of the EDE generated startup code to make OCDS connections more stable.
- Updated CrossView Pro configuration files for better FLASH support
- All of v8.5r1 patch 1

v8.5r1 patch 1:

- Solved EDE problem PR33779

Patch Date

2005-03-10

Components

- EDE DOIL file (etc/c166.dol) build #386.1.1
- CrossView Pro (bin/xfw166.exe) build #338
- Evaluation board support (bin/dieva166.dll) build #131
- Simulator (bin/disim166.dll) build #147
- Peripheral Simulation (bin/psm166.dll) build #026
- OCDS support (bin/diocds.dll) build #064

Installation

To install the patch run the setup.exe

Solved problems

SOLVED PR34018: Simulator crashes when DIVL instruction is executed

The simulator crashes when the DIVL R14 instruction from the example is executed.

```
int foo ( long l, int x )
{
#pragma asm
mov MDH, R13
mov MDL, R12
divl R14
#pragma endasm
}
```

```
int main(void)
{
return foo( -2147483648, -1);
}
```

SOLVED PR33779: E 252: expression syntax error when CPU.21 bypass is enabled

When CPU.21 bypass is enabled and at least two BUSCON registers are included in the startup code, the file start.asm shows a missing parenthesis at the BUSCON initialization:

```
AND BUSCON0, #(~0xD6FF)|0
OR BUSCON0, #((0x0&~0)&0xD6FF)
AND BUSCON1, #~0xD6FF
OR BUSCON1, #(0xD6FF&0x0 <== missing closing parenthesis
```

As a result, the following assembler error is issued:

```
E 252: expression syntax error
```

SOLVED PR33879: When specifying a user defined *.def file, the *.cfg file is not updated

At the dialog 'Project Options | Assembler | Miscellaneous' one can specify a user defined sfr file (*.def). However, this file does not show up in the *.cfg file. As a result, CrossView uses the wrong one.

SOLVED PR33798: ROM monitor for XC16x device couldn't change the CC1_T01CON SFR register

When debuging with OCDS on a XC167CI derivative you could change the CC1_T01CON SFR register

content without any problems. But when debuging the same program via the ROM monitor debugger you cannot change the content of this SFR register.

SOLVED PR33924: Simulator keeps on executing the same line

After building the example (selected CPU = ST10X269), CrossView Simulator does not continue after the assembly instruction, but keeps on executing the same line over and over again.

```
int main()
{
#pragma asm
MOV MRW,#0ffffh
#pragma endasm
return 0;
}
```

SOLVED PR33753: Faulty MAC unit Simulation result

Faulty MAC unit Simulation result, see example:

```
/*
project options: all default, using ST10F269 CPU

Using the Crossview Pro Simluator the following result is shown:
MSW MAH MAL MRW MCW
=======================
01ff fffe 0001 0000 0000
05ff fffc 0002 0000 0000
05ff fffa 0003 0000 0000


An Emulator shows the following result (in accordance with the user manuals of
Infineon/ST)


MSW MAH MAL MRW MCW
=======================
0000 FFFE 0001 0000 0000
1001 FFFC 0002 0000 0000
1002 FFFA 0003 0000 0000
*/

#include <stdio.h>


void test_it(unsigned int *a)
{
#pragma asm
MOV MCW,#0
MOV MRW,#0
MOV R2,R12


MOV R1,#0ffffh
CoMULu R1,R1
CoSTORE [R2+],MSW
CoSTORE [R2+],MAH
```

```
CoSTORE [R2+],MAL
CoSTORE [R2+],MRW
CoSTORE [R2+],MCW


CoMACu R1,R1
CoSTORE [R2+],MSW
CoSTORE [R2+],MAH
CoSTORE [R2+],MAL
CoSTORE [R2+],MRW
CoSTORE [R2+],MCW


CoMACu R1,R1
CoSTORE [R2+],MSW
CoSTORE [R2+],MAH
CoSTORE [R2+],MAL
CoSTORE [R2+],MRW
CoSTORE [R2+],MCW
#pragma endasm
}


int main()
{
unsigned int a[15];
int i;


test_it(a);


printf(" MSW MAH MAL MRW MCW\n=======================\n");
for (i = 0; i < 3; i++)
printf("%04x %04x %04x %04x %04x\n", a[i*5], a[i*5+1],
a[i*5+2], a[i*5+3], a[i*5+4]);


return 0;
}
```

SOLVED PR33761: After starting CrossView from EDE, CrossView crashes

After starting CrossView from EDE, CrossView crashes. Strange enough, this behaviour cannot be reproduced from the command line. Deleting xvw.ini solves the problem.

SOLVED PR33837: The Simulator should not allow the application to change read-only memory

When an application writes to ROM or a read-only register, the Simulator should not modify the memory locations. Besides, it should be possible to change the register in the register or command window.

SOLVED PR33880: It's not possible to initialize a read-only register when using the Simulator

When defining a register in the sfr file (*.def) it is not possible to pass a default initialization value to the Simulator

SOLVED PR33931: CrossView source lines disappears when source and disassembly is active

When debugging with CrossView the source lines sometimes disappears when the source and disassembly window is active.

SOLVED PR31994: When RTS/CTS handshake is selected XVW hangs when connecting

When RTS/CTS handshake is selected while the hardware does not support this, XVW hangs when connecting to the target.

SOLVED PR33198: Flash programming not verified

After flashing by CrossView, there is no verification. When e.g. the serial baud rate is too high, flash programming may fail now and then. Please add a check box at the dialog 'Project options | CrossView Pro | Initialization' to execute a 'compare application' after flashing. This check box should be enabled by default.

SOLVED PR33878: CrossView debugger doesn't show register name defined by DEFA

CrossView doesn't show register names defined by DEFA in the disassembly window: `MOV R12,#0xaa`
`MOV 0xfce0,R12`

instead of:

```
MOV R12,#0AAh
MOV SRCP0,R12
```

as listed in the *.src file.

SOLVED PR34066: C166S V1 core does not have a SYSCON bit named XPERSHARE

According to Infineon's latest C166S V1 User's Manual from 08.2001, bit0 of SYSCON is not defined. Therefore it must not be showed as XPERSHARE at the dialog 'Project Options | Startup | SYSCON'.

Also there seem to be more errors in the .def and .h files for the C166S V1. A review and update of these files is required.

SOLVED PR33771: Missing fast external interrupt control registers in C161U register files

The SFR definitions for the fast external interrupt registers FEI2IC-FEI7IC and their corresponding bits are missing in the C161U SFR register files.

SOLVED PR33746: Missing registers in super10F397 register files

The following registers cannot be programmed in the startup code, and therefore they are not listed in EDE:

FCONCS5, TCONCS5, ADDRSEL5, TCONBURST5, FCONCS7, TCONCS7, ADDRSEL7, TCONBURST7

However, they should be defined in the corresponding register header and definition files.

SOLVED PR33747: Additional sfr support for super10F397 register files

Please add the following register definitions to ST10F397.h and ST10F397.def:

- OTR (0xEA10) Ownership Trace Register:
- DAC (0xEA0E) Data Acquisition Control Register
- DQM0/DQM1 (0xEA0C/0xEA0A) Data Acquisition Channel Register 0/1.

These registers only support word access.

SOLVED PR33992: Wrong BUSCON0 initialization in startup code

Following the CPU manual, when pin EA is low during reset, BUSACT0 and ALECTL0 are set to "1" and BTYP is loaded with the bus configuration via PORT0. So when "Preserve bits set externally on reset" is activated and CPU.21 is checked, BUSACT0 and ALECTL0 must not be cleared by the AND instruction in the startup code:

0010 6686C029 42 AND BUSCON0, #(~0xD6FF)|0x00C0

Because this AND instruction will deactivate BUSCON0 (BUSACT0 is cleared) and subsequently the program ceashes. So for this configuration the mask 0x00C0 must be changed into 0x06C0.

SOLVED PR33888: WDTCON must be initialized before EINIT when using the ext2 architecture

WDTCON is write protected after the execution of EINIT by the register security mechanism for the ext2 arichitecture. Therefore, WDTCON must be initialized before EINIT in the startup code, and not after it, as it is now.

SOLVED PR34010: CrossView tries to set user breakpoints while flashing the application

When debugging first with the simulator and you left some breakpoints set within your application this could influence the flashing with a next CrossView startup. With a new CrossView startup while the application should be flashed CrossView also tries to set the breakpoints saved within the xvw.ini file. When these breakpoints where set within the ROM range these breakpoint couldn't be set and you will get the message:

Placing code breakpoint at 0x.. failed: BreakpointSet(): Write access at SW breakpoint address failed

Finally the flashing will not succeed and you will get the message:

Closing download failure

SOLVED PR34063: CrossView crashes easily when debugging with ROM/RAM Monitor

When debugging using the ROM/RAM Monitor, CrossView may crash easily when switching to another windows application.

SOLVED PR33997: The simulator doesn't simulate CAPCOM interrupts in Compare Mode 0-3

The simulator has problems to simulate CAPCOM interrupts. The example uses the timer T7 in Compare Mode 0 and does not generate a CC16 interrupt.
