# PCIe-OPTO16x16

# User's Manual

## 16 Input Bits

## 16 Output Bits

## Opto-Isolator Board

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## PREFACE

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This user's manual provides information on the specifications, theory of operation, register level programming, installation of the board and information required for customized hardware/software development.

## RELATED PUBLICATIONS

The following manuals and specifications provide the necessary information for in depth understanding of the specialized parts used on this board.

EIA Standard for the RS-422A Interface (EIA order number EIA-RS-422A)

PCI Local Bus Specification Revision 2.1 June 1, 1995. Questions regarding the PCI specification be forwarded to:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433- 5177 (U.S.)
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(503) 234-6762 (FAX)

## PCIe-OPTO16x16 Documentation History

1. Alterations for PCIe-OPTO16x16 Board Assembly.
2. 2010-09-15
   Added PCI Sub-System Identifier.
   Section 3.2.1 Added Firmware Revision Identifiers.
   Finished adding Mailbox Information.
3. 2011-02-07 – Rev A
   Re-Wrote PLX EEPROM section.
   Added Full PLX EEPROM as an Appendix.
   Manually added the Appendix's into the Table of Contents .
   Added / Explained how the PEX8311AA works.
   Updated Layout Picture to Rev A.
   Added Test Register 1 and 2
   Changed Register bit level descriptions. Tried to Clarify descriptions.
   Added Register Contents tables for all registers.
   Added Note, Schmidt Trigger Input has been removed.
   Fix descriptions for COS Byte Clears.
   Fixed “Differences from OPTO32” - Introduction, Input's and Outputs were mixed up.
4. 2011-02-08 – Rev B
   Changes Per Don
   Revision History is on this page.
   Period missing on page 11
   Period missing on page 13
   Fixed COS Polarity Type.
   Fixed Initialization Punctuation.
   Fixed Class code description.
   Fixed Typo in Interrupt Appendix, test for if this board generated Interrupt.
   Made Page Numbers Consistent.

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# SECTION 1

# 1. Introduction

The PCIe-OPTO16x16 board is a high performance Single Lane PCI Express card offering 16 Opto-Isolated inputs and 16 Opto-Isolated outputs.

## *1.1 Differences From OPTO32 Family*

The PCIe-OPTO16x16 is based on the OPTO32 family. It was designed to provide a migration path from the OPTO32 family to the OPTO16 on the PCIe Bus.

The following differences exist between the OPTO32 and the PCIe-OPTO16x16.

- Output Bits 0-7 are the same as the OPTO32 Family.
- Input Bits 0-15 are the same as the OPTO32 Family.
- Input Bits 16-23 have been removed.
    - Output Bits 8-15 were placed where OPTO32 Input 16-23 were at.
- Special Schmidt Trigger Input has been removed. All Inputs are the same.
- True PCIe Form factor.

## 1.2 Card Features

- 16 optically isolated inputs
    - Selectable input voltage range thru use of field replaceable bias resistors.
    - Industry Standard 8 Pin Sip Resistors – 770-83-Rxx Series.
- 16 optically isolated outputs - 12 normal, 4 Diode Clamped
- Software Programmable clock debounce rate
- Software Programmable Change of State detection. Rising edge or falling edge per input channel
- Software Programmable Interrupts on any or all Change of State bit(s)
- Software Pre-loadable Event counter on Input Bit 15
- Programmable Interrupt on Event Counter Overflow
- Built in Self-Test Features.
    - Registers are Read / Write.
    - Ability to monitor the Debounce Clock.

The board uses the PEX 8311 PCIe single lane interface chip to provide the advanced features of the PCIe interface environment. These features include:

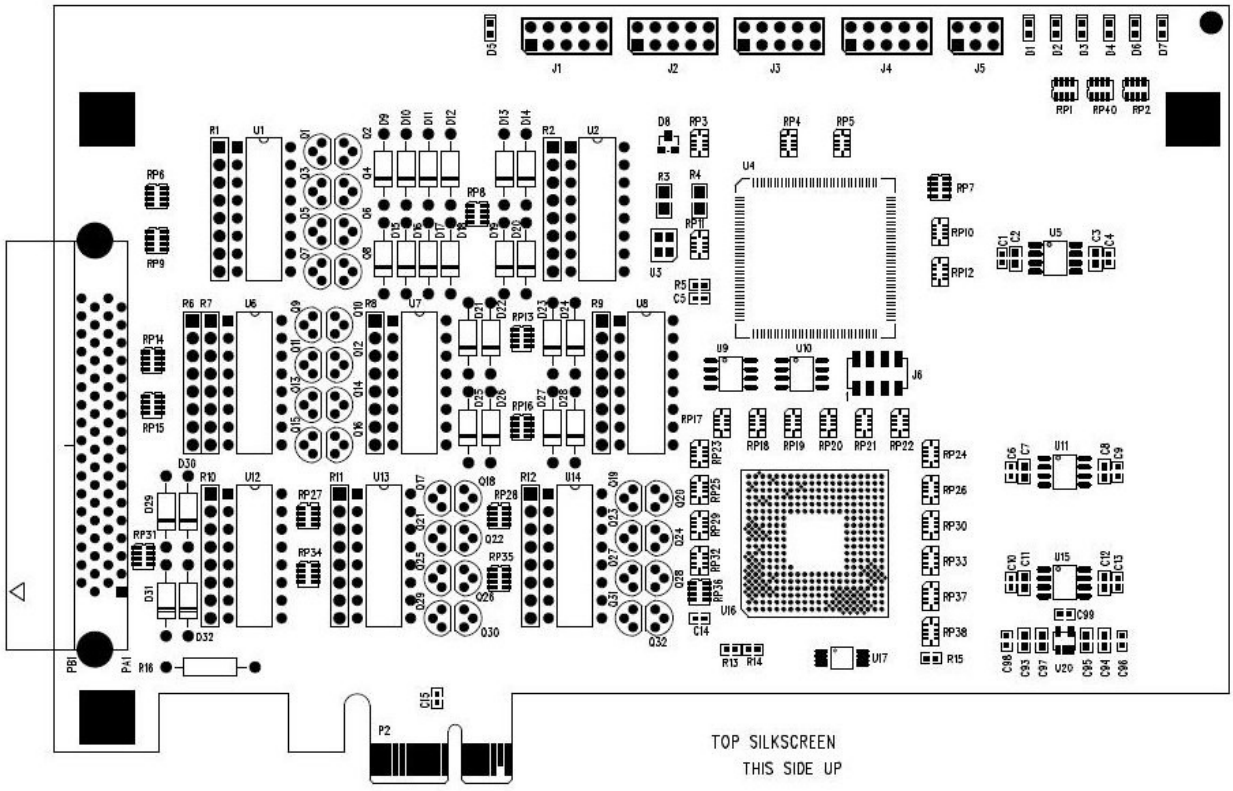
- Programmable Little Endian / Big Endian swapping
- PCIe cycles Asynchronous to local bus cycles
- Software Programmable board base address

# SECTION 2

# 2. INSTALLATION AND MAINTENANCE

## *2.1 Card Configuration*

*Figure 1 Board Layout*




## *2.2 Installation*

### 2.2.1 Physical Installation

Selectable input voltage range thru use of field replaceable bias resistors using standard 8 pin SIP isolation resistors. These bias resistor packages are socketed for easy replacement. One bias resistor package will affect the input channels on nibble boundaries.

### 2.2.2 Input / Output Cable Connectors

*Table 2-1 Input / Output Cable Pin Assignments*

| PIN NUMBER | SIGNAL | PIN NUMBER | SIGNAL |
|---|---|---|---|
| 1 | IN CH00 HI | 35 | LOG OUT CH9 HI |
| 2 | IN CH00 LO | 36 | LOG OUT CH9 LO |
| 3 | IN CH01 HI | 37 | LOG OUT CH10 HI |
| 4 | IN CH01 LO | 38 | LOG OUT CH10 LO |
| 5 | IN CH02 HI | 39 | LOG OUT CH11 HI |
| 6 | IN CH02 LO | 40 | LOG OUT CH11 LO |
| 7 | IN CH03 HI | 41 | LOG OUT CH12 HI |
| 8 | IN CH03 LO | 42 | LOG OUT CH12 LO |
| 9 | IN CH04 HI | 43 | LOG OUT CH13 HI |
| 10 | IN CH04 LO | 44 | LOG OUT CH13 LO |
| 11 | IN CH05 HI | 45 | LOG OUT CH14 HI |
| 12 | IN CH05 LO | 46 | LOG OUT CH14 LO |
| 13 | IN CH06 HI | 47 | LOG OUT CH15 HI |
| 14 | IN CH06 LO | 48 | LOG OUT CH15 LO |
| 15 | IN CH07 HI | 49 | LOG OUT CH0 HI |
| 16 | IN CH07 LO | 50 | LOG OUT CH0 LO |
| 17 | IN CH08 HI | 51 | LOG OUT CH1 HI |
| 18 | IN CH08 LO | 52 | LOG OUT CH1 LO |
| 19 | IN CH09 HI | 53 | LOG OUT CH2 HI |
| 20 | IN CH09 LO | 54 | LOG OUT CH2 LO |
| 21 | IN CH10 HI | 55 | LOG OUT CH3 HI |
| 22 | IN CH10 LO | 56 | LOG OUT CH3 LO |
| 23 | IN CH11 HI | 57 | PWR OUT CH4 HI |
| 24 | IN CH11 LO | 58 | PWR OUT CH4 LO |
| 25 | IN CH12 HI | 59 | PWR OUT CLAMP 4 |
| 26 | IN CH12 LO | 60 | PWR OUT CH5 HI |
| 27 | IN CH13 HI | 61 | PWR OUT CH5 LO |
| 28 | IN CH13 LO | 62 | PWR OUT CLAMP 5 |
| 29 | IN CH14 HI | 63 | PWR OUT CLAMP 6 |
| 30 | IN CH14 LO | 64 | PWR OUT CH6 HI |
| 31 | IN CH15 HI | 65 | PWR OUT CH6 LO |
| 32 | IN CH15 LO | 66 | PWR OUT CLAMP 7 |
| 33 | LOG OUT CH8 HI | 67 | PWR OUT CH7 HI |
| 34 | LOG OUT CH8 LO | 68 | PWR OUT CH7 LO |

## 2.3 System Configuration

### 2.3.1 Opto-Isolated Inputs

Selectable input voltage range thru use of field replaceable bias resistors, labeled RIN, using standard 8 pin SIP isolation resistors. These bias resistor packages are socketed for easy replacement One bias resistor package will affect the input channels on nibble boundaries as follows:

*Table 2-2 Input Channels Bias Resistors Locations.*

| Resistor Location | Input Channels |
|---|---|
| R10 | IN CH00 thru IN CH03 |
| R9 | IN CH04 thru IN CH07 |
| R8 | IN CH08 thru IN CH11 |
| R2 | IN CH12 thru IN CH15 |

Current Limiting Resistor Values should be chosen to provide a Minimum input current of 2.3 mA. Typical resistor values for input voltage levels are as follows:

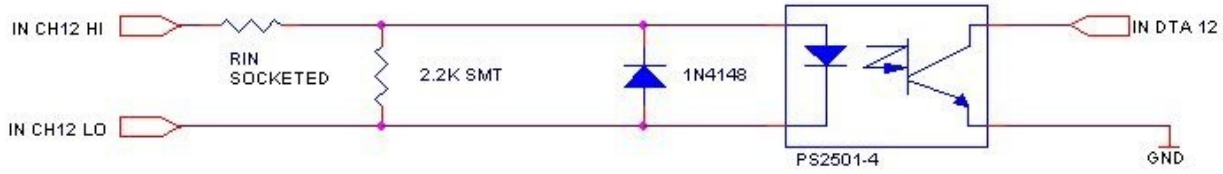
*Table 2-3 Input Channels Bias Resistor Values*

| Input Voltage Range | Bias Resistor Values |
|---|---|
| 5 V | 2200 ohms |
| 12 V | 5100 ohms |
| 28 V | 12000 ohms |
| 48 V | 20000 ohms |

### *2.3.1.1 Input Channels 0-15*

Isolation Voltage – 5000 V
Current Transfer Ratio – 80-600%
Min Input Current – 2.3 mA.
Max Input Current – 80 mA.
Typical Ton/Toff – 3/5 uSec.

*Figure 2 Input Channels 0-15, Typical*



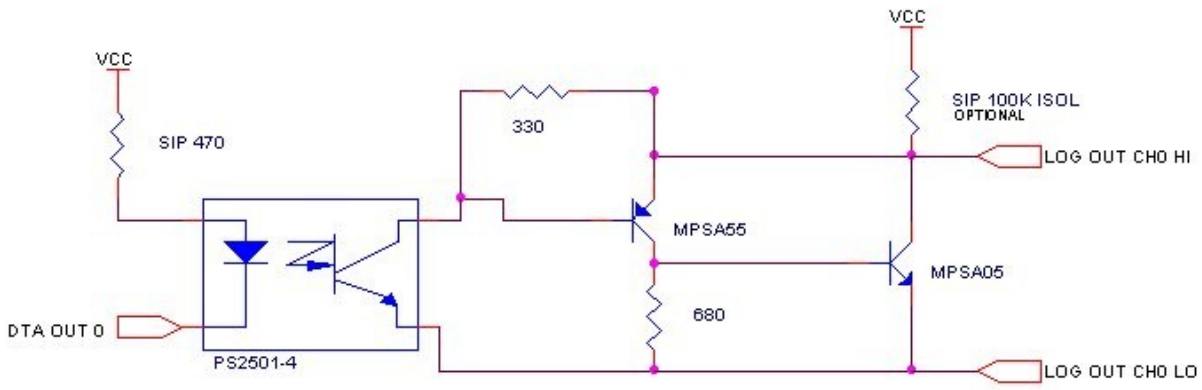
## 2.3.2 Opto-Isolated Outputs

### *2.3.2.1 Normal Outputs Bits 0-3, 8-15*

Output Bits 0-3 contain an Optional Pullup resistor to VCC that is not normally installed. Output Bits 8-15 are the same as bits 0-3 except the optional resistor does not exist.

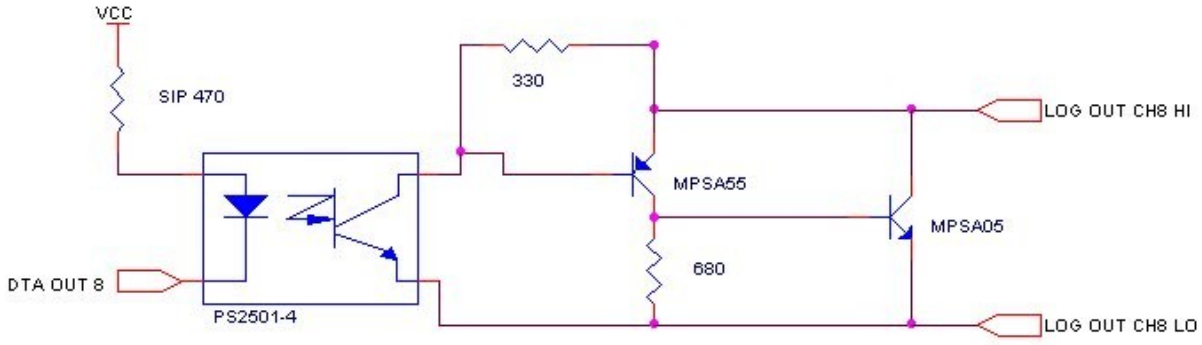
Isolation Voltage – 5000 V
VCEO (Max) – 60 V
Maximum Current – 100 ma.
Typical Ton/Toff – 3/5 uSec.

*Figure 3 Normal Outputs, Bits 0-3*




100 K isolation Resistor is Optional and is not normally installed.

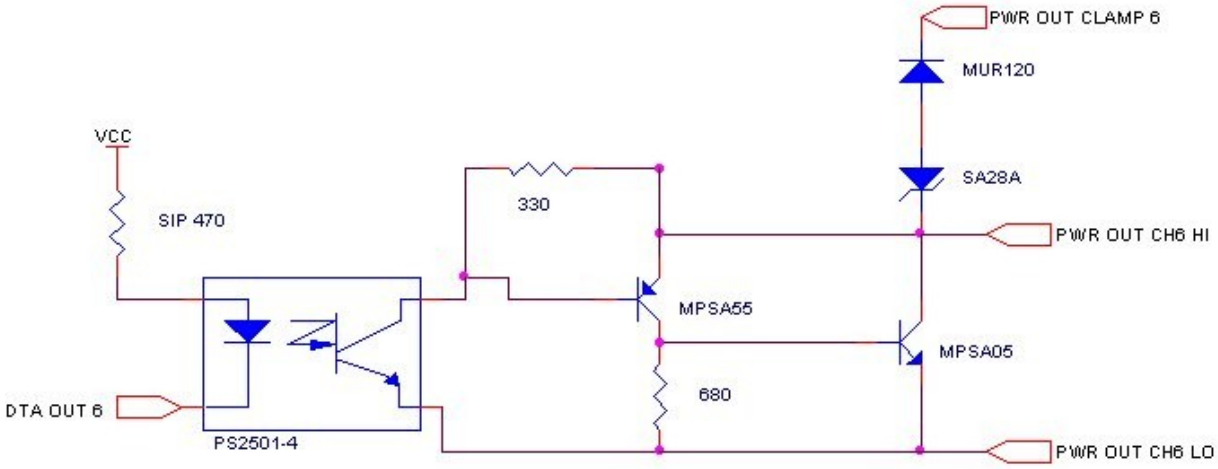
*Figure 4 Normal Outputs, Bits 8-15*



### *2.3.2.2 Diode Clamped Outputs Bits 4-7*

Isolation Voltage – 5000 V
VCEO (Max) – 60 V
Maximum Current – 100 ma.
Typical Ton/Toff – 3/5 uSec.

*Figure 5 Diode Clamped Outputs, Bits 4-7*



# SECTION 3

# 3. CONTROL SOFTWARE

## *3.1 Introduction*

## *3.2 Board Register Descriptions*

*Table 3-4 Register Address Map*

| Board Offset | Size | Register Name |
|---|---|---|
| 0x00 | 32 Bits Read Only | Board Status Register |
| 0x00 | 8 Bits Write Only | Board Control Register |
| 0x04 | 16 bits Read ONLY | Received Data Register |
| 0x08 | 16 bits Read / Write | Change of State Register |
| 0x0c | 16 bits Read / Write | Receive Event Counter |
| 0x010 | 16 bits Read / Write | COS Interrupt Enable Register |
| 0x014 | 16 bits Read / Write | COS Polarity Register |
| 0x018 | 24 bits Read / Write | Clock Division Register |
| 0x01c | 16 bits Read / Write | Output Data Register |
| 0x020 | 32 Bits Read / Write | Test Register 1 |
| 0x024 | 32 Bits Read / Write | Test Register 2 |

### 3.2.1 Board Status Register - Board Offset 0x00

32 Bits read only. With Firmware Rev B this Register expanded to 32 Bits with Fields to Identify the Firmware Revision Level, and the Board ID.

*Table 3-5 Board Status Register*

| Field | Description |
|---|---|
| Bit[0] | Int Byte LO Out H = bits 7 - 0 COS interrupt status |
| Bit[1] | Int Byte MD Out H = bits 15 - 8 COS interrupt status |
| Bit[2] | Reserved |
| Bit[3] | Rx Event Overflow H = Event Overflow status |
| Bit[4] | Master Int Out = Master Interrupt Status – 1=Interrupt into the PLX |
| Bit[5] | Slow Debounce Clock ; |
| Bit[6] | Enable Rx Event Overflow H = Interrupt Enable for Event Overflow Read Back |
| Bit[7] | Fail LED ON L – Read Back |
| | Prior to Firmware Rev B, Bits 8..31 were not used and Undefined.<br>With Firmware Rev B the Following Fields were added. |
| Bit[15..8] | Reserved – Set to 0x00. |
| Bit[23..16] | Current Firmware Rev Level - was added with Rev B – Set to 0x01 for Rev B. |
| Bit[31..24] | Board Identifier. Set to 0x01 to Identify the OPTO16x16 Board Family. |

When the FW Rev field was added it was set to 0x01because it was the first time the Field was Present. If there is a future revision it will be adjusted to be consistent with the Actual Firmware Revision Level.

### 3.2.2 Board Control Register - Board Offset 0x00 -

8 Bits write only. -

*Table 3-6 Board Control Register*

| Field | Description |
|---|---|
| Bit[0] | Clear Int Byte LO H = clear COS bits 7 - 0 |
| Bit[1] | Clear Int Byte MD H = clear COS bits 15 - 8 |
| Bit[2] | Reserved |
| Bit[3] | Clear Rx Event Overflow H =Clear Event Counter Overflow Status |
| Bit[4] | Master Clear = - Clear All COS bits and Event Counter Overflow Status bit. |
| Bit[5] | Reserved |
| Bit [6] | Enable Rx Event Overflow H - 1 = Interrupt enable. |
| Bit [7] | Fail LED ON L - 0=LED On / 1 = LED Off |

*NOTE: Bits 0-4 are self-clearing pulses that are written as a 1 to clear the interrupt source. The bits will then self clear so that another host operation is not required.*

*NOTE: The Clear COS Bytes, or the Master Clear (bit[4]), will clear ANY COS register bit that is set regardless of the bits Interrupt Enable Status. For Individual COS bit clearing, Write a 1 to the COS bit you wish to clear.*

Event Overflow status will only be cleared by Clear Event Overflow or by Master Clear, Bit[4]. Loading the Event Counter WILL NOT clear out the event overflow status.

### 3.2.3 Received Data Register - Board Offset 0x04

16 bits. Debounced Receive data bits 0 - 16. Read ONLY.

The Input Data Bits, After they have been Debounced

*Table 3-7 Received Data Register*

| Field | Description |
|---|---|
| 15:0 | Debounced Receive Data bits 0 - 16. Read ONLY The Debounced Input Data Bits. |
| 31:16 | Reserved – Undefined |

### 3.2.4 Change of State Register - Board Offset 0x08

16 bits - Change of State Detected. Polarity programmed thru COS Polarity register, 0x014.

If a COS bit is set, then it will stay set until cleared by the host. A COS bit can be cleared by writing a 1 to a COS bit that is set. Writing a zero will have no effect. Writing a 1to a bit that is 0 will do nothing. COS bits may also be cleared by using the board control register Byte clears or using the board control master clear.

*Table 3-8 Change of State register*

| Field | Description |
|---|---|
| 15:0 | Change of State Data bits 0 - 16. Writing a 1 will clear a bit that is set. |
| 31:16 | Reserved – Undefined |

### 3.2.5 Receive Event Counter - Board Offset 0x0c

16 bits Read / Write. Reset to Zero.

This counter may be read at any time by the host. Counter will increment once for every Debounced Rising edge detected on input data bit 15. When the counter is 0x0ffff and increments the Rx event overflow status bit will be set and can be used to generate an interrupt.

*Table 3-9 Receive Event Counter*

| Field | Description |
|---|---|
| 15:0 | Receive Event Counter |
| 31:16 | Reserved – Undefined |

### 3.2.6 COS Interrupt Enable Register - Board Offset 0x010

16 bits. Read / Write. Reset to Zero.

Each bit will be bitwise ANDED with the COS register and all of the results OR'ed together to generate an Interrupt. A 1 will enable the corresponding interrupt. A 0 will disable that bit from generating an interrupt.

*Table 3-10 COS Interrupt Enable Register*

| Field | Description |
|---|---|
| 15:0 | COS Interrupt Enable Register 1=Enable Interrupt for that corresponding COS bit. |
| 31:16 | Reserved – Undefined |

### 3.2.7 COS Polarity Register - Board Offset 0x014

16 bits. Read / Write. Reset to Zero.

When the corresponding bit is zero, the COS detection for that bit will be set by a detected High to Low transition. When Set to a 1 the COS detection for that bit will look for Low to High transitions. Reset to all zeros.

*Table 3-11 COS Polarity Register*

| Field | Description |
|---|---|
| 15:0 | COS Polarity Register - 1=Low to Hi will set COS Bit. 0=Hi to Low will set COS, Per Bit. . |
| 31:16 | Reserved – Undefined |

### 3.2.8 Clock Division Register - Board Offset 0x018

24 bits. Read / Write. Reset to Zero.

*Table 3-12 Clock Division Register*

| Field | Description |
|---|---|
| 23:0 | Clock Division Register - Sets the Clock Division Rate. |
| 31:24 | Reserved – Undefined |

*NOTE >>>> when altering this register, disable all interrupts and expect unusual results in the COS Detection register.*

A 24 Bit clock divider is provided for programmable Debounce delays. The debounce circuit registers the incoming data 3 times in a daisy chain. When ALL 3 registers are high, the incoming data is a high. When the debounced data register contains a 1, then ALL three registers must contain zero for the debounced data to transition back to a zero. The clock for these holding registers is programmable thru the clock divider.

The Basic clock of the board is 20 MHz, 50 Ns. The Basic Clock Counter will always divide by 4, 200 Ns. Values of 0x0000 or 0x0001 will not alter this. When the clock divider is loaded with a larger value then the clock division will be (count * 2) + 2. The Total debounce time will be 3 X (clock division time).

For Example: for a 15ms. debounce time. Clock period should be 5ms.

5ms / 50 Ns = 100000. -2 = 99998.

99998 / 2 = 49999 = 0x0c34f Hex.

### 3.2.9 Output Data Register - Board Offset 0x01c.

16 bits - Read / Write. Reset to Zero.

The 16 bit output data register. Reset to All Zero's. Writing a 1 to a bit will make that opto output conductive and current will flow from 'HI' to 'LO'. Writing a 0 will turn the opto off and the output will be Non -Conductive from 'HI' to 'LO'

*Table 3-13 Output Data Register*

| Field | Description |
|---|---|
| 15:0 | Output Data Register - Controls the Opto-Isolated Outputs. . |
| 31:16 | Reserved – Undefined |

### 3.2.10 Test Register 1

32 Bits – Read / Write. Reset to Zero.

32 bit Register does not do anything. It was added to test 8, 16, and 32 Bit Reads and Writes.

*Table 3-14 Test Register 1*

| Field | Description |
|---|---|
| 31:0 | Test Register 1 - Can be used for anything. |

### 3.2.11 Test Register 2

32 Bits – Read / Write. Reset to Zero.

32 bit Register does not do anything. It was added to test 8, 16, and 32 Bit Reads and Writes.

*Table 3-15 Test Register 2*

| Field | Description |
|---|---|
| 31:0 | Test Register 2 - Can be used for anything. |

# 4. PEX 8311 Notes

The PCIe-OPTO16x16 uses the PLX Technologies PEX8311AA Interface chip. In the System Devices list this chip will show up as 2 devices, a 8311 PCIe to PCI bridge and a 9056 PCI to local bus adapter.

## *4.1 Initialization*

When the PEX8311 is reset, the 9056 part of the chip will initialize itself from an on board serial EEPROM that is programmed at General Standards. A brief description of some of the Registers follows.

*Table 4-16 EEPROM Register Initialization*

| Eeprom Addr | PCI Addr | Description | Value After Reset |
|---|---|---|---|
| 0x00 | 0x00 | Device ID / Vendor ID | 0x905610B5 |
| 0x44 | 0x2c | Sub-System ID / Vendor ID | 0x346010b5 |
| 0x04 | 0x08 | Class Code / Revision | 0x078000ba |
| 0x0c | 0x78 | Mailbox 0 | 0x00020002 |
| 0x10 | 0x7c | Mailbox 1 | 0x00020100 |
| 0x14 | | Space 0 range PCI to Local | 0xffffff80 |
| 0x18 | | Space 0 Base Address (remap) | 0x00000001 |

A list of the full EEPROM contents is located in Appendix B.

### 4.1.1 Device ID / Vendor ID

Device ID and Vendor ID are used to identify the PLX Device during configuration cycles.

*Table 4-17 Device ID / Vendor ID Register Description*

| Field | Description | Value After Reset |
|---|---|---|
| 15:0 | Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX | 0x10B5 |
| 31:16 | Device ID - Identifies the particular device. Defaults to the PLX part number for PCI interface chip. | 0x9056 |

### 4.1.2 Sub-System ID / Vendor ID

Sub-System ID and Vendor ID are used to identify the PCIe-OPTO16x16 during configuration cycles.

*Table 4-18 Sub-System ID and Vendor ID Register Description*

| Field | Description | Value After Reset |
|---|---|---|
| 15:0 | Vendor ID - Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX. | 0x10B5 |
| 31:16 | Sub-System ID - Identifies the particular device. Sub-System ID Assigned to the OPTO16x16 by PLX. | 0x3460 |

### 4.1.3 Class Code / Revision

When loaded from the EE Prom this register will identify the device Base Class Code, Sub-Class Code and Revision of the PLX Device. PLX Revision is hard coded in the device.

*Table 4-19 Class Code / Revision Register*

| Field | Description | Value After Reset |
|---|---|---|
| 07:00 | Revision Level of the PLX – currently | 0xba |
| 15:08 | Register Level Programming Interface - 0x00 - None Defined | 0x00 |
| 23:16 | Sub-Class Code - 0x80 – Other Communications Device | 0x08 |
| 31:24 | Base Class Code 0x07 – Simple Communications Controller | 0x07 |

### 4.1.4 Mailbox 0

When loaded from the EE Prom, this mailbox is used to contain values to identify the PLD revision, and EE Prom Revision levels of this board.

*Table 4-20 Mailbox 0*

| Field | Description | Value After Reset |
|---|---|---|
| 15:0 | PLD Revision Level – Revision Level of the FPGA on the OPTO16x16.<br>Currently 0x02 = Rev B . | 0x0002 |
| 31:16 | EE Prom Revision Level – Revision Level of the PLX EEPROM contents.<br>Currently 0x02 = Rev B . | 0x0002 |

### 4.1.5 Mailbox 1

When loaded from the EE Prom, this mailbox register is used to identify the overall Board assembly level, and to Identify this Assembly.

*Table 4-21 Mailbox 1*

| Field | Description | Value After Reset |
|---|---|---|
| 15:0 | Assembly Identifier –<br>0x0100 Identifies the OPTO16x16 | 0x0100 |
| 31:16 | Board Assembly Revision Level<br>Currently 0x02 = Rev B . | 0x0002 |

### 4.1.6 Address Space 0 Range PCI to Local

Size of the Address Space required for the OPTO16x16. The OPTO16x16 uses 128 Bytes of Memory Space.

*Table 4-22 Space 0 Range PCI to Local*

| Field | Description | Value After Reset |
|---|---|---|
| 31:00 | Address Space 0 Range – Zero's indicate the size in Bytes of the Address Space to be reserved for the Board.<br>Bit 0 Indicates the Board is mapped into Memory Space.<br>The OPTO16x16 uses 128 Bytes of Memory Space. | 0xffffff80 |

### 4.1.7 Address Space 0 Base Address (Remap)

There is no address space Remap for the Board. Bit Zero indicates that Address Space 0 is Active for writing to Local Registers on the Board.

*Table 4-23 Address Space 0 Base Address (Remap)*

| Field | Description | Value After Reset |
|---|---|---|
| 31:00 | Address Space 0 Base Address (Remap) 0x01<br>Bit 0 Indicates that Address Space 0 is Active. | 0x00000001 |

# Appendix A

## *INTERRUPTS:*

For Interrupt Operation, the Desired Interrupts are Enabled on the Opto isolator board AND Interrupts MUST be enabled At / Thru the PLX Interface chip. To enable Event Counter Overflow Interrupts, Bit[6] of the Board Control Register must be set to a 1.

```
outportb(Opto_register_base_address + 0x00, 0xc0 );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
outportl(Opto_register_base_address + 0x0c, 0x0fffe );
        // Long word write, Event Counter, -2.
        // The Second Rising Edge detected will generate the Interrupt
```

To Enable COS Interrupts, Any / All Desired COS Interrupt bit's are enabled thru the COS Interrupt Enable Register.

```
outportl(Opto_register_base_address + 0x010, 0x08421 ) ;
        // Long word write, Offset 0x010, Enable Interrupts on
        // COS Bit's 0, 5, 10, and 15.
```

All other Machine dependent actions should be taken before the final steps in the process. Make ABSOLUTELY sure that there is NO Pending status laying around that is already setting an interrupt action. Either use the master clear's

```
outportb(Opto_register_base_address + 0x00, 0xdf );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
        // Master Clear All COS and Clear the Event Counter overflow .
        // NOTE NOTE NOTE NOTE
        // The Master Clear will Clear ALL COS Bits.
        // The Byte Clear's will ALSO Clear ALL COS Bits in that Byte.
        // To Only Clear the Bit generating the Interrupt,
        // you must use the individual Clear's as
        // Described below.
```

Or, Individual Clears for the COS and Event Overflow.

```
Outportl(Opto_register_base_address + 0x08, 0x08421 ) ;
        // Long word write, Offset 0x08, COS register, Clear
        // COS Bit's 0, 5, 10, and 15. If they are set.

Outportb(Opto_register_base_address + 0x00, 0xc8 );
        // Byte write, Turn LED off, Enable Event Overflow Interrupt.
        // Clear Event Overflow
```

The final step is the write to the PLX interface that will enable it to generate Interrupts onto the PCI bus.

```
Outportl(PLX_io_base_address + 0x068, 0x00900 );
        // Long word write, PLX interrupt control register,
        // Bit's 8 and 11, Enable Local input to generate PCI interrupts
```

In the Interrupt Handler, there is NO action required to / with the PLX Interface chip. The only requirement to remove the Asserted interrupt is to remove the Local source of the interrupt. Which would be the COS bit or the event overflow.

```
temp = inportb(Opto_register_base_address + 0x00 ) ;
        // Read the OPTO Board Status register
if ( (temp & 0x010) == 0x010 )
        {
                // Master Interrupt bit will be set in the Board Status
                // Register if this board generated the Interrupt.
                // Status Bits 0 thru 3 could also be examined to
                // Determine Which Byte generated the Interrupt
                // Or if the Event Counter Overflow generated
                // The Interrupt.
                .
                .
                .
                .
                // Finished processing, Now It's time to clear the
                // Pending Interrupt.

        Outportl(Opto_register_base_address + 0x08, 0x08421 ) ;
                // Long word write, Offset 0x08, COS register, Clear
                // COS Bit's 0, 5, 10, and 15. If they are set.

        Outportb(Opto_register_base_address + 0x00, 0xc8 );
                // Byte write, Turn LED off, Enable Event Overflow Interrupt.
                // Clear Event Overflow
        }
```

To Disable All Interrupt's From the OPTO board, write to the PLX interface Chip.

```
Outportl(PLX_io_base_address + 0x068, 0x0000 );
        // Long word write, PLX interrupt control register,
        // Clear Bit's 8 and 11, disable All PCI interrupts
```

# Appendix B

## *PLX EEPROM Contents:*

The Full contents of the OPTO16x16 EEPROM for the 9056 portion of the interface chip are as follows.

*Table B-24 PLX EEPROM Contents*

| **Eeprom Addr** | **Description** | **Value After Reset** |
|---|---|---|
| 0x00 | Device ID / Vendor ID | 0x905610B5 |
| 0x04 | Class Code / Revision | 0x07800002 |
| 0x08 | Max / Min Latency / Int. Pin / Int. Line Routing Value | 0x00000100 |
| 0x0c | Mailbox 0 | 0x00020002 |
| 0x10 | Mailbox 1 | 0x00020100 |
| 0x14 | Space 0 range PCI to Local | 0xffffff80 |
| 0x18 | Space 0 Base Address (remap) | 0x00000001 |
| 0x1c | Mode / DMA Arbitration register | 0x01200000 |
| 0x20 | VPD Boundary -Big / Little Endian descriptor | 0x00300500 |
| 0x24 | Expansion ROM Range – Not Used | 0x00000000 |
| 0x28 | Expansion ROM Re-Map – Not Used | 0x00000000 |
| 0x2c | Space 0 / Expansion ROM Descriptor | 0x42000140 |
| 0x30 | Direct Master to PCI Range – Not Used | 0x00000000 |
| 0x34 | Direct Master to PCI Local Base Address – Not Used | 0x00000000 |
| 0x38 | Direct Master to PCI IO/CFG Base Address -Not Used | 0x00000000 |
| 0x3c | Direct Master to PCI Memory Re-Map – Not Used | 0x00000000 |
| 0x40 | Direct Master to PCI IO/CFG PCI – Not Used | 0x00000000 |
| 0x44 | Sub-System ID / Vendor ID | 0x346010b5 |
| 0x48 | Space 1 range PCI to Local – Not Used | 0x00000000 |
| 0x4c | Space 1 Base Address (remap) – Not Used | 0x00000000 |
| 0x50 | Space 1 Descriptor – Not Used | 0x00000000 |
| 0x54 | Hot Swap Control | 0x00004c06 |
| 0x58 | PCI Arbiter Control | 0x00000000 |
| 0x5c | PM Capabilities | 0x00024801 |
| 0x60 | PM Control / Status | 0x00000000 |