OKI Open up your dreams

FEUL9636-01

ML9636GDZ45A User's Manual

Issue Date: January 10, 2008

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Preface

The ML9636GDZ45A User's Manual consists of the following two documents:

ML9636GDZ45A User's Manual		FEUL9636-01
A Separate Volume for the ML9636 User's Manual	Command Details	FEUL9636CMD-01

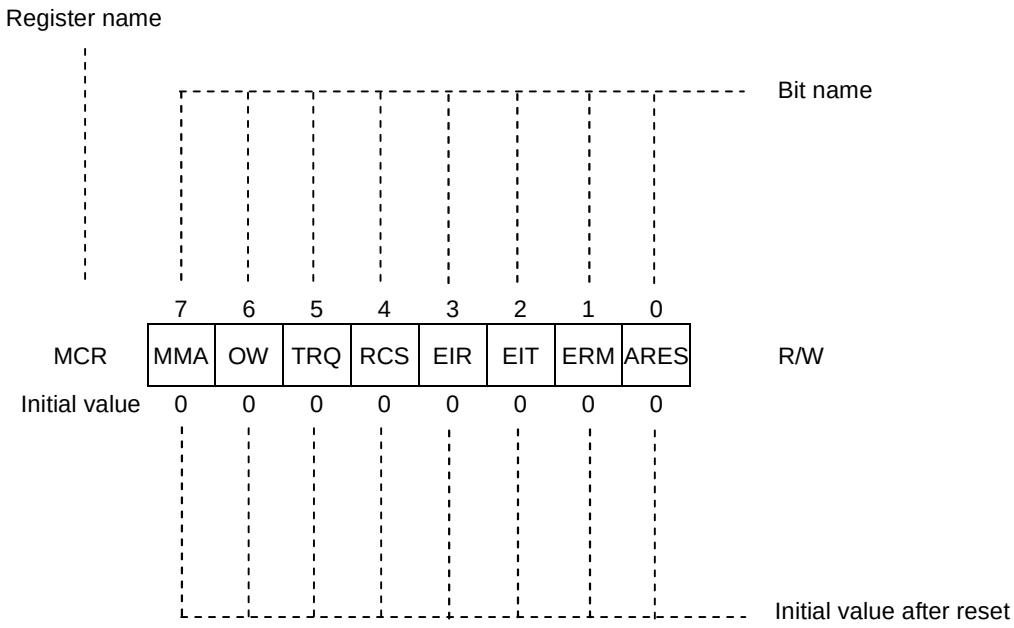
This user's manual describes the operation of the ML9636.

Notation

Classification	Notation	Description
• Numeric value	0x*nn*	Indicates a hexadecimal number.
• Address	0x*nnnn_nnnn*	Indicates a hexadecimal number (represents 0xnnnnnnnn).
• Unit	word, WORD	1 word = 32 bits
	byte, BYTE	1 byte = 8 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
• Terminology	"H" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

• Register description

Read/write attribute: R indicates a readable bit and W indicates a writable bit.
MSB: Most significant bit of the 8-bit register (memory)
LSB: Least significant bit of the 8-bit register (memory)



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1. Overview

The ML9636GDZB5A (Called ML9636 in following) conforms to ARIB STD-T75 (dedicated short-range communications (DSRC) system standard) version 1.3. It is an IC whose RF and MODEM sections are integrated into a single chip and can be used for 5.8 GHz ASK/QPSK DSRC communication. The IC can be applied to DSRC systems in combination with a baseband LSI for DSRC.

1.1 Features

- Conforms to ARIB STD-T75 (dedicated short-range communications (DSRC) system standard) version 1.3.
- Includes receive and transmit circuits, a synthesizer, and a digital modulation and demodulation circuit.
- The digital circuit also includes a split phase coding and decoding circuit in ASK mode.
  However this is only for the split phase code of 1024kbps. (Manchester code)
- The interface with a base-band is for digital signals and low-speed analog signals (RSSI) only
- Radio frequency range
  Downlink
  D7 5775 MHz, D6 5780 MHz, D5 5785 MHz, D4 5790 MHz,
  D1 5795 MHz, D3 5800 MHz, D2 5805 MHz
  Uplink
  U7 5815 MHz, U6 5820 MHz, U5 5825 MHz, U4 5830 MHz,
  U1 5835 MHz, U3 5840 MHz, U2 5845 MHz
- Data transfer speed
  In ASK mode: 1024 kbps
  In QPSK mode: 4096 kbps
- Supply voltage

I/O section	VDDIO: 3.3 V Typ.	3.15 V Min.	3.45 V Max.
CORE and RF sections	VDDCORE:1.6 V Typ.	1.5 V Min.	1.65 V Max.

- Supply current

During reception:	115 mA (Max.)
During transmission:	95 mA (Max.: When –7 dBm is transmitted from the TX_P pin)

- Package

48-pin WQFN	P-WQFN48-0707-0.50-63

1.2 Block Diagram

Figure 1-1 shows a block diagram of this IC. Table 1-1 shows a functional summary of each block.

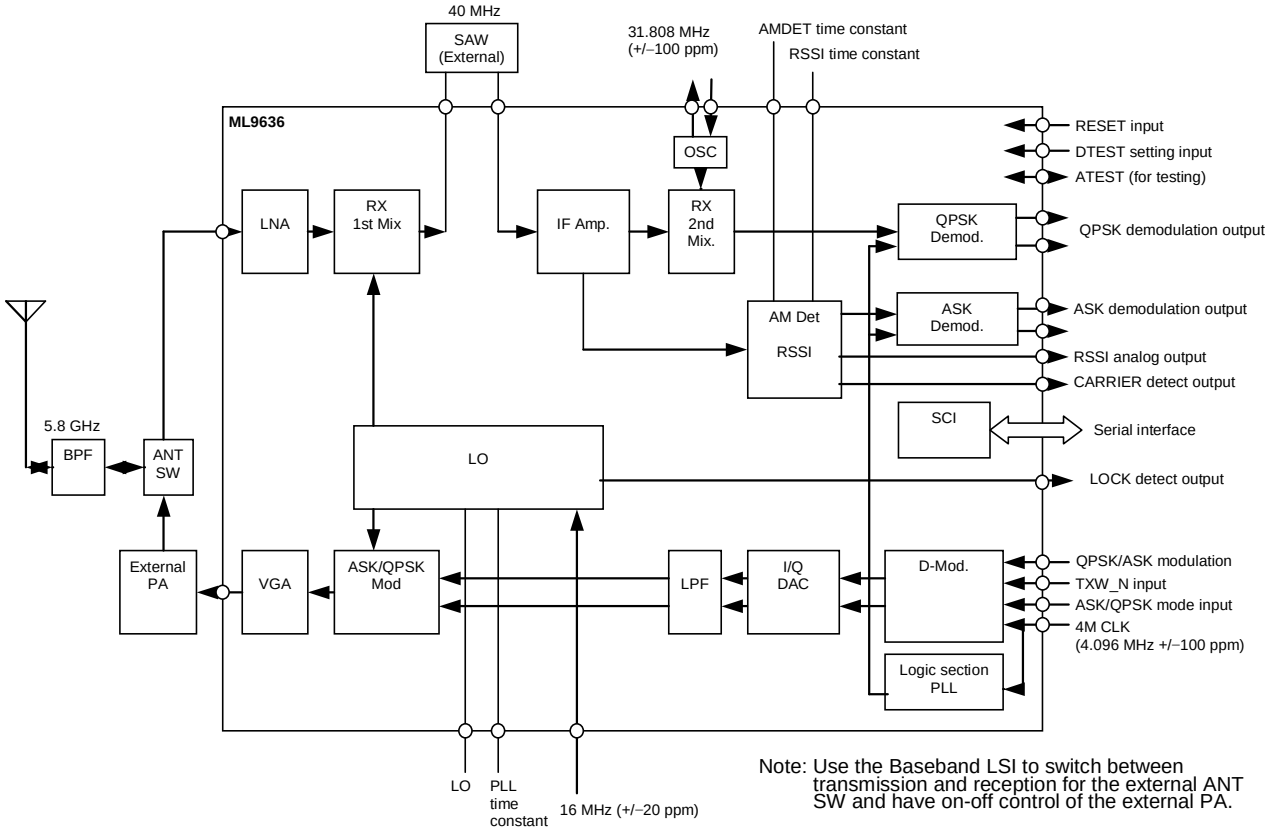


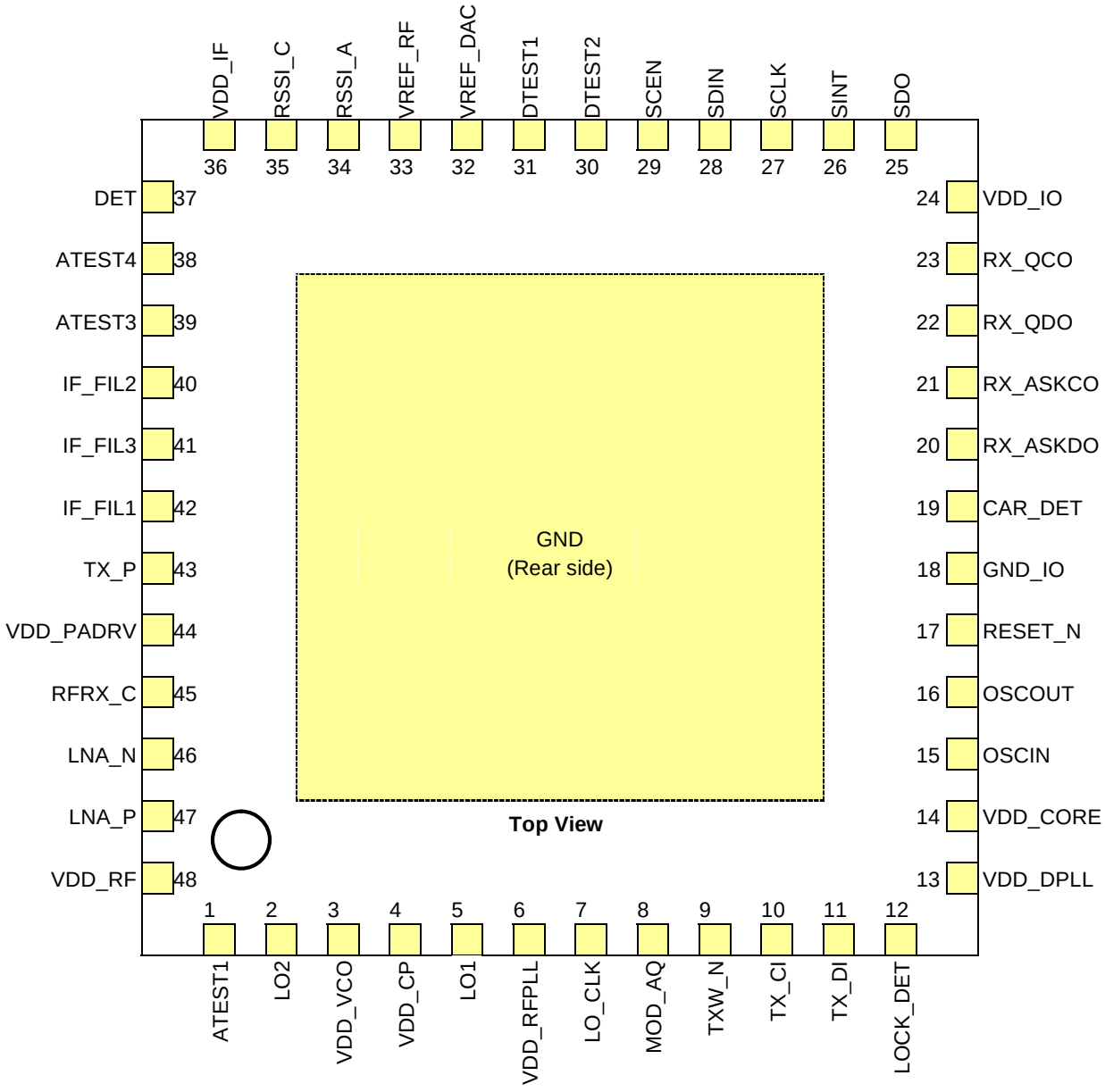
Figure 1-1 Block Diagram of ML9636

Table 1-1 Functional Summary of Each Block

Block	Function
LNA	Low noise amplifier
RX 1st Mix	1st receive mixer
IF Amp	Intermediate frequency amplifier
RX 2nd Mix	2nd receive mixer
OSC	Oscillator for 2nd mixer (31.808 MHz)
AM Det RSSI	Amplitude detect / RSSI carrier detect
LO	Local oscillator
VGA	Variable gain amplifier
ASK/QPSK Mod	ASK/QPSK modulation
LPF	Low-pass filter
I/Q DAC	Digital to analog conversion for I/Q
QPSK Demod	QPSK digital demodulation
ASK Demod	A decoding for split phase of 1024kbps and a clock recovery for ASK
D-Mod	Digital modulation (includes split phase coding of 1024kbps for ASK)
Logic section PLL	PLL for the logic section (generates the clock based on 4M CLK)
SCI	Serial interface used to configure settings for registers

1.3 Pins

1.3.1 Pin Configuration



48-Pin WQFN (Top View)

* The actual pads are not visible since this pin configuration shows the top view.

Figure 1-2 Pin Configuration of ML9636

Note: The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.

1.3.2 Pin Descriptions

Pin	Symbol	I/O (*1)	Description	State at reset	Active level
RF related pins					
47	LNA_P	I_{RF}	Receive antenna input pin P	—	—
46	LNA_N	I_{RF}	Receive antenna input pin N	—	—
43	TX_P	O_{RF}	Output pin P to transmit PA	—	—
42	IF_FIL1	O_A	Output pin for the external 40 MHz filter	—	—
40	IF_FIL2	I_A	Input pin for the external 40 MHz filter	—	—
41	IF_FIL3	I_A	Connection pin for the external 40 MHz filter	—	—
45	RFRX_C	—	Connection pin for the external capacitor for RF	—	—
37	DET	—	Connection pin for the external capacitor (for ASK demodulation)	—	—
35	RSSI_C	—	Connection pin for the external capacitor (for RSSI integration)	—	—
5	LO1	—	Connection pin for the external capacitor and resistor (for PLL)	—	—
2	LO2	—	Connection pin for the external capacitor and resistor (for PLL)	—	—
7	LO_CLK	I_A	16 MHz input pin for LO (*2)	—	—
32	VREF_DAC	—	Reference pin for DAC (connected to GND via a 0.01 μF capacitor)	—	—
33	VREF_RF	—	Reference pin for RF (connected to the 1.6 V supply)	—	—
MODEM interface (RX) related pins					
20	RX_ASKDO	O	RX ASK split phase demodulation data output pin	L	—
21	RX_ASKCO	O	Clock output pin for RX ASK (1.024 MHz)	L	—
22	RX_QDO	O	RX QPSK data output pin	L	—
23	RX_QCO	O	Clock output pin for RX QPSK (equivalent to 4.096 MHz)	L	—
19	CAR_DET	O	Carrier detect output pin H: Detect	—	H
34	RSSI_A	O_A	RSSI analog output pin	—	—
MODEM interface (TX) related pins					
11	TX_DI	I	TX data input pin	—	—
10	TX_CI	I	TX clock input pin (4.096 MHz) Digital reference clock (*3)	—	—
9	TXW_N	I	Input pin for output timing control L: Transmission, H: Reception	—	—
8	MOD_AQ	I	Input pin for ASK/QPSK output switching H: ASK, L: QPSK	—	—
Synchronous communication interface (SCI) related pins					
28	SDIN	I	Synchronous communication interface Data input pin	—	—
25	SDO	O	Synchronous communication interface Data output pin	L	—
27	SCLK	I	Synchronous communication interface Clock input pin	—	—
26	SINT	O	Synchronous communication interface Interrupt output pin	H	L
29	SCEN	I	Synchronous communication interface Chip enable pin	—	L
System control pins					
17	RESET_N	I	Hardware reset pin	—	L
15	OSCIN	I_{OS}	31.808 MHz crystal connection pin 1 External clock input pin	—	—
16	OSCOUT	O_{OS}	31.808 MHz crystal connection pin 2 Leave this pin open when OSCIN is used as an external clock input pin.	—	—
12	LOCK_DET	O	PLL LOCK detecting output pin H: Lock, L: Unlock	—	H

Pin	Symbol	I/O (*1)	Description	State at reset	Active level
Control pins for testing					
31	DTEST1	I_D	Test mode setting pin 1. Fix to "L."	—	—
30	DTEST2	I_D	Test mode setting pin 2. Fix to "L."	—	—
1	ATEST1	I_{RF}/O_{RF}	RF circuit test pin	Hi-Z	—
39	ATEST3	I_A/O_A	IF and analog circuits test pin	Hi-Z	—
38	ATEST4	I_A/O_A		Hi-Z	—
Power supply pins (*4)					
48	VDD_RF	—	Power supply pin for LNA and DET (1.6 V typ.)	—	—
6	VDD_RFPLL	—	Power supply pin for RF PLL (1.6 V typ.)	—	—
3	VDD_VCO	—	Power supply pin for RF VCO (1.6 V typ.)	—	—
4	VDD_CP	—	Power supply pin for RF CP (1.6 V typ.)	—	—
36	VDD_IF	—	Power supply pin for IF and MOD (3.3 V typ.)	—	—
44	VDD_PADRV	—	Power supply pin for PA drivers (3.3 V typ.)	—	—
13	VDD_DPLL	—	Power supply pin for digital PLL (1.6 V typ.)	—	—
14	VDD_CORE	—	Power supply pin for digital CORE (1.6 V typ.)	—	—
24	VDD_IO	—	Power supply pin for digital IO (3.3 V typ.)	—	—
18	GND_IO	—	Ground pin for digital IO	—	—
Ground on the package rear side					
—	GND	—	Ground for the analog section and digital core section (on the rear side)	—	—

*1 I/O definition

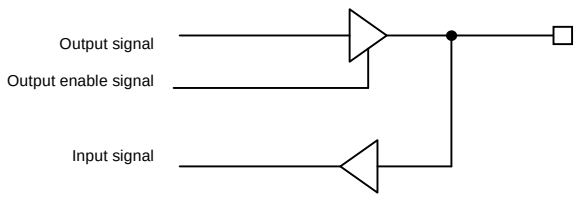
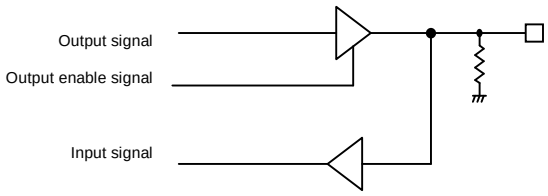
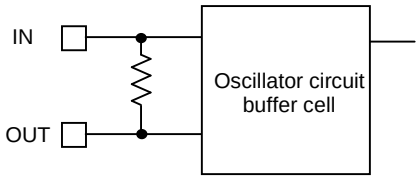
I_{RF}	:	RF input pin
I_A	:	Analog input pin
I	:	Digital input pin
I_D	:	Pulled-down digital input pin
I_{OS}	:	Oscillator circuit input pin
O_{RF}	:	RF control output pin
O_A	:	Analog output pin
O	:	Digital output pin
O_{OS}	:	Oscillator circuit output pin

*2 Do not stop the 16 MHz input while the ML9636 is operating.
*3 Since TX_CI serves as the reference clock of the digital circuits, do not stop it all the time.
*4 The 3.3 V supply should be used for VDD_IO, VDD_IF, and VDD_PADRV and the 1.6 V supply for VDD_RF, VDD_VCO, VDD_CP, VDD_RFPLL, VDD_DPLL, and VDD_CORE.
Never leave the power supply pins or the GND pins open.
The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.

1.3.3 Pin Structure

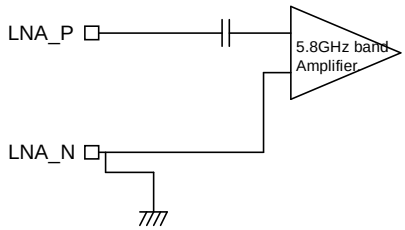
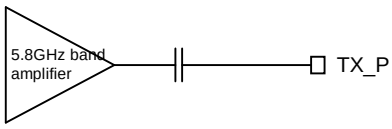
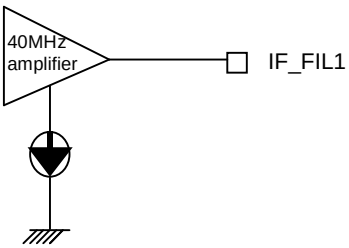
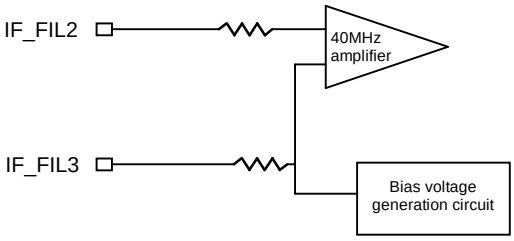
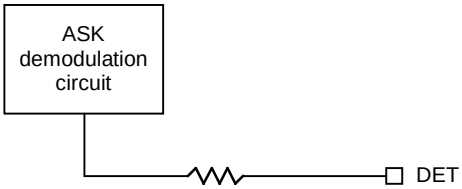
Tables 1-2, 1-3, 1-4, and 1-5 show the simplified pin structures that this IC has.

Table 1-2 Pin Structure (1 of 4)

Type	Symbol	Pin structure
Input pin/Output pin	RX_ASKDO, RX_ASKCO, RX_QDO, RX_QCO, CAR_DET, TX_DI, TX_CI, TXW_N, MOD_AQ, RESET_N, LOCK_DET, SDIN, SDO, SCLK, SINT, SCEN	 Input/output pin
Input/output pin with pull-down resistor	DTEST1, DTEST2	 Input/output pin with pull-down resistor
Oscillator pin	OSCIN, OSCOUT	 Oscillator pins

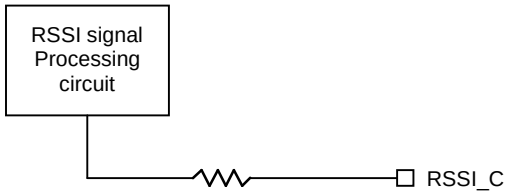
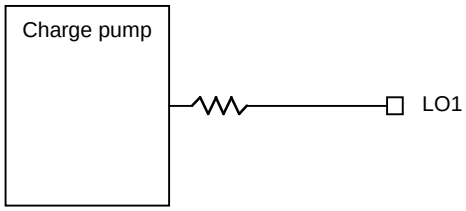
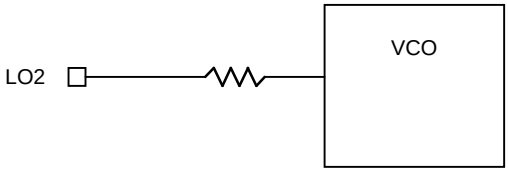
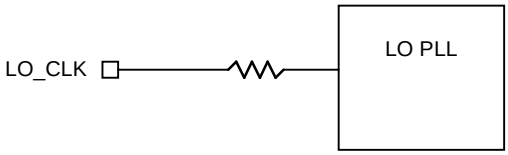
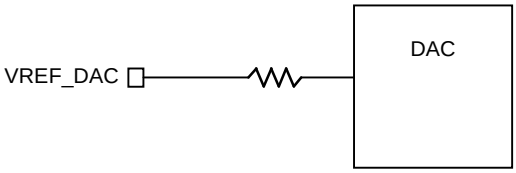
* The input protection circuits are not shown in the figures above.

Table 1-3 Pin Structure (2 of 4)

Type	Symbol	Pin structure
RF pin	LNA_P, LNA_N	
RF pin	TX_P	
Analog pin	IF_FIL1	
Analog pin	IF_FIL2, IF_FIL3	
Analog pin	DET	

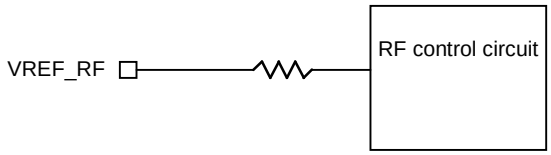
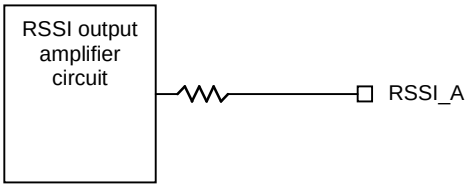
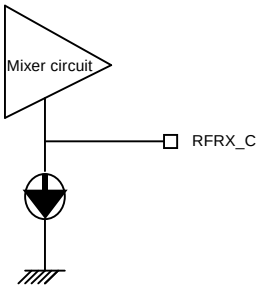
* The input protection circuits are not shown in the figures above.

Table 1-4 Pin Structure (3 of 4)

Type	Symbol	Pin structure
Analog pin	RSSI_C	
Analog pin	LO1	
Analog pin	LO2	
Analog pin	LO_CLK	
Reference pin	VREF_DAC	

* The input protection circuits are not shown in the figures above.

Table 1-5 Pin Structure (4 of 4)

Type	Symbol	Pin structure
Reference pin	VREF_RF	
Analog pin	RSSI_A	
Analog pin	RFRX_C	

* The input protection circuits are not shown in the figures above.

1.3.4 Handling of Unused Pins

Table 1-6 shows how unused pins of this IC should be handled. Be sure to connect the other input pins than shown below to appropriate signal lines according to their use.

Table 1-6 Handling of Unused Pins

Pin	If unused, connect to:
DTEST1	GND
DTEST2	GND
ATEST1	Open
ATEST3	Open
ATEST4	Open

Notes:
- When left open, a digital input pin may carry an excessive supply current.
- Never leave power supply pins or GND pins open.
  The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.

2. MODEM Function

2.1 DEMOD Interface (RX) Function

2.1.1 QPSK Demodulation Function

The QPSK demodulation section demodulates the QPSK signal and regenerates clocks. Figure 2-1 shows the data and clock waveform during normal output for the QPSK demodulation function. The QPSK demodulation performs modulation in units of symbols and, as shown in the figure below, produces a 2-bit output at 2.048 MHz for normal output.
When no carrier signal is detected (CAR_DET = "L"), data and clock outputs go "L." This masking function can be disabled using a register setting command SET_DEMOD_SET.
While the IC is transmitting TX data, demodulation data and clock outputs stop and go "L."

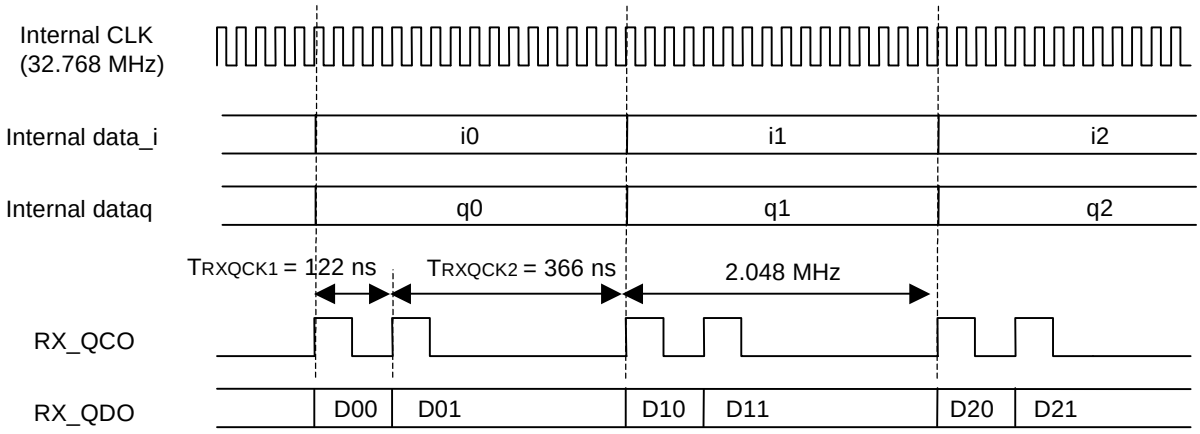


Figure 2-1 QPSK Demodulation Data and Data Clock Timings

The QPSK demodulation section of the IC has a function to pull in frequency synchronously. At synchronous pulling-in or at detection of a frequency drift compared with the roadside unit, timing adjustment is performed; therefore, the output clock (RX_QCO) may change.

Figure 2-2 shows the output timing waveforms when a frequency drift is the largest in cases where timing adjustment occurs backwards (upper diagram) and timing adjustment occurs forwards (lower diagram).
The output width of the 2nd bit of the one symbol that is demodulated is normally 366 ns, as shown in Figure 2-1; however, if timing adjustment occurs, the width is a value between a maximum of 611 ns (see the upper diagram of Figure 2-2) and a minimum of 122 ns (see the lower diagram of Figure 2-2).

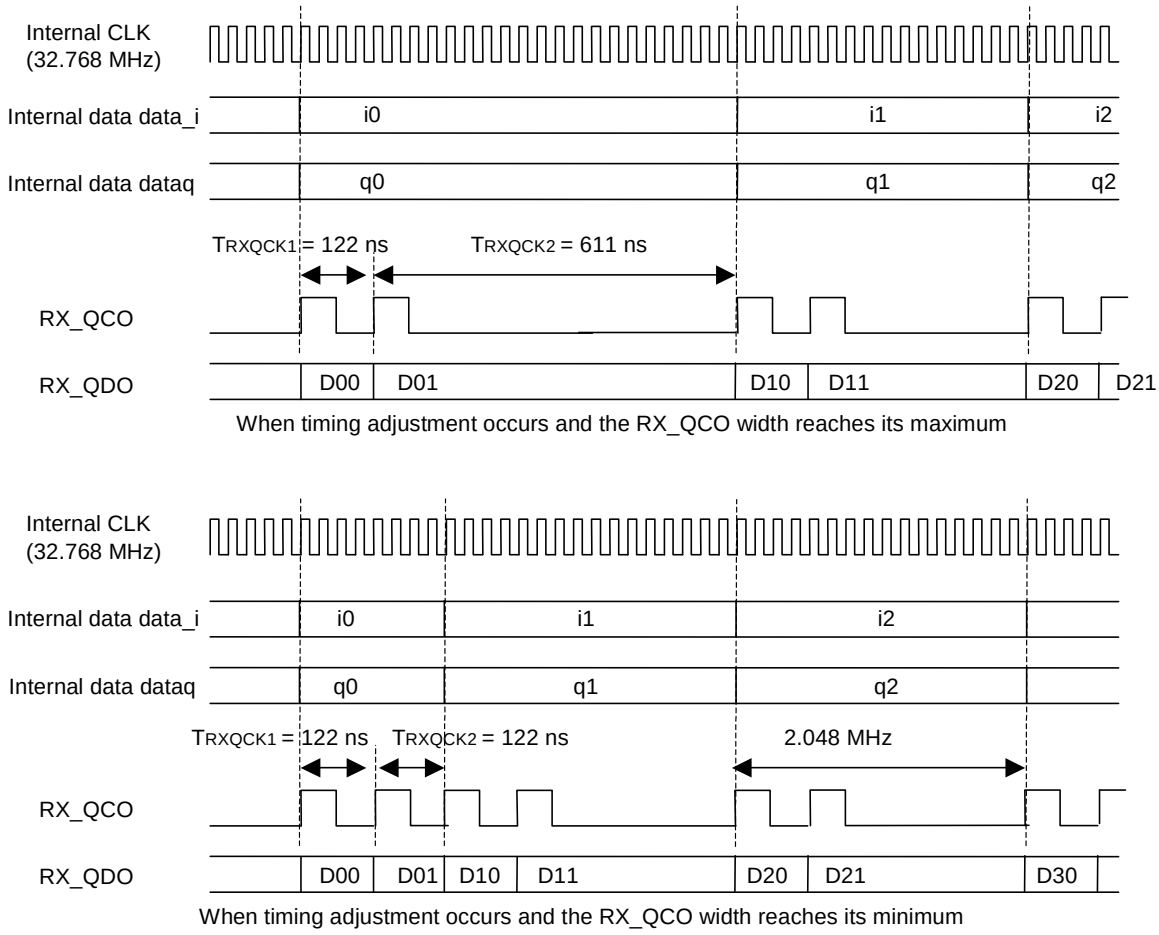


Figure 2-2 Timing Adjustment at Synchronous Pulling-In

2.1.2 ASK Demodulation Function

The ASK demodulation section has a decryption function for split phase of 1024kbps and a clock recovery function and outputs a 1.024 MHz clock.
In the clock recovery function, timing adjustment is performed at synchronous pulling-in or at detection of a frequency drift compared with roadside unit; therefore, the output clock (RX_ASKCO) may change.
When no carrier signal is detected (CAR_DET = "L"), data and clock outputs go "L." This masking function can be disabled using a register setting command SET_DEMOD_SET.
While the IC is transmitting TX data, demodulation data and clock outputs stop and go "L."
In addition, the ASK demodulation function can be disabled using a register setting command SET_DEMOD_SET. In this case, no split phase will be decrypted, nor will clock (ASK_CO) be output; only data (ASK_DO) will be output.

2.2 MODEM Interface (TX) Function

This IC performs ASK modulation and π/4 shift QPSK modulation as transmission (TX side) functions. Switching between ASK and QPSK is made by the MOD_AQ signal sent from the baseband LSI (BB LSI).
The TX_CI clock input has a frequency of 4.096 MHz bon in QPSK mode and in ASK mode. Since the TX_CI clock serves as the reference clock of the digital processing section of the IC, do not stop clock input even during the period other than during transmission.
Figure 2-3 shows the relationship between the timing signal generating circuit and the blocks to be controlled during transmission.
The RF signal transmission is triggered by the TXW_N signal from the BB LSI. Note that it must be done from the BB LSI to switch between transmission and reception at the external ANT SW or have on-off control of the external PA.

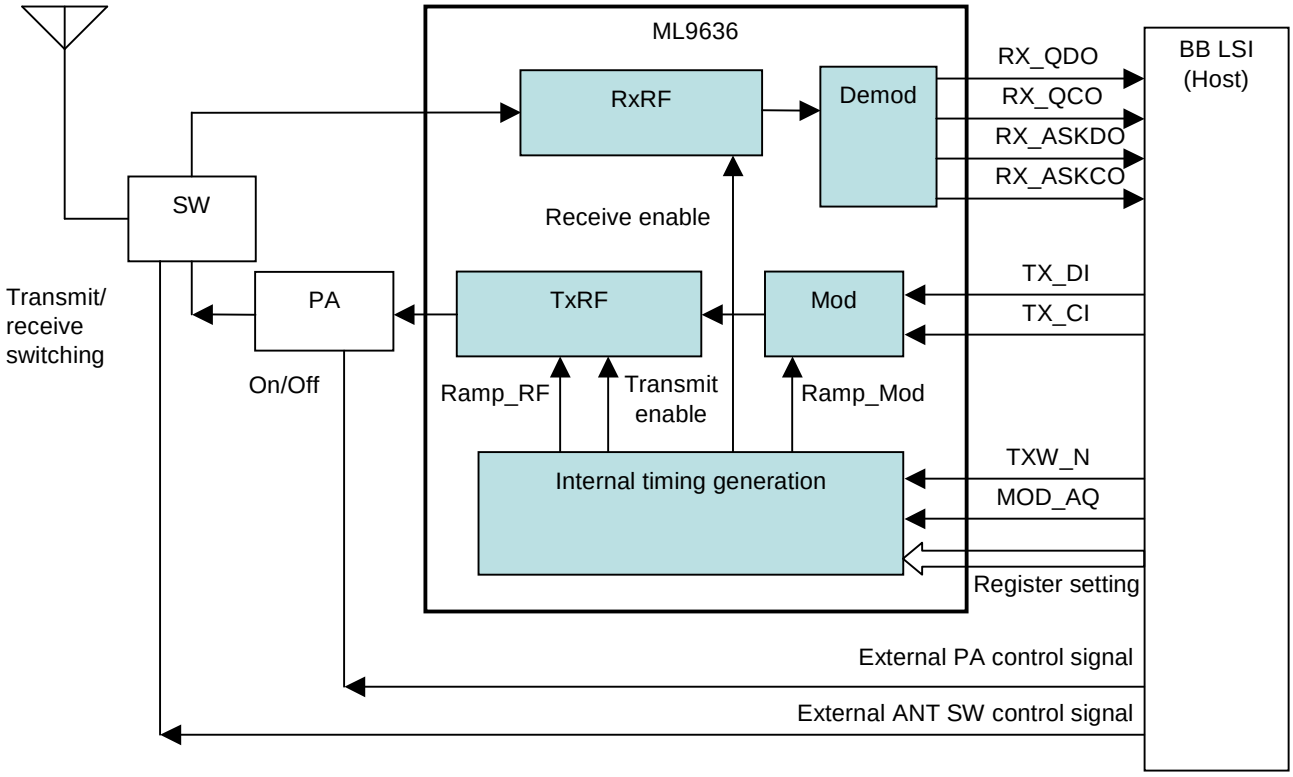


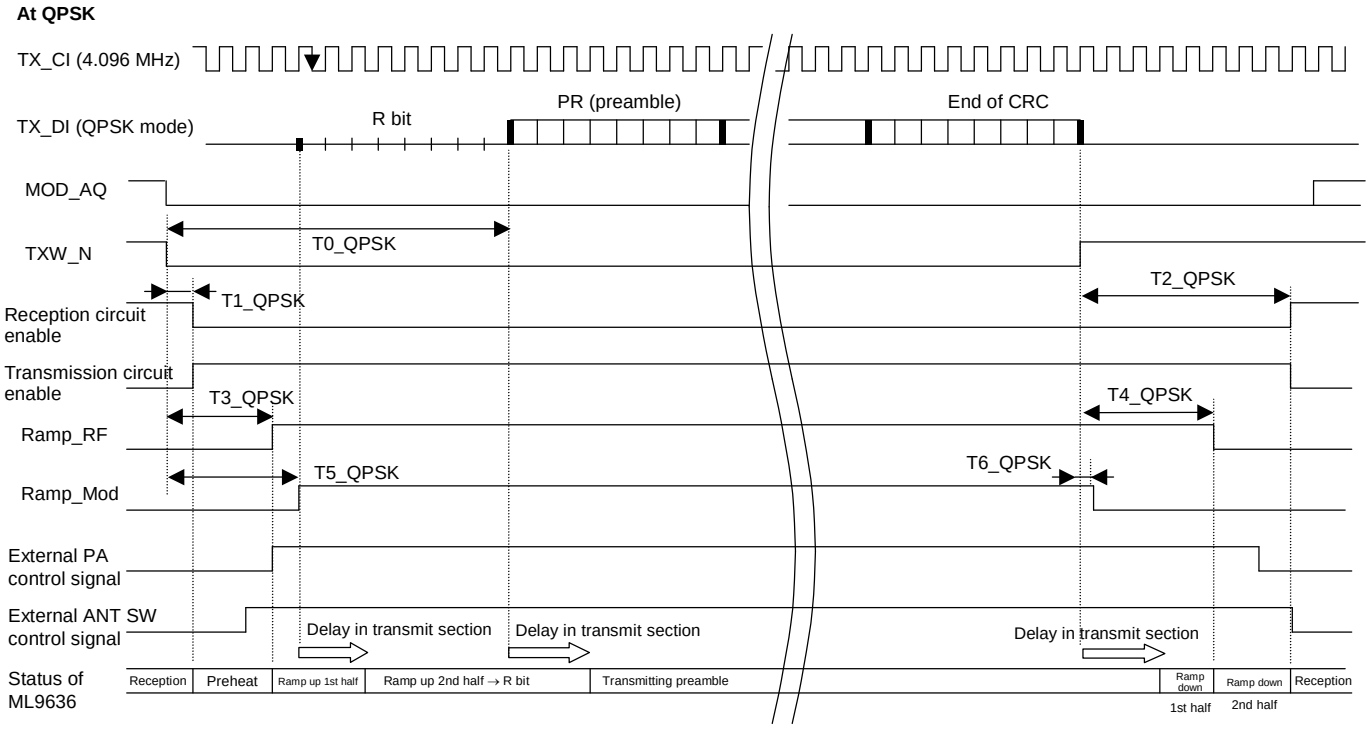
Figure 2-3 Block Diagram of Timing Control Function at Transmission

The following timing diagrams shows the relationships between the data/clock during data transmission, the transmit/receive circuit enable signal (on-off signal), the Ramp_RF signal, and the Ramp_Mod signal in the respective cases of ASK mode and QPSK mode.

As the clock to be input, a 4.096 MHz clock is used both in QPSK mode and in ASK mode. When in QPSK mode, the data to be input is the QPSK mode data at 4.096 Mbps; when in ASK mode, the data to be input is the data at 1.024 Mbps before split-phase coding. In ASK mode, the boundary of ASK data at 1.024 Mbps is identified by the TXW_N signal falling edge timing. Then the "Mod" circuit performs the split phase coding of 1.024Mbps.

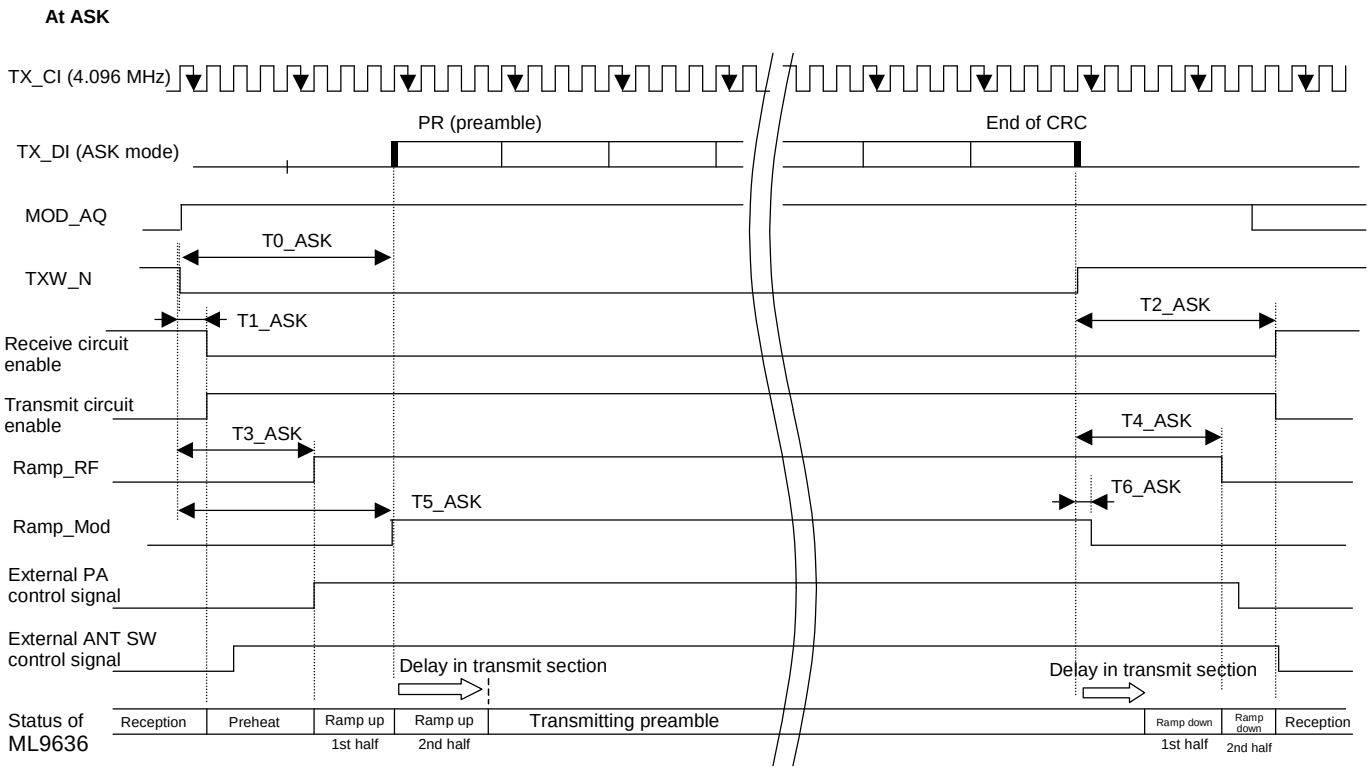
It is necessary for the BB LSI to enable the TXW_N signal prior to the transmit channel data. It is also necessary for the BB LSI to be provided with a setting function that can change the TXW_N enable timing with respect to transmit channel data. It is recommended that the variable values (T0_QPSK, T0_ASK) for antecedent output be set to 0 to 255 cycles (approx. 0 to 62 μs) at an equivalent clock frequency of 4.096 MHz.
The TXW_N signal disabling timing is the end of the CRC bit of the TX_DI transmit channel data.

This IC generates timing for internal control signals (transmit/receive enable, Ramp_RF, and Ramp_Mod) based on the TXW_N signal. So, the user needs to configure the settings for appropriate internal registers.
Fix the MOD_AQ signal at the same time as, or before, the assertion of the TXW_N signal. The MOD_AQ signal is only fetched at the first cycle during which the TXW_N signal is asserted, and no decision between ASK and QPSK is made in any other timing.
Because the R bit in QPSK mode is added before the input data from TX_DI, fix TX_DI to "L" during the R bit addition timing . Hold the TX_DI input "L" also after CRC is finished.



* A value of 0 to 255 cycles (approx. 62 μs) at an equivalent clock frequency of 4.096 MHz can be set in each of T1_QPSK, T3_QPSK, and T5_QPSK.
* A value of 0 to 63 cycles (approx. 16 μs) at an equivalent clock frequency of 4.096 MHz can be set in each of T2_QPSK, T4_QPSK, and T6_QPSK.
* T0_QPSK is set on the BB LSI side.
* The external PA control signal and the external ANT SW control signal are controlled from the BB LSI.

Figure 2-4 Transmit Timing Diagram in QPSK Mode



* A value of 0 to 255 cycles (approx. 62 μs) at an equivalent clock frequency of 4.096 MHz can be set in each of T1_ASK, T3_ASK, and T5_ASK.
* A value of 0 to 63 cycles (approx. 16 μs) at an equivalent clock frequency of 4.096 MHz can be set in each of T2_ASK, T4_ASK, and T6_ASK.
* T0_ASK is set on the BB LSI side.
* The external PA control signal and the external ANT SW control signal are controlled from the BB LSI side.

Figure 2-5 Transmit Timing Diagram in ASK Mode

2.3 Test Signal Generation Test Function

This IC is equipped with a test pattern generating circuit. Figure 2-6 shows the configuration of the test pattern generating circuit.

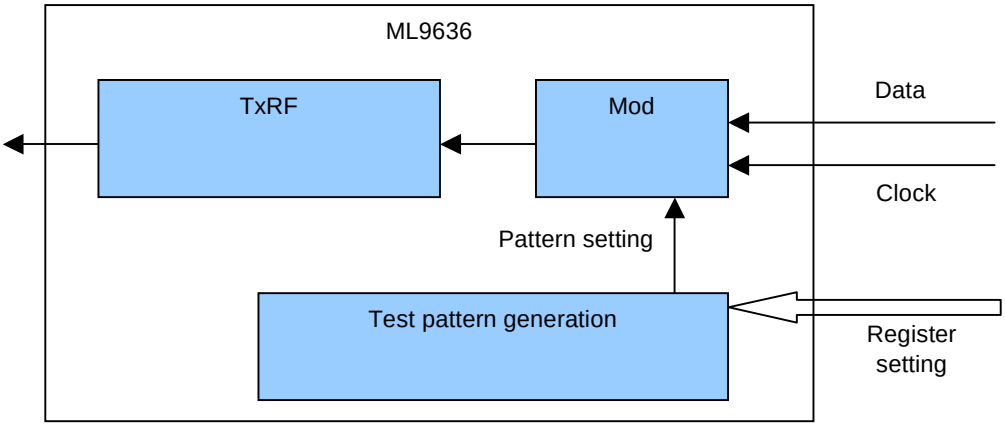


Figure 2-6 Configuration of the Test Pattern Generating Circuit

Table 2-1 lists the patterns that can be generated.
Each test pattern is transmitted by first writing a value for the test pattern to the register of the test command (SET_TEST_SEND) and then setting TXW_N = "L" with a clock being input to TX_CI.

Table 2-1 Test Patterns That Can Be Generated

Pattern	Description
CW0	Transmits an ASK carrier-off level equivalent continuous wave. If QPSK mode is selected (MOD_AQ = "L"), the neutral data (origin) signal of QPSK is transmitted.
CW1	Transmits an ASK carrier-on level equivalent continuous wave. If QPSK mode is selected (MOD_AQ = "L"), the neutral data (origin) signal of QPSK is transmitted.
PN15	Transmits a random pattern (PN15) continuously. The data to be transmitted in ASK mode is the data after split phase coding. X15+X14+1 is used as the generating polynomial, and an inverted value is output.

3. Synchronous Communication Interface (SCI) Function

The ML9636 is equipped with a synchronous communication interface (SCI) as an interface with the host.

3.1 Clock Timing

The SCI that the ML9636 has is for slave use only, and input clocks from the host are applied to rising edges only. Only MSB first is supported for transmit/receive data.

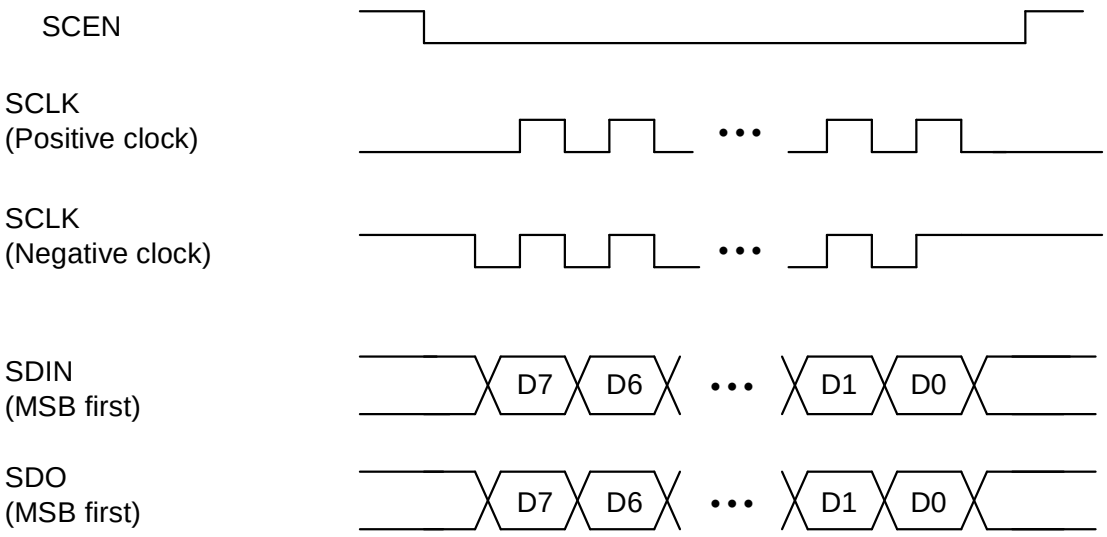


Figure 3-1 SCI Clocks and Data Transmit/Receive Waveforms

3.2 Data Format

Figure 3-2 shows the transfer data format.
Transfer data consists of request or status byte, command byte, and data byte(s). The number of data bytes is either one or two depending on the command.
The types of commands are: SET commands to set registers, GET_request and GET_confirm commands to read registers, and SET_confirm command that is returned from the ML9636 if a SET command error occurs.
To configure settings from the host to the ML9636, write setting values using the SET command. To read from the host into the ML9636, send the GET_request command from the host, and the ML9636 will assert SINT and returns the corresponding GET_confirm command and the read value if set to output enable for reading from the host. If a SET command error is detected, the ML9636 asserts SINT and, if set to output enable for reading from the host, returns the SET_confirm command.

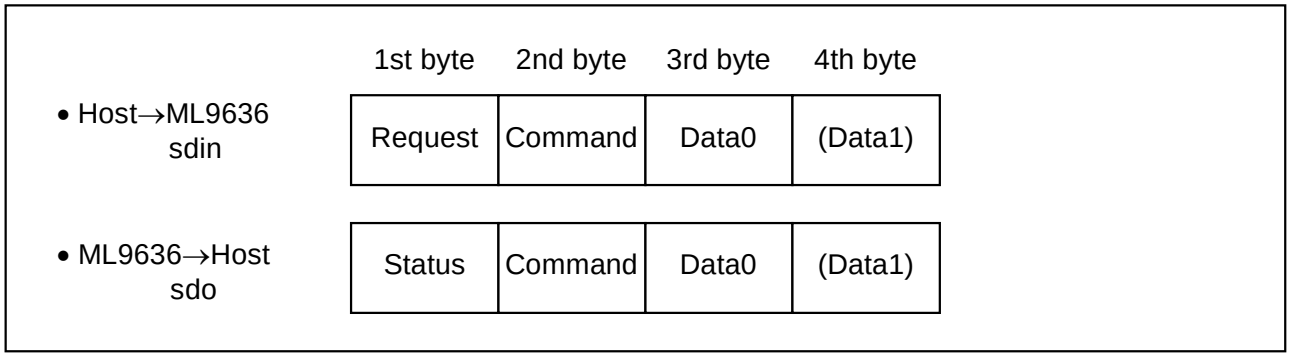


Figure 3-2 Transfer Data Format

3.2.1 Transaction

The request is exchanged with the status between the host and the ML9636 at the first trasnfer byte. If host →ML9636 or ML9636→host or both are feasible, data transfer for the second byte onwards is carrired out.
Use the SET command to write a setting value to the ML9636 and the GET command to read the set value from it.

3.2.2 Request/Status Byte

The host sends a request to the ML9636 and at the same time, the ML9636 sends the status to the host. For the request and status, only bits 3 and 2 out of the eight bits (bits 7–0) are used (positive logic) and the other bits are Don't Care, as shown below. When the bits at the same bit position in the request and status transmitted from the host and the ML9636 are both in the "1" state, a handshaking between the host and the ML9636 is established and data transmission/reception for the second bytes onwards starts.
In the actual ML9636 status output, "0x0C"(both bits 3 and 2 are "1") is always returned to the host in order to support read and write to the host at the same time.

Bit	Request (Host→ML9636)	Status (ML9636→Host)
3	Setup data write request	Setup data write enable
	Setup data read request	Setup data read enable
2	Confirm enable	Confirm request

3.2.3 Command Byte and Data Bytes

There exist commands and data that accompanies them. For the details of each command, refer to "A Separate Volume for the ML9636 User's Manual Command Details."

3.2.4 Timing Diagram

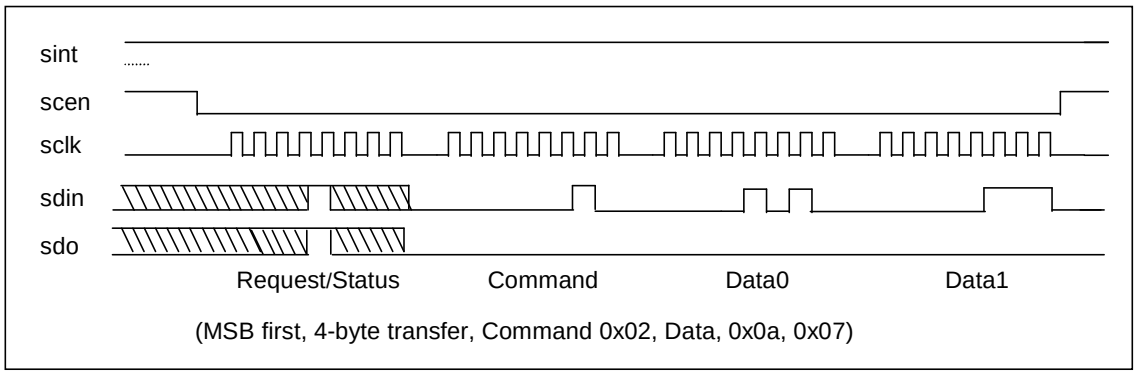
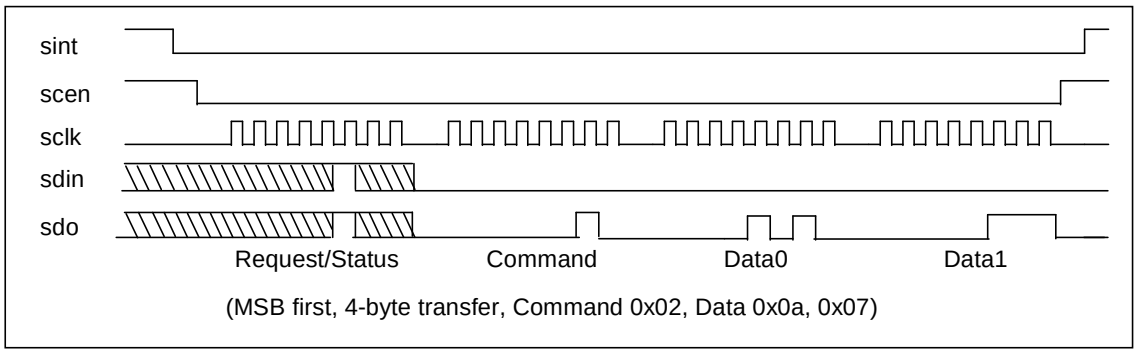


Figure 3-3 Host→ML9636 Data Write (SET command)



* Do not negate (scen="H") scen during transfer. If it is negated, the transfer data is invalid.
* The interrupt (sint) changes only when scen is "H".
* When only a write operation is performed after interrupt occurrence, the ML9636 first negates sint and then asserts sint again.

Figure 3-4 ML9636→Host Data Read (GET command)

3.3 Setting Write Data

Use the SET command to write a setting value from the host to the ML9636.
Register setting to the ML9636 can be achieved by setting bit 3 of byte 1 to "1" and writing a setting value to byte 2 onwards using the SET command and sending the data to the ML9636 from the host.
The internal register update timing varies depending on whether the length of the setting data is two bytes or one byte. If the length of setting data is two bytes, the update timing for DATA0 is hundreds of nanoseconds after the first rising edge of SCLK of the subsequent DATA1 transmission, and the update timing for DATA1 is hundreds of nanoseconds after the SCLK rising edge at the eighth bit of DATA1. Meanwhile, if the length of the setting data is one byte, the update timing is hundreds of nanoseconds after the SCLK rising edge at the eighth bit of DATA0. Figures 3-5 and 3-6 shows the outlines of update timing.

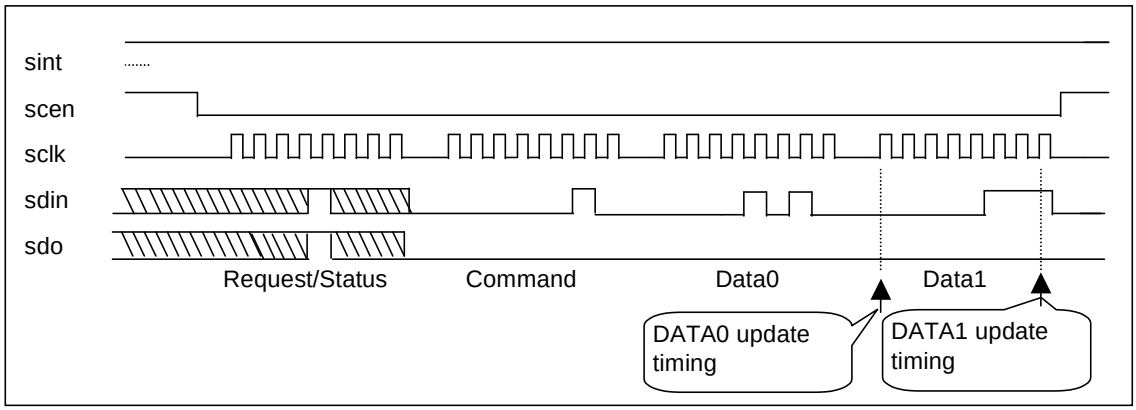


Figure 3-5 Data Write Timing (Setting Data: 2 Bytes)

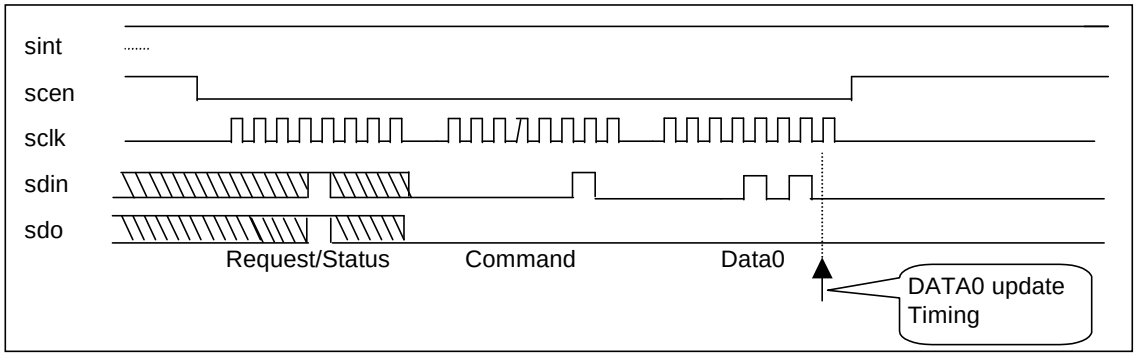


Figure 3-6 Data Write Timing (Setting Data: 1 Byte)

If a data write is not carried out correctly, the ML9636 asserts the SINT signal and notifies the host of a write error.
When SINT has been asserted, the command at the error occurrence and the error contents will be output from the ML9636 by setting the request byte (first tranfer byte) to "Confirm enable" (set bit 2 to "1") from the host. (Reading by a SET_confirm command.)
The command at the error occurrence to be output is displayed as a value (command) of the target SET command incremented by 1.
When reading of the error state is completed, the SINT signal is negated.
If reading by a SET_confirm command is not executed upon the assertion of SINT, SINT is left asserted. So, be sure to execute a SET_confirm command read.

At a read by a SET_confirm

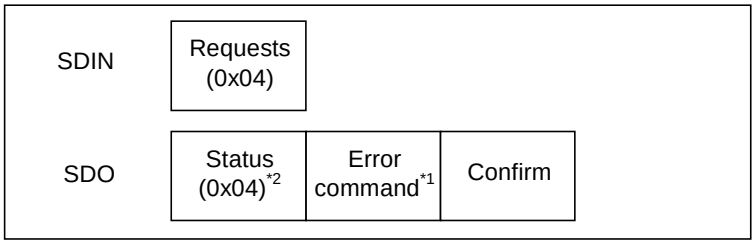


Figure 3-7 SET_Confirm Data Format

*1 The command at an error occurrence is output as a value (command) of the target SET command incremented by 1.

*2 In the actual ML9636 status output, "0x0C" is always returned in order to support read and write to the host at the same time.

[Details of Confirm]

Contents	Data	Description
UNSUPPORTED_ATTRIBUTE	0x0A	Error occurred that indicates set data being too short.

The conditions for causing incorrect writing and the possible resultant operations are shown below.

Command conditions	SCEN negate timing	Operation
All SET commands	When SCEN is negated before completion of transmission up to the Command data	The command fails. Operates normally at the next command and onwards.
	When SCEN is negated after completion of transmission up to the Command data	For a SET command, the data write ends in failure and the ML9636 asserts SINT. After that, when a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT.
Commands where the number of data bytes to be set is 1	When SCEN is negated before the SCLK rising edge at the eighth bit 8	Since the data write fails, the internal register is not updated. The ML9636 asserts SINT and notifies the host of the write error. When a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT.
	When SCEN is negated immediately after the SCLK rising edge at the eighth bit (when SCEN is negated without observing the interface regulations)	If the data write fails, the ML9636 asserts SINT and notifies the host of the write error. When a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT. If SINT is not asserted, it indicates that the data write has succeeded. However, whether the set value is correct is not guaranteed.
	When the number of SCLK clock pulses is larger than the number prescribed for the command	The data write succeeds and setting in the register is performed normally. The excessive clocks and data are ignored.

Command conditions	SCEN negate timing	Operation
Commands where the number of data bytes to be set is 2	When SCEN is negated before the SCLK rising edge at the first bit in the second byte (DATA1)	Since the data write fails, the internal register is not updated. The ML9636 asserts SINT and notifies the host of the write error. When a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT.
	When, although transmission was done normally up to the first bit (SCLK rising edge) in the second byte (DATA1), SCEN is negated before the transmission of the eighth bit (SCLK rising edge) in the second byte	Writing of the data (DATA0) at the first byte is effected and DATA0 is updated. However, DATA1 is not updated, because writing of the data at the second byte ends in failure. The ML9636 asserts SINT and notifies the host of the write error. When a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT.
	When SCEN is negated immediately after the SCLK rising edge at the eighth bit 8 (when SCEN is negated without observing the interface regulations)	If the data write fails, the ML9636 asserts SINT and notifies the host of the write error. In this case, the data (DATA0) at the first byte is updated but the data (DATA1) at the second byte is not. When a read request is received, the ML9636 sends the command(*1) at the error occurrence and the error contents and negates SINT. If SINT is not asserted, it indicates that the data write has succeeded. However, whether the DATA1 set value is correct is not guaranteed.
	When the number of SCLK clocks is larger than the number prescribed for the command	The data write succeeds and the register is set normally. The excessive clocks and data are ignored.

*1 The command at an error occurrence is output as a value (command) of the target SET command incremented by 1.

3.4 Reading Set Data

For the host to read set values in the ML9636, use a GET command.
By setting bit 3 of the first byte to "1" and transmitting a GET_request command at the second byte, the ML9636 prepares for a read. When the ML9636 completes the preparation, it asserts the SINT signal. It takes several microseconds after the negation of SCEN to assert SINT. The host must confirm that the SINT signal has been asserted and then execute the read request (read output enable).
Figure 3-8 shows the timing diagram for read. A simultaneous operation of a read and a write is also possible. Figure 3-9 shows the timing diagram when performing a read and a write simultaneously.

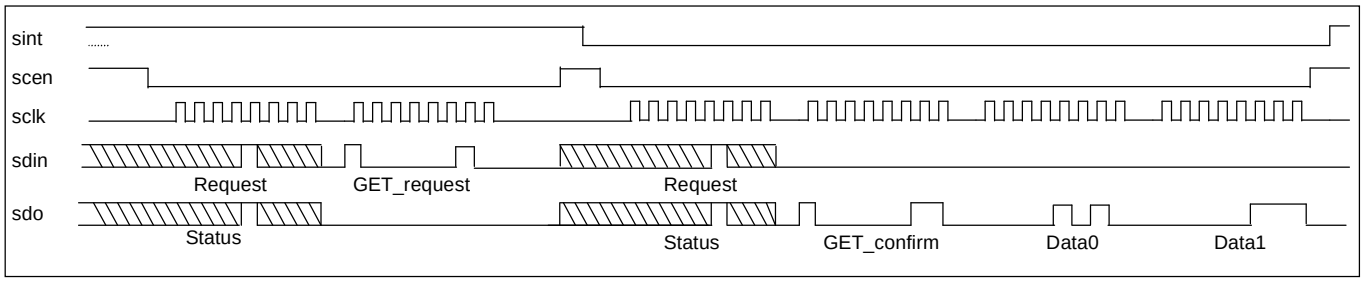


Figure 3-8 Timing Diagram for Read

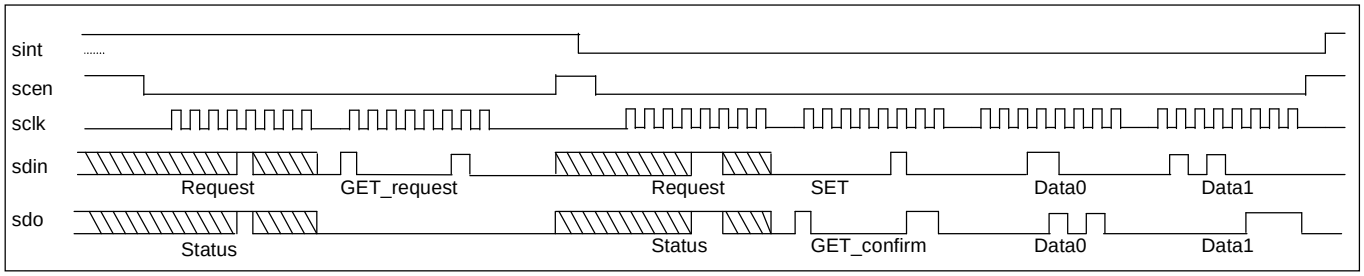


Figure 3-9 Timing Diagram for Read and Write (when read and write are simultaneously performed)

The conditions for causing incorrect reading and the possible resultant operations are shown below.

Command conditions	SCEN negate timing	Operation
GET commands	When SCEN is negated before completion of transmission up to the Command data	The command fails. Operates normally at the next command and onwards.
	When SCEN is negated after completion of transmission up to the Command data	In the case of a GET command, the ML9636 asserts SINT after completion of the preparation for a read.
	When SCEN is asserted before SINT is asserted after the GET_request command is transmitted	The GET_confirm command is not returned from the ML9636. SINT is asserted after SCEN is negated, thereby enabling the GET_confirm command to be read.
	When one GET_request command is transmitted and then another GET_request command is transmitted	The ML9636 can hold a maximum of two GET_request commands. Therefore, when the first read is executed, the GET_confirm command that corresponds to the first GET_request command is transmitted, and when the second read is executed, the GET_confirm command that corresponds to the second GET_request command is transmitted. If three or more GET_request commands are executed in succession, the GET_request command being held at the second time will be overwritten. When the reads are executed, the GET_confirm command that corresponds to the first GET_request command is transmitted, then the GET_confirm command that corresponds to the last GET_request command is transmitted.
	When the GET_request command is transmitted and then a SET command is executed without performing a read	SINT is once negated and the SET command is executed normally. When SCEN is negated after the SET command is executed, SINT is asserted again, thereby enabling a read.
	When SCEN is negated before all the GET_confirm command data is transmitted	SINT will be left asserted. If a read is performed again, the GET_confirm command is transmitted; however, the read data at that time is not guaranteed. Transmit the GET_request command again.

4. List of Commands

The following table lists the commands required for normal data transmission/reception. These commands can be input from the SCI interface.

Command (code)	Name	Description	Direction
0x02	SET_VCV_RAW	VCO calibration control setting	Host→ML9636
0x04	SET_FMAP	PLL counter setting	Host→ML9636
0x06	SET_HDAC_QPSK1	QPSK HDAC adjustment 1	Host→ML9636
0x08	SET_HDAC_QPSK2	QPSK HDAC adjustment 2	Host→ML9636
0x0A	SET_HDAC_ASK	ASK HDAC adjustment	Host→ML9636
0x0C	SET_TPC	Gain control for QPSK/ASK	Host→ML9636
0x0E	SET_RF_TMP	RF section adjustment (RF_TEMP)	Host→ML9636
0x10	SET_CAR_DET_LVL	Carrier detection level setting	Host→ML9636
0x12	SET_CAR_DET_CTL	Carrier detection hysteresis width adjustment	Host→ML9636
0x16	SET_RF0	RF section adjustment 0	Host→ML9636
0x18	SET_RF1	RF section adjustment 1	Host→ML9636
0x1A	SET_RF2	RF section adjustment 2	Host→ML9636
0x1C	SET_RF3	RF section adjustment 3	Host→ML9636
0x20	SET_DEMOD_SET	DEMOD section configuration	Host→ML9636
0x22	SET_TEST_SEND	Generation of test patterns for transmission	Host→ML9636
0x24	SET_TX_ON_ASK	TX ON/RX OFF timing adjustment (T1_ASK)	Host→ML9636
0x26	SET_TX_OFF_ASK	TX OFF/RX ON timing adjustment (T2_ASK)	Host→ML9636
0x28	SET_RAMP_RF_ON_ASK	RAMP RF ON timing adjustment (T3_ASK)	Host→ML9636
0x2A	SET_RAMP_RF_OFF_ASK	RAMP RF OFF timing adjustment (T4_ASK)	Host→ML9636
0x2C	SET_RAMP_MOD_ON_ASK	RAMP MOD ON timing adjustment (T5_ASK)	Host→ML9636
0x2E	SET_RAMP_MOD_OFF_ASK	RAMP MOD OFF timing adjustment (T6_ASK)	Host→ML9636
0x30	SET_TX_ON_QPSK	TX ON/RX OFF timing adjustment (T1_QPSK)	Host→ML9636
0x32	SET_TX_OFF_QPSK	TX OFF/RX ON timing adjustment (T2_QPSK)	Host→ML9636
0x34	SET_RAMP_RF_ON_QPSK	RAMP RF ON timing adjustment (T3_QPSK)	Host→ML9636
0x36	SET_RAMP_RF_OFF_QPSK	RAMP RF OFF timing adjustment (T4_QPSK)	Host→ML9636
0x38	SET_RAMP_MOD_ON_QPSK	RAMP MOD ON timing adjustment (T5_QPSK)	Host→ML9636
0x3A	SET_RAMP_MOD_OFF_QPSK	RAMP MOD OFF timing adjustment (T6_QPSK)	Host→ML9636
0x3C	SET_TEST_MODE	Test monitor mode setting	Host→ML9636
0x3E	SET_INITIAL	Initial setting	Host→ML9636
0x82	GET_VCV_RAW_request	VCO calibration results register read request	Host→ML9636
0x83	GET_VCV_RAW_confirm	VCO calibration results register read	ML9636→HOST
0x84	GET_FMAP_request	PLL counter settings read request	Host→ML9636
0x85	GET_FMAP_confirm	PLL counter settings read	ML9636→HOST
0x86	GET_HDAC_QPSK1_request	I ch DC offset and amplitude adjustment value read request	Host→ML9636
0x87	GET_HDAC_QPSK1_confirm	I ch DC offset and amplitude adjustment value read	ML9636→HOST
0x88	GET_HDAC_QPSK2_request	QchDC offset, amplitude, and phase adjustment value read request	Host→ML9636
0x89	GET_HDAC_QPSK2_confirm	QchDCoffset, amplitude, and phase adjustment value read	ML9636→HOST
0x8A	GET_HDAC_ASK_request	ASK DC offset and amplitude adjustment value read request	Host→ML9636
0x8B	GET_HDAC_ASK_confirm	ASK DC offset and amplitude adjustment value read	ML9636→HOST
0x8C	GET_TPC_request	QPSK/ASK gain control value read request	Host→ML9636
0x8D	GET_TPC_confirm	QPSK/ASK gain control value read	ML9636→HOST
0x8E	GET_RF_TMP_request	RF section adjustment value read request	Host→ML9636
0x8F	GET_RF_TMP_confirm	RF section adjustment value read	ML9636→HOST

Command (code)	Name	Description	Direction
0x90	GET_CAR_DET_LVL_request	Carrier detection level setting value read request	Host→ML9636
0x91	GET_CAR_DET_LVL_confirm	Carrier detection level setting value read	ML9636→HOST
0x92	GET_CAR_DET_CTL_request	Carrier detection hysteresis width adjustment value read request	Host→ML9636
0x93	GET_CAR_DET_CTL_confirm	Carrier detection hysteresis width adjustment value read	ML9636→HOST
0x94	GET_INIT_READ_request	This command is canceled	Host→ML9636
0x95	GET_INIT_READ_confirm	This command is canceled	ML9636→HOST
0x96	GET_RF0_request	RF section adjustment 0 value read request	Host→ML9636
0x97	GET_RF0_confirm	RF section adjustment 0 value read	ML9636→HOST
0x98	GET_RF1_request	RF section adjustment 1 value read request	Host→ML9636
0x99	GET_RF1_confirm	RF section adjustment 1 value read	ML9636→HOST
0x9A	GET_RF2_request	RF section adjustment 2 value read request	Host→ML9636
0x9B	GET_RF2_confirm	RF section adjustment 2 value read	ML9636→HOST
0x9C	GET_RF3_request	RF section adjustment 3 value read request	Host→ML9636
0x9D	GET_RF3_confirm	RF section adjustment 3 value read	ML9636→HOST
0xA0	GET_DEMOD_request	DEMOD section settings read request	Host→ML9636
0xA1	GET_DEMOD_confirm	DEMOD section settings read	ML9636→HOST
0xA2	GET_TEST_SEND_request	Read request for generation settings of test patterns for transmission	Host→ML9636
0xA3	GET_TEST_SEND_confirm	Read generation settings of test patterns for transmission	ML9636→HOST
0xA4	GET_TX_ON_ASK_request	TX ON/RX OFF timing value read request	Host→ML9636
0xA5	GET_TX_ON_ASK_confirm	TX ON/RX OFF timing value read	ML9636→HOST
0xA6	GET_TX_OFF_ASK_request	TX OFF/RX ON timing value read request	Host→ML9636
0xA7	GET_TX_OFF_ASK_confirm	TX OFF/RX ON timing value read	ML9636→HOST
0xA8	GET_RAMP_RF_ON_ASK_request	RAMP RF ON timing value read request	Host→ML9636
0xA9	GET_RAMP_RF_ON_ASK_confirm	RAMP RF ON timing value read	ML9636→HOST
0xAA	GET_RAMP_RF_OFF_ASK_request	RAMP RF OFF timing value read request	Host→ML9636
0xAB	GET_RAMP_RF_OFF_ASK_confirm	RAMP RF OFF timing value read	ML9636→HOST
0xAC	GET_RAMP_MOD_ON_ASK_request	RAMP MOD ON timing value read request	Host→ML9636
0xAD	GET_RAMP_MOD_ON_ASK_confirm	RAMP MOD ON timing value read	ML9636→HOST
0xAE	GET_RAMP_MOD_OFF_ASK_request	RAMP MOD OFF timing value read request	Host→ML9636
0xAF	GET_RAMP_MOD_OFF_ASK_confirm	RAMP MOD OFF timing value read	ML9636→HOST
0xB0	GET_TX_ON_QPSK_request	TX ON/RX OFF timing value read request	Host→ML9636
0xB1	GET_TX_ON_QPSK_confirm	TX ON/RX OFF timing value read	ML9636→HOST
0xB2	GET_TX_OFF_QPSK_request	TX OFF/RX ON timing value read request	Host→ML9636
0xB3	GET_TX_OFF_QPSK_confirm	TX OFF/RX ON timing value read	ML9636→HOST
0xB4	GET_RAMP_RF_ON_QPSK_request	RAMP RF ON timing value read request	Host→ML9636
0xB5	GET_RAMP_RF_ON_QPSK_confirm	RAMP RF ON timing value read	ML9636→HOST
0xB6	GET_RAMP_RF_OFF_QPSK_request	RAMP RF OFF timing value read request	Host→ML9636
0xB7	GET_RAMP_RF_OFF_QPSK_confirm	RAMP RF OFF timing value read	ML9636→HOST
0xB8	GET_RAMP_MOD_ON_QPSK_request	RAMP MOD ON timing value read request	Host→ML9636
0xB9	GET_RAMP_MOD_ON_QPSK_confirm	RAMP MOD ON timing value read	ML9636→HOST
0xBA	GET_RAMP_MOD_OFF_QPSK_request	RAMP MOD OFF timing value read request	Host→ML9636
0xBB	GET_RAMP_MOD_OFF_QPSK_confirm	RAMP MOD OFF timing value read	ML9636→HOST
0xBC	GET_TEST_MODE_request	Test monitor mode settings read request	Host→ML9636
0xBD	GET_TEST_MODE_confirm	Test monitor mode settings read	Host→ML9636
0xBE	GET_INITIAL_request	Initial settings read request	Host→ML9636
0xBF	GET_INITIAL_confirm	Initial settings read	Host→ML9636

Do not access any unimplemented command. If any unimplemented command is issued, the ML9636 neglects such a command.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Parameter		Symbol	Condition	Rating	Unit
Supply voltage (3.3 V)	(*1)	V_{DD3}	Ta = +25°C	–0.3 to +4.6	V
Supply voltage (1.6 V)	(*2)	V_{DD16}		–0.3 to +2.0	V
Digital pin voltage		V_D		–0.3 to V_{DD3}+0.3	V
3.3 V analog pin voltage	(*3)	V_{A3}		–0.3 to V_{DD3}+0.3	V
1.6 V analog pin voltage	(*4)	V_{A16}		–0.3 to V_{DD16}+0.3	V
RF pin RF signal level	(*5)	P_{RF}		+7	dBm
Digital output current		I_{DO}		–16 to +16	mA
Analog output current	(*6)	I_{AO}		–5 to +5	mA
Power dissipation		P_d		900	mW
Storage temperature		T_{stg}	—	–55 to +150	°C

*1: 3.3 V power supply pins:
V_{DD3}: VDD_IO = VDD_IF = VDD_PADRV
*2: 1.6 V power supply pins:
V_{DD16}: VDD_RF = VDD_VCO = VDD_CP = VDD_RFPLL = VDD_DPLL = VDD_CORE
*3: 3.3 V analog pins:
IF_FIL1, IF_FIL2, IF_FIL3, DET, RSSI_C, TX_P, RSSI_A, VREF_DAC, RFRX_C
*4: 1.5 V analog pins:
LNA_P, LNA_N, LO1, LO2, LO_CLK, OSCIN, OSCOUT, ATEST1, ATEST3, ATEST4, VREF_RF
*5: RF pins:
LNA_P, LNA_N, TX_P
*6: Analog output pin:
RSSI_A

5.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage (I/O)	V_{DDIO}	VDD_IO pin	3.15	3.3	3.45	V
Supply voltage (CORE)	V_{DDCORE}	VDD_CORE pin	1.5	1.6	1.65	V
Supply voltage (RF)	V_{DDRF}	VDD_RF = VDD_VCO = VDD_CP = VDD_RFPLL = VDD_DPLL = VREF_RF	1.5	1.6	1.65	V
Supply voltage (analog)	V_{DDRF3}	VDD_IF = VDD_PADRV	3.15	3.3	3.45	V
Operating temperature	Ta	—	–30	+25	+85	°C
RF synthesizer reference frequency deviation	F_{MCK1}	Input frequency: 16.000 MHz LO_CLK pin	–20	—	+20	ppm
RF 2nd LO crystal oscillator frequency deviation	F_{MCK2}	Input frequency: 31.808 MHz OSCIN and OSCOUT pins	–100	—	+100	ppm
Digital clock frequency deviation	F_{DCLK}	Input frequency: 4.096 MHz TX_CI pin	–100	—	+100	ppm
Digital clock duty ratio	D_{TX_CI}	TX_CI pin	45	50	55	%

5.3 DC Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}	(*2)(*3)	2.0	—	V_{DDIO} +0.3	V
	V_{IH2}	(*4) When inputting signals externally	1.2	—	V_{DDcore} +0.3	V
Low level input voltage	V_{IL}	(*2)(*3)	–0.3	—	0.8	V
	V_{IL2}	(*4) When inputting signals externally	–0.3	—	0.4	V
Input leakage current	I_{IH1}	VIH = V_{DDIO} (*2)	—	—	10	μA
	I_{IH2}	VIH = V_{DDIO} (*3)	10	—	200	μA
	I_{IH3}	VIH = 1.65 V (*4)		—	1.0	μA
	I_{IL1}	VIL = 0 V (*2)(*3)	–10	—	—	μA
	I_{IL2}	VIL = 0 V (*4)	–1.0	—	—	μA
High level output voltage	V_{OH}	IOH = –100 μA (*5)	V_{DDIO} –0.2	—	—	V
		IOH = –4 mA (*5)	2.4	—	—	V
Low level output voltage	V_{OL}	IOL = 100 μA (*5)	—	—	0.2	V
		IOL = 4 mA (*5)	—	—	0.4	V
Supply current (*1)	I_{DD1}	When receiving signals				
		3.3 V supply (50 pF loaded)	—	—	37	mA
		1.6 V supply	—	—	78	mA
	I_{DD2}	When transmitting signals (*6)				
		3.3 V supply (50 pF loaded)	—	—	37	mA
		1.6 V supply	—	—	58	mA

*1: The total current supplied to the 3.3 V supply pins (V_{DD3}: VDD_IO = VDD_IF = VDD_PADRV) and the 1.6 V supply pins (V_{DD16}: VDD_RF = VDD_VCO = VDD_CP = VDD_RFPLL = VDD_DPLL = VDD_CORE).
*2: The pin shown as I in the I/O column in the table in Section 1.3.2, "Pin Descriptions."
*3: The pin shown as I_D in the I/O column in the table in Section 1.3.2, "Pin Descriptions."
*4: The pin shown as I_{OS} in the I/O column in the table in Section 1.3.2, "Pin Descriptions."
*5: The pin shown as O in the I/O column in the table in Section 1.3.2, "Pin Descriptions."
*6: When –7 dBm is transmitted from the TX_P pin.

5.4 AC Characteristics

5.4.1 RF Characteristics

(V_{DD3} = 3.3 V, V_{DD16} = 1.6 V, Ta =25°C)

Parameter	Condition	Min.	Typ.	Max.	Unit
LO characteristics					
LO lock-up time		—	—	500	μs
Transmit characteristics (TX_P pin)					
Transmit PA driver output	When the maximum output is set	−7	—	—	dBm
	When the minimum output is set	—	—	−18	dBm
Transmit power control slope	Variation for one step of TPC command PA driver output: −7 to −18 dBm	0.7		2.5	dB
Center frequency tolerance	The RF synthesizer reference frequency should have an accuracy specified by the recommended operating condition.	−20	—	+20	ppm
Adjacent channel leakage power	ASK |f−fc| = 5 MHz PA driver output: −7 to −18 dBm	—	—	−36	dBc
	ASK |f−fc| = 10 MHz PA driver output: −7 to −18 dBm	—	—	−44	dBc
	QPSK |f−fc| = 5 MHz PA driver output: −7 to −18 dBm	—	—	−37	dBc
	QPSK |f−fc| = 10 MHz PA driver output: −7 to −18 dBm	—	—	−50	dBc
EVM	QPSK PA driver output: −7 to −18 dBm	—	6	—	%
Eye aperture ratio	ASK (time) PA driver output: −7 to −18 dBm	85	—	—	%
	ASK (amplitude) PA driver output: −7 to −18 dBm	85	—	—	%
Modulation index	ASK PA driver output: −7 to −18 dBm	0.82	—	—	—
Leakage power at carrier-off		—	—	−44	dBm
Spurious emission intensity	Image leakage, local harmonic components, and RF output harmonic components	—	—	−32	dBm
	Others	—	—	−44	dBm
Burst transmit transient response time	When the transmit power is ±1 dB of the final value	—	—	5	μs

Note: The values in the table show characteristics which are calibrated and compensated using external components and circuits specified by OKI.
Spurious emmision at transmissio needs to be attenuated using an external filter.

- Transmission frequencies (uplink)
  U7 5815 MHz, U6 5820 MHz, U5 5825 MHz, U4 5830 MHz,
  U1 5835 MHz, U3 5840 MHz, U2 5845 MHz

(V_{DD3} = 3.3 V, V_{DD16} = 1.6 V, Ta =25°C)

Parameter	Condition	Min.	Typ.	Max.	Unit
Receive characteristics (LNA_P and LNA_N pins)					
Receiver sensitivity	QPSK BER 1E-5 or less	—	−75	—	dBm
	ASK BER 1E-5 or less	—	−68	—	dBm
Maximum input level	QPSK BER 1E-5 or less	−25	—	—	dBm
	ASK BER 1E-5 or less	−33	—	—	dBm
RSSI_A output voltage 1	RF input: −73 dBm	—	0.8	—	V
RSSI_A output voltage 2	RF input: −33 dBm	—	2.2	—	V
RSSI detect rise time	Time taken for the RSSI output to reach ±1 dB of the final value after switching from transmssion to reception	—	—	30	μs
Upper limit of CarrierDet setting range	When the upper limit is set	−58	—	—	dBm
Lower limit of CarrierDet setting range	When the lower limit is set	—	—	−73	dBm
CarrierDet detect rise time	Time taken until CarrierDet is detected after switching from transmssion to reception	—	—	30	μs
Spurious emission level		—	—	−30	dBm

Note: The values in the table show characteristics which are calibrated and compensated using external components and circuits specified by OKI.

- Reception frequencies (downlink)
  D7 5775 MHz, D6 5780 MHz, D5 5785 MHz, D4 5790 MHz,
  D1 5795 MHz, D3 5800 MHz, D2 5805 MHz

5.4.2 Digital Characteristics

(1) Modulation/Demodulation Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
QPSK demodulation section receive delay time	T_{RQDLY}		2.0		μs	
ASK demodulation section receive delay time	T_{RADLY}		1.0		μs	ASK demodulation section used
			0.3		μs	ASK demodulation section skipped
QPSK modulation section transmit delay time	T_{TQDLY}		3.6		μs	
ASK modulation section transmit delay time	T_{TADLY}		3.2		μs	
QPSK demodulation section AFC characteristics		–25		+25	ppm	5.8 GHz-band frequency offset resistance
QPSK demodulation section clock recovery characteristics			32	48	Symbol	Synchronous pulling-in time

(2) MODEM RX QPSK Interface Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RX_QCO clock width 1	T_{RXQCK1}	Load capacitance C_L = 50 pF	—	122	—	ns
RX_QCO clock width 2	T_{RXQCK2}		122	366	611	ns
RX_QCO high pulse width	T_{WQCKH}		50	—	70	ns
RX_QCO low pulse width	T_{WQCKL}		50	—	—	ns
RX_QDO output delay time	T_{QDOD}		–15	—	+35	ns

Notes: All timings are measured at 20% and 80% of V_{DDIO}.
The DCLK clock frequency F_{DCLK} is 2400 Hz/4800 Hz.

(3) MODEM RX ASK Interface Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RX_ASKCO clock frequency	F_{RXACK}	Load capacitance C_L = 50 pF	—	1.024	—	MHz
RX_ASKCO high pulse width	T_{WACKH}		440	—	540	ns
RX_ASKCO high pulse width	T_{WACKL}		440	—	540	ns
RX_ASKDO output delay time	T_{ADOD}		–15	—	+35	ns

Notes: All timings are measured at 20% and 80% of V_{DDIO}.

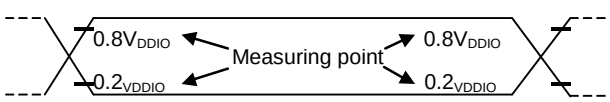
(4) MODEM TX Interface Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TX_CI clock frequency	F_{TXCK}	Load capacitance C_L = 50 pF		4.096		MHz
TX_DI input setup time	T_{TXDS}		15	—	—	ns
TX_DI input hold time	T_{TXDH}		15	—	—	ns

Notes: All timings are measured at 20% and 80% of V_{DDIO}.

Measuring Points:



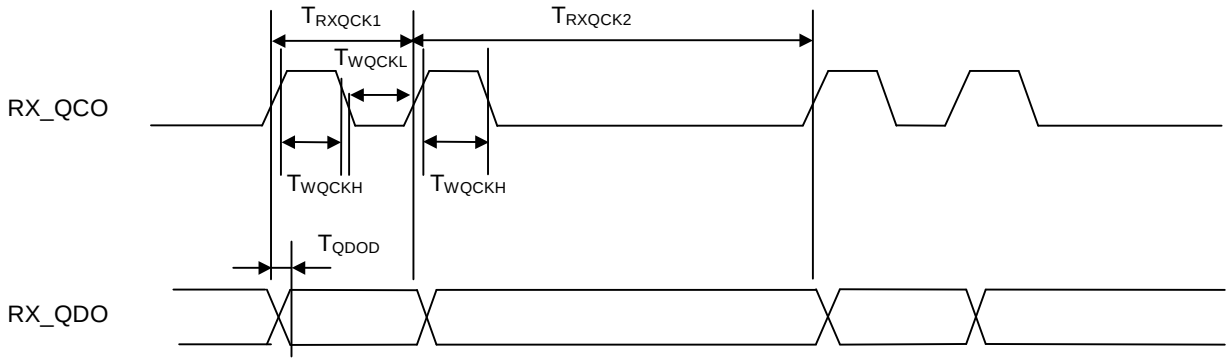


Figure 5-1 Timing Diagram of MODEM RX QPSK Interface

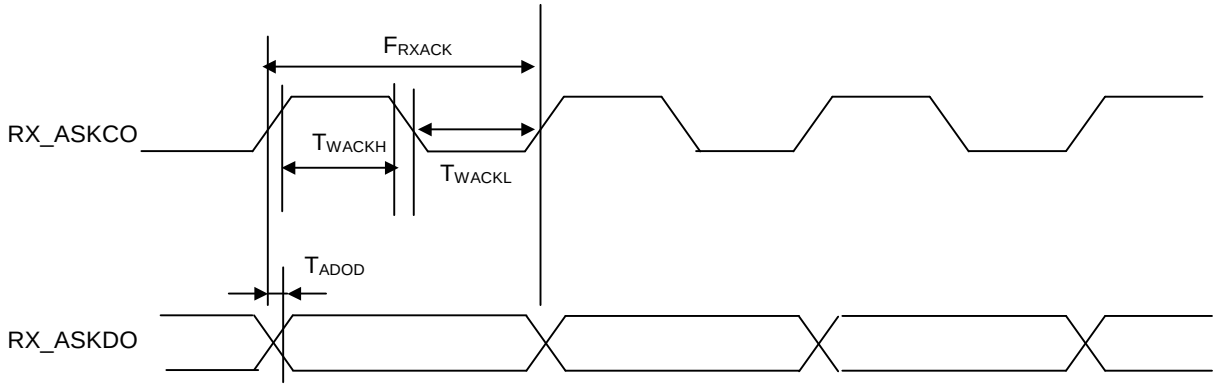
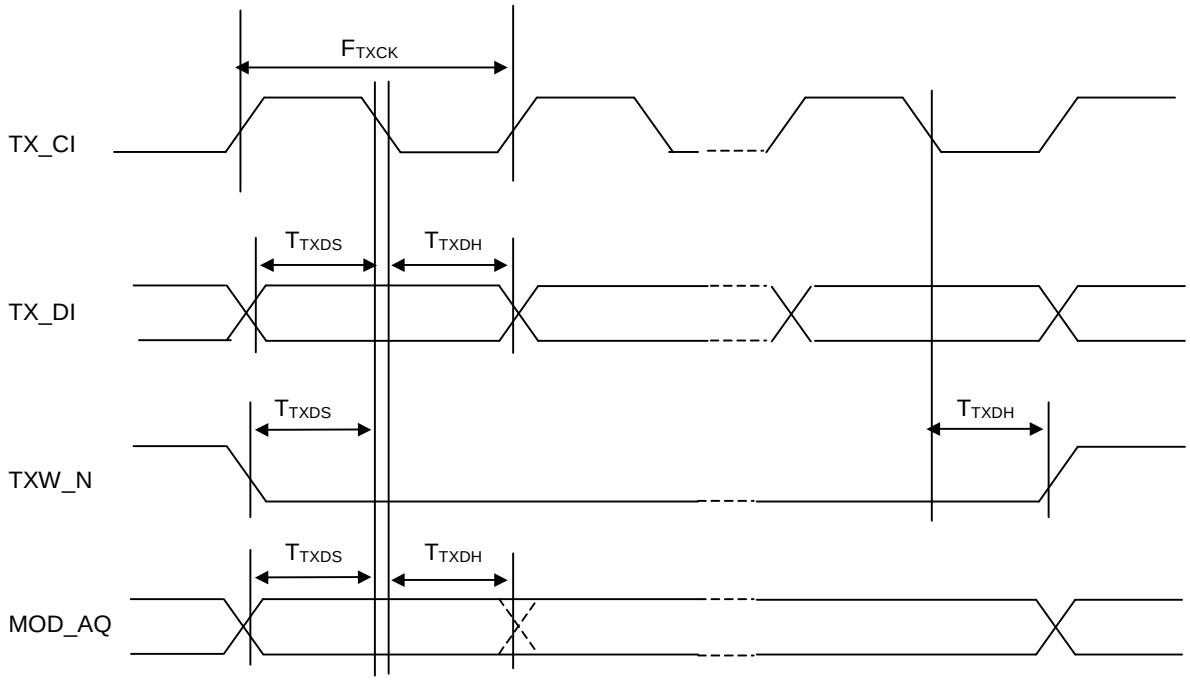


Figure 5-2 Timing Diagram of MODEM RX ASK Interface



Note:
Signals are fetched on the falling edge of the TX_CI signal at 4.096 MHz irrespective of QPSK or ASK mode.
The MOD_AQ signal is fetched only in the first cycle after the TXW_N signal goes "L".
Therefore, fix the MOD_AQ signal either at the same time as the fixation of the TXW_N signal or before that.
A change in the MOD_AQ signal level during transmission does not affect the transmission signal.

Figure 5-3 Timing Diagram of MODEM TX Interface

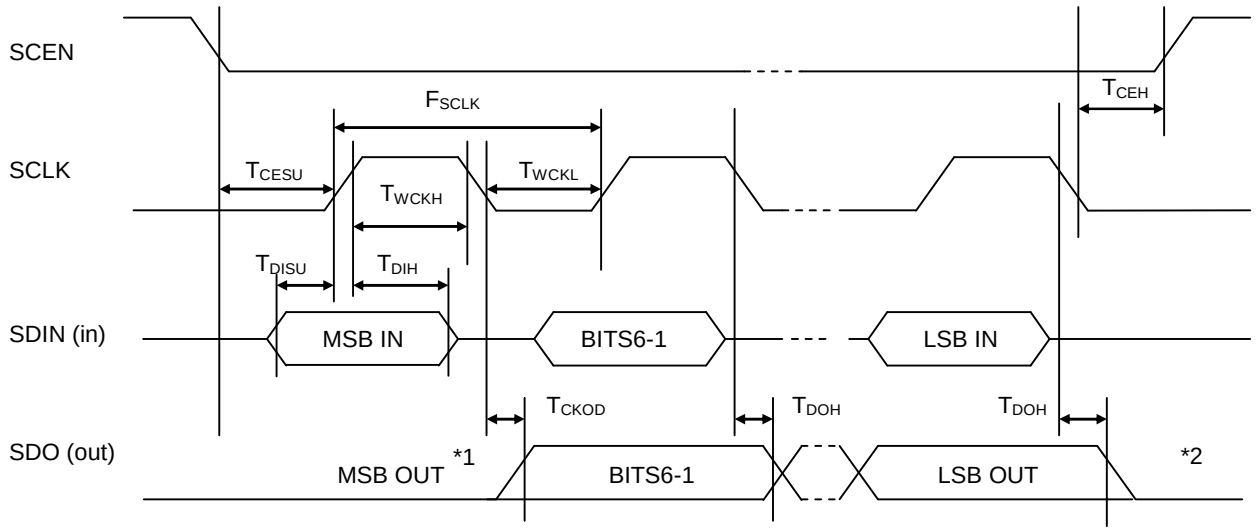
(5) Synchronous Communication Interface (SCI) Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
SCLK clock frequency	F_{SCLK}	Other than in a suspended state	Load capacitance C_L = 50 pF	0.1	2	4	MHz
SCEN input setup time	T_{CESU}			125	—	—	ns
SCEN input hold time	T_{CEH}			125	—	—	ns
SCLK high pulse width	T_{WCKH}			50	—	—	ns
SCLK high pulse width	T_{WCKL}			50	—	—	ns
SDIN input setup time	T_{DISU}			20	—	—	ns
SDIN input hold time	T_{DIH}			20	—	—	ns
Interval between one SCEN assert and the next	T_{CEITVL}			450	—	—	ns
SCLK output delay time	T_{CKOD}			—	—	40	ns
SDO output hold time	T_{DOH}			5	—	—	ns
SCEN enable time	T_{CEON}			0	—	—	ns
SINT disable time	$T_{SINTDIS}$			—	—	0.5	µs

Notes: All timings are measured at 20% and 80% of V_{DDIO}.

When SCLK is a positive clock

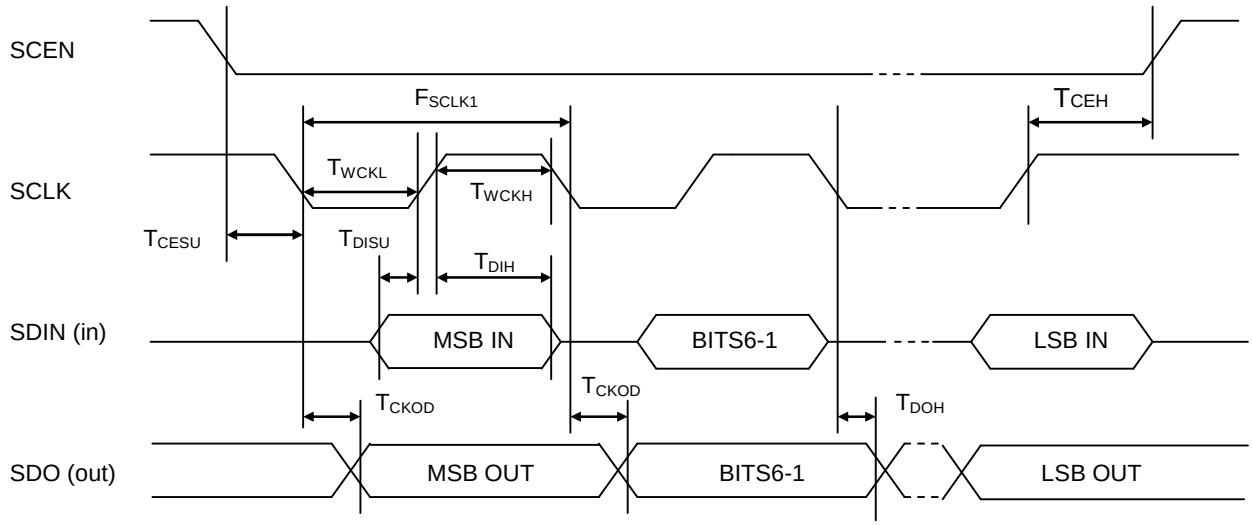


A rise/fall of the SINT pin occurs asynchronously with other clock synchronous serial interface related pins.

*1 "MSB OUT" bit is always low, because "MSB OUT" is a first bit of "status" byte. (Refer to section 3.2.2 and 3.2.4.)
*2 "SDO" goes low after "LSB OUT" output.

Figure 5-4 Timing Diagram of SCI Interface (Positive Clock)

When SCLK is a negative clock



A rise/fall of the SINT pin occurs asynchronously with other clock synchronous serial interface related pins.

Figure 5-5 Timing Diagram of SCI Interface (Negative Clock)

Interval between one SCEN assert and the next

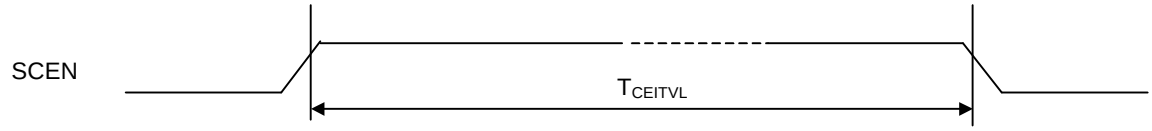


Figure 5-6 Timing Diagram of SCEN Interface

When an interrupt occurs

Figure 5-7 SINT Interface

(6) Reset Time

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET_N pulse width 1	t_{RSTW1}	At power-on (*1)	1	—	—	ms
RESET_N pulse width 2	t_{RSTW2}	Other than above (*2)	1	—	—	μs

*1: At power-on, reset the IC for 1 ms or more (until the logic section PLL is locked) with stable TX_CI clock (4.096 MHz clock) being input after the power supply voltage is stabilized.

*2: Resetting during operation will reset the internal circuts even if the reset period is less than 1 μs. The regulation in the table is to ensure that all the internal circuits and internal registers are reset, in which case a reset period of 1 μs or more is required.

RESET_N input timing

Figure 5-8 Timing Diagram of RESET_N

RESET_N Input Procedure:

At power-on, reset the IC for 1 ms or more (until the logic section PLL is locked) with stable TX_CI clock (4.096 MHz clock) being input after the power supply voltage is stabilized. A reset is made asynchronously with the internal registers, and a reset is not released unless TX_CI is input at the time of reset release.

When making a reset during operation, do so for 1 μs or more to ensure that the internal circuits and the internal registers are initialized. In this case also, the reset is not released unless the TX_CI clock is input at the time of reset release. When a reset is made during operation, all the internal digital circuits and setting registers are initialized; therefore, no normal data transmission/reception is available. In this case, all the RF control signals and MODEM control signals for transmission are disabled to prevent erroneous transmission.

Stable Wait Time after Cancelling RESET_N:

After RESET_N is released, a stabilization wait time of 1 μs is required for releasing of the internal reset signal to stabilize. When executing an SCI command, take care to take an interval of 1 μs after RESET_N is released.

(7) Oscillation Circuit Characteristics (31.808 MHz OSC)

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation stabilization time	t_{OSC}	—	—	—	10	ms

Note:
After power is turned on, no normal RF reception is available until the oscillation circuit is stabilized after the power supply voltage is stabilized. For this reason, to start reception processing at the system, be sure to do so after the oscillation stabilization time elapses.

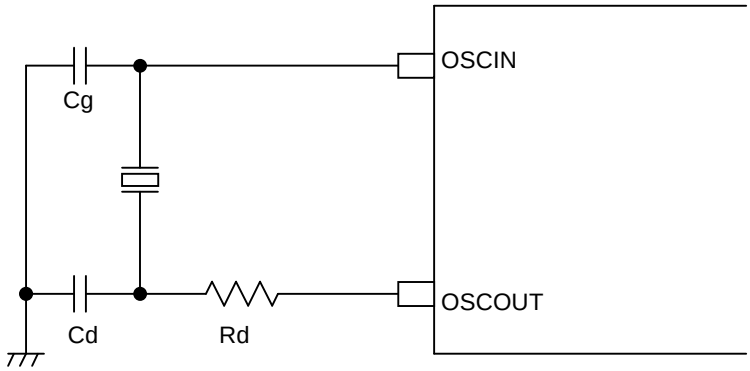


Figure 5-9 Example of Oscillation Circuit

(8) Input Section LO Clock (16 MHz) Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input amplitude level	V_{LO_CLK}	—	1.0	—	V_{DD16}	V_{P-P}

Figure 5-10 shows an LO_CLK pin connection example. For connection to the LO_CLK pin, insert a coupling capacitor because a DC component is to be cut off. As an input waveform, inputting a square wave whose amplitude level is V_{DD16} (V_{P-P}) is recommended from the viewpoint of the optimization of RF characteristics.

Do not stop the 16 MHz input while the ML9636 is operating.

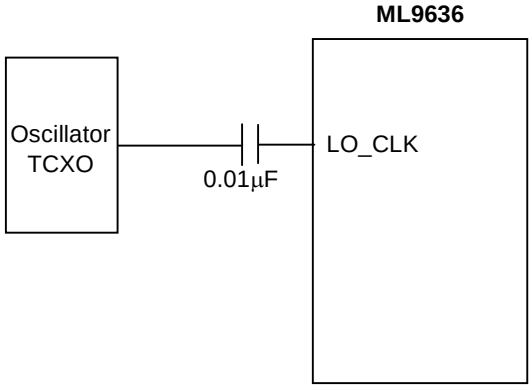


Figure 5-10 LO_CLK Pin Connection Example

(9) Logic Section PLL Characteristics

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PLL lock time	t_{OSC}	—	—	—	1	ms

The reference clock for the digital processing section (receive section, transmit section, and SCI section) is generated based on the 4.096 MHz input clock from the TX_CI pin. Note that if the input clock from the TX_CI pin is stopped or the frequency is changed, the digital processing section may lose normal functioning.

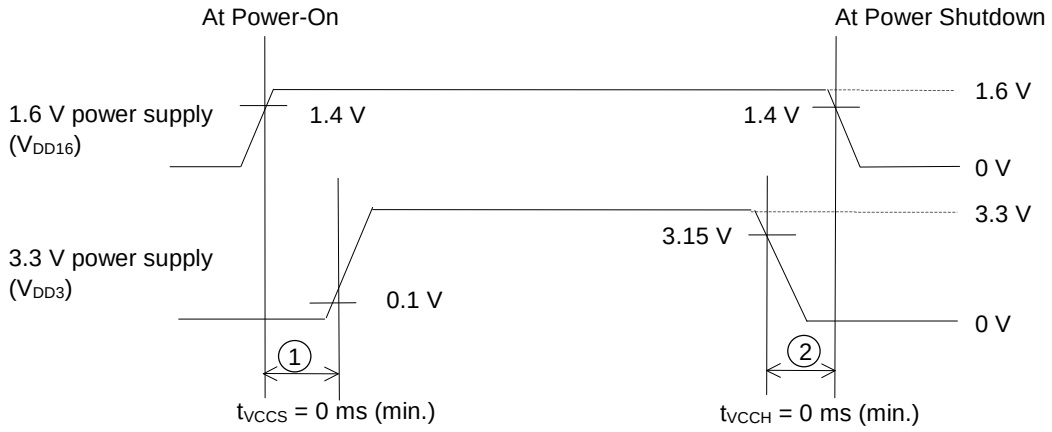
(10) Power-On/Shutdown Time

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-on time difference	t_{VCCS}	At power-on	0	—	10	ms
Power shutdown time difference	t_{VCCH}	At power shutdown	0	—	10	ms

Note:

- When turning power on, apply power to the 1.6 V (for RF and Logic core) power supplies and 3.3 V (for IO and DAC) power supplies at the same time (tvccs = 0 ms), or the 1.6 V power supplies first.
- When shutting power down, shut down the 1.6 V (for RF and Logic core) power supplies and 3.3 V (for IO and DAC) power supplies at the same time (tvcch = 0 ms), or the 3.3 V power supplies first.
- If power is turned on or shut down without following the above sequences, it is possible that pins that are originally for input will be configured as "output" because every digital IO circuit of this IC uses bi-directional buffer, and, as a result, a signal conflict may be caused with output pins of the opposing BB LSI.



Recommended power-on/shutdown sequences:

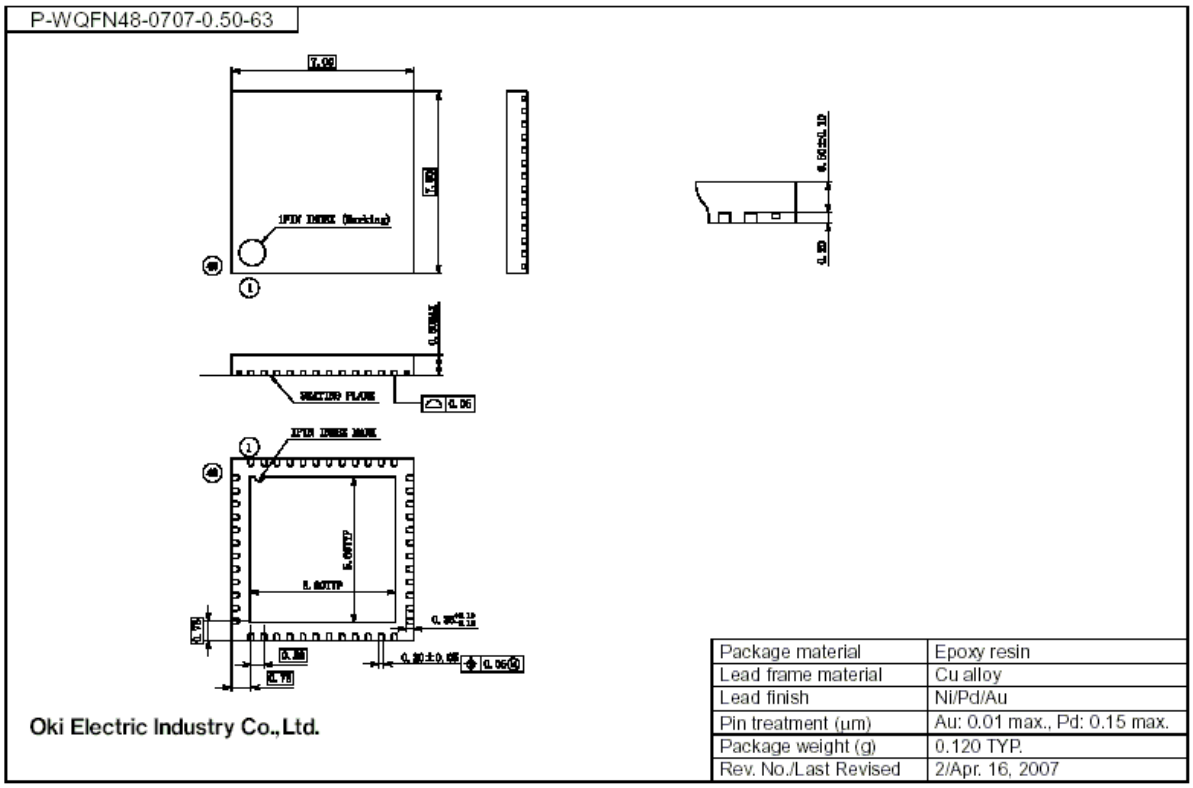
① When turning power on, apply power to the 1.6 V (for RF and Logic core) power supplies and 3.3 V (for IO and DAC) power supplies at the same time (tvccs = 0 ms), or the 1.6 V power supplies first.

② When shutting power down, shut down the 1.6 V (for RF and Logic core) power supplies and 3.3 V (for IO and DAC) power supplies at the same time (tvcch = 0 ms), or the 3.3 V power supplies first.

Figure 5-11 Power-On/Shutdown Sequences

6. Package Dimensions

Unit: mm



Note: The exposed die attach pad must be connected to a solid ground plane as this is the ground connection for the chip.

Figure 6-1 Package Dimensions

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

7. Temperature Correction for RF Characteristics

This capter describes how to adjust RF characteristics (transmission and reception) and make temperature correction. A correction operation is performed by measuring an ambient temperature using an external circuti such as a thermistor and then writing a correction value appropriate for the temperature into a predetermined register from the serial interface of the ML9636.

7.1 Transmission Characteristics

7.1.1 Transmission Blocks and Transmission Power Adjustment Registers

Figure 7-1 shows the relationship between ML9636's transmission blocks and the setting registers.

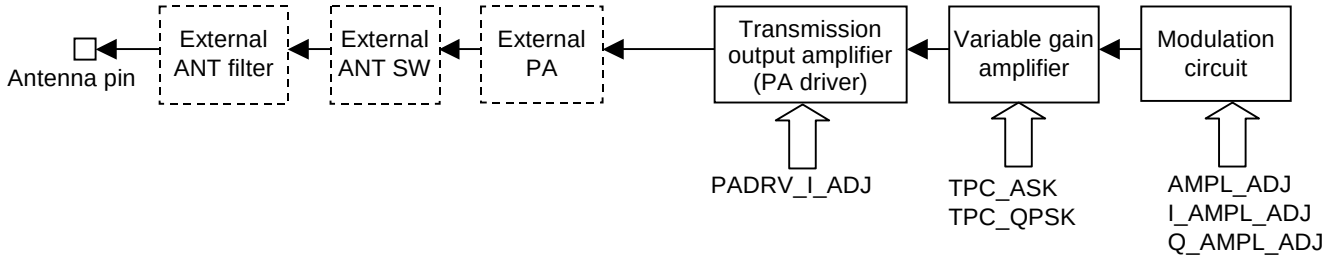


Figure 7-1 Relationship between ML9636 Transmission Blocks and Setting Registers

In the explanations below, it is assumed that the transmission power of the entire system including the external components such as the power amplifier will be adjusted using the functions of the ML9636.
Transmission power is adjusted by configuring the following three types of registers:

- PADRV_I_ADJ register
  This register sets the transmission output amplifier (PA driver block) gain adjustment value.

- TPC_ASK and TPC_QPSK registers
  These registers correct the gain fluctuation by adjusting the variable gain amplifier to make the transmission output power from the antenna pin constant. Gain fluctuation elements include interdevice variation in ML9636, temperature fluctuation in ML9636, interdevice variation in external components (ANT filter, ANT SW, and SAW filter) from device to device, and temperature fluctuation in external components. Adjustments are necessary for ASK mode and QPSK mode separately.

- AMPL_ADJ, I_AMPL_ADJ, and Q_AMPL_ADJ registers
  Gain fluctuation is corrected in combination with the TPC_ASK and TPC_QPSK registers above. Adjustments are necessary for ASK mode and QPSK mode separately.

The TPC_ASK and TPC_QPSK registers have an adjustment resolution of about 1 dB and the AMPL_ADJ, I_AMPL_ADJ, and Q_AMPL_ADJ registers about 0.1 dB.

For the PADRV_I_ADJ register, write the values (RF1[15:12]) which is presented by OKI separately. This is the fixed values regardless of the ambient temperature.
For the TPC_ASK, TPC_QPSK, AMPL_ADJ, I_AMPL_ADJ, and Q_AMPL_ADJ registers, write a correction value calculated by the method explained in Sections 7.1.2 to 7.1.5 to each of these registers periodically based on the ambient temperature measurement result.

7.1.2 Outline of the Method of Setting Transmission Power Adjustment Registers (TPC Register, AMPL_ADJ Register)

In ASK mode, transmission output is corrected using a combination of the TPC_ASK register and AMPL_ADJ register.
In QPSK mode, transmission output is corrected using a combination of the TPC_QPSK register, I_AMPL_ADJ register, and Q_AMPL_ADJ register. Normally, set the I_AMPL_ADJ register and the Q_AMPL_ADJ register to the same value.

Table 7-1 shows the outline of coding for the registers (refer to Chapter 4 and the separate volume).

Table 7-1 Transmission Power Adjustment Registers (TPC Register, AMPL_ADJ Register)

Output power	ASK mode		QPSK mode	
	SET_TPC command	SET_HDAC_ASK command	SET_TPC command	SET_HDAC_QPSK1 command SET_HDAC_QPSK2 command
	TPC_ASK[3:0] bits	AMPL_ADJ[5:0] bits	TPC_QPSK[3:0] bits	I_AMPL_ADJ[5:0] bits Q_AMPL_ADJ[5:0] bits
	Coarse adjustment	Fine adjustment	Coarse adjustment	Fine adjustment
Max. →	1111	1 11111 1 11110 1 11101 • • • 1 00010 1 00001 Approx. +0.1 dB 0 00000 Center value 0 00001 Approx. –0.1 dB 0 00010 • • • 0 11101 0 11110 0 11111	1111	1 11111 1 11110 1 11101 • • • 1 00010 1 00001 Approx. +0.1 dB 0 00000 Center value 0 00001 Approx. –0.1 dB 0 00010 • • • 0 11101 0 11110 0 11111
	1110	Same as above	1110	Same as above
	1101	Same as above	1101	Same as above
	1100	Same as above	1100	Same as above
	1011	Same as above	1011	Same as above
	• • •	• • •	• • •	• • •
	0010	Same as above	0010	Same as above
← Min.	0001	Same as above	0001	Same as above
	0000	Same as above	0000	Same as above

In the explanations below, the "TPC register," when used in ASK mode, denotes the TPC_ASK register and when used in QPSK mode, it denotes the TPC_QPSK register. Likewise, the "AMPL_ADJ register" means in ASK mode the AMPL_ADJ register, and in QPSK mode the I_AMPL_ADJ and Q_AMPL_ADJ registers.

The TPC register has an adjustment resolution of about 1 dB and the AMPL_ADJ register about 0.1 dB. By fine adjusting each adjustment step of the TPC register with respect to the AMPL_ADJ register settings, a desired adjustment resolution can be achieved.
Since the AMPL_ADJ register variable width is greater than the adjustment width per step of the TPC register, all the AMPL_ADJ settings are not used for normal operation. For adjustment, a list of combinations of the TPC and AMPL_ADJ settings is used, where the transmission power of the ML9636 varies at roughly the same widths monotonously (Table 7-2 being the standard table prepared by OKI). In Table 7-2, decimal values are used for the TPC and AMPL_ADJ register values, and the correspondences with the bits are shown in Tables 7-3 and 7-4. In Table 7-2, the setting No. 0 indicates the setting for the lowest transmission power.

The flowchart below shows the calculation procedure for calculating the setting values for the transmission power adjustment registers above. The procedure needs to be taken for ASK mode and QPSK mode separately.
Each step in the procedure is described in details in Sections 7.1.3 to 7.1.5.

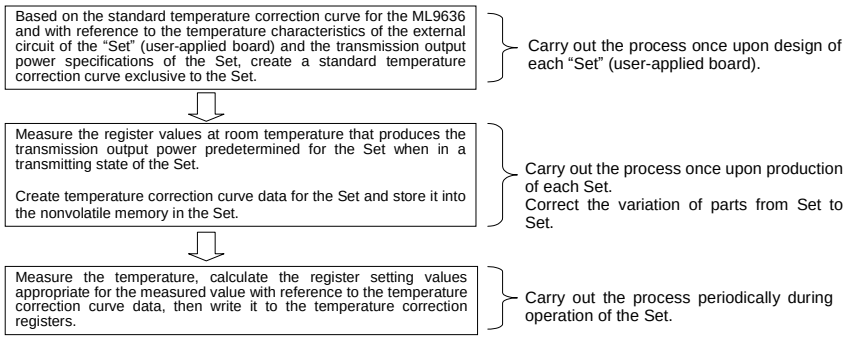


Figure 7-2 Procedure for Calculating the Setting Values for the Transmission Power Adjustment Registers (TPC Register, AMPL_ADJ Register)

Table 7-2 Standard Table for Transmission Registers

Setting No.	TPC (DEC)	AMPL_ADJ (DEC)
0	0	−22
1	0	−21
2	0	−20
3	0	−19
4	0	−18
5	0	−17
6	0	−16
7	0	−15
8	0	−14
9	0	−13
10	0	−12
11	0	−11
12	0	−10
13	0	−9
14	0	−8
15	0	−7

Setting No.	TPC (DEC)	AMPL_ADJ (DEC)
16	0	–6
17	0	–5
18	0	–4
19	0	–3
20	0	–2
21	0	–1
22	0	0
23	0	1
24	0	2
25	0	3
26	0	4
27	0	5
28	0	6
29	1	–6
30	1	–5
31	1	–4
32	1	–3
33	1	–2
34	1	–1
35	1	0
36	1	1
37	1	2
38	1	3
39	1	4
40	1	5
41	1	6
42	2	–6
43	2	–5
44	2	–4
45	2	–3
46	2	–2
47	2	–1
48	2	0
49	2	1
50	2	2
51	2	3
52	2	4
53	2	5
54	2	6
55	3	–6
56	3	–5
57	3	–4
58	3	–3
59	3	–2
60	3	–1
61	3	0
62	3	1
63	3	2
64	3	3
65	3	4
66	3	5

Setting No.	TPC (DEC)	AMPL_ADJ (DEC)
67	3	6
68	4	–6
69	4	–5
70	4	–4
71	4	–3
72	4	–2
73	4	–1
74	4	0
75	4	1
76	4	2
77	4	3
78	4	4
79	4	5
80	4	6
81	5	–5
82	5	–4
83	5	–3
84	5	–2
85	5	–1
86	5	0
87	5	1
88	5	2
89	5	3
90	5	4
91	5	5
92	5	6
93	6	–5
94	6	–4
95	6	–3
96	6	–2
97	6	–1
98	6	0
99	6	1
100	6	2
101	6	3
102	6	4
103	6	5
104	6	6
105	7	–5
106	7	–4
107	7	–3
108	7	–2
109	7	–1
110	7	0
111	7	1
112	7	2
113	7	3
114	7	4
115	7	5
116	7	6
117	8	–5

Setting No.	TPC (DEC)	AMPL_ADJ (DEC)
118	8	–4
119	8	–3
120	8	–2
121	8	–1
122	8	0
123	8	1
124	8	2
125	8	3
126	8	4
127	8	5
128	8	6
129	9	–5
130	9	–4
131	9	–3
132	9	–2
133	9	–1
134	9	0
135	9	1
136	9	2
137	9	3
138	9	4
139	9	5
140	10	–5
141	10	–4
142	10	–3
143	10	–2
144	10	–1
145	10	0
146	10	1
147	10	2
148	10	3
149	10	4
150	10	5
151	11	–5
152	11	–4
153	11	–3
154	11	–2
155	11	–1
156	11	0
157	11	1
158	11	2
159	11	3
160	11	4
161	11	5
162	12	–4
163	12	–3
164	12	–2
165	12	–1
166	12	0
167	12	1
168	12	2

Setting No.	TPC (DEC)	AMPL_ADJ (DEC)
169	12	3
170	12	4
171	13	–4
172	13	–3
173	13	–2
174	13	–1
175	13	0
176	13	1
177	13	2
178	13	3
179	13	4
180	14	–4
181	14	–3
182	14	–2
183	14	–1
184	14	0
185	14	1
186	14	2
187	14	3
188	14	4
189	15	–4
190	15	–3
191	15	–2
192	15	–1
193	15	0
194	15	1
195	15	2
196	15	3
197	15	4
198	15	5
199	15	6
200	15	7
201	15	8
202	15	9
203	15	10
204	15	11
205	15	12
206	15	13
207	15	14
208	15	15
209	15	16
210	15	17
211	15	18
212	15	19
213	15	20
214	15	21
215	15	22

Table 7-3 Correspondence between TPC Values and Bits

TPC[3:0]	TPC (DEC)
1111	15
1110	14
1101	13
1100	12
1011	11
1010	10
1001	9
1000	8
0111	7
0110	6
0101	5
0100	4
0011	3
0010	2
0001	1
0000	0

Table 7-4 Correspondence between AMPL_ADJ Values and Bits

AMPL_ADJ[5:0]	AMPL_ADJ (DEC)
110110	22
110101	21
110100	20
110011	19
110010	18
110001	17
110000	16
101111	15
101110	14
101101	13
101100	12
101011	11
101010	10
101001	9
101000	8
100111	7
100110	6
100101	5
100100	4
100011	3
100010	2
100001	1
000000	0
000001	–1
000010	–2
000011	–3
000100	–4
000101	–5
000110	–6
000111	–7
001000	–8
001001	–9
001010	–10
001011	–11
001100	–12
001101	–13
001110	–14
001111	–15
010000	–16
010001	–17
010010	–18
010011	–19
010100	–20
010101	–21
010110	–22

7.1.3 Creating a Standard Temperature Correction Curve

At the dispersion temperature points on both ends of the pre-selected temperature zone, evaluate the transmission power as a system (Set, or user-applied board) including the ML9636 and peripheral components such as the external power amplifier and then determine the standard setting value at each dispersion temperature.
For example, when the dispersion temperature points are set to –30°C, –15°C, 15 °C, 27.5°C (room temperature), 45°C, 75°C, and 85°C, determine the setting No. (Standard value) in Table 2 that produces the required transmission power as a Set, at the Set evaluation stage (xx1 to xx7 in Figure 7-3).

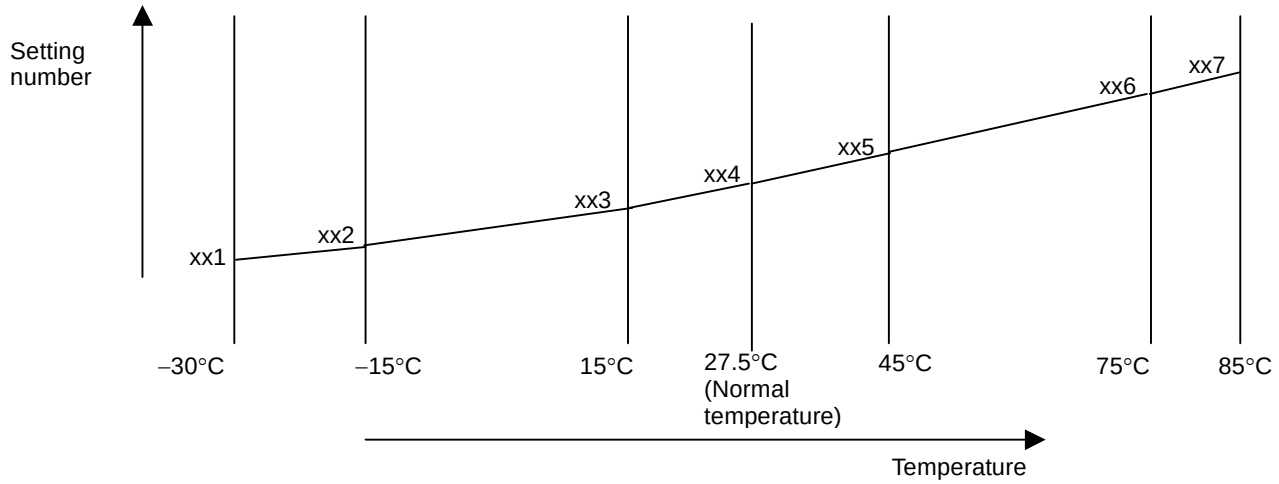


Figure 7-3 Standard Temperature Correction Curve

7.1.4 Creating a Temperature Correction Curve for Each Individual Set

As one of the adjustment items, create temperature correction curve data for each individual Set (user-applied board) in the Set production process and store it into the nonvolatile memory in the Set.
Temperature correction curve data for each Set can be created in the following way using the standard temperature correction curve created in Section 7.1.3:
- Determine the register values from the value measured at room temperature that produces the transmission output power predetermined for the Set when in a transmitting state. Then, create a temperature correction curve for the Set by translating that standard temperature correction curve so that the curve passes over this measurement point (measured register values at room temperature).

Store the values at both end of each of the temperature zone for the created temperature correction curve into the nonvolatile memory.

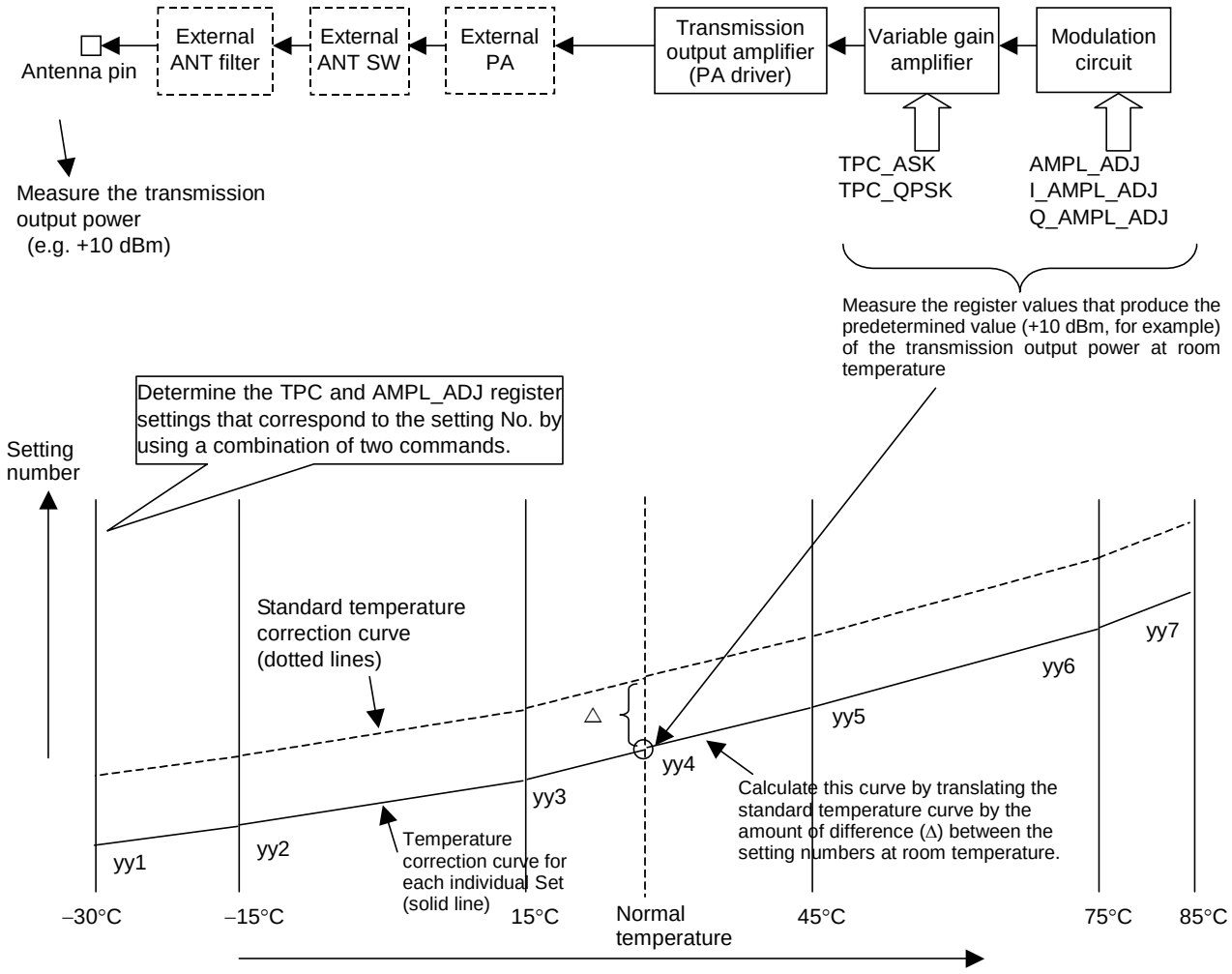


Figure 7-4 Creation of a Temperature Correction Curve for a Set

7.1.5 Correcting Temperatures during the Operation of a Set

After power is applied to a Set (user-applied board) and the Set is initialized, measure the temperature using a thermistor etc. periodically, calculate the register setting values appropriate for the measured value with reference to the temperature correction curve data, then write it to the temperature correction registers. For each of the measurement temperatures, the setting number can be calculated by linear interpolation by using the setting numbers of both ends of the temperature zone including the temperature. Determine the TPC and AMPL_ADJ settings that correspond to the obtained setting numbers from Table 7-2.
For example, the method of determing the register setting values when the measured temperature is 60°C is as follows:
Assume that the setting number for 45°C and that for 75°C obtained in Section 7.1.4 are 132 (corresponds to TPC_ASK = 9, AMPL_ADJ = –2) and 172 (corresponds to TPC_ASK = 13, AMPL_ADJ = –3) respectively. Here, since calculating the setting number for 60°C by linear interpolation procduces 152, the register setting values will be TPC_ASK = 11 and AMPL_ADJ = –4.

How often the temperature correction registers are to be set depends on the temperature distribution inside the Set or the rate of temporal temperature change. In the ML9636, frequency at about tens of seconds is assumed. In addition, it is assumed that the correction data for transmission characteristics will be written at the same frequency as the correction data for reception characteristics.
Do not write to the temperature correction registers during transmission.

7.2 Reception Characteristics

7.2.1 Reception Blocks and Reception Characteristics Adjustment Registers

Figure 7-5 shows the receive blocks of the ML9636.

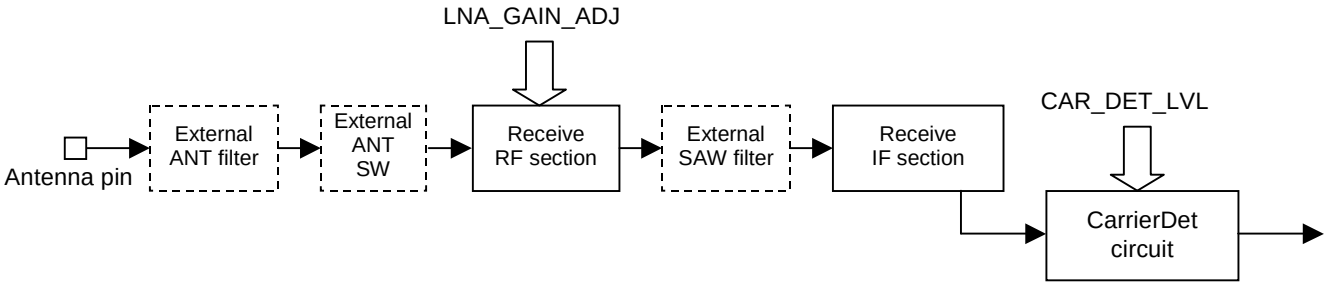


Figure 7-5 Relationship between Reception Blocks and Setting Registers

The setting registers are the following two. (For the relevant commands and registers, refer to Chapter 4 and the separate volume for this manual.)

- LNA_GAIN_ADJ: Corrects the temperature characteristics of the gains of the receive RF section amplifier circuit and keeps good receiver sensitivity characteristics (maximum and minimum reception levels).

- CAR_DET_LVL: Corrects the fluctuations in gain from the antenna pin to the carrier detect circuit. The gain fluctuation factors include variations in ML9636 devices, temperature fluctuation in an ML9636 device, variations in external components (ANT filter, ANT SW, and SAW filter), and temperature fluctuation in external component.

7.2.2 Method of Setting the Reception Characteristics Adjustment Registers

(1) Setting the LNA_GAIN_ADJ register

Divide the temperature range into five temperature zones and, based on the measured temperature information, write the value appropriate for the corresponding temperature zone to the SET_RF0 command LNA_GAIN_ADJ[3:0] bits. Since the ML9636 has been trimmed during the production process at OKI, use this trimming value to calculate the value appropriate for the temperature zone Use this trimming value to calculate the value appropriate for the corresponding temperature zone and set it ot the register. The following figure shows an example flow of setting the LNA_GAIN_ADJ register.

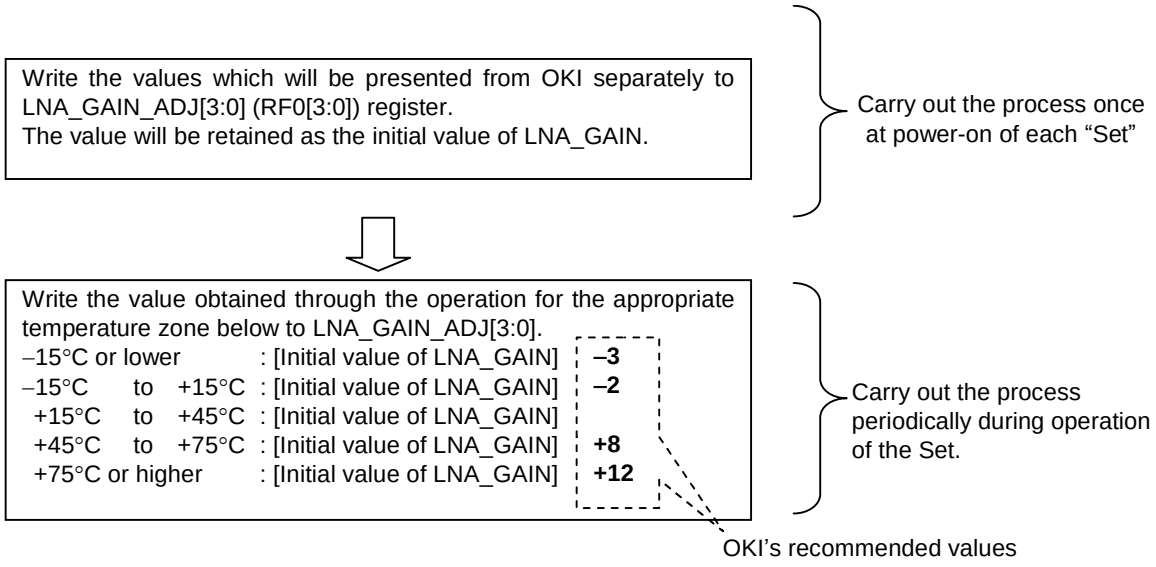


Figure 7-6 Method of Setting Reception Characteristics Adjustment Registers [1]

(2) Setting the CAR_DET_LVL register

Following shows how to calculate the CAR_DET_LVL register setting values (correspond to SET_CAR_DET_LVL command CAR_DET_LVL[8:0](bits 15–7)).

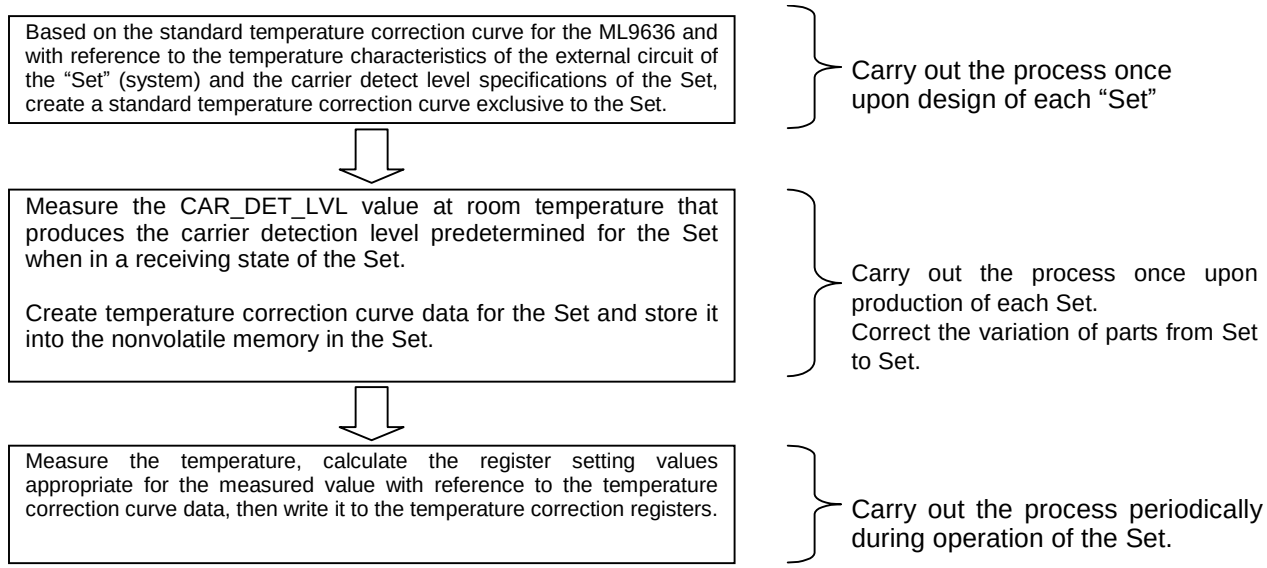


Figure 7-7 Method of Setting Reception Characteristics Adjustment Registers [2]

7.2.3 Creating a Standard Temperature Correction Curve

Create a standard temperature correction curve as a Set, based on the ML9636 satandard temperature correction curve provided by OKI, with reference to the temperature characteristics of external components (ANT filter, ANT SW, and SAW filter) that are used in the actual Set, and according to the carrier detection level specifications as a Set. The figure below shows the standard value (carrier detect level: –64 dBm). For details see Figure 7-10.

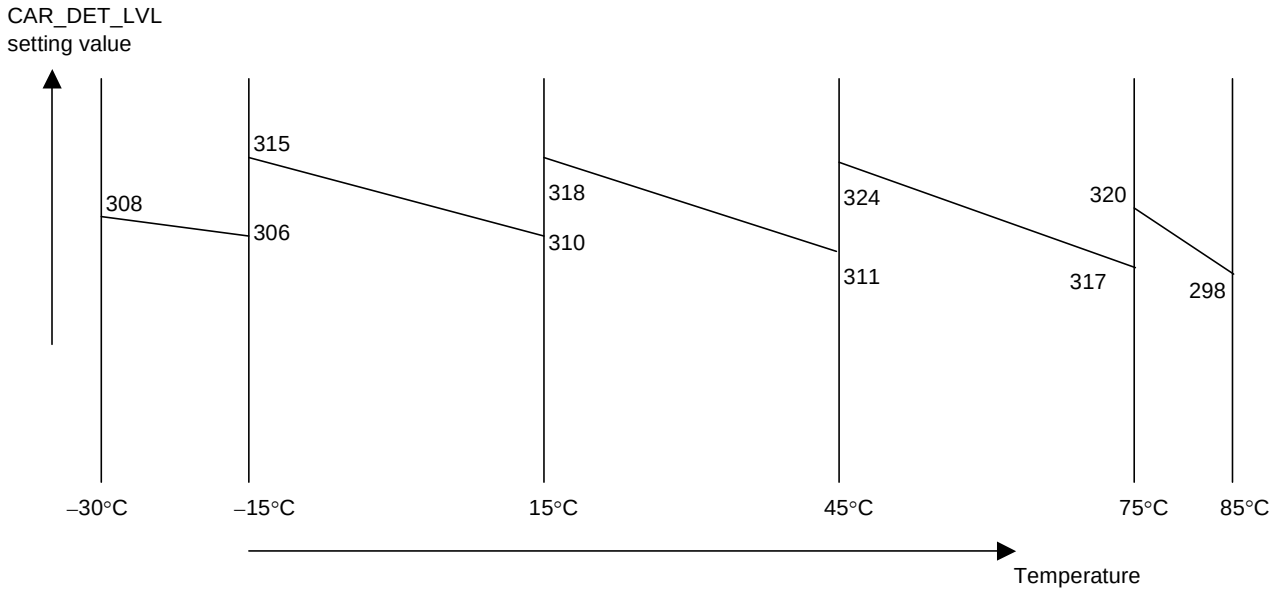


Figure 7-8 Creation of a Receive Standard Temperature Correction Curve

7.2.4 Creating a Temperature Correction Curve for Each Individual Set

As one of the adjustment items, create temperature correction curve data for each individual Set in the Set production process and store it into the nonvolatile memory in the Set.

Measure the CAR_DET_LVL value at room temperature that produces the carrier detection level predetermined for the Set when in a receiving state. Then, create a temperature correction curve for the Set by translating that standard temperature correction curve so that the curve passes over this measurement point (measured CAR_DET_LVL value at room temperature).
Store the values at both end of each of the temperature zone for the created temperature correction curve into the nonvolatile memory.

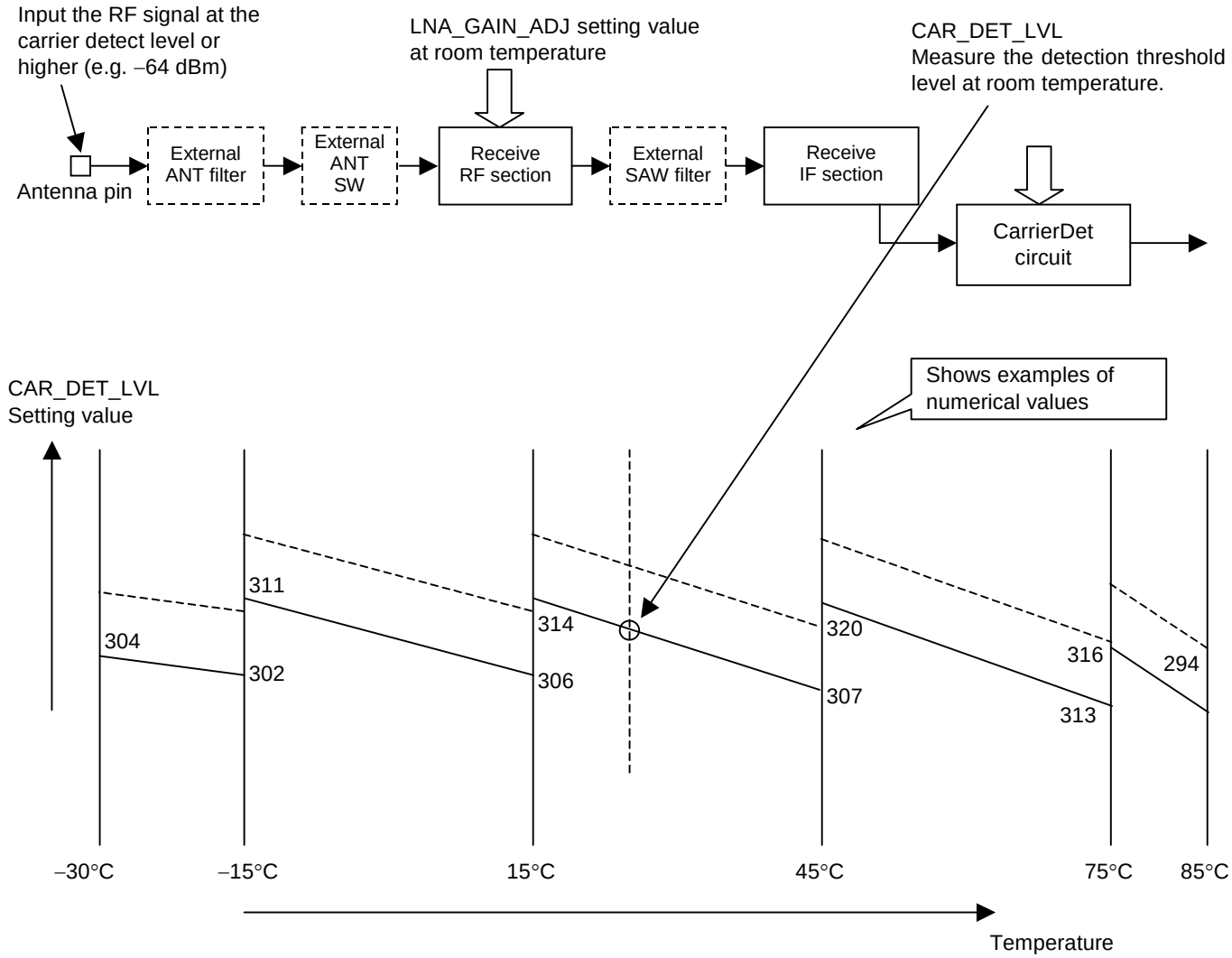


Figure 7-9 Creation of a Temperature Correction Curve for a Set

7.2.5 Correcting Temperatures during the Operation of a Set

After power is applied to a Set and the Set is initialized, measure the temperature periodically, calculate the register setting values appropriate for the measured value with reference to the temperature correction curve data, then write it to the temperature correction registers.

How often the temperature correction registers are to be set depends on the temperature distribution inside the Set or the rate of temporal temperature change. In the ML9636, frequency at about tens of seconds is assumed.
Do not write to the temperature correction registers during burst signal reception.

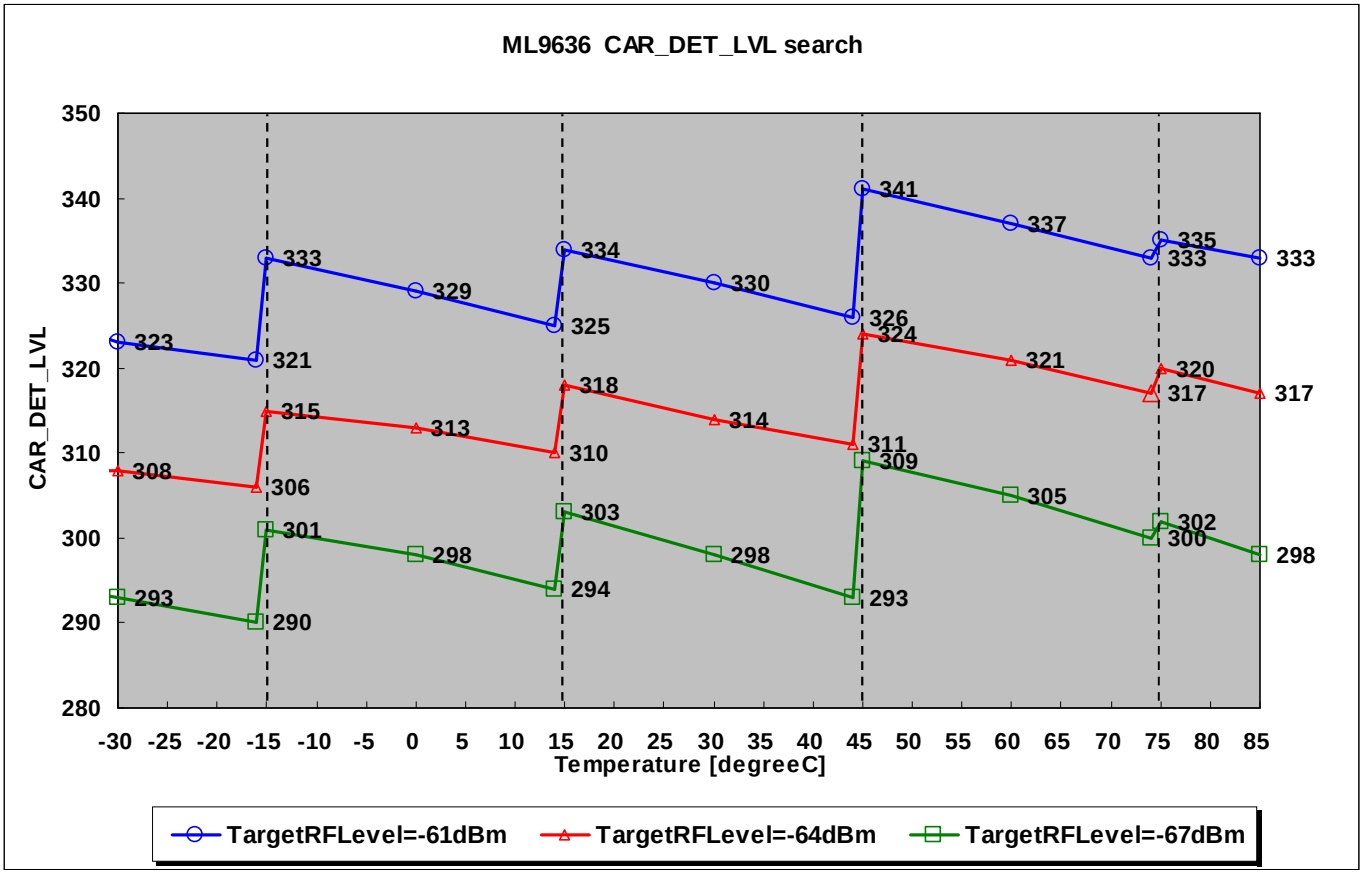


Figure 7-10 Standard Values of CAR_DET_LVL When Setting the Carrier Detection Level to –61, –64, and –67 dBm [Reference Data]

Appendixes

A. SCI Timing Specifications (Reference Values)

A.1 Internal Register Update Timing at Write (Reference Values)

Figure A-1 shows the internal register update timing for SCLK at the time of writing by SCI. If the length of the setting data is one byte, the update timing is the same as "DATA1 update timing" in the figure.
The update timing in the table below shows the timing of LSI internal operation, and the values shown in the table are for reference only.

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal register update time	T_{RENEW}		—	—	190	ns

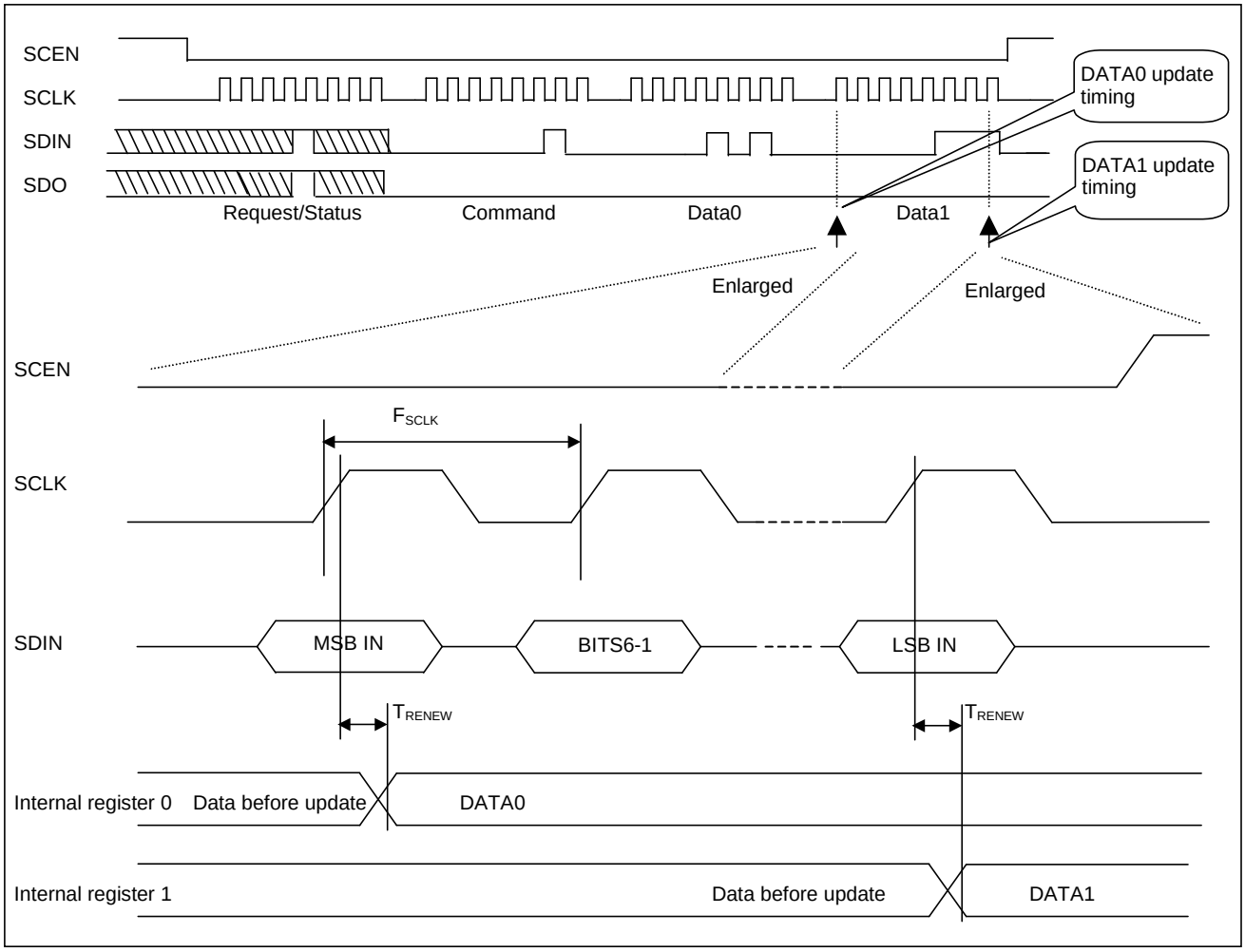


Figure A-1 Internal Register Update Timing at Write (Setting Data: 2 Bytes)

A.2 SINT Assert Timing at Read (Reference Values)

The SINT assert time (reference values) at read is shown below.
Figure A-2 shows the timing of SINT assert after SCEN negate at read by the GET_request command.
Figure A-3 shows the timing of SINT reassert when two read data items are retained.

(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SINT assert time at read	T_{SIAST}	Load capacitance	—	—	2.4	µs
SINT reassert time	$T_{SIREAST}$	C_L = 50pF	—	—	2.0	µs

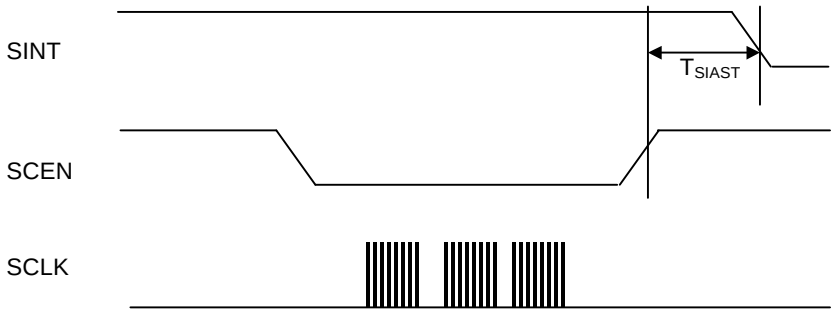


Figure A-2 SINT Assert Timing at Read

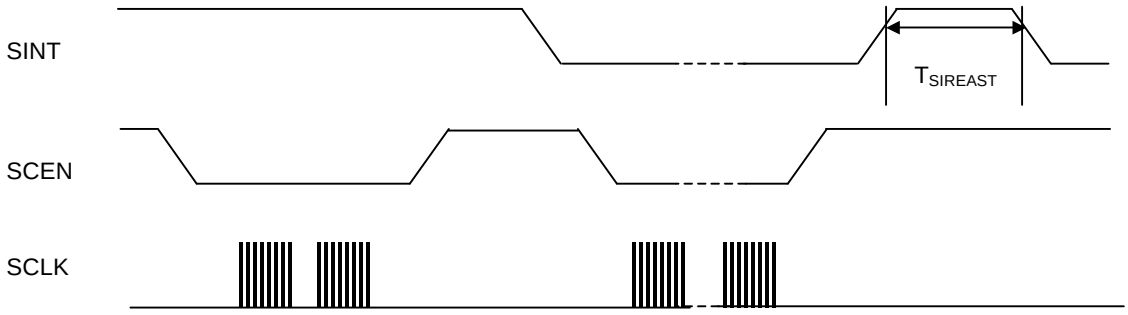
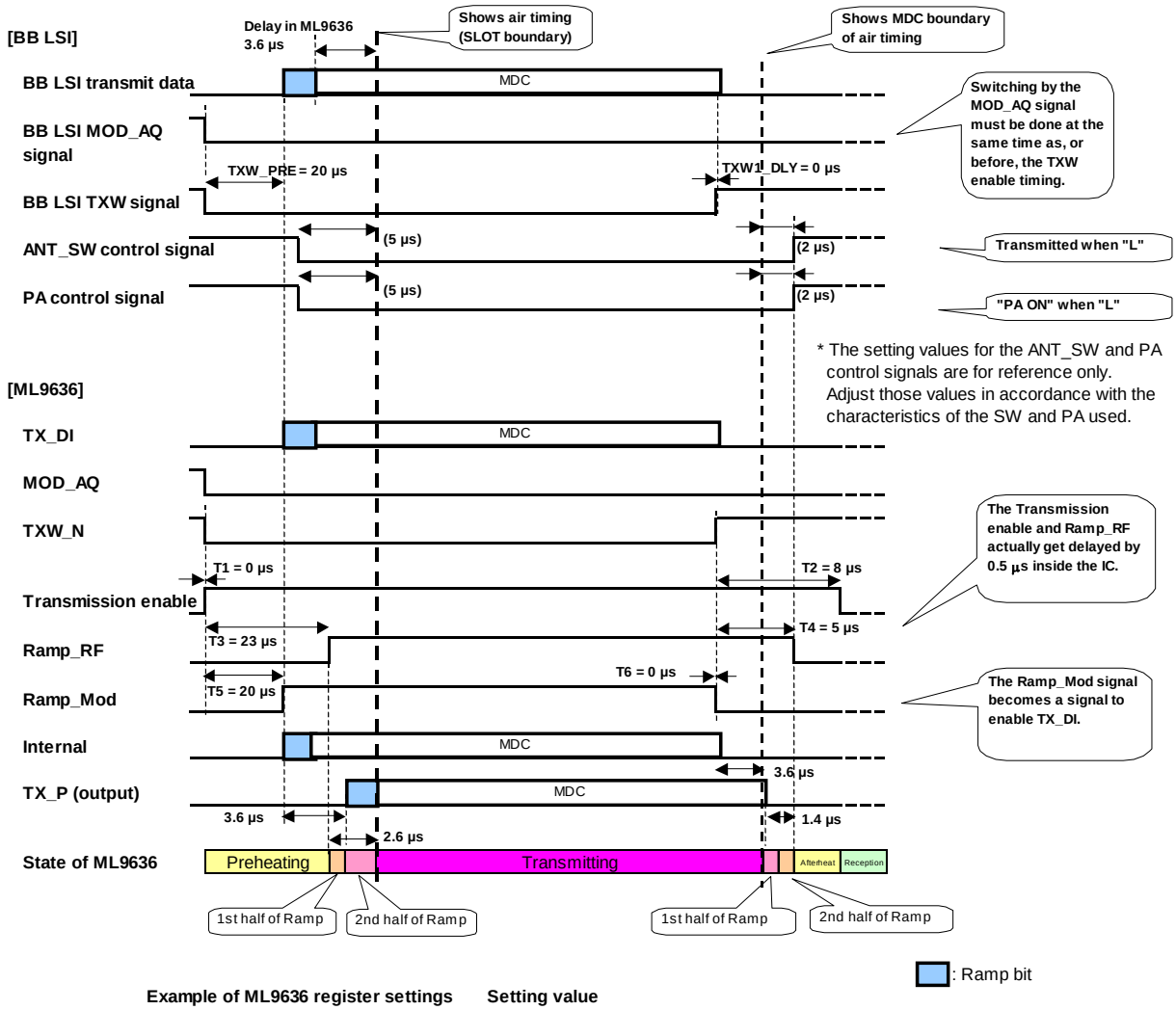


Figure A-3 SINT Reassert Timing

B. Example of Setting Transmit Timing

B.1 Example of Setting QPSK Transmit Timing



Example of ML9636 register settings		Setting value	
TX_ON_QPSK	T1	0x00	0 µs
TX_OFF_QPSK	T2	0x20	7.81 µs
RAMP_RF_ON_QPSK	T3	0x5C	22.45 µs
RAMP_RF_OFF_QPSK	T4	0x14	4.88 µs
RAMP_MOD_ON_QPSK	T5	0x50	19.53 µs
RAMP_MOD_OFF_QPSK	T6	0x00	0 µs

Figure B-1 Example of Setting QPSK Transmit Timing

Figure B-1 shows the timing of the BB LSI and the ML9636 during QPSK data output and example of settings for the ML9636 registers for timing adjustment.

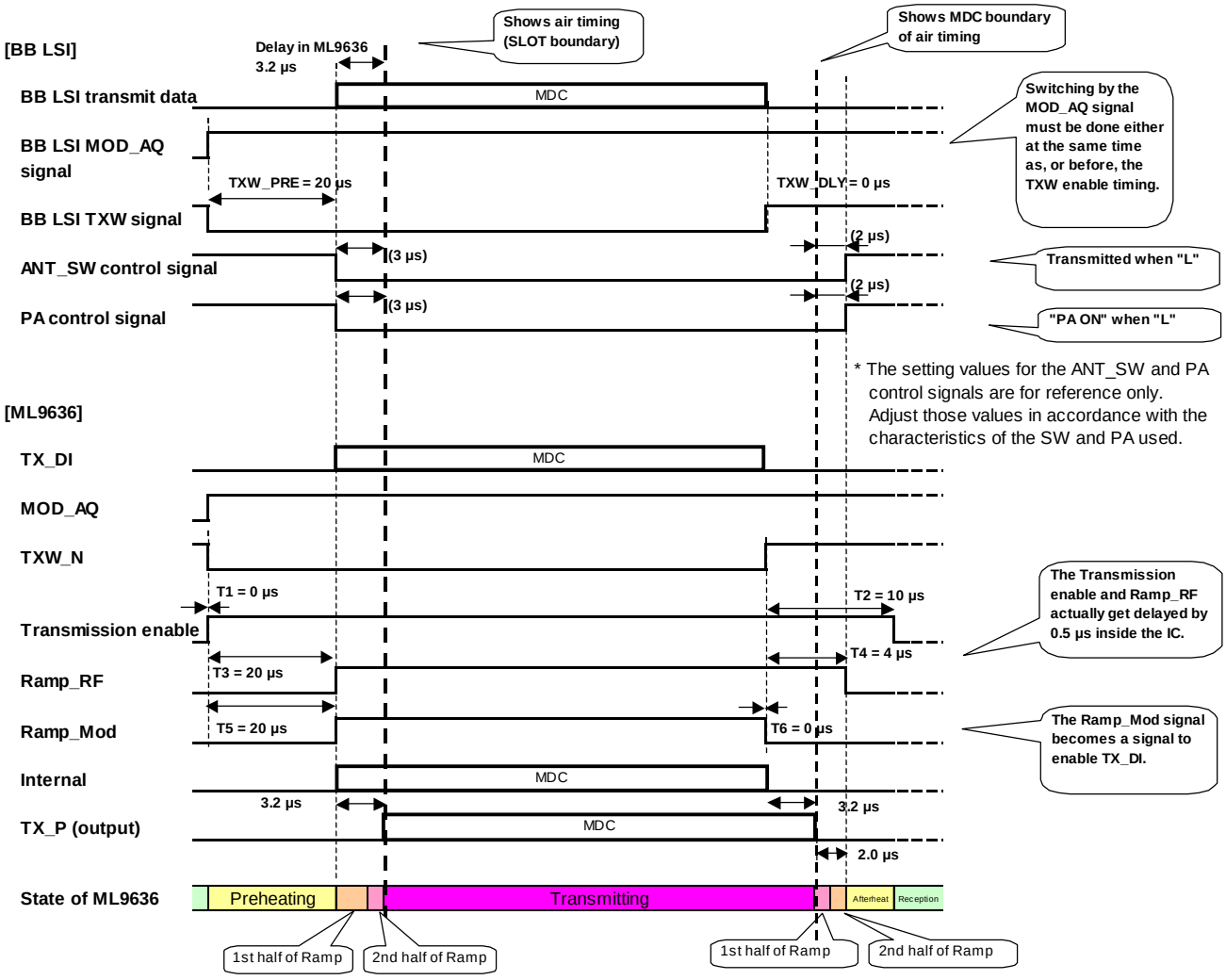
The ML9636 requires a "preheating" time for the PA section of the transmit RF section. A "preheating" time of about 20 µs is assumed in th figure above. Because of this "residual heat" time, configure timing settings so that the TXW outpu from the BB LSI will be enabled ("L") 20 µs ahead of the head of the Ramp bit of the transmit data "TX_DI".

When the TXW signal is output 20 µs ahead of the head of the Ramp bit from the BB LSI, transmit data (TX_DI) can be received at the correct timing by setting "T5" to 20 µs.

The "preheating" time mentioned above refers to the time required to stabilize various fluctuations associated with a change in power supply voltage caused by activation of transmitter circuits including the external AP circuit. The "preheating" time is affected by external components and board patterns. If there are no power supply voltage fluctuations associated with activation of transmitter circuits including the external PA circuit, the ML9636's transmitter circuits are activated within 5 µs (worst value).

When in QPSK mode, be careful of the handling of the Ramp.
In the figure above, the timing of outputting the TXW signal from the BB LSI is indicated by reference to the head of the Ramp.
The register settings shown in the figure above are those which were considered as optimized values at the design stage of the ML9636 and are not guaranteed values. Determine the definitive settings after verification after system evaluation on the customer side.

B.2 Example of Setting ASK Transmit Timing



Example of ML9636 register settings		Setting value	
TX_ON_ASK	T1	0x00	0 ms
TX_OFF_ASK	T2	0x28	9.76 ms
RAMP_RF_ON_ASK	T3	0x50	19.53 ms
RAMP_RF_OFF_ASK	T4	0x10	3.90 ms
RAMP_MOD_ON_ASK	T5	0x50	19.53 ms
RAMP_MOD_OFF_ASK	T6	0x00	0 ms

Figure B-2 Example of Setting ASK Transmit Timing

Figure B-2 shows the timing of the BB LSI and the ML9636 during ASK data output and example of settings for the ML9636 registers for timing adjustment.
The ML9636 requires a "preheating" time for the PA section of the transmit RF section. A "preheating" time of about 20 μs is assumed in th figure above. Because of this "residual heat" time, configure timing settings so that the TXW outpu from the BB LSI will be enabled ("L") 20 μs ahead of the head of the PR bit of the transmit data "TX_DI".
When the TXW signal is output 20 μs ahead of the head of the PR bit from the BB LSI, transmit data (TX_DI) can be received at the correct timing by setting "T5" to 20 μs.
The "preheating" time mentioned above refers to the time required to stabilize various fluctuations associated with a change in power supply voltage caused by activation of transmitter circuits including the external AP circuit. The "preheating" time is affected by external components and board patterns. If there are no power supply voltage fluctuations associated with activation of transmitter circuits including the external PA circuit, the ML9636's transmitter circuits are activated within 5 μs (worst value).
When in QPSK mode, be careful of the handling of the Ramp.
In the figure above, the timing of outputting the TXW signal from the BB LSI is indicated by reference to the head of the Ramp.
The register settings shown in the figure above are those which were considered as optimized values at the design stage of the ML9636 and are not guaranteed values. Determine the definitive settings after verification after system evaluation on the customer side.

C. RF Burst Receive Timing (Reference Values)

Shown below are the carrier detect signal rise time and the time for receive data to stabilize at RF signal input (reference values). Figure C-1 shows the timing.

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(V_{DD3} = 3.15 V to 3.45 V, V_{DD16} = 1.5 V to 1.65 V, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Carrier detect signal rise time (*1) (*2)	T_{CDET}	At no-modulation wave input		3 (*3)	14	µs
QPSK receive stabilization time	T_{STABLE_QPSK}		—	14	20	µs
ASK receive stabilization time	T_{STABLE_ASK}		—	—	3	µs

*1 Indicates reference data that is in effect when the RSSI_C pin capacitance value is 1000 pF. As this capacitance value is made smaller, the carrier detect signal rise time and fall time will get shorter. However, in that case, note that the carrier detect signal may go on and off uselessly.

*2 Note that the carrier detect signal rise time changes depending on the RSSI_C capacitance, CAR_DET_LVL setting, or power supply voltage.

*3 Standard condition: When a no-modulation wave is input with V_{DD16} = 1.6 V, V_{DD3} = 3.3V, and CAR_DET_LVL = 256 (decimal value).

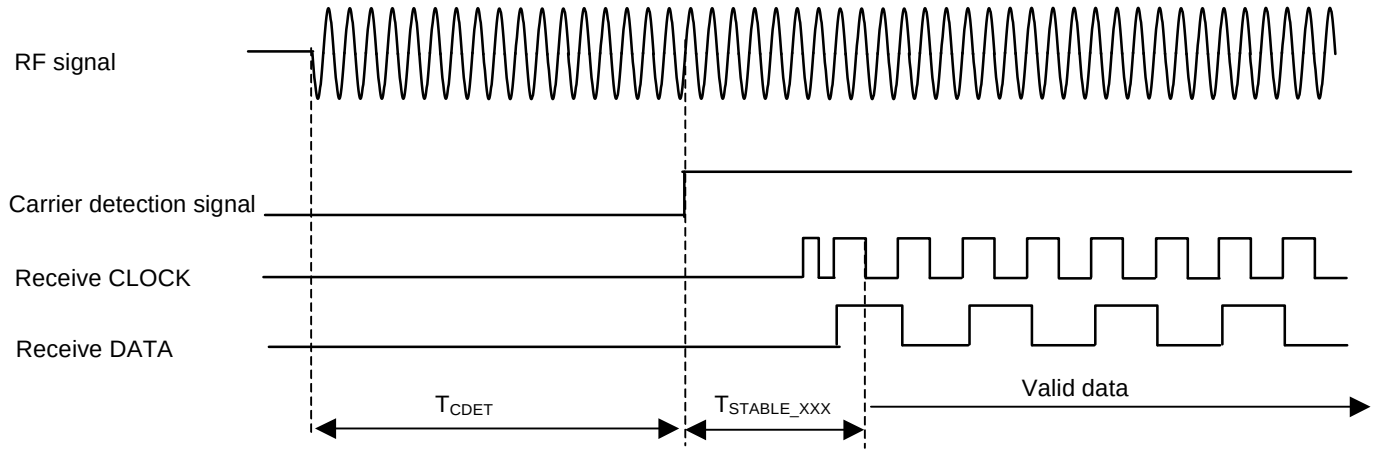
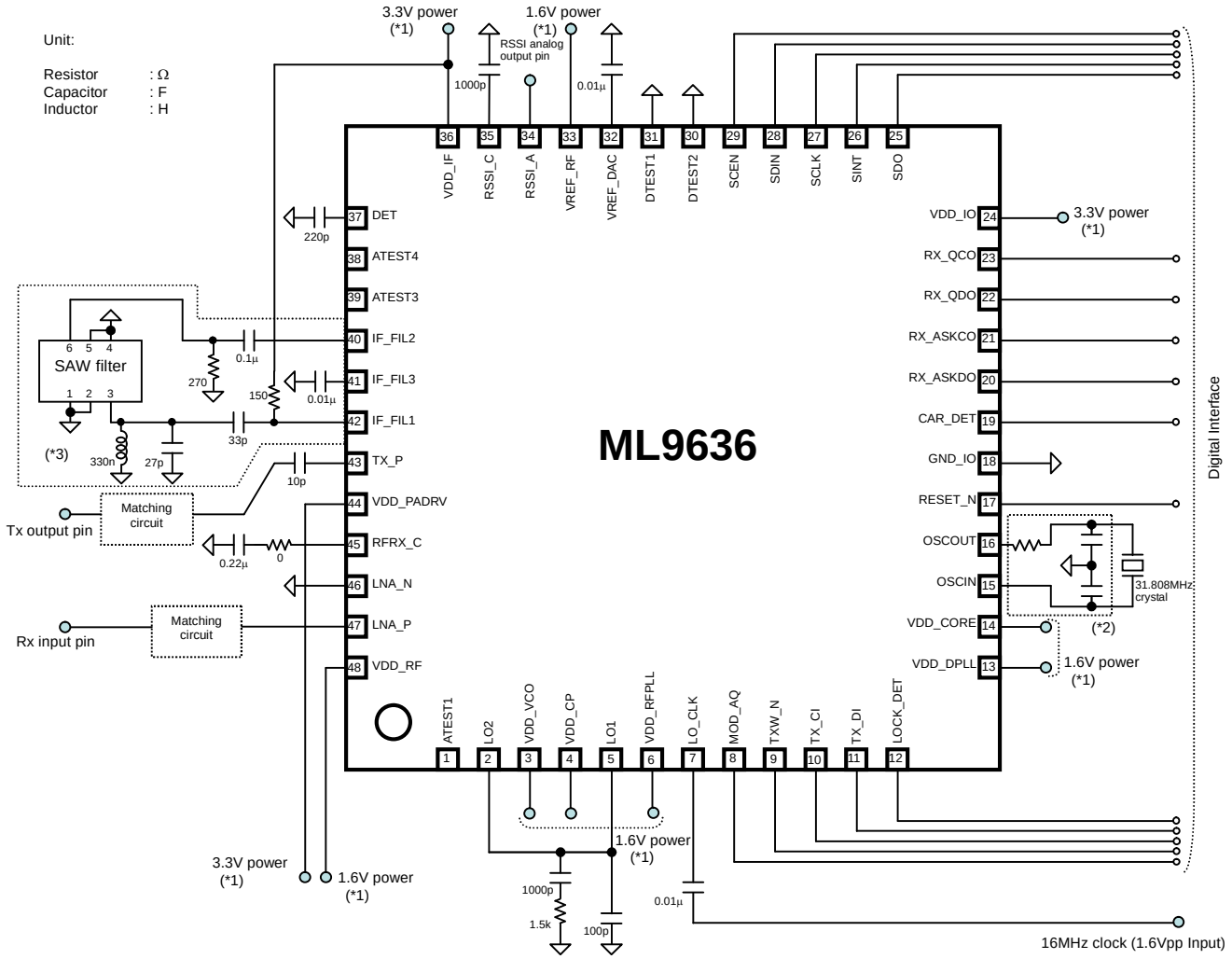


Figure C-1 RF Burst Receive Timing

E. Example of External Circuit

The following figure shows an example of external circuit configuration for the ML9636.



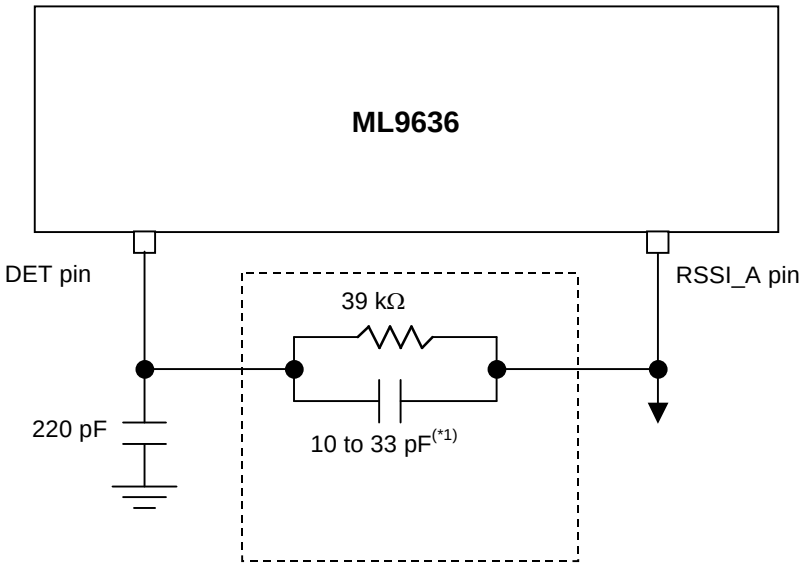
*1 In the figure, the bypass capacitor for each power supply and the one for the VREF_RF pin have been omitted.
*2 Determine the peripheral circuit constants
*3 The circuit and constants between pin 42 and pin 40 show examples when used in combination with the filter MKFCC40M0CC0P00R05 or MKFCC40M0CD0P00R05 manufactured by MURATA Manufacturing. If another filter is used, it is necessary to change the circuit and constants because of the input/output impedance of a filter.

Figure E-1 Example of External Circuit Configuration

F. Example of Improving the demodulation tracking characteristics with respect to a sudden change in the bottom level of a input modulation signal

This section gives an example of an improvement in the demodulation tracking characteristics with respect to a sudden change (when there is a large difference between the 500 kHz component and 1 MHz component) in the bottom level of a input modulation signal during the ASLK receive operation of the ML9636.

As shown in the figure below, the slice level can be optimized by connecting a resistor and a capacitor between the RSSI_A pin and the DET pin.
In that case, it may be necessary to optimize the external components and comparator slice level (SET_RF1 command ASK_SLICE_OFS[2:0] bits).



*1 Depending on the mounting conditions, the value of the parallel capacitor needs to be adjusted so that the reception characteristics will be optimized.

Figure F-1 Example of Slice Level Adjustment Circuit Configuration

G. Notes on Hardware Design

G.1 When Designing Power Supplies

G.1.1 Power-On Sequence

When power is turned on, apply power to the 1.6 V power supplies and the 3.3 V power supplies either at the same time or the 1.6 V power supplies first. In doing so, make the time difference between the power suppliy turned on first and those turned on later within 1 ms. After power-on, satisfy the regulations as to the reset time specified for the RESET_N pin. If the recommended voltage is exceeded at startup, be sure not to release the reset state.

G.1.2 Bypass Capacitor Insertion

G.1.2.1 Example of Bypass Capacitor Insertion

It is recommended that bypass capacitors be inserted in each of the VDD–GND lines, as shown below.

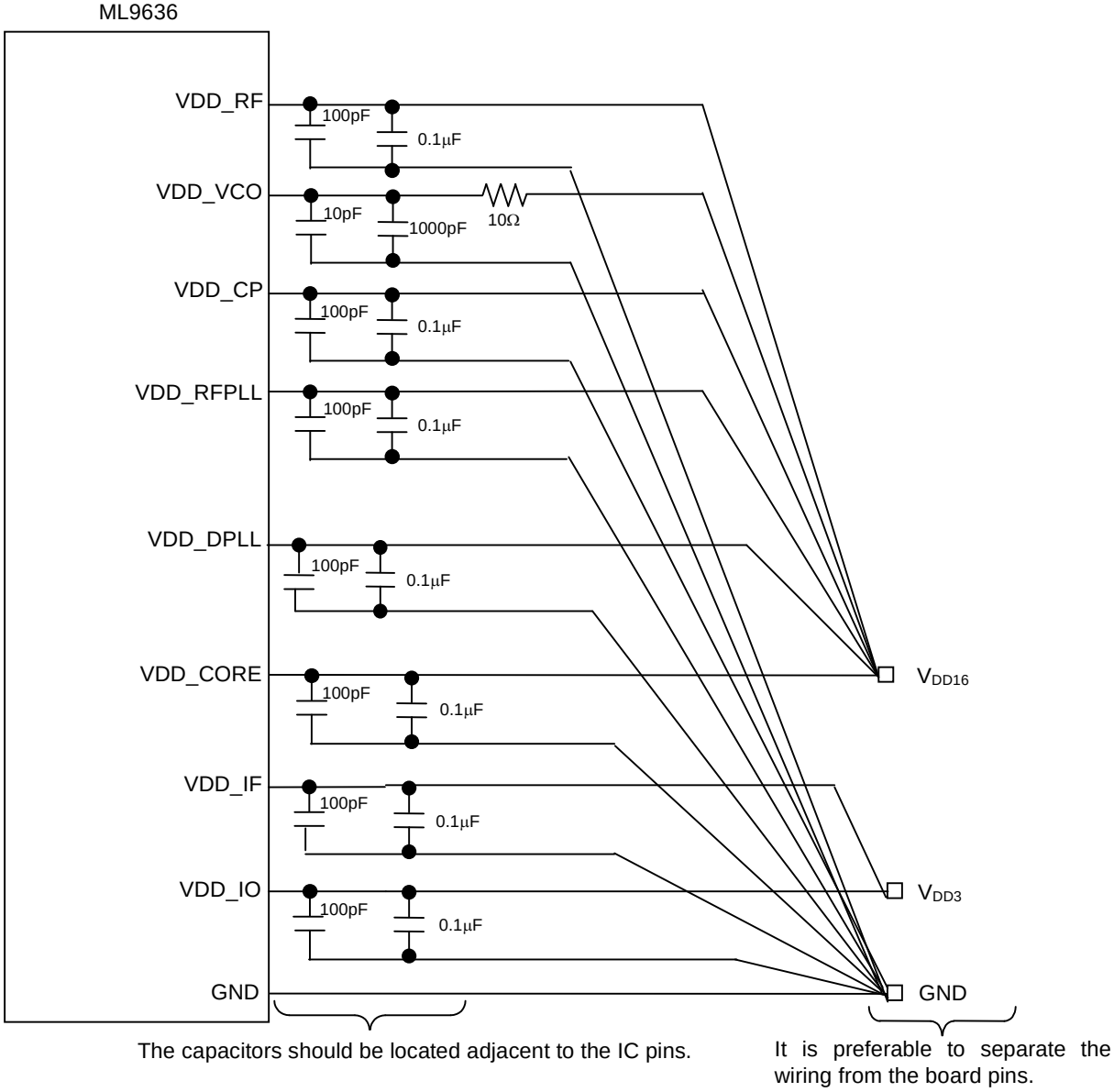


Figure G-1 Example of Wiring around the ML9636 Power Supplies

G.1.2.2 Notes on Inserting Bypass Capacitors

Not the following when inserting bypass cpapacitors:

- For the wiring for VDD and GND, use wider wires than other signal lines.
- Make the wire length between a bypass capacitor and VDD and that between a bypass capacitor and GND as short as possible.
- Make the wire length between a bypass capacitor and VDD and that between a bypass capacitor and GND as equal as possible.

G.1.2.3 Notes on Power Supply Voltages

The power supply voltage conditions are as follows. The recommended operating conditions and all electrical characteristics are specified in this range. If any voltage being outside the range is used, the electrical characteristics may no longer be satisfied or the device may malfuction.
VDD_IO = VDD_IF = VDD_PADRV = 3.15 to 3.45 V
VDD_RF = VDD_VCO = VDD_CP = VDD_RFPLL = VDD_DPLL = VDD_CORE = 1.5 to 1.65 V
When adjusting the transmission power or carrier detection level (CAR_DET_LVL), use a regulator for each power supply because a change in a power supply voltage after correction will accompany a change in the characteristics.

G.2 When Configuring Oscillation Circuits

G.2.1 When Using a Crystal Oscillation Circuit

G.2.1.1 Example of Crystal Oscillation Circuit Configuration

The following figure shows an example of typical configuration of a crystal oscillation circuit.
Determine the definitive constants after evaluation including the floating capacitance of the custormer's board.

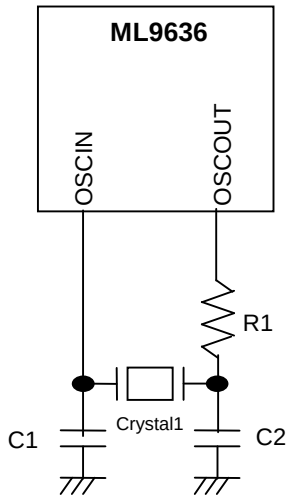


Figure G-2 Example of ML9636 Crystal Oscillation Circuit Configuration

G.2.1.2 Notes on Configuring a Crystal Oscillation Circuit

Note the following when configuring a crystal oscillation circuit:

- The respective values of C1, C2, and R1 need to be set according to the specifications of the crystal resonator (Crystal1) used. In determining those values, evaluate the oscillation characeristics using the resonator having the target frequency on the mounting board and using the actual IC by such means as making a request to a manufacturer of crystal resonators.
- Ensure an accuracy of ±100 ppm or less for the 31.808 MHz master clock while taking temperature fluctuations, power supply voltage fluctuations, and aging into account.
- Do not make any signal line cross over the external wiring pulled out from the OSCIN and OSCOUT pins. Also, do not wire any signal line that carry a large current near the external wiring pulled out from the OSCIN and OSCOUT pins. Surround the periphery of the pins and external components by GND patterns as much as possible so as to make the patterns less subject to noise interference.
- Make the ground point of the capacitors of the oscillation circuit alway have the same potential as GND and do not connect it to a GND that carries a large current.
- Do not supply any signal to another oscillation circuit from this oscillation circuit.

G.2.1.3 Examples of Applicable Crystal Resonators

The table below lists the applicable crystal resonators. OKI does not provide any guarantees as to the operation of them. So, be sure to check the operation on the customer's board before use.

Table G-1 Examples of Crystal Resonators

Manufacturer	Type name	Representative frequency [MHz]	Equivalent resistance [Ω](Max.)	Load capacitance [pF](Min.)	Excitation level [μW](Max.)	Overtone order	Frequency deviation [ppm] (Min.)	Application	Package	Frequency range
Daishinku	DSX321G	30	100	8	300	Fundamental	10	Automotive	SMD	28-50MHz
Daishinku	DSX321GA	30	100	8	300	Fundamental	30	Automotive	SMD	12-40MHz
Kyocera Kinseki	CX5032GA	30	50	12	100	Fundamental	100	Automotive	SMD	25-40MHz

G.2.2 When Configuring an External Clock as the Input to an Oscillation Circuit

G.2.2.1 Example of Configuring an External Oscillation Circuit

The figure below shows an example of configuration where an external clock is intput to the oscillation circuit of this IC.
Determine the definitive constants after evaluation including the floating capacitance of the custormer's board.

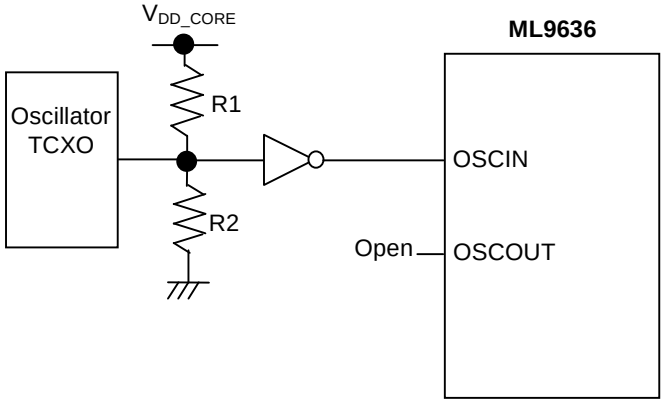


Figure G-3 Example Configuration of ML9636 External Oscillation Circuit

G.2.2.2 Notes on Configuring an External Crystal Oscillation Circuit

Note the following when configuring an external clock as the input to an oscillation circuit:

- The input level at OSCIN is a 1.5 V CMOS input. If the output level of the oscillator used does not satisfy the CMOS input specifications or exceeds a maximum voltage of 1.65 V, insert a buffer for level conversion.
- Leave OSCOUT open.
- Adjust the values of the resistors R1 and R2 so that the amplitude of the output clock of the oscillator (TCXO) satisfies the input threshold level of the buffer.
- The oscillation circuit of this IC has an internal feedback resistor. When inputting an external clock, turn off the feedback resistor by setting bit 4 of the SET_EXT_VCO command to "1" from the serial interface (SCI). If the ML9636 is used without turning off the feedback resistor, no normal reception of an external clock may be available.

G.3 On Designing a High-Frequency Circuit

G.3.1 General Notes

(1) Power supplies
Use stable, ripple-free power supplies.

(2) Patterning
Avoid parallel or cross wiring among signal lines as much as possible, and guard clock signal lines and other signal lines with GND patterns in order not to interfere with other signal lines.

(3) Parts layout
Keep any parts that emit strong signals such as a clock from the periphery of an antenna having a high sensistivity or the input section of an amplifier.

G.3.2 High-Frequency Circuit Design

(1) Loop filter and crystal oscillation circuit section
- Parts
  Select parts whose temperature characteristics are flat and temperature coefficients have been standardized. Some parts of high permittivity type or of semiconductor type may have a large margin of error or have non-linear temperature characteristics.
- Parts layout
  For layout, keep parts away from power supply lines as much as possible in order to avoid interference with the power supply circuit and being interfered with high-frequency noise from the power supply circuit. Also note that an oscillation frequency may drift depending on the floating capacitance of the pattern.

(2) GND
Lower the GND impedance by such means as wiring all around with one GND line and through-hole in order to avoid deterioration of characteristics due to a GND impedance.

(3) Power supply isolation
For voltage supply, it is recommended to isolate the power supply pins between one pin and the next using a filter circuit that uses a coil and bypass capacitors.

(4) Capacitors
For a power supply bypassing capacitor, select one with a value that allows low- to high-frequency components to be bypassed sufficiently enough.
Some capacitors with poor temperature characteristics may spoil high-frequency characteristics or stability due to capacitor dried up at a low or high temperature.

H. Register Setting Procedure

H.1 Example of Activation Procedure at Power-On

The figure below shows the commands that need setting at power on.
Write the values which will be presented from OKI separately to each command registers except the commands that the adjustment is necessary individually.
For the order of setting commands, set the SET_INITIAL command first; there are no restrictions on the setting order as to the other commands.
However, take care not to carry out transmission even if this initialization has been completed, until temperature correction described in Section H.4 is made.

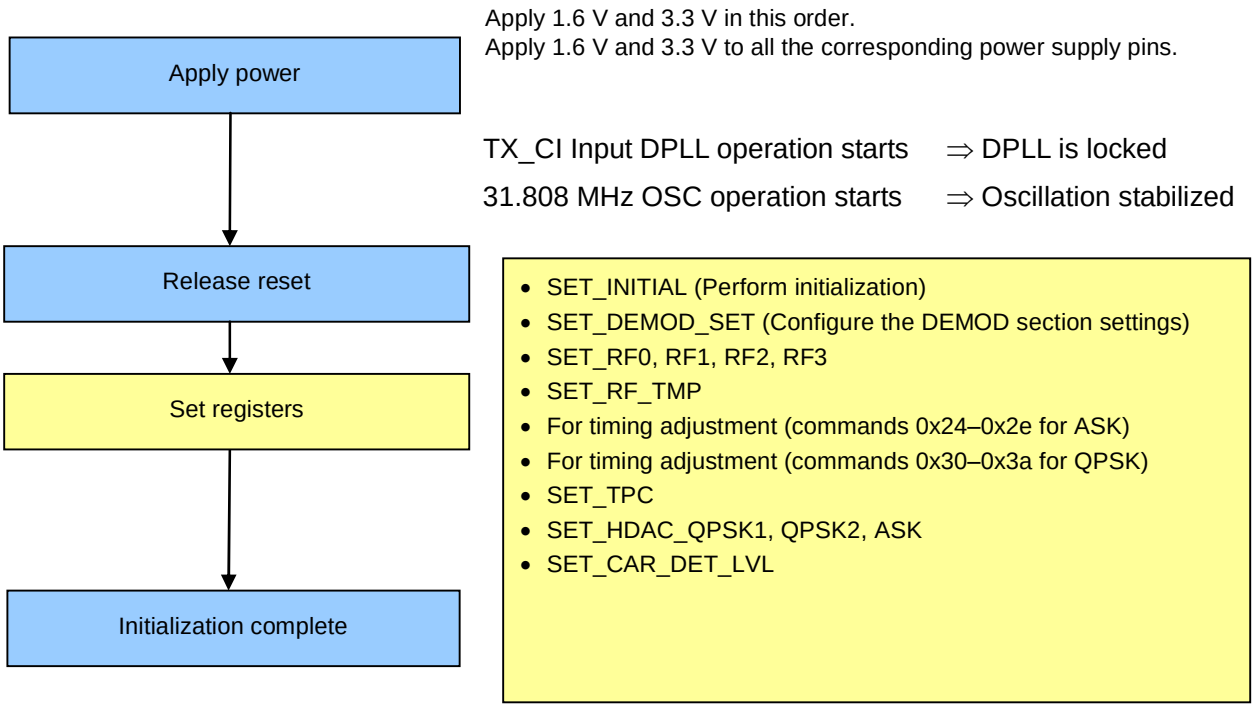


Figure H-1 Example of Activation Procedure at ML9636 Power-On

H.2 Example of Procedure at Power Shutdown

The figure below shows an example of procedure at power shutdown.

When shutting the power down, be sure to make sure that no data is being transmitted, then shut the power down.

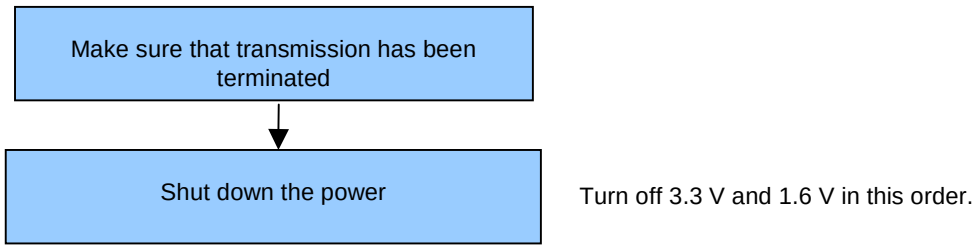


Figure H-2 Example of Procedure at ML9636 Power Shutdown

H.3 Example of Procedure (for Frequency Selection) during Operation

Figure below shows an example of a procedure for selecting a frequency.

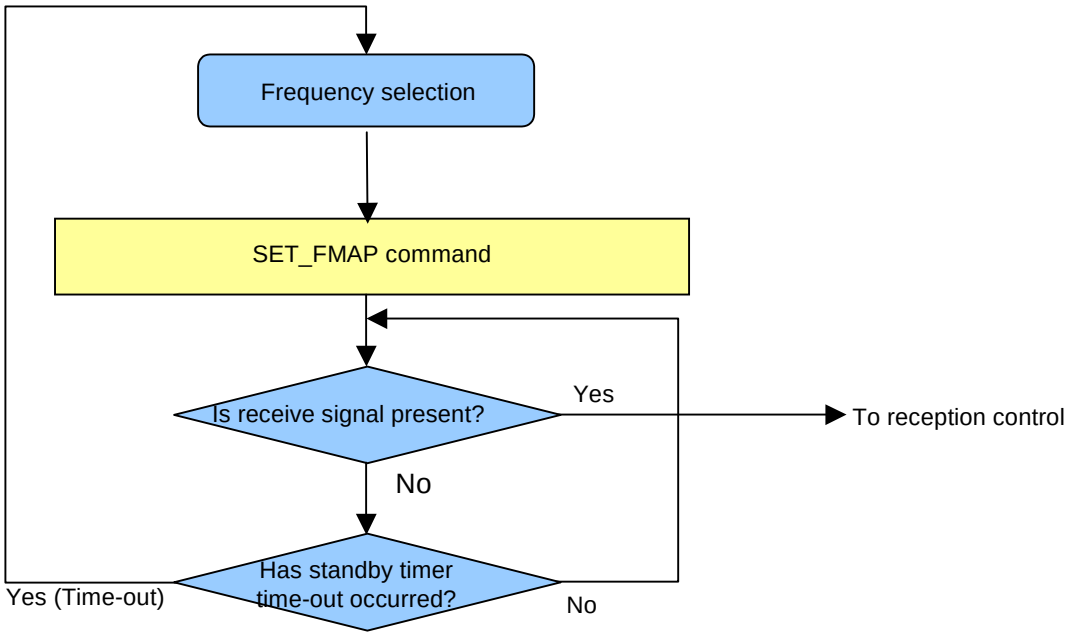
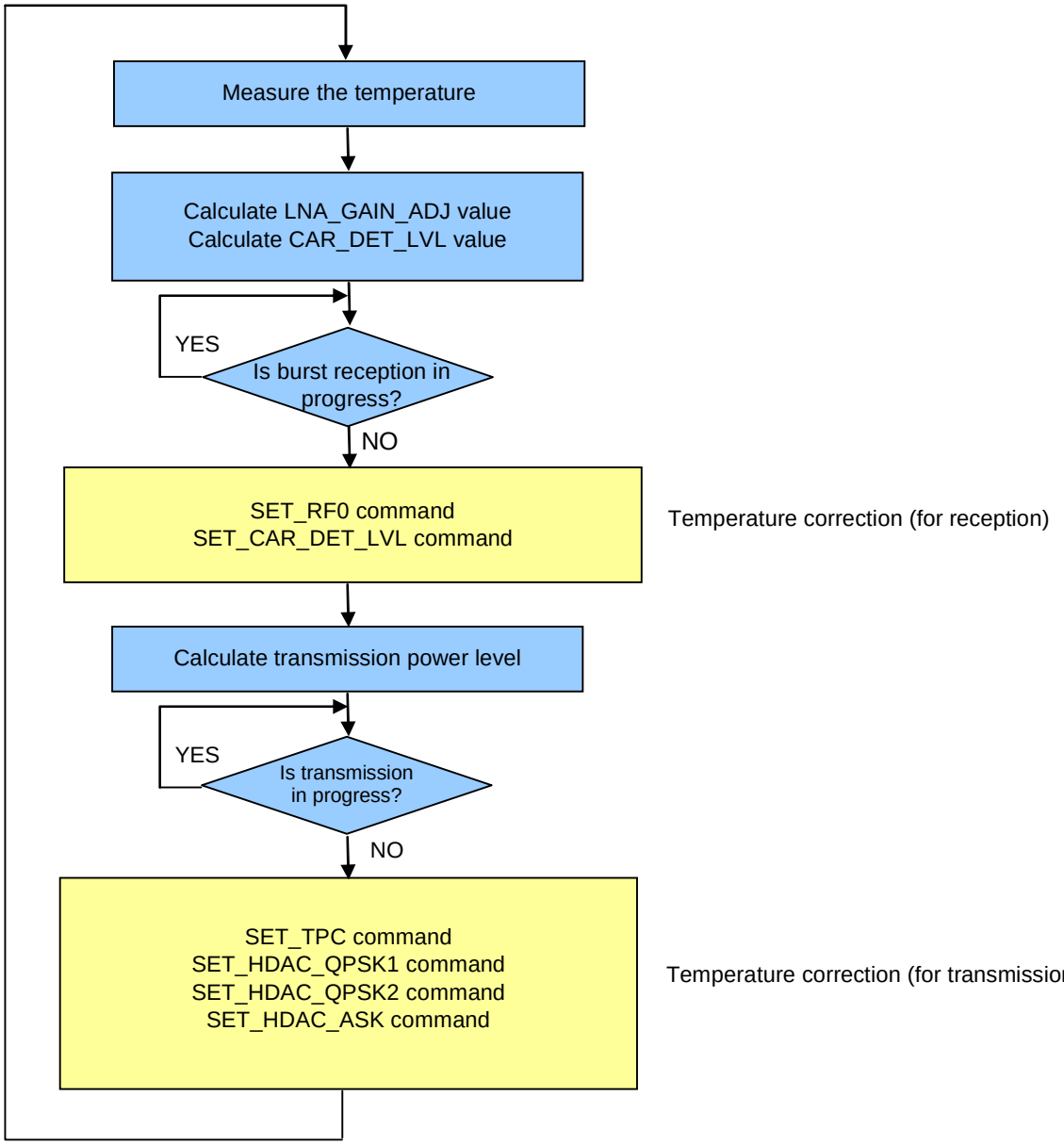


Figure H-3 Example of Procedure (for Frequency Selection) during Operation of ML9636

H.4 Example of Procedure (for Temperature Correction) during Operation

Figure below shows an example of a procedure for correcting a temperature. For how to calculate the value in accordance with the temparature zone to be written to each registers, see Chapter 7 Temperature correction.



- Even during a continuous receiving state, repeat the "temperature measurement⇒re-setting the LNA_GAIN_ADJ and CAR_DET_LVL values, then writing (updating) of the value of transmission power level" operations taking temperature fluctuations in account.
- Do not start transmission before making temperature correction.
- If CAR_DET_LVL is set to an extremely small value, CAR_DET pin may be indicated as "H" even when there is no RF reception signal.

Figure H-4 Example of Procedure (for Temperature Correction) during Operation of ML9636

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEUL9636-01	Jul. 10, 2007	–	–	Preliminary edition 1
PEUL9636-02	Oct. 18, 2007	74	72	Preliminary edition 2 Modify Chapter 5 Modify Chapter 7 Delete Appendix D Modify Appendix H
FEUL9636-01	Jan. 10, 2008	72	72	Formal edition 1 Chapter 5 5.3 DC Characteristics: Modify the DC characteristics of VIH2 and VIL2. 5.4.2(5) SCI Characteristics: Delete the characteristics of SCEN output enable time and disable time.