Model 2015A Spectroscopy Amplifier/Timing SCA

9231694B 01/05

User's Manual

ISO 9001 SYSTEM CERTIFIED

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The information in this document describes the product as accurately as possible, but is subject to change without notice.

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Notes

1. Introduction

The Canberra Model 2015A combines, in one singlewidth module, the functions of a spectroscopy amplifier and a timing single channel pulse height analyzer.

The Model 2015A Amplifier/TSCA uses integrated circuit construction for maximum reliability and simplicity. The entire unit is designed to optimize energy resolution in spectroscopy applications with Ge and Si detectors even at high count rates. The amplifier's restorer includes circuitry for use with optical feedback preamplifiers. The Model 2015's broad gain range (X12 to X1280) makes it equally compatible with high purity Ge, scintillation, photomultipliers, gas proportional and surface-barrier detectors.

The usefulness and application of the Canberra Model 2015A is enhanced by the following unique design features not found in comparable amplifiers: internally selectable shaping time constants of 0.5 µs or 2 µs, count rate optimization with Canberra's unique gated restorer, front panel pole/zero adjustment, a ten turn fine gain control, and low noise design (less than 7 microvolts referred to the input at 2 ms shaping).

The Model 2015A is further enhanced by the addition of a timing SCA contained in the same package, offering two modes of single channel pulse height (energy) analysis. In the SCA mode of operation an SCA OUTPUT is generated whenever the peak value of the unipolar falls between the energy levels defined by the front panel LOWER LEVEL (E) and WINDOW (ΔE) settings. In the Timing (TSCA) mode the SCA OUTPUT is generated for the same E and ΔE conditions except that it is time referenced to the preamp's leading edge. This develops a true leading edge timing technique, while minimizing timing jitter.

In addition to the SCA output the Model 2015A offers a multifunction DISC connector which can be used as a LOWER LEVEL (E) discriminator output, an Upper Level (E + ΔE) discriminator output, or an LLD SWEEP input. One of the three modes is internally selected with jumper plugs.

The Model 2015A has one additional unique feature: a LED indicator electronically linked to the LOWER LEVEL (E) control. The LED indicator is a visual means of adjusting the LOWER LEVEL (E) control above the system noise level.

Both the LOWER LEVEL (E) and WINDOW (ΔE) controls are ten turn potentiometers for maximum accuracy, resolution and resetability. A rear panel switch controls the WINDOW (E) range: 0 to 10 volts, or 0 to 1 volt.

Applications

This section is not intended as a complete survey of applications. It is intended to highlight the most important features of the module and to indicate representative areas where they might be applied.

The Model 2015A overcomes the past necessity of using two individual modules, an amplifier and single channel analyzer, by performing both tasks in one convenient single-width module.

The amplifier's two selectable time constants, 0.5 µs for high count rates and 2 µs for optimum resolution, makes it useful for NaI, Ge(Li), surface barrier and proportional counter applications. Using the amplifier and single channel analyzer outputs, the Model 2015A, in conjunction with a delay module, represents an ideal method for performing energy discrimination. The SCA OUTPUT can gate the multichannel analyzer to control the acceptance or rejection of the amplifier's delayed linear output signal. In addition, the amplifier's output allows the signal to be analyzed by other energy discriminators so that more than one energy band may be selectively studied from the same amplifier.

The Single Channel Analyzer section is used in either the Timing SCA (TSCA) or SCA mode. In the timing mode, the SCA OUTPUT logic pulse is placed consistently in time (200 nanoseconds) past the AMPLifier OUTPUT pulse peak. Thus, the Model 2015A may serve to replace an amplifier and individual timing SCA, sometimes required for coincidence experiments. With its SCA and ULD or LLD DISC outputs, the 2015A Amp/TSCA may be used to identify two different energies or particles depending on the particular setting of the discriminator levels.

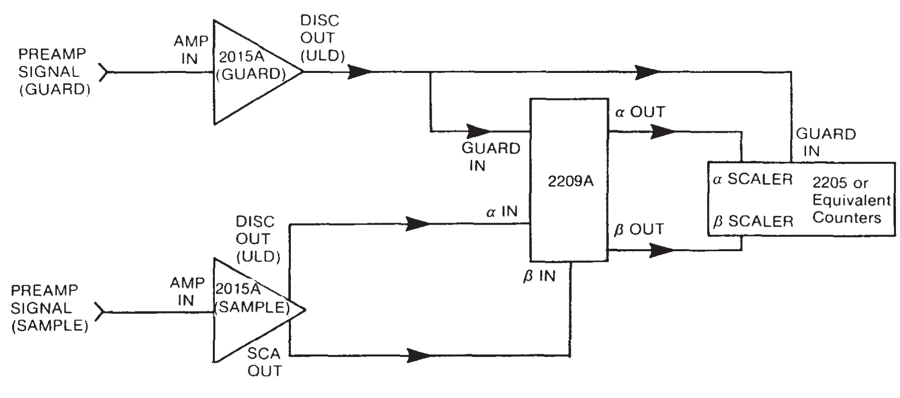
Low Level α/β Counting System

The Canberra LOW BACKGROUND ALPHA/BETA DETECTOR SYSTEM (2200 & 2201) depicts a particular application of the Model 2015A. In this system, two detectors are used in anti-coincidence to distinguish true sample events from cosmic or interference radiation associated with the local environment. The system is ideally suited for measuring isotopes such as ^{14}C, ^{89}Sr, ^{210}Po, and so forth.

There are two Model 2015A Amp/TSCA modules involved in this system configuration. One is used in the guard channel path and the other in the sample channel path. In the guard channel the Model 2015A is used as an amplifier/discriminator combination, where the extremely low threshold setting of the LOWER LEVEL (E) discriminator is used to detect the cosmic events. The Model 2209A, monitoring the guard 2015A DISC (ULD = LLD) output, gates off or inhibits the Scaler/Timer when a cosmic INPUT signal exceeds the LOWER LEVEL (E) threshold.

In the sample channel, the Model 2015A accepts the signal from the preamplifier, shapes, delays and directs it through the SCA section for two simultaneous discriminations. In this application the proportional counter detector is biased to the beta plateau; the output information from the detector is then indicative of both alpha and beta energies. Typically, the Single Channel Analyzer is set such that the SCA OUTPUT represents beta particles and the DISC (ULD) OUTPUT represents alpha particles. the DISC (LLD) OUTPUT represents the sum of the alpha and beta particles.

The desired outputs from the single channel analyzer section are connected to the Model 2209A AUTO FLOW METER and subsequent scalers. Figure 1 shows the SCA and DISC information being routed by the 2209A to the respective scalers indicating alpha and beta events. Both 2015A's use the DISC output to provide ULD information. However, the WINDOW (ΔE) control on the 2015A associated with the cosmic channel is set to 0.00, thus its threshold is equal to that provided by the LOWER LEVEL (E) control. The equipment setup is simplified since the 2015A internal controls are set the same. By utilizing the WINDOW (ΔE) function, the cosmic channel 2015A provides LLD information. The model 2015A's included in this instrumentation makes the Alpha/Beta System a versatile, accurate, and cost effective system.



Block Diagram of 2015A Application in Low Level α/β Counting System.

Figure 1 Block Diagram of 2015A Application in Low Level α/β Counting System

2. Controls and Connectors

Front Panel

This is a brief description of the 2015A's front panel controls and connectors. For more detailed information, refer to Appendix A.

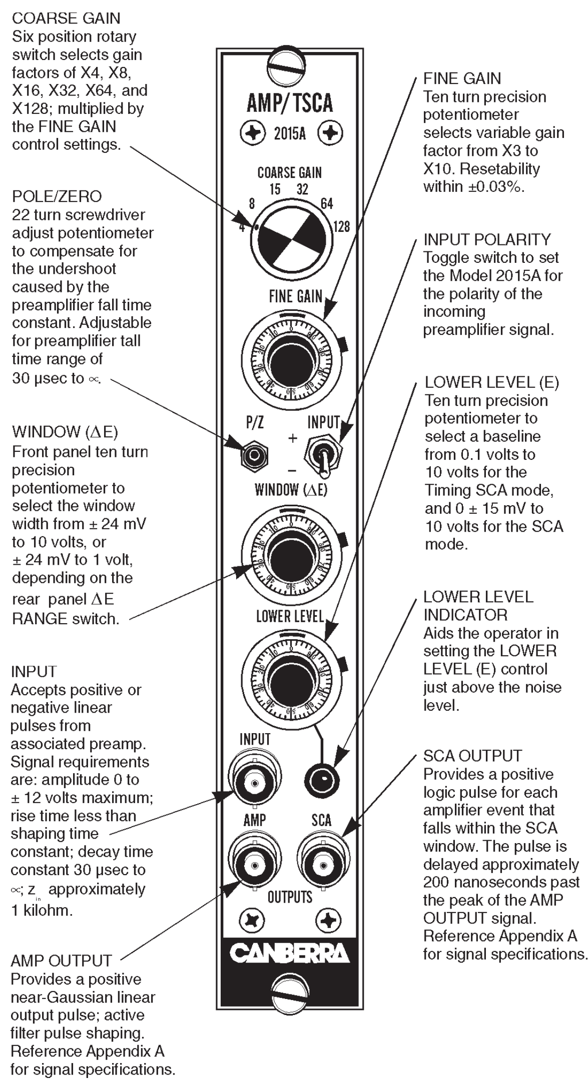


Figure 2 Front Panel Controls and Connectors

Rear Panel

This is a brief description of the 2015A's rear panel connectors. For more detailed information, refer to Appendix A.

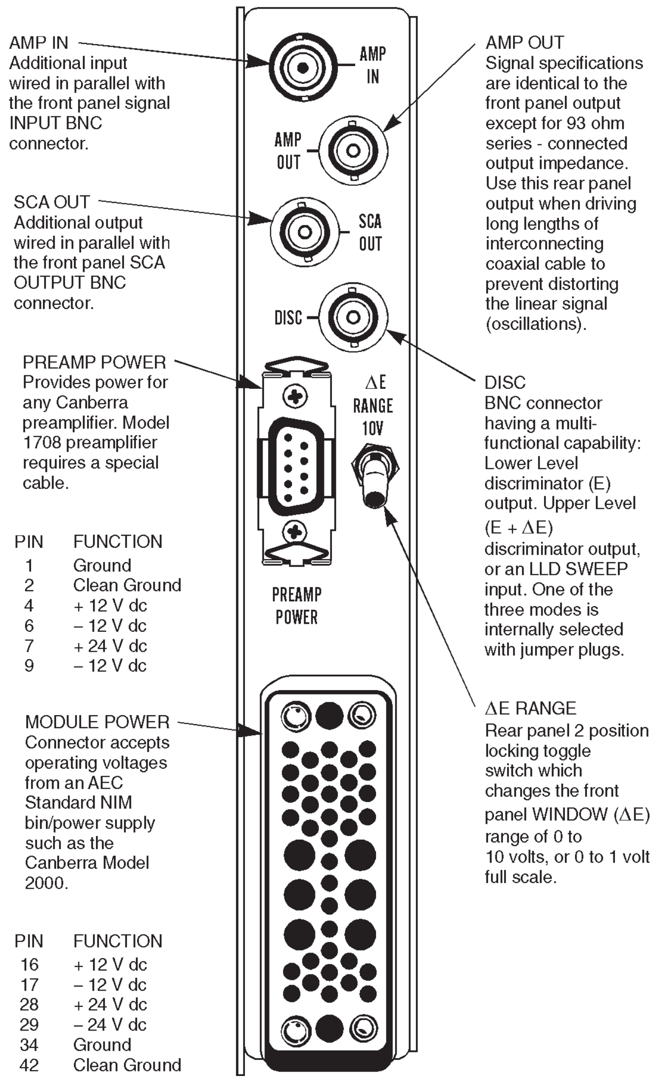


Figure 3 Rear Panel Connectors

Internal Controls

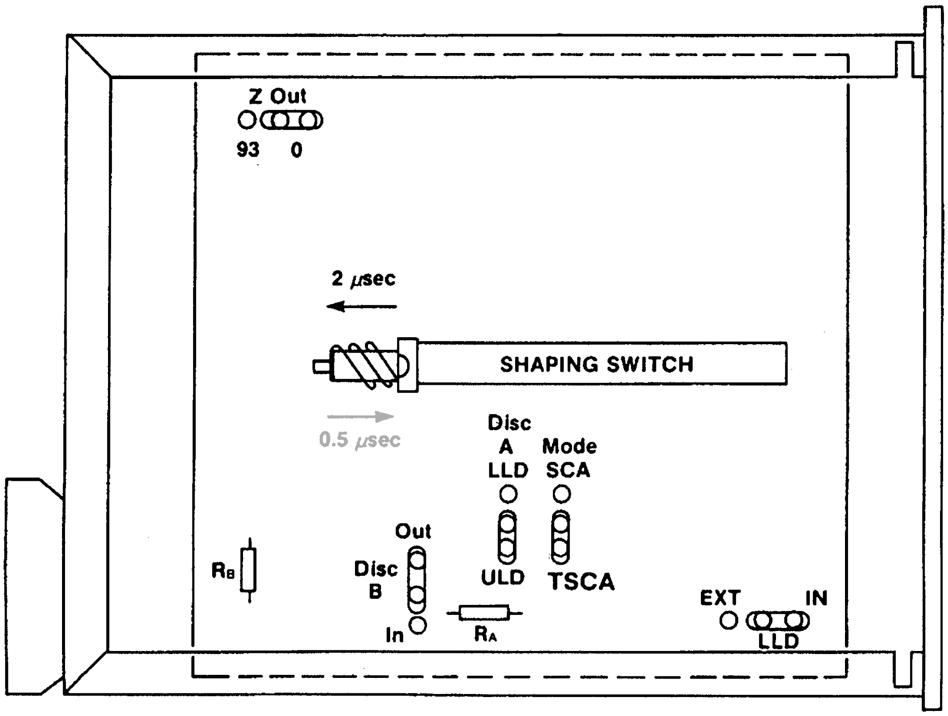


Figure 4 Internal Controls

3. Operating Instructions

The purpose of this section is to familiarize you with the operation and controls of the Model 2015A Amplifier/TSCA so that best performance can be obtained. Since it is difficult to determine the exact system configuration in which the module will be used, explicit operating instructions cannot be given. However, if the following procedures are carried out, you will gain sufficient familiarity with this instrument to permit its proper use in the system at hand.

Spectroscopy System Operation

Setup

A block diagram of a typical Canberra gamma spectroscopy system is shown in Figure 5.

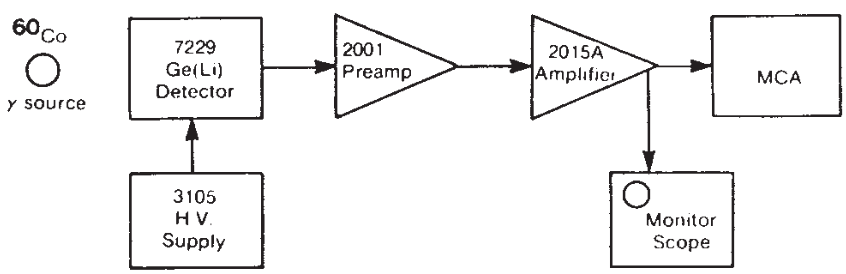


Figure 5 Typical Gamma Spectroscopy System

1. Prior to installation and setup, the internal jumper plugs should be set to their desired positions. See Figure 4 (Internal Controls) on page 6.

   The Z_{OUT} jumper plug controls the output impedance of the front panel (only) AMP OUTPUT. The output impedance can be changed from 0 ohms to 93 ohms. The 2015A is shipped with the front panel output impedance set for ≤ 1 ohm. The rear output has a fixed output impedance of approximately 93 ohms, series connected.

When using the front panel low impedance output, short lengths of interconnecting coaxial cable need not be terminated. To prevent possible oscillations, longer cable lengths should be terminated at the receiving end in a resistive load equal to the cable impedance (93 ohms for type RG-62 cable).

The rear panel 93 ohm output may be safely used with RG-62 cable up to a few hundred feet. However, the 93 ohm output impedance is in series with the load impedance, and a decrease in the total signal range may occur. For example, a 50% loss will result if the load impedance is 93 ohms.

2. Insert the 2015A into a standard NIM BIN. Preamp power is provided by a 9 pin connector located on the 2015A rear panel. Allow the total system to warm up and stabilize.

3. Set the 2015A controls as indicated below:

SHAPING:	2 ms (internal)
COARSE GAIN:	16
FINE GAIN:	2.2

This will give approximately 9 volts output when using a preamp gain of 100 mV/MeV and ^{60}Co radioactive source.

4. Install a “tee” connector on the 2015A AMP OUTPUT. Connect one end of the “tee” connector to the analyzer ADC input. To fully exploit the count rate capabilities of the Model 2015A Amplifier the ADC should be direct coupled. All Canberra ADC’s are dc coupled. Connect the second end of the “tee” connector to an oscilloscope and monitor the AMP OUTPUT.

Performance Adjustments

1. The pole/zero is extremely critical for good high count rate resolution. See note 1 on page 11. Adjust the radiation source count rate between 2 kcps and 25 kcps. While observing the AMP OUTPUT on the scope, adjust the pole/zero so that the trailing edge of the unipolar pulse returns to the baseline with no over or undershoots.

Figure 6 shows the correct setting of the pole/zero control, with Figures 7 and 8 showing under and over compensation, respectively for the preamplifier decay time constant. Notice some small amplitude signals with long decay times in Figure 6. These are due to charge trapping in the detector and cannot be corrected by the pole/zero control.

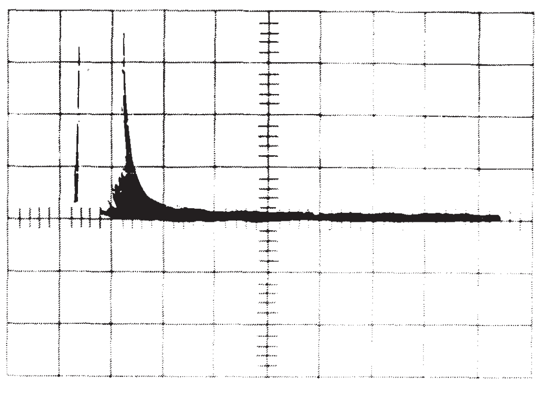


Figure 6 Correct Pole/Zero Compensation

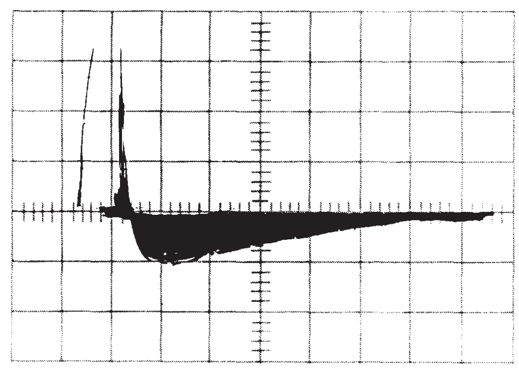


Figure 7 Undercompensated Pole/Zero

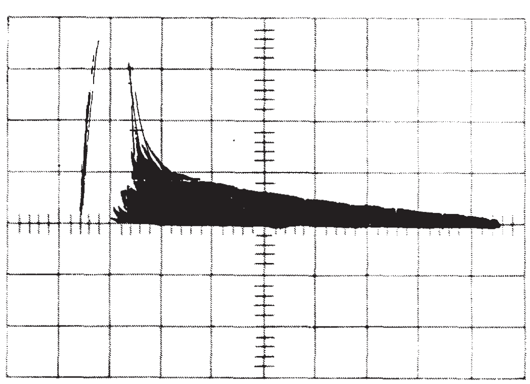


Figure 8 Overcompensated Pole/Zero

Scope
Vertical: 50 mV/cm
Horizontal: 10µs/cm

Source ^{60}Co
1.33 MeV peak: 9 V amplitude
Count rate: ≈ 3kcps
Shaping: 2 µs

2. Pole/zero adjustment using a square wave and preamp test input. See note 2 on page 12.

   Driving the preamp test input with a square wave, will allow a more precise adjustment of the amplifier pole/zero.

   a. The Amplifier's controls should be basically set for its intended application: COARSE GAIN, shaping, INPUT POLARITY.

   b. Adjust the square wave generator for a frequency of approximately 1 kHz.

   c. Connect the square wave generator's output to the preamp's TEST INPUT.

   d. Remove all radioactive sources from the vicinity of the detector.

   e. Set the scope's channel 1 vertical sensitivity to 5 volts/cm, and adjust the main time base to 0.2 ms/cm. Monitor the 2015A's AMP OUTPUT and adjust the square wave generator's amplitude control (attenuator) for output signals of ± 10 volts.

Note Both positive and negative near-Gaussian linear pulses will be observed at the output.

   f. Reduce the scope vertical sensitivity to 50 mV/cm. See Note 1 on page 11.

      Figure 9 shows the correct setting of the pole/zero control. Figures 10 and 11 show under and over compensation, respectively for the preamplifier decay time constant. As illustrated in Figure 9, the AMP OUTPUT signal should have a clean return to the baseline with no bumps, overshoots or undershoots.

Figure 9 Correct Pole/Zero Compensation

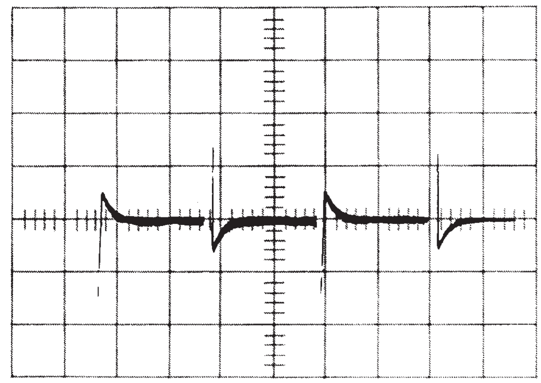


Figure 10 Undercompensation Pole/Zero

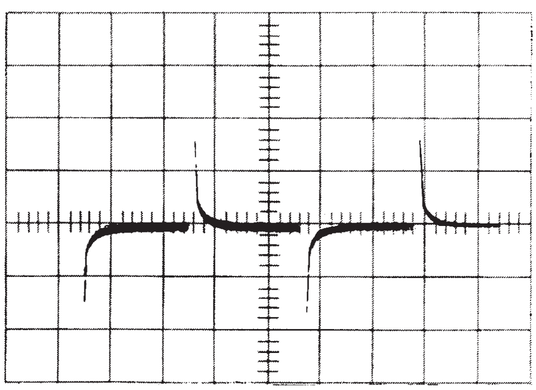


Figure 11 Overcompensation Pole/Zero

Scope
Vertical: 50 mV/cm
Horizontal: 0.2 µs/cm

Source
Square wave pulse and preamp test input.

3. HPGe detectors and Si Systems with Optical Feedback Preamps.

For normal Si Systems, the pole/zero is usually set at ∞ fully counterclockwise. However, on some systems, the pole/zero may need to be slightly tweaked for optimum overload recovery when responding to the preamps reset pulse.

Note 1: At high Count rates the pole. zero adjustment is extremely critical for maintaining good resolution and low peak shift. For precise and optimum pole/zero setting, a scope vertical sensitivity of 50 mV cm should be used.

Higher scope sensitivities can also be used, but result in a less precise pole zero adjustment. However, most scopes will overload for a 10 volt input signal when the vertical sensitivity is set for 50 mV/cm. Scope overload will distort the signals recovery to the baseline. Thus the pole/zero will be incorrectly adjusted resulting in a loss of resolution at high count rates. To prevent scope overloading a clamping circuit, such as the one illustrated in Figure 12 can be used at the scope input.

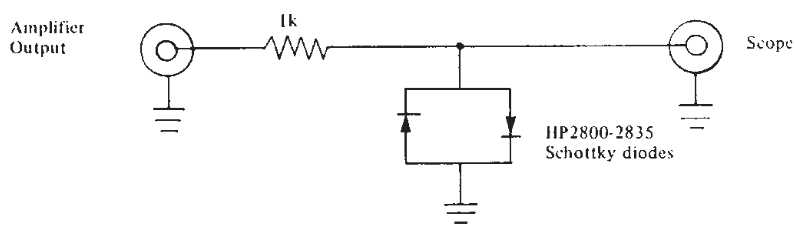


Figure 12 Scope Input Clamp

Note 2: When adjusting the pole/zero using the square wave technique, the calibration square wave generated by the oscilloscope can be used Most scopes generate a 1 kHz square wave used to calibrate the vertical gain and probe compensation. Connect the scope CALIBRATION output through an attenuator to the preamp test input and repeat Performance Adjustments step 2 (pole/zero adjustment).

4. The AMP OUTPUT DC level is factory calibrated to 0 ± 5 millivolt.

5. To get optimum resolution. the Lower Level Discriminator on the MCA ADO should be set just above the noise so that the effects of pileup are minimized.

Resolution Versus Count Rate and Shaping

A 2 µs shaping is optimum for Ge(Li) detector systems over a wide range of incoming count rates. For high resolution larger shaping time constants offer a better signal to noise ratio, resulting in better resolution. However, as the count rate increases, the effects of pileup degrade the resolution much sooner. The optimum shaping time constant depends on the detector (such as its size, configuration and collection characteristics), preamplifier and incoming count rate. Below is a list of optimum shaping time constants for some other common detectors.

Detector	Optimum Shaping (µsec)
Scintillation Pholomultiplier	0.5
Gas Proportional Counters	0.5 through 2
Silicon Surface-Barrier	0.5 through 2
Lithium Dialed Germanium [Ge(Li)]	2 through 4
Cooled Silicon	8 through 12

The Model 2015A is factory set for 0.5 or 2 µs shaping time constants. However, the shaping time constants can be changed to 8 and 12 µs to be compatible with cooled Silicon detectors. Change the components as follows:

1. Change C1 from 560 pF to 9100 pF
2. Change C2 from 1600 pF to 560 pF
3. Change R1 from 19.1 k ohms to 226 k ohms
4. Change R2 from 52.3 k ohms to 11 k ohms
5. Change C3 from 130 pF to 2000 pF
6. Change C4 from 360 pF to 1300 pF
7. Change C5 from 200 pF to 2400 pF
8. Change C6 from 510 pF to 1600 pF
9. Change C25 from 47 pF to 1000 pF
10. Change C26 from 200 pF to 510 pF
11. Change C76 from 390 pF to 1800 pF
12. Change R143 from 604 k to 499 k ohms
13. Change RV12 from 20 k to 50 k ohms

All resistors are RN60Cs and capacitors are 1% silver mica or 1% ceramic NPO. (See Figure 13)

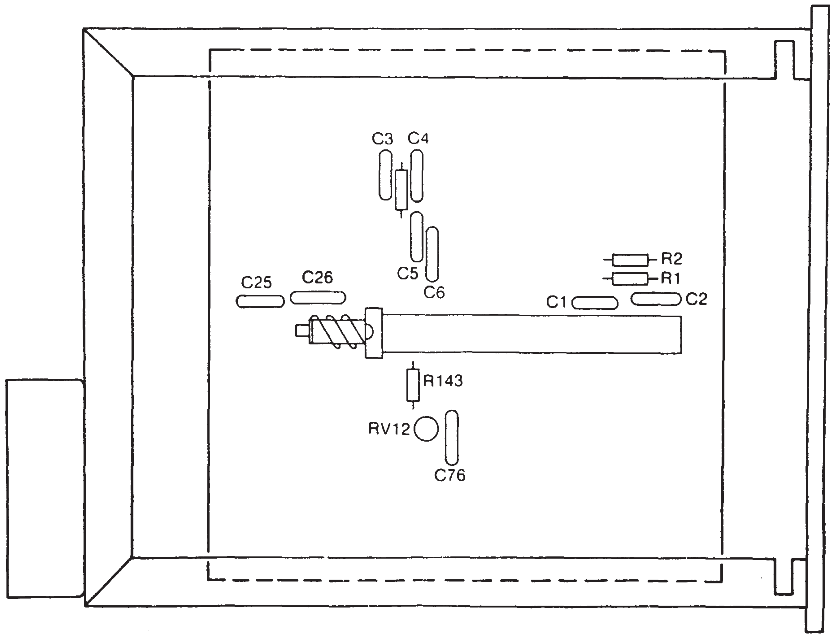


Figure 13 Internal Shaping Components

Resolution Destroying Interfaces

1. Vibration transmitted to the detector and cryostat. This can be through the floor or mounting, as well as direct audio coupling through the air. Vibration isolators in the mounting and sound absorbing covers around the detector can reduce this problem.

2. The close proximity of a radio station can be picked up by the “dipstick” of the cryostat. Good contact between the dipstick and the cryostat can often help solve this problem. Beware of grounding the cryostat and dipstick as this may increase power line frequency (50 or 60 cycle) ground loops.

3. Ground Loops: power line frequency interference can be caused by long cable connections between the detector, preamplifier, and shaping amplifier. There is no general solution for this problem. As a first step, the preamp should use the power supplied by the main shaping amplifier. Second, the system should have a single point house ground. For example, on a general system connect the NIM Bin to house ground via the ac line cord. Isolate all other equipment requiring ac voltage from the house ground. Connect all chassis’ in the system to the grounded NIM Bin using heavy braided wire.

4. High voltage power supplies: generally, the HVPS should float from power line ground with the only ground being made at the preamplifier through the high voltage connecting cable.

5. Analyzer EMI: if the detector is located within about 6m (20 feet) of a multichannel analyzer containing a ferrite core memory, it can receive EMI (electro-magnetic interference). This is due to high memory core currents during the memory cycle of the analyzer. The only practical cure for this problem is to operate the analyzer in the “Live” Mode of accumulation. In this way, the memory cycle only operates while no signal is being analyzed.

6. Is the output of the spectroscopy amplifier and the input of the ADC fully compatible? This may seem an obvious consideration, but it is commonly overlooked. The shaping time constant as stated on the spectroscopy amplifier is not the rise time of its output signal. In the case of a Model 2015A Amplifier, the time-to-peak of the AMP OUTPUT is 1.75X the shaping time constant. Therefore, a 12 µs shaped pulse required 21 µsec to reach full amplitude. Many analyzers will not handle this; instead of analyzing the peak of the signal, they analyze a percentage of the rise time.

7. Amplifier parasitic oscillations. If the cable connecting the front panel outputs of the amplifier to the ADC exceed about 3m (10 feet) in length, oscillations can occur. The cure is to use RG-62 cable (93 ohm impedance) and terminate the ADC end of the cable with a 93.1 ohm metal film resistor. Alternatively, the 93 ohm output impedance of the amplifier can be used with no terminator.

SCA Operation

Setup

1. Connect the INPUT of the 2015A to the ATTEN OUTPUT of a reference pulser, such as the Canberra Model 1407.

2. Connect the AMP OUTPUT signal to channel 1 of an oscilloscope. Connect the SCA OUTPUT to channel 2 of an oscilloscope. Simultaneously observe both outputs on the oscilloscope, or observe the AMP OUTPUT on a multichannel analyzer. Set the oscilloscope vertical sensitivity for 5 V/cm and sweep speed to 1 µs/cm.

3. Set the 2015A controls as indicated below:

   SHAPING: 2 µs

COARSE GAIN:	16
FINE GAIN:	2.2
INPUT POLARITY:	(+) Pos
LOWER LEVEL (E):	5.00
WINDOW (E):	1.00
ΔE RANGE	10 V

4. Set thp internal jumpers as indicated below:

Disc A	LLD
Disc B	OUT
Mode	TSCA
LLD	INT

5. Set the 1407 pulser output polarity to POS. Adjust the 1407 pulser PULSE HEIGHT until the 2015A AMP OUTPUT attains an amplitude of 4 volts.

6. Adjust the 2015A pole/zero as outlined in "Performance Adjustments" on page 8.

7. Slowly increase the pulser PULSE HEIGHT until the 2015A SCA OUTPUT is just observed. Measure the AMP OUTPUT visually on the oscilloscope or on a calibrated multichannel analyzer and compare with the LOWER LEVEL (E) setting. The AMP OUTPUT signal should have an amplitude of 5.0 ± 0.1 volts.

8. Increase the 1407 PULSE HEIGHT until the 2015A SCA OUTPUT just begins to disappear. Again measure the AMP OUTPUT visually on the oscilloscope or on a calibrated multichannel analyzer. The AMP OUTPUT signal should have an amplitude of 6.0 ± 0.1 volts.

9. Very the LOWER LEVEL (E) and WINDOW (ΔE) settings and repeat steps 7 and 8; a plot of the AMP OUTPUT versus LOWER LEVEL (E) or WINDOW (ΔE) settings will give the linearity curves, which should be within ±0.25% of full scale or ± 25 mV.

10. Connect channel 2 of the oscilloscope to the rear panel DISC output. When the AMP OUTPUT signal on channel 1 of the oscilloscope, exceeds the LOWER LEVEL (E) discriminator setting a positive logic pulse will appear.

11. Change the DISC A jumper plug to the ULD position. Monitor the rear panel DISC output with channel 2 of the oscilloscope. When the AMP OUTPUT

signal, on channel 1 of the oscilloscope, exceeds the LOWER LEVEL (E) plus the WINDOW (ΔE) discriminators, a positive logic pulse will appear. Change the DISC A jumper plug back to the LLD position.

12. Change the DISC B jumper plug to the IN position and the LLD jumper plug to the EXT position. The LOWER LEVEL (E) discriminator function will no longer be controlled by the front panel LOWER LEVEL (E) control. The function will now be controlled by an external voltage of 0 to + 10 volts at the rear panel DISC BNC. Change the DISC B jumper plug back to the OUT position and the LLD jumper plug to the INT position.

Reference Data on Cables

Figures 14 and 15 show a typical output pulse at the load end of the designated RG-58 cable, and the same point using RG-62 cable. In each case Figures 14 and 15 show high impedance (1 kΩ) and 50 Ω termination conditions. Clearly the fastest, cleanest pulse is realized with the RG-58 cable. With the source match provided, loading effects are limited to amplitude changes only. RG-58 cable is therefore recommended for best compatibility with the DISC and SCA OUTPUTS.

RG-58 cable:	R_{source} = 50 ohms
Upper Trace:	R_{load} = 1k ohms
Lower Trace:	R_{load} = 50 ohms
Scope:	Horizontal = 0.1 µs/cm

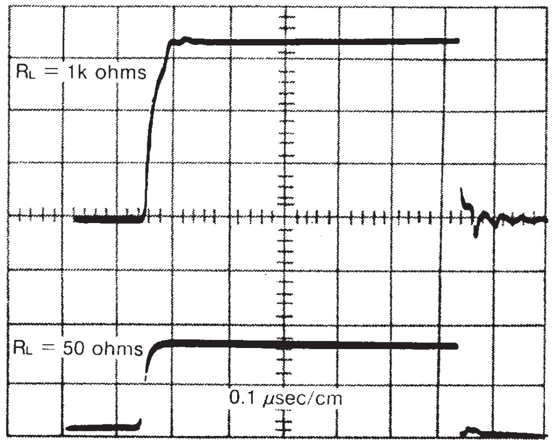


Figure 14 Typical Output Pulse Using a RG58/U Cable

RG-62 cable:	R_{source} = 50 ohms
Upper Trace:	R_{load} = 1k ohms
Lower Trace:	R_{load} = 50 ohms
Scope:	Horizontal = 0.1 µs/cm

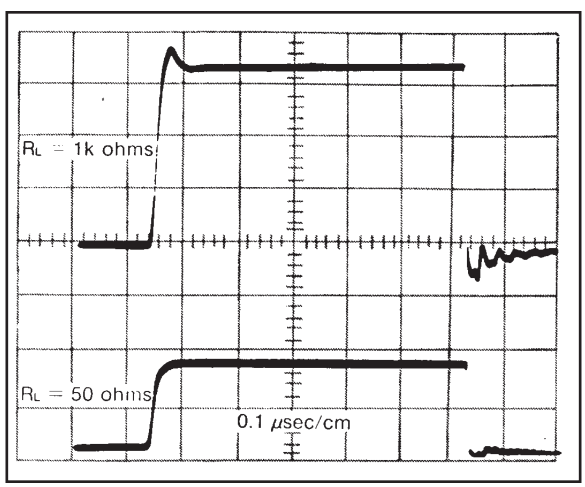


Figure 15 Typical Output Pulse Using a RG62/U Cable

The Figure 16 shows the same pulses with a source mismatch caused by driving the cables with the transistor switches directly. The waveforms indicate how important and effective source matching is in eliminating instabilities which cause phenomena such as multiple counting or triggering. For this reason the Model 2015A provides source matched outputs.

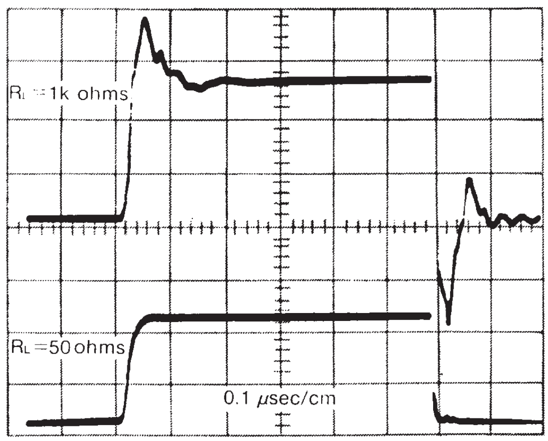


Figure 16 Typical Output Pulse with a Source Mismatch

Upper Trace:	R_{load} = 1k ohms
Lower Trace:	R_{load} = 50 ohms
Scope:	Horizontal = 0. 1 μs/cm

Preventative Maintenance

Preventative maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Remove power from the unit before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because of access holes in the NIM wrap, DO NOT use any liquids to clean the wrap, side or rear panels.

4. Performance Check

The purpose of this section is for checking the performance of the Model 2015A AMP/TSCA. The checkout will serve to verify that the module is in good operating order. If the Model, 2015A should not meet the performance requirements given in this procedure, it is strongly suggested that the unit be sent back to the factory for calibration and/or repair. The instructions which follow are directed primarily toward the Model 2015A only. Please refer to the Instruction Manuals of the other equipment used if questions or difficulties in their use arise.

Equipment Required

In order to perform the checkout procedure detailed in subsequent steps, the following equipment (or equivalents) will be required:

1. Canberra Model 2000 BIN/Power Supply
2. Canberra Model 1407 Reference Pulser
3. Calibrated dual trace 100 MHz oscilloscope (Tektronix 454, 475 or equivalent)
4. RMS Noise Meter (Hewlett Packard HP-400H or equivalent)
5. 4-1/2 digit, ± 0.1% full scale accuracy Digital Voltmeter (Data Precision 3500, or equivalent)
6. Resistive Voltmeter Probe (1k ohms in series)
7. Current Meters

NIM Voltage Check

With a DVM, measure the NIM Power Supply voltages and adjust if they are outside of the following ranges:

+24 V dc	+23.98 to +24.02 V dc
–24 V dc	–23.98 to –24.02 V dc
+12 V dc	+ 11.99 to + 12.01 V dc
–12 D dc	– 11.99 to –12.01 V dc

Current Measurements

Apply power to the 2015A and measure the currents. They should be within the following ranges:

+24 V dc	40 to 0 mA
+12 V dc	150 to 170 mA
– 12 V dc	60 to 80 mA
– 24 V dc	40 to 60 mA

Note: A greater deviation in currents indicates a faulty unit. Gross errors would probably be due to faulty or reversed capacitors, shorted or open AMP Output transistors, etc.

Amplifier Operational Checks

Setup

1. Set controls as follows:

Model 2015A Controls:

COARSE GAIN:	4
FINE GAIN:	10
SHAPING:	2 µs (internal)
POLE ZERO:	fully CCW
INPUT POLARITY:	POS

Model 1407 Controls:

PULSE HEIGHT:	5.4
NORMALIZE:	10
POS/NEG:	POS
LINE/OFF/90 Hz:	90 Hz
RISE TIME:	MIN
FALL TIME:	400 µs
ATTENUATION:	X10

2. Connect a 93 or 100 ohm terminator to the 2015A rear panel INPUT.

3. Connect the 1407 ATTEN OUTPUT to the 2015A front panel INPUT with RG-62 coax cable.

4. Connect the 1407 NORMAL OUTPUT to the EXT TRIG input of the scope. Set the scope triggering to EXT, (+).

Outputs

1. Connect the AMP OUTPUT to the scope with RG-62 coax cable using a "tee" connector at the scope. You should observe the near-Gaussian shaped linear pulse shown in Figure 17.

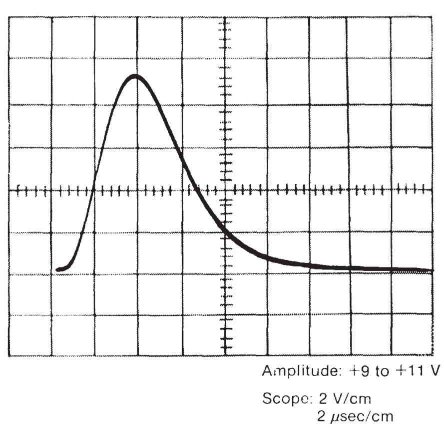


Figure 17 Amp Output Showing a Near Gaussian Shaped Pulse

2. Adjust the 1407 PULSE HEIGHT until the AMP OUTPUT amplitude is + 9.9 to +10.1 volts.

3. Place jumper plug J4 in the 93 ohm position. Connect a 93 ohm terminator to the “tee” connector at the scope input. The amplitude of the pulse should be +4.8 to –5.2 volts. Remove the 93 ohm terminator.

4. Place jumper plug J4 in the 0 ohm position.

5. Connect the 93 ohm terminator; the amplitude should not decrease by more than 100 mV. There should be no discernible distortion in the pulse shape. Remove the terminator.

6. Remove all 1407 ATTENUATION. The AMP OUTPUT pulse should be clamped at +11.5 to +12.5 volts.

7. Set the 1407 ATTENUATION to X10.

Pole/Zero Adjustment

1. Set the 1407 FALL TIME to 50 µs.

2. Observe the AMP OUTPUT on the scope and adjust the pole/zero control so that the tail of the unipolar pulse returns to the baseline as fast as possible with NO under or overshoot, as in Figure 18.

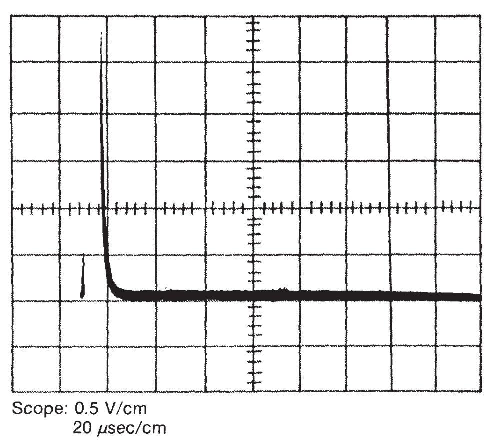


Figure 18 Pole/Zero Adjust

Coarse and Fine Gain Controls

1. Set the 2015A COARSE GAIN to 128; FINE GAIN to 10.0.

2. Connect the AMP OUTPUT to the scope with RG-62 coax cable.

3. Set the 1407 ATTENUATION to X500. Adjust the Model 1407 PULSE HEIGHT until the AMP OUTPUT pulse attains an amplitude of +9.9 to +10.1 volts.

4. Measure the AMP OUTPUT on the scope for each COARSE GAIN setting. The amplitudes should, reduce proportionately with each COARSE GAIN setting.

5. Set the 2015A CORSE GAIN to 128.

6. Monitor the AMP OUTPUT on the scope and turn the 2015A FINE GAIN control to minimum. The signal amplitude should decrease by approximately 2/3.

7. Return the FINE GAIN to maximum.

Shaping Checks

1. Set the 2015A to 2 µs shaping.

2. Set the 1407 ATTENUATION to X500. Adjust the 1407 PULSE HEIGHT until the AMP OUTPUT pulse attains an amplitude of +9.9 to +10.1 volts.

3. Observe the AMP OUTPUT pulse on the scope. For each of the shapings (2.0 µs and 0.5 µs), the unipolar pulse should appear as in Figure 19.

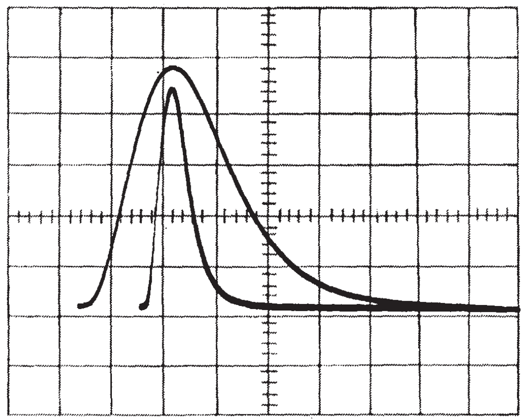


Figure 19 AMP OUTPUT Showing a an Unipolar Pulse

Noise Measurement

1. Set the 2015A controls as follows:

   COARSE GAIN: 16

   SHAPING: 2 µs

2. Connect a 93 ohm terminator to the 2015A rear panel signal INPUT BNC connector.

3. Put side covers on the Model 2015A.

4. Using RG-62 coax cable, connect one side of the “tee” connector to the Model 1407 pulser ATTEN OUTPUT. Using RG-62 coax cable, connect the other end of the “tee” connector to the scope input. You will observe a positive tail pulse on the scope. Set the 1407 ATTENUATION to X10 and adjust the 1407 PULSE HEIGHT until the tail pulse attains an amplitude of 100 mV.

5. Monitor the 2015A AMP OUTPUT on the scope and adjust the pole/zero for no under or overshoots, see Figure 18. Adjust the 2015A FINE GAIN for an OUTPUT pulse amplitude of +9.9 to +10.1 volts.

6. Remove the “tee” connector and cables from the 2015A INPUT. Leave the 93 ohm terminator on the rear panel INPUT. Set the 1407 LINE/OFF/90 Hz switch to OFF. Connect the AMP OUTPUT to the Noise Meter with RG-62 coax cable and measure the noise. It should be 0.58 mV maximum for an averaging meter and 0.66 mV for a true rms voltmeter.

Linearity Check

Integral nonlinearity is a measure, expressed in percentage, of maximum deviation when a straight line is compared to an OUTPUT versus input plot. The OUTPUT is exercised over its full dynamic range. A test for nonlinearity can be conducted using the resistive summing network shown in Figure 20.

The test is performed by first adjusting the amplifier gain, polarity and pulser attenuation so that a negative ten volt (NORMAL) pulser OUTPUT produces a positive 10 volt amplifier OUTPUT. The pulser NORMAL OUTPUT should be –10 volts coincident with the amplifier OUTPUT peak. Next, while observing the summing point on the oscilloscope, the amplifier fine gain is carefully adjusted to bring the vertical gain should be set to obtain the desired resolution.

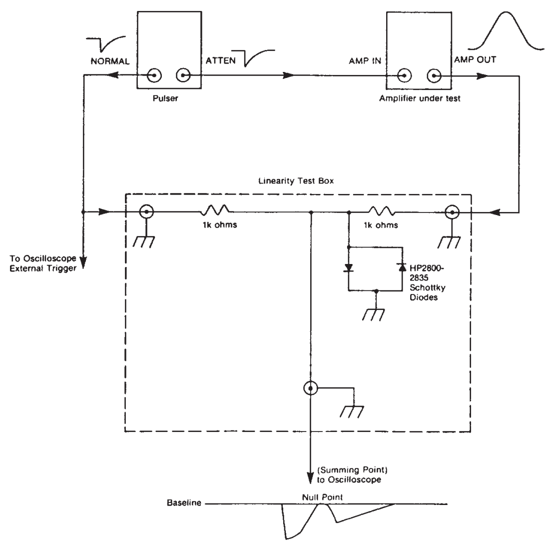


Figure 20 Test Setup, Linearity Check

Note: The Model 1407 must be modified for a 20 V OUTPUT for this test.

When this condition is obtained, turn the 1407 PULSE HEIGHT control downward from ten volts to the lowest level that will still trigger the oscilloscope, and observe the maximum difference between the baseline and the null point. The integral nonlinearity of the amplifier under test is then equal to:

$$\frac{\text{Maximum deviation in volts} \times 2 \times 100\%}{10 \text{ volts}}$$

The maximum deviation must be less than ± 2.5 mV in order to meet the ± 0.05% specification.

As the input is decreased, the amplifier gain should remain constant (OUTPUT should decrease linearly); whether or not it does is tested by comparing the OUTPUT to a signal known to decrease linearly with the amplifier input; the pulser's direct OUTPUT meets this requirement since it is related to the amplifier input by a passive attenuator. The factor of two must be included because the summing network also serves as a voltage divider decreasing the apparent deviation by a factor of two.

Note that nonlinearity and instability in the pulser OUTPUT do not enter into the measurement, because both direct and attenuated outputs will be affected identically, save for negligible effect of the pulser's attenuator instabilities over the short time period required for the test. Instabilities in the baseline level on the oscilloscope null point equal with the baseline. The oscilloscope are due to oscilloscope triggering, dc level fluctuations and noise, and need not be of concern in this test.

SCA Operational Checks

If the SCA section of the 2015A needs to be recalibrated, it is strongly suggested that the unit be sent back to the factory.

Setup

1. Set the 2015A controls as follows:

LOWER LEVEL:	1.0
WINDOW:	12
LLD (J5):	INT
SCA MODE (J6):	TSCA
DISC A (J7):	ULD
DISC B (J8):	OUT
ΔE RANGE:	10
COARSE GAIN:	4
FINE GAIN:	MAX
SHAPING:	2 µs

3. Connect the ATTEN OUTPUT of the 1407 to the 2015A INPUT.

4. Set the 1407 PULSER FALL TIME to 50 µs, RISE TIME to MIN, ATTEN to X10, and the LINE/OFF/90 Hz switch to 90 Hz.

5. Adjust the 1407 PULSE HEIGHT until the AMP OUTPUT on the 2015A attains an amplitude of approximately 9 volts.

6. Set the LOWER LEVEL (E) discriminator to 1.0 volts and the WINDOW (ΔE) discriminator to 10.0 volts.

Outputs

1. Connect the SCA OUTPUT to the scope with RG-58 coax. You should observe a positive logic pulse with the following parameters:

Amplitude	4.5 to 5.5 volts
Width	350 to 650 nsec
Rise/Fall Time	25 nsec Max.

2. Place the DISC A jumper plug in the ULD position; the DISC (ULD) OUTPUT should disappear.

3. Set the rear panel ΔE RANGE switch to 1V; the DISC (ULD) OUTPUT should reappear.

4. Return the RANGE to 10 V.

5. The front panel LOWER LEVEL indicator should be dimly illuminated.

Timing Walk Test

1. Set the ΔE RANGE switch to 10 V, LOWER LEVEL (E) discriminator to 0.10 volts and the WINDOW (ΔE) to 10.0 volts.

2. Adjust the Model 1407 PULSE HEIGHT until the AMP OUTPUT attains an amplitude of 10.0 volts (or maximum with an SCA OUTPUT).

3. Observe the SCA OUTPUT leading edge on the scope. Increase the 1407 ATTENUATION by X50 and measure the leading edge walk. It should be 50 nsec maximum.

4. Move the MODE jumper to the SCA position. Adjust the 1407 PULSE HEIGHT for a 2015A AMP OUTPUT of 10 volts. Vary the LOWER LEVEL (E) discriminator; the SCA OUTPUT pulse will move in time as a function of the LOWER LEVEL (E) discriminator; i.e., the SCA is no longer a timing SCA. Set the MODE jumper plug back to the TSCA position.

External Lower Level Check

1. Place the LLD jumper plug in the EXTernal position and the DISC B jumper in the IN position.

2. With a jumper wire, connect the +5 volt supply to the rear panel Disc BNC.

3. Adjust the 1407 PULSE HEIGHT for a flickering SCA OUTPUT

4. Measure the AMP OUTPUT amplitude, it should be 4.5 to 5.5 volts.

Normal Internal Control Settings

Verify that the shaping switch and all jumper plugs are in the desired position before replacing the side covers. The following listing is a guide to the usual positions of the jumpers (see Figure 4):

Zout	0
LLD	INT
SCA MODE	TSCA
DISC A	LLD
DISC B	OUT
SHAPING	2 µs

5. Circuit Description

This section of the manual contains a description of the circuitry used in the Model 2015A Amplifier/Timing SCA. Components are referred to by “reference designations” such as Q2, C5, and R10. Throughout the following circuit analysis, refer to the block diagram and circuit schematics located in the drawings section.

Block Diagram Description

The signal flow is as follows:

The Amplifier

The preamp signal enters either the front panel INPUT BNC (J1) or rear panel INPUT BNC (J101). The INPUT signal is differentiated (by C1 or C2 and the appropriate amplifier input resistance, selected by S2) and pole zeroed by RV1 and R1 or R2. The differentiated signal is amplified by gain amplifiers K1 and K2. Amplifier K1 is either inverting or noninverting depending on the INPUT POLARITY switch (S2) position. The amplified signal is next integrated by the complex pole integrator. The integrated signal is used to drive the combination OUTPUT amplifier, real pole integrator and dc restorer. The processed signal is then connected to the SCA and front and rear panel BNC connectors, J3 and J102, respectively.

The SCA Section

The AMPlifier OUTPUT signal is connected to the LLD and the ULD discriminators A13 and A9. The LLD DISCriminator reference voltage is generated from +12 volts by R114, RV4, and RV5, and buffered by A15. The ULD reference voltage is the sum of the LLD reference and the voltage picked off of RV6. The voltage developed across RV6 is generated by current source Q27. The ULD reference voltage range is selected by the rear panel toggle switch S101.

The fast amplified signal (OUTPUT of gain amp K2) is ac coupled to the FAST DISCriminator, A14. The FAST DISCriminator utilizes the LLD voltage modified by A16 as its reference. The leading edge information from the FAST DISC (A14) and LLD DISC (A13) outputs is extracted by the subsequent pulse-former circuits. Jumper plug J6 selects the FAST DISCriminator of LLD DISCriminator to trigger the timing monostable A7a. When A7a times out, its subsequent pulse-former triggers monostable A71b. If monostable A7b was enabled, it will generate as SCA OUTPUT pulse.

The enable for monostable A7b is generated by the LLD DISCriminator setting flip flop A6b/A6c. At the conclusion of the SCA OUTPUT pulse, flip flop A6b/A6c is cleared via A8a and Ab. If the AMP OUTPUT pulse, exceeds the ULD reference voltage, its OUTPUT clears timing monostable (A7a) and flip flop A6b/A6c, terminating the SCA OUTPUT pulse cycle. The SCA OUTPUT driver provides the additional drive capability required for driving 50 ohm terminated lines. The SCA OUTPUT pulse is connected to the front and rear panel BNC connectors, J2 and J103 respectively, through 47 ohm resistors.

Monostable A11b is triggered by the LLD or ULD DISCriminators, selected by J7, providing the respective OUTPUT DISC pulse at BNC J104. With the aid of jumper plugs J8and J5, the rear panel DISC BNC (J104)can also be used as an LLD sweep input.

The timing monostable trigger pulse, OUTPUT of A8c or A6a, also triggers monostable Alla providing a drive signal for LED DS1. LED DS1 is provided asa visual aid for setting the LOWER LEVEL (E) control.

Description of Circuit

Gain Amplifier

Most of the gain (K1 and K2) is accomplished before the integration occurs. As a result the input amplifier K1 is the dominant noise source. Each of the two gain stages operate at relatively low closed loop gains providing stable operation with time and temperature.

Amplifiers K1 (Q14 through Q19) and K2 (Q8 through Q13) are both basically the same configuration. Therefore only K1 will be fully described.

The differential input pair Q19 drives the common base transistors Q18 and Q15. Transistors Q18 and 015 operate at low current levels, providing a high OUTPUT impedance to drive the OUTPUT transistors Q17 and Q14 through the common source FET Q16. The necessary current to drive the FET and circuit capacitance at high frequencies is derived directly from the input transistor Q19, through the low impedance of Q18 and Q15. This gives a typical slew rate for the amplifier of 140 volts per microsecond. C12 provides feedback for closed loop stability, and allows the amplifier to follow a 100 nanosecond rise time input signal with very low distortion. Since the gain amplifiers do not require dc stability and are operated as inverting amplifiers, a constant current source is not needed in the emitters of Q19. Transistors Q17 and Q14 are biased on by R30 and R33, with the junction of R31 and R32 providing the low impedance OUTPUT.

Input Amplifier K1

The differentiation network, POLE/ZERO cancellation circuitry and INPUT POLARITY selection are located at the inverting input of K1. The SHAPING switch S3 (sections S1 through S3 and P1 through P3) selects the passive differentiator capacitors C3, C4, and pole/zero control RV1 sets the degree of pole/zero compensation. INPUT POLARITY is selected by switch S2. For (–) input polarity, gain is determined by R23 and R15. With (+) input polarity, the gain is determined by the combination of R23, R15, R12, and R13. Diode D1 is a fast switching protection diode for overload signals, enhancing good overload recovery.

Gain Amplifier K2

Amplifier K2 is an inverting gain amplifier. Its gain is controlled by the ratio of the series combination of input resistors R46 through R51, selected by the COARSE GAIN switch S1a (section R1), and the feedback resistor R65. The base-emitter of Q31 is reverse biased as a zener diode. It, and diodes D3, D4 and base-collector of Q31 provide overload protection, enhancing good overload recovery. Capacitor C35 ac couples the signal to the amplifier summing junction. Front panel control RV2, resistors R92 and R65 form the feedback network which controls the FINE GAIN function.

Integrator Amplifier A5

ACTIVE INTEGRATOR A5 provides complex pole pairs where the locus of poles are equidistant from the abscissa on the S-plane. The real part of the complex poles equal that of the input differentiator. The real pole of the last integrator is 1.6 times this value. Active filter networks for A5 are selected by the SHAPING switch S3 (sections Cl, C2, C3, and El, E2, and E3) for the desired time constant.

Amplifier A5 is a wide band, high slew rate, integrated circuit operational amplifier. It is connected in a non-inverting configuration with a dc gain of 2, determined by R5 and R6.

The OUTPUT of integrator A5 is connected through an RC filter network, R17, R24, and C15 back to the summing junction of gain amplifier K2. The integrator also serves as a buffer providing the necessary dc stabilization for gain amp K2.

Amp OUTPUT Integrator and Driver

The unipolar OUTPUT amplifier is comprised of A3 and a power OUTPUT driver Ql, Q2, and 03. Integrated circuit A3 is a wide band, high slew rate operational amplifier. The overall amplifier (op-amp and driver) provides an inverting gain of 2 with single pole integration (C25, C26,and R35) to minimize noise introduced after the ACTIVE INTEGRATOR A5.

The OUTPUT driver transistors are connected Class “AB”. Diodes D11, D14, and current source Q2 form the biasing network for the OUTPUT transistors.

Diodes D12 and D13 provide short circuit protection. With an improper load connected to the OUTPUT, the voltage drop across R71 and R72 forward bias diodes D12 and D13 respectively. For this condition, the respective OUTPUT transistor is bypassed, the OUTPUT current is derived from the op-amp and limited to approximately ± 200 mA. Diodes D9 and D10 provide limiting preventing OUTPUT transistors saturation which prohibits base-emitter charge storage, enhancing good overload recover.

Two AMP OUTPUTS are provided. The front panel OUTPUT provides either ≤ 1 ohm or 93 ohm OUTPUT impedance, drive up to 10 feet of 93 ohm coax cable where the 93 ohm OUTPUT can drive a few hundred feet. The rear panel has a fixed 93 ohm series-connected OUTPUT impedance.

Restorer

The restorer circuitry consists of OUTPUT amplifier A3, transistor array Al, a dual differential comparator A2 and transistors Q4 through Q7, Q29 and Q30. The restorer is a transconductance type amplifier that is; it monitors the AMP OUTPUT (TP1) OUTPUT voltage and develops a constant current of correct polarity at its OUTPUT (junction of Q4 collector and A1e pin 15). The voltage on C24 is buffered by FET Q6 and summed in at A3 pin 3, forcing the AMP OUTPUT (TP1) to 0 volts maintaining the baseline. The AMP OUTPUT signal (TP1) is clamped by diode network D15 and D16 and connected to the comparator input A2 pins 5 and 2. If A2 detects a signal, its OUTPUT turns Q29 off. Q7 switches on a current sufficient to back bias current source A1a disabling the restorer. Capacitor C40 ac couples the transistor Q29 preventing potential restorer latch up problems.

The negative restorer gate threshold is set at –100 mV by resistors R103 and R100. The positive threshold is variable and depends on the coarse gain switch setting S1a (section R2), and resistors R94 through R99. Pot RV3 adjusts the restorer offset and AMP OUTPUT (TP1) to 0 ± 5 mV dc.

SCA Section

SCA OUTPUT

In the following discussion, Logic “l” is referred to as a high voltage level of +2.4 to +5 volts. A Logic “0” is referred to as a low voltage level of 0 to +0.8 volts.

The OUTPUT of GAIN AMP K2 is ac coupled, through C64, to the fast discriminator A14. The differentiated signal is also attenuated by 2.5 through resistors R126 and R127. If the signal exceeds the fast discriminator threshold, A14 pin 2, its OUTPUT goes to a logic “1" which drives the pulse former Al2d and A8c. If the SCA mode jumper plug J6 is in the TSCA position, the OUTPUT of A8c is inverted by Al2e and connected to the true input of A7a. The positive trigger pulse sets A7a’s OUTPUT to a logic “0”, R146 and C78 prevent A7a from retriggering on multiple inputs. The time duration A7a remains set is determined by shaping switch S3 (B1 through B3), component R143, R144, RV11, RV12, and C76. The OUTPUT of A7a will return to a logic “1” approximately 200 nanoseconds past the peak of the AMP OUTPUT signal. Longer SCA OUTPUT delays are obtainable by readjusting RV11 and RV12 for 2 µs and 0.5 µs shaping respectively.

When monostable A7a times out and its OUTPUT returns to a logic “1”, A7b pin 9 is triggered from the positive transition supplied by pulse former A8d and A12b. If enabled by flip flop A6b/A6c, monostable A7b generates a 500 nanosecond SCA OUTPUT pulse. The AMP OUTPUT signal is attenuated by 2.5 and connected to the LOWER LEVEL and the WINDOW discriminators A13 and A9 respectively. If the AMP OUTPUT signal crosses the LLD discriminator threshold, its OUTPUT (A13 pin 7) goes to a logic “l ”. Pulse former Al 2a and A6a extracts the positive transition and sets flip flop A6b/A6c. The OUTPUT of A6c pin 8 is inverted by Al 2f and enables A7b to generate the internally selectable by J4. The low OUTPUT impedance can 500 nanosecond SCA OUTPUT pulse when triggered. If the AMP OUTPUT signal also exceeds the WINDOW (ΔE) discriminator threshold the SCA OUTPUT pulse is aborted. Flip flop A6b/A6c is reset removing A7b’s enable and clearing A7a ending its time out. A8a and A8b also monitor the SCA OUTPUT and during each OUTPUT pulse reset flip flop A6b/A6c and monostable A7a, arming them for the next cycle.

The OUTPUT of monostable A7b is inverted by Q20 with Q21 and Q22 forming a pair of complementary low OUTPUT impedance emitter followers. The SCA OUTPUT pulse is brought out through the two 47 ohm resistors R164 and R165 to the front and rear BNC connectors respectively. The SCA OUTPUT is nominally +5 volts (unterminated), however will increase to approximately +8 volts (unterminated) is resistor R_B (3.9 k ohms) is removed.

When in the TSCA mode, monostable A11a is triggered by the fast discriminator (A14) “OR” Lower Level discriminator A13. The “OR” function is made possible by diodes D25 and D26. When in the SCA mode, the fast discriminator is not used and monostable A11a is triggered by the Lower Level discriminator only. Monostable A11a provides a drive signal for the front panel LOWER LEVEL (E) LED. Its time constant is approximately 100 µs, allowing the LED to be discernible to the eye when indicating amplifier input events. The front panel LED is a user aid, determining the noise threshold of both the fast and LLD discriminators.

When the SCA MODE jumper plug (J6) is in the SCA position the timing monostable (A7a) is now triggered from the LLD discriminator. The SCA OUTPUT will be generated as before, however the timing information is lost. The timing monostable trigger point is now dependent on the AMP OUTPUT signal rise time and LOWER LEVEL (E) discriminator setting.

Disc Output

Depending on the DISC A (J7) jumper plug position, the DISC OUTPUT can provide LLD or ULD information. With the DISC A jumper plug (J7) in the LLD position, DISC monostable A11b is triggered from the lower level discriminator through pulse-former Al2a and A6a. Monostable A11b generates a 500 nanosecond pulse every time the AMP OUTPUT signal crosses the LOWER LEVEL (E) discriminator threshold. If the DISC A jumper plug (J7) is in the ULD position, monostable A11b is triggered through inverter A12c from the WINDOW discriminator. Monostable A11b is inverted by Q23 with Q24 and Q25 forming a pair of complementary low OUTPUT impedance emitter followers. The DISC OUTPUT is nominally +5 volts (unterminated); however will increase to approximately +8 volts (unterminated) if resistor R_A (3.9k ohms) is removed.

Lower Level (E) Threshold Circuit

The raw +12 volts is attenuated by a 3:1 divider network composed of R114, RV4, and RV5. RV4 is calibrated so that 4 volts appears across RV5. Some fraction of this voltage is picked off, using the LOWER LEVEL discriminator control (RV5), and buffered by the high input impedance amplifier A15. The, OUTPUT of A15 provides the reference voltage for the LOWER LEVEL discriminator A13.

When the DISC B jumper plug (J8) is connected to the IN position and the LLD jumper plug (J5) connected to the EXT position, control of the LOWER LEVEL (E) discriminator is now possible by an external voltage source (0 to +10 volts) through the rear panel DISC BNC.

The external sweep input voltage is attenuated by the 2.5:1 divider network R167 and R168. This voltage is buffered by amplifier Al 5 providing an external reference voltage for the Lower Level discriminator A13. RV7 calibrates the low end of the LOWER LEVEL (E) adjustment range.

Window (∆E) Threshold Circuits

Here the raw +24 volts is used to generate the WINDOW (E) reference voltage. Transistor Q27 is a current source generating a current through the WINDOW (E) control (RV6). Resistors R118, pot RV8, and transistor Q28 are used to bias the current source. Transistor Q28 also provides a temperature compensation for Q27. The ULD Cal pot (RV8) is adjusted for 4 volts across RV6. Pin2 of the WINDOW (∆E) potentiometer is connected to the OUTPUT of the LOWER LEVEL (E) discriminator buffer amplifier, A15; thus the voltage developed across RV6 is summed with the LOWER LEVEL reference voltage. Some fraction of this additive voltage is picked off using RV6, buffered by A10, and connected to A9 pin 2 providing the WINDOW (∆E) reference voltage. Resistors R122, R123, and diode D20 form a 5 volt clamp preventing the buffer Amp OUTPUT, A10, from exceeding +5 volts. RV9 nulls out the window buffer amp (A10) OUTPUT offset.

Fast Discriminator Reference Voltage

Op-amp A16 generates a reference voltage, having a nonlinear characteristic for fast discriminator (A14). R109 through R1 13 sets up a bias voltage of approximately –80 mV. When the LOWER LEVEL (E) discriminator is less than 100 mV, diode D19 becomes reversed biased and the junction of R110 and R1 09 is held at approximately –80 mV. This is attenuated to approximately –20 mV by R109 and R1 13 and represents +90 mV when referenced to the AMP OUTPUT signal. Diode D18 clamps the OUTPUT of A16 pin 6 to +600 mV, preventing A16 from saturating. As the LOWER LEVEL (E) control is increased above 100 mV, diode D19 begins to conduct increasing the fast discriminator reference voltage. Further increases in the LOWER LEVEL (E) control cause further increases in the fast discriminator reference voltage. This relationship continues until the junction of R110 and R109 reaches approximately –600 mV at which point diode D17 becomes forward biased, clamping the amplifier OUTPUT. Op-amp A16 will no longer track the LLD control, the fast discriminator reference voltage has reached its upper limit, –600 mV, at the junction of R109 and R110 is approximately 158 mV between pins 2 and 3 of the fast discriminator and represents approximately 700 mV when referenced to the AMP OUTPUT. The nonlinear fast discriminator references voltage characteristic allows the LOWER LEVEL (E) control to adjust the fast discriminator just above the noise region while maintaining optimum timing performance.

5 Volt Power Supply

Resistors R170 and R39 attenuate the +12 V power supply to 5 volts. Diode D24 compensates for temperature related V_{be} variations of transistor Q26. Transistor Q26 is an emitter follower and supplies the necessary +5 volt current. Resistor R171 acts as a current limiter protecting the 5 volt supply in the event of a short circuit.

Troubleshooting

The Model 2015A AMP/TSCA is designed and constructed to provide reliable trouble-free service with normal usage and care in operation. Should module malfunction occur, the following information is provided to facilitate troubleshooting of the AMP/TSCA. Information contained in other sections of this manual should be used along with the following information to aid in locating the source of trouble.

Troubleshooting Aids

- Test Equipment (refer to “Equipment Required” on page 20)
- NIM Module Power Extender Cable Canberra Model C-1403
- Detailed Block Diagram Drawing B-17635
- Circuit Schematic Drawing B-17636

Troubleshooting Techniques

1. **Check Control Settings.** The first and most important prerequisite for successful troubleshooting is a thorough understanding of module operation and function. Often, suspected malfunctions are caused by improper control settings. The troubleshooting aids and techniques should be applied only after it has been firmly established that the difficulty cannot be eliminated by the Operating Instructions, refer to page 7.

2. **Check Associated Equipment.** An investigation should be made to ensure that the trouble is not a result of conditions external to the Model 2015A. Check that the equipment used with this instrument is operating correctly. Make certain that signals are properly connected and that the interconnecting cables are not defective. Also, check the power source. The substitution method can be applied to check for proper operation of the Model 2015A if another similar type unit is available.

3. **Visual Check.** Conduct a visual inspection of the Model 2015A for possible burned or unsoldered components, broken wires or any other obvious conditions which might suggest a source of trouble.

4. **Isolate Trouble to a Circuit.** To isolate trouble to a particular circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check affected circuits by taking voltage and waveform readings. Incorrect operation of all circuits often indicates trouble in the power supply (internal or external). However, defective components in the module can appear as a power supply trouble and may affect the operation of other circuits. After the

defective circuit has been located, proceed to locate the defective component(s).

5. **Check Voltages and Waveforms.** Often the defective component(s) can be located by checking for the correct voltage or waveform in the malfunction circuit. Logic levels and truth tables for the digital integrated circuits used in the instrument are given in the this chapter.

Component Replacement

All replacement parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance. Many components in the Model 2015A are standard electronic parts available locally. However, all parts can be obtained through Canberra Industries. When ordering replacement parts from Canberra, include the following information.

- Instrument Model Number.
- Instrument Serial Number.
- A description of the part (if electrical, include circuit number - A2, Q3, etc.)
- Canberra part number (if available)
- Canberra schematic drawing number.

A. Specifications

Inputs

INPUT – Accepts positive or negative linear pulses from associated preamplifier; amplitude: ±10 V divided by the selected gain, ±12 V maximum; rise time less than shaping time constant; decay time constant 30 µs to ∞; Z_{in} ≈ 1 kΩ; front and rear panel BNC connectors.

Outputs

AMP OUTPUT – Provides prompt +10 V full scale unipolar OUTPUT; active filter near-Gaussian shaping; dc restored; dc level is factory calibrated to 0 ±5 mV dc; short circuit protected, front and rear panel BNC connectors; front panel Z_{out} <1 Ω or ≈ 93 Ω, internally selectable; rear panel Z_{out} ≈ 93 Ω.

SCA OUTPUT – Provides a nominally 5 V (unterminated) 500 ns positive pulse, delayed approximately 200 ns past the peak of the AMP OUTPUT signal; rise time and fall time ≤25 ns; Z_{out} ≈ 50 Ω; BNC connectors located on front and rear panels; short circuit protected; OUTPUT amplitude can be changed to 8 V by means of an internal jumper.

Input/Output

DISC – Rear panel BNC connector having a multi-function capability; lower level (E) DISCriminator OUTPUT, upper level (E + ΔE) DISCriminator OUTPUT, or LLD SWEEP INPUT; one of these three modes is internally selected with jumper plugs; shipped in E position.

When used as:

Lower Level (E) DISCriminator OUTPUT: Provides a positive 5 V (unterminated), 500 ns pulse; rise time and fall time ≤25 ns; Z_{out} ≈ 50 Ω; the LLD pulse is generated when the positive edge of the AMP OUT signal crosses the Lower Level (E) threshold setting; OUTPUT amplitude can be changed to +8 V by internal jumper.

Upper Level (E + ΔE) DISCriminator OUTPUT: Same as lower level DISCriminator except the pulse appears when the AMP OUT signal crosses the threshold set by the sum of the LOWER LEVEL (E) and WINDOW (ΔE) controls.

LLD SWEEP INPUT: Accepts 0 to + 10 V input to externally control the SCA's lower level discriminator; $Z_{in} \approx 5.1$ kΩ; dc coupled.

Controls

COARSE GAIN – Rotary switch selects gain factors of X4, X8, X16, X32, X64, X128.

FINE GAIN – Ten-turn precision locking dial potentiometer selects variable gain factor of X3 to X10.

P/Z – Front panel multi-turn screwdriver pole/zero adjustment optimizes the amplifier baseline recovery and overload performance for the preamplifier fall time constant and the main amplifier pulse shaping chosen; 30 µs to ∞ preamp fall time constant range.

INPUT – Toggle switch sets the Model 2015A for the polarity of the incoming preamplifier signal.

TIME CONSTANTS – Internal pushbutton switch selects SHAPING TIME constant of 0.5 µs or 2.0 µs; factory set to 2.0 µs.

LOWER LEVEL (E) – Ten-turn locking dial precision potentiometer selects a baseline from 0.1 V to 10 V for the timing SCA mode, and 0 ±15 mV to 10 V for the normal SCA mode.

WINDOW (ΔE) – Ten-turn locking dial precision potentiometer selects window width from 0 to 10 V or 0 to 1 V depending on the position of the rear panel ΔE RANGE switch.

ΔE RANGE – Rear panel toggle switch selects the front panel WINDOW (ΔE) range as 0 to 10 V or 0 to 1 V, full scale.

LED INDICATOR – Aids in setting the LLD just above the system noise.

Internal Controls

Z_{out} – Jumper plug selects AMP OUTPUT impedance of ≤1 Ω or ≈ 93 Ω; factory set to ≤1Ω.

DISC B – Jumper plug sets the rear panel DISC BNC connector as an OUTPUT or input; factory set to OUT.

DISC A – Jumper plug sets the rear panel DISC BNC connector to OUTPUT the Lower Level (E) Discriminator or the Upper Level (E + ΔE) discriminator when DISC B is in the OUT position; factory set to ULD.

LLD – Jumper plug sets the LOWER LEVEL discriminator threshold for INternal or EXTernal; if EXTernal with DISC B set to IN, the rear panel DISC BNC connector can be used as the LLD SWEEP input; factory set to IN.

SCA MODE – Jumper plug which allows the SCA to operate in the TSCA or SCA mode; factory set to TSCA.

Performance

AMPLIFIER

GAIN – Continuously variable from X12 to X1280; product of COARSE and FINE GAIN controls.

GAIN DRIFT – <±0.0075%/°C.

DC LEVEL DRIFT – <±50 μV/°C.

INTEGRAL NONLINEARITY – ≤±0.05% of full scale.

OVERLOAD RECOVERY – Recovers to ±2% of full scale OUTPUT in two pulse widths for a X1000 overload with pole/zero cancellation properly set.

NOISE CONTRIBUTION – <7 μV referred to the INPUT for gains ≥100X and 2 μs SHAPING.

PULSE SHAPING – Near-Gaussian shape; one differentiator, two active integrators and only one secondary time constant; time to peak ≈ 1.75 X shaping time constant.

RESTORER – Active, gated.

SPECTRUM BROADENING – FWHM of a ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 50 kcps and a 9 V pulse height will change less than 16%. These results may not be reproducible if associated detector exhibits an inordinate amount of long rise time signals.

PEAK STABILITY – The peak position of a ^{60}Co 1.33 MeV gamma peak for an incoming count rate of 2 kcps to 50 kcps and a 9 V pulse height will shift less than 0.025%.

SCA

By resetting an internal jumper, the SCA OUTPUT can be used as an SCA referenced to the AMP OUTPUT crossing the LOWER LEVEL (E) discriminator or as a Timing SCA referenced to the leading edge of the amplified preamp signal; shipped in the Timing SCA mode.

TSCA OUTPUT TIMING – ≈ 200 ns from the peak of the AMP OUT signal.

TSCA OUTPUT WALK – ≤±50 ns for a 50:1 change in the AMP OUTPUT signal amplitude.

INTEGRAL NONLINEARITY – ≤±0.25% of full scale range for LOWER LEVEL (E) and WINDOW (ΔE).

PULSE PAIR RESOLUTION – With the SCA driven from a rectangular shaped pulser for LOWER LEVEL (E) thresholds ≥100 mV, the pulse pair resolution is ≤500 ns over the full linear range for the DISC (LLD) OUTPUT.

TEMPERATURE DRIFT (E and ΔE) –≤±0.005% of full scale/°C (50 ppm).

POWER SUPPLY SENSITIVITY – Both discriminators are referenced to the +12 and +24 V Bin supplies.

Connectors

SIGNAL CONNECTORS – BNC type.

PREAMP POWER – Rear panel, Amphenol 17-10090.

Power Requirements

+24 V dc – 50 mA	+12 V dc – 160 mA
–24 V dc – 50 mA	–12 V dc – 70 mA

Physical

SIZE – Standard single-width NIM module 3.43 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-0457T.

NET WEIGHT – 1.1 kg (2.5 lb).

SHIPPING WEIGHT – 2.3 kg (5.0 lb).

Environmental

OPERATING TEMPERATURE - 0 to 50 °C.

RELATIVE HUMIDITY - Up to 80%, non-condensing.

Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution Degree 2.

B. Installation Considerations

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- A rack or tabletop enclosure fully closed on all sides with rear door access
- Single point external cable access
- Blank panels to cover open front panel Bin area
- Compliant grounding and safety precautions for any internal power distribution
- The use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit's compliance with the specified EU requirements.

Warranty

Canberra (we, us, our) warrants to the customer (you, your) that for a period of ninety (90) days from the date of shipment, software provided by us in connection with equipment manufactured by us shall operate in accordance with applicable specifications when used with equipment manufactured by us and that the media on which the software is provided shall be free from defects. We also warrant that (A) equipment manufactured by us shall be free from defects in materials and workmanship for a period of one (1) year from the date of shipment of such equipment, and (B) services performed by us in connection with such equipment, such as site supervision and installation services relating to the equipment, shall be free from defects for a period of one (1) year from the date of performance of such services.

If defects in materials or workmanship are discovered within the applicable warranty period as set forth above, we shall, at our option and cost, (A) in the case of defective software or equipment, either repair or replace the software or equipment, or (B) in the case of defective services, reperform such services.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES OR REMEDIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, EXEMPLARY, PUNITIVE, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE. REPAIR OR REPLACEMENT OF THE SOFTWARE OR EQUIPMENT DURING THE APPLICABLE WARRANTY PERIOD AT CANBERRA'S COST, OR, IN THE CASE OF DEFECTIVE SERVICES, REPERFORMANCE AT CANBERRA'S COST, IS YOUR SOLE AND EXCLUSIVE REMEDY UNDER THIS WARRANTY.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident, neglect or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our Service Personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows, or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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