OKI Semiconductor

PEDL86V7667-00
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ML86V7667

Preliminary

NTSC/PAL Digital Video Decoder

GENERAL DESCRIPTION

The ML86V7667 is an LSI that converts NTSC and PAL analog video signals into the standard digital format or 8-bit digital data conforming to ITU-R recommendation BT.601/BT.656 YCbCr.
The video input has a built in 1-channel 10-bit A/D converter and supports composite video signals.
The composite video signal is separated into luminance and chrominance signals by an adaptive 2-dimensional Y/C separation filter (2- or 3-line adaptive comb filter) and converted into general purpose video data format.
The sampling methods that can be used are the asynchronous sampling method which is a feature of Oki's decoders and the line-locked clock sampling method using a digital PLL.
As for image jitter, which is a problem in asynchronous sampling methods in normal cases, jitter-free output data can be obtained because the ML86V7667 incorporates into it a pixel position correction circuit and a FIFO for pixel count correction.

USES AND APPLICATION EXAMPLES

The ML86V7667 can be used as a video signal input interface IC in any system carrying out digital image processing. It can be operated using digital PLL with line-locked clock in applications requiring high picture quality. Also, high-speed synchronous operation using asynchronous clock is possible in applications requiring high-speed synchronization, such as switching operation using multichannel inputs.

Application Examples

- Various types of TVs and equipment for TV reception such as:
  TFT/PDP or other flat panel TVs, PC TVs, digital TVs, set-top boxes for TV broadcast reception
- Image recording devices such as:
  DVD-R/W, HDD recorders, digital VTRs, digital video cameras, and digital cameras
- Monitoring systems such as:
  Multidisplay devices, long-time recording devices, transmission devices for remote monitoring
- PC peripheral devices such as:
  Video capture boards, image editing devices, Internet monitoring cameras

FEATURES

Input Section

- Supports composite video signals in NTSC/PAL format
- Two composite video inputs can be connected
- Clamping circuit and video amplifier built-in
- 1-channel 10-bit A/D converter built-in
- Line-locked clock sampling mode or asynchronous sampling mode selectable
- Supported pixel frequencies (sampling clock: double speed):
  27 MHz : NTSC/PAL ITU-R BT.601
  24.545454 MHz : NTSC Square pixel
  28.63636 MHz : NTSC 4fsc
  29.5MHz : PAL Square pixel

Digital Processing Section

- Two dimensional Y/C separation using adaptive filter
  Common to NTSC systems: 2-line or 3-line adaptive type comb filter
- Recognition of data within the VBI period (closed caption, CGMS, WSS) and function to read data from I^2C bus (can be detected in all operating modes)
- Copyguard detection (such as Macrovision AGC and color burst)
- Can decode signals in a special standard such as NTSC443, PAL-N, and M.
- Built-in AGC/ACC (Automatic luminance level adjustment/automatic chrominance level adjustment) circuit
- Incorporates a decimation filter in the input stage, thereby simplifying the filter of the front end of the A/D converter (during double speed input mode operation)
- Automatic NTSC/PAL identification (only during the ITU-R BT.601 mode)

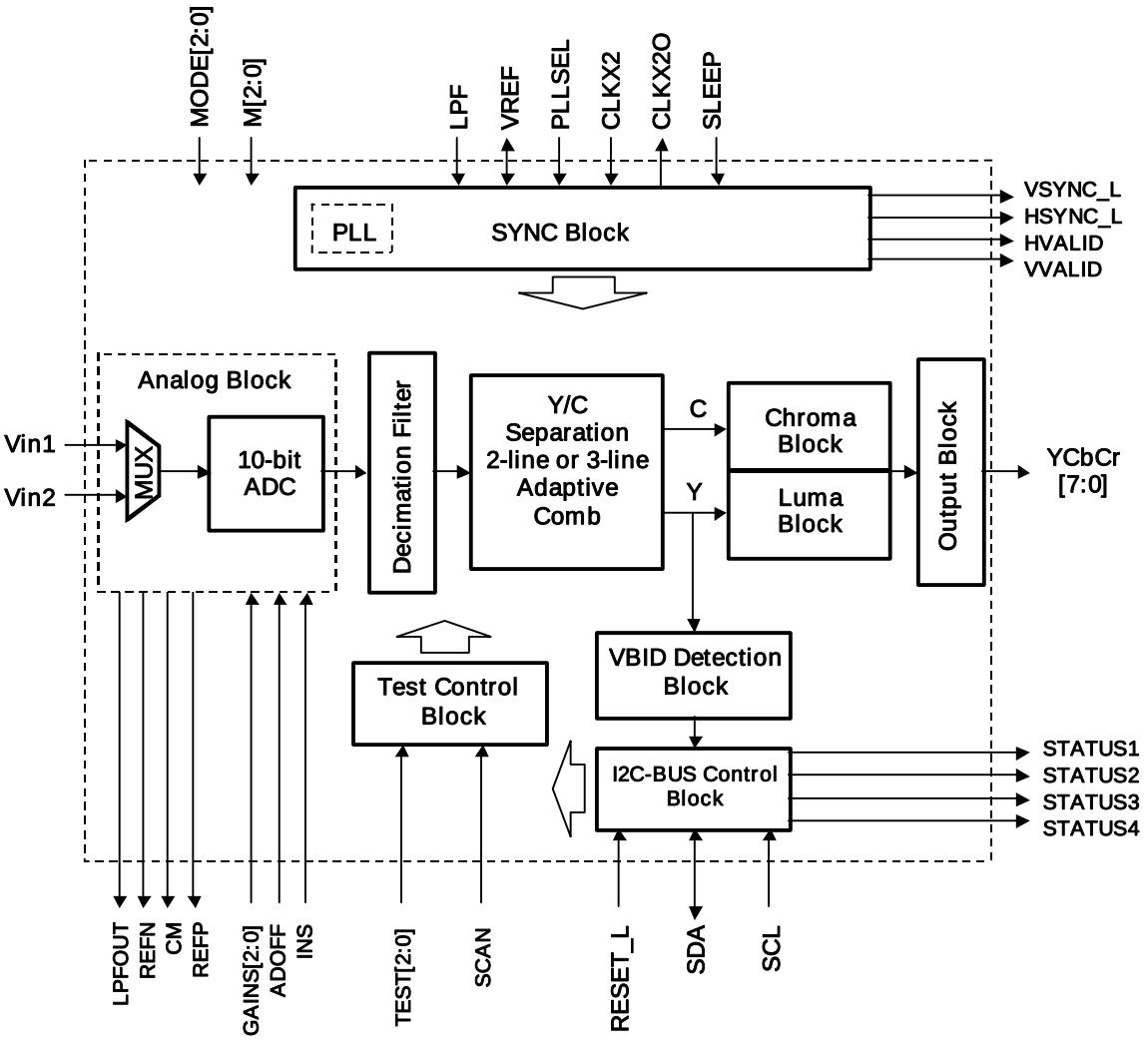
Output Section

- Selectable from the two output interfaces:) + SAV, EAV
  - ITU-R BT.656-4 : 8 bits (Y/CbCr)
  - 8-bit Y/CbCr : 8 bits (YCbCr) (4:2:2)/(4:1:1) + Sync.
- Output pixel count correction function using built-in FIFO
  FIFO Mode/FIFO through mode selectable
- Automatic switching between FIFO and FIFO through modes
- Sleep mode
- Hi-impedance mode for output pins

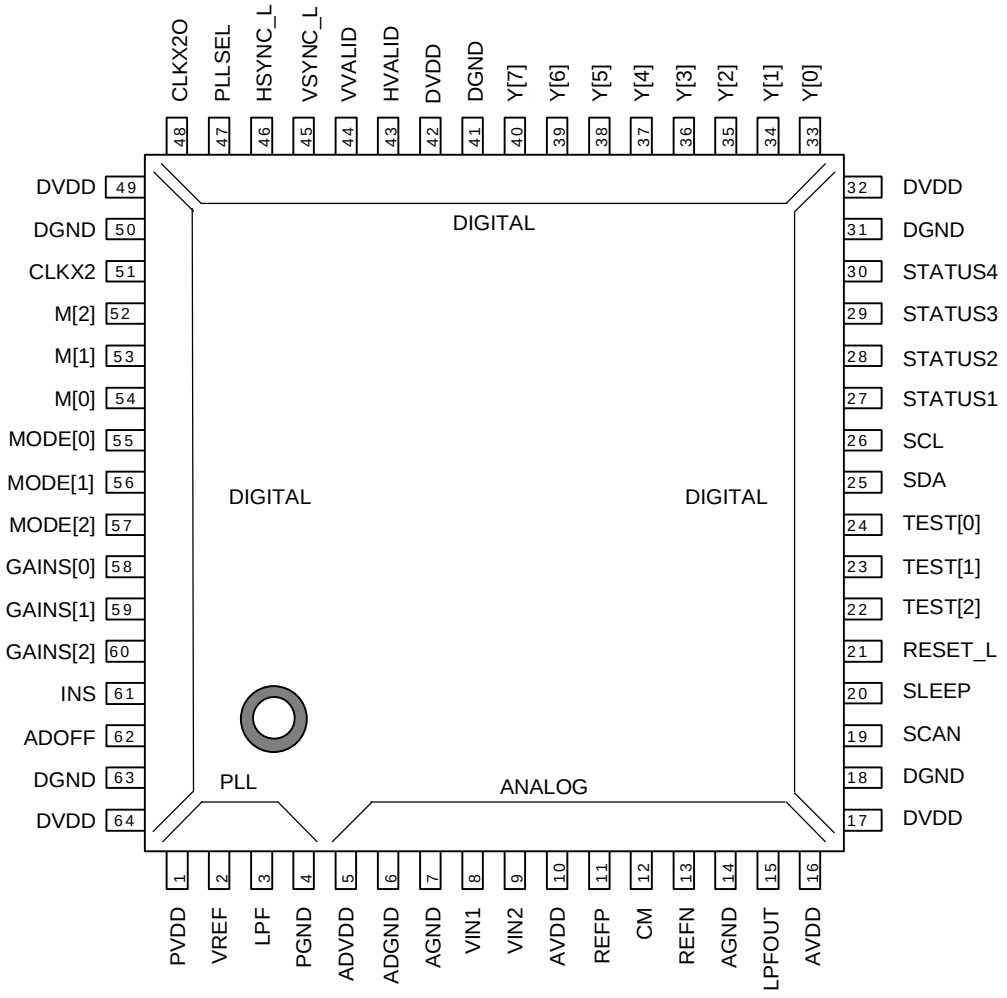
Other Sections

- I^2C-bus interface
- Single 3.3 V power supply (5 V tolerant input)
- Package: 64-pin plastic TQFP (TQFP64-P-1010-0.50-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic TQFP (TQFP64-P-1010-0.50-K)

PIN DESCRIPTIONS

Pin	Symbol	I/O	Description
1	PVDD	–	PLL power supply
2	VREF	O	Center frequency setting pin. Connect to the PGND pin when not used.
3	LPF	I	Analog PLL loop filter connection pin. Connect to the PGND pin when not used. See the sample circuit provided in the User's Manual.
4	PGND	–	PLL ground
5	ADVDD	–	Digital power supply in the analog block.
6	ADGND	–	Digital ground in the analog block.
7	AGND	–	Analog ground
8	VIN1	I	Composite-1 input Connect this pin to AGND when not used.
9	VIN2	I	Composite-2 input Connect this pin to AGND when not used.
10	AVDD	–	Analog power supply
11	REFP	O	A/D C reference voltage (high) Should be left pen.
12	CM	O	A/D C reference voltage (middle) Should be left pen.
13	REFN	O	A/D C reference voltage (low) Should be left pen.
14	AGND	–	Analog ground
15	LPFOUT	O	Not used. Open
16	AVDD	–	Analog power supply
17	DVDD	–	Digital power supply
18	DGND	–	Digital ground
19	SCAN	I	Not used. Should be fixed to "0".
20	SLEEP	I	Sleep signal input. “0”: Normal operation, “1”: Sleep operation
21	RESET_L	I	Reset signal input. “0”: Reset, 1: Normal operation Reset after power ON.
22	TEST [2]	I	Not used. Should be fixed to "0".
23	TEST [1]	I	Not used. Should be fixed to "0".
24	TEST [0]	I	Not used. Should be fixed to "0".
25	SDA	I/O	I^2C bus data input/output pin. Pulled up by a 4.7 kΩ resistor. Putt this pin into the “0” state when not used.
26	SCL	I	I^2C bus clock input. Put this pin into the “0” state when not used.
27	STATUS1	O	STATUS output pin 1. Selected by the internal register. Default HVALID
28	STATUS2	O	STATUS output pin 2. Selected by the internal register. Default VVALID
29	STATUS3	O	STATUS output pin 3. Selected by the internal register. Default ODD/EVEN
30	STATUS4	O	STATUS output pin 4. Selected by the internal register. Default CSYNC

Pin	Symbol	I/O	Description
31	DGND	–	Digital ground
32	DVDD	–	Digital power supply
33 | 42	Y [0] | Y [7]	O	Data output Y[7]:MSB toY[0] ITU-R BT.656 mode: Y/CbCr 8-bit data output 8-bit Y/CbCr mode: Y/CbCr 8-bit data output The output mode is set by the MODE pin or register $00/MRA[7]
41	DGND	–	Digital ground
42	DVDD	–	Digital power supply
43	HVALID	O	Horizontal active pixel timing output. Outputs a “H” level during an valid period.
44	VVALID	O	Vertical active line timing output. Outputs a “H” level during a valid period.
45	VSYNC_L	O	Vertical sync signal output (V sync)
46	HSYNC_L	O	Horizontal sync signal output (H sync)
47	PLLSEL	I	PLL clock select pin. 0: Fixed clock, 1: PLL clock
48	CLKX2O	O	System clock output Clock with the same frequency as the system clock is output.
49	DVDD	–	Digital power supply
50	DGND	–	Digital ground
51	CLKX2	I	System clock input or Reference clock input for PLL Fixed clock (Pin 47 = “0”) NTSC ITU-R BT.601 27 MHz NTSC Square Pixel 24.545454 MHz NTSC 4Fsc 28.63636 MHz PAL ITU-R BT.601 27 MHz PAL Square Pixel 29.5 MHz Reference clock for PLL (Pin 47 = “1”) Register $20/PLLR1[6] 0: 32 MHz 1: 25 MHz
52	M [2]	I	I2C bus slave address selection. Put this pin into the “0” state when not used. 0: 1000 001X (X: 0 = Write 1 = Read) 1: 1000 011X (X: 0 = Write 1 = Read)

Pin	Symbol	I/O	Description
53	M [1]	I	Pin for selecting the control method of amplifier gain setting and input pin selection 0: External pin mode Amplifier gain setting: Pins 58 to 60 GAINS[2:0] are used Input pin setting: Pin 61 INS is used 1: Register mode Amplifier gain setting: Register $1F/ADC2[6:4] Input pin setting: Register $1E/ADC1[0] The internal register settings are invalid when the external pin mode is set.
54	M [0]	I	Not used. Should be fixed to "0".
55 56	MODE [0] MODE [1]	I	Input mode external setting pins. Put these pins into the “0” state when not used. Valid when register $00/MRA[0] is “0” (default “0”). MODE[1] 0:NTSC, 1:PAL Invalid when the register bit $02/MRC[7] is “1” (automatic NTSC/PAL identification) MODE[0] 0:ITU-R BT.601, 1: Square Pixel NTSC 4fsc can only be specified by the register bits $00/MRA[5:3].
57	MODE [2]	I	Output mode external setting pin. Put this pin into the “0” state when not used. Valid when register bit $00/MRA[0] is “0” (default “0”). 0:ITU-R BT.656 (8-bit Y/CbCr + SAV, EAV, blank) 1:8-bit Y/CbCr
58 | 60	GAINS [0] | GAINS [2]	–	Amplifier gain external setting pins. Put these pins into the “0” state when not used. Valid when external pin 53 M[1] = “0”. GAINS [2:0] Gain (X times) [000] 0.55 [001] 0.70 [010] 0.93 [011] 1.21 [100] 1.60 [101] 2.09 [110] 2.65 [111] 3.45
61	INS	I	External setting pin for input pin switching. Put this pin into the “0” state when not used. Valid when external pin 53 M[1] = “0”. INS Input pin [0] VIN1(pin 8) Composite-1 [1] VIN2(pin 9) Composite-2
62	ADOFF	I	ADC stop signal. Normally set to “0”.
63	DGND	–	Digital ground.
64	DVDD	–	Digital power supply.

FUNCTIONAL DESCRIPTION

This section explains the basic functions of the IC in terms of the blocks shown in the block diagram.
Refer to the User's manual for detailed explanations of the internal registers and any functions that are not covered in this data sheet.

Analog Section

The analog section inputs video signals. The analog section uses the video signal channel selector, AMP and 10-bit ADC to select the desired channel from among several video signals and convert the input to digital video data.

- Analog input selector

  The analog input selector is compatible with composite signals. The maximum number of input connections is 2 channels of composite signals. The selection of these input connections can be changed by external pins or by register controls using the I^2C-bus.

  # Related register: $1E/ADC1[0]

Analog Input Requirements

Input signal	Control pin	Register	Input pin	
	Pin 53 M[1] = 0	Pin 53 M[1] = 1		
	INS	ADC1[0]	VIN1	VIN2
*Composite-1 input	[0]	*[0]	Composite	
Composite-2 input	[1]	[1]		Composite

*: Default setting after LSI is reset.

- Clamp function

  The clamp fixes the video input signal in the ADC input range. Clamping is performed by sync chip clamp. Setting register $1F/ADC2[3:1] to "111" and raising the clump voltage allows the luminance level to be stabilized and saturation of the luminance level to be relaxed.

  # Related register: $1F/AD2

- AMP/analog AGC function

  This function converts video input signals to the optimum level for the ADC using the analog AMP of the AGC function. The AGC function has an output level adjust function in the luminance block of the digital section in addition to the AMP input level adjust function. Manual setting of the AMP gain is also possible.

  # Related register: $1F/ADC2

Analog Amplifier Manual Gain Control

Pin 53 M[1] = 0	Pin 53 M[1] = 1	Setting gain value Typical value (X times)
Gain setting pin GAINS[2:0]	Register $1F/ADC2[6:4]	
[000]	[000]	0.55
[001]	*[001]	0.70
[010]	[010]	0.93
[011]	[011]	1.21
[100]	[100]	1.60
[101]	[101]	2.09
[110]	[110]	2.65
[111]	[111]	3.45

Pin 53 M[1] "0": External pin analog gain setting mode
"1": Internal register analog gain setting mode

• A/D converter

This 10-bit A/D converter (ADC) converts analog video signals to digital video data. There is 1 channel built into the ADC. Sampling is performed at the pixel frequency or double-speed.

Related registers: $1E/ADC1, $1F/ADC2

Digital Section

The digital section separates the video data digitized by the ADC into Y and C data, converts these data to various data formats and outputs them. The digital section also performs output level adjustment, image quality adjustment and various corrections.

• Decimation filter

This filter is applied during double speed sampling mode.

Since internal processing is performed at a single speed even during the double speed sampling mode, this filter is needed to reduce the data that has been doubled by one-half. Using the decimation filter after double-speed sampling reduces high-frequency noise and provides data having better high frequency characteristics.

Related register: $02/MRC[4]

2-dimensional Y/C Separation Block

This block separates composite data into Y (luminance) data and C (chrominance) data. The Y/C separation function works only for lines which are active as image data and is bypassed for composite signals in the V blanking period.

• 2-Dimensional Y/C Separation Function

With the Y/C separation filter, composite data is separated into Y (luminance) data and C (chrominance) data. There are various Y/C separation filters available, which can be selected in an internal register.

Related register: $01/MRB

MRB[5:3]	NTSC Y/C separation	PAL Y/C separation
*000	2-line/3-line adaptive comb filter	2-line comb/trap adaptive transition filter
001	3-line comb filter	2-line comb filter
010	Trap filter	Trap filter
011	3-line comb/trap adaptive filter	Undefined
100	3-line comb/trap adaptive filter 2	Undefined
101	2-line/3-line adaptive transition filter	Undefined
110	Undefined	Undefined
111	Undefined	Undefined

• Special Broadcasting Standard Decode Function

Signals of the following special standards other than normal NTSC/PAL signals can be decoded.

Related register $00/MRA[2:1]

MRA[2:1] = "00" Normal mode

MRA[2:1] = "01" NTSC443

MRA[2:1] = "10" PAL M, N

MRA[2:1] = "11" Setting prohibited

Luminance Block

The luminance block removes sync signals from the luminance data after Y/C separation, and performs adjustments such as luminance level adjustment and luminance image quality correction and adjustment. The digital decoded data that is output conforms with ITU-R BT.601.

- Pixel Position Correction Function

  This function corrects sampling error in asynchronous sampling and loss of PLL synchronization. Error correction is made in the horizontal direction, which improves vertical line jitter on the screen.

  # Related register: $02/MRC[6]

- Digital AGC Function

  This function adjusts the output level of luminance signals. Adjustment is automatically performed by the digital AGC, but the adjustment can also be set manually by using an internal register to set digital MGC. In the digital AGC mode, the sync level is compared with a reference value to determine the amplification rate of the luminance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. In the digital MGC mode, the signal amplification rate and the black level are adjusted with register settings. The black level is adjusted by means of pedestal level adjustment (register $11/SSEPL[7] = "1").

  Regarding the AGC function, in addition to the output level adjust function in the digital section, the input level adjust function of the AMP in the analog section also operate separately.

  Note: AGC (Auto Gain Control), MGC (Manual Gain Control)

  # Related registers: $0D/AGCLA, $0E/AGCLB, $0F/AGCRC, $11/SSEPL, $10/CLC

- Image Quality Adjustment

  The following image filters are provided for adjusting luminance image quality.
  Refer to the User's Manual for the characteristics of each filter.

  #### Edge emphasizing pre-filter

  Filter for emphasizing edges of luminance component signals.
  The pre-filter and the sharp filter operate simultaneously.
  # Related register $OC/LUMC[7]

  #### Aperture bandpass filter, coring filter for contour compensation, and luminance pre-filter

  Adjustment is performed by combining the following registers.
  Aperture bandpass filter coefficient setting:
  # Related register $OC/LUMC[6:5]
  Coring range setting:
  # Related register $OC/LUMC[4:3]
  Aperture weighting factor setting:
  # Related register $OC/LUMC[2:0]

Chrominance Block

This block decodes chroma data to Cb/Cr data and performs level adjustment and color adjustment. To eliminate unnecessary bands, this block first passes data through a bandpass filter (bypass is possible) and then through an ACC correction circuit to maintain a stable chroma level, before performing UV decoding. The result of the UV decoding is passed through a low-pass filter and output as a chrominance signal.
Related registers: $12/CHRCA, $13/CHRCB

- Digital ACC Function

  The digital ACC is the gain adjustment for the chrominance signal output level. Adjustment is automatically performed by the digital ACC (Auto Chrominance Control), but the adjustment can also be set manually by using an internal register to set digital MCC (Manual Chrominance Control). In the digital ACC mode, the burst level is compared with a reference value to determine the amplification rate of the chrominance level. The default is automatically adjusted to sync level 40IRE, but the level can also be adjusted in an internal register. Separate U/V level adjustment is also possible.
  # Related registers: $12/CHRCA, $14/ACCC, $15/ACCRC

- Hue Adjust Function

  The function for adjusting hue.
  Hues can be adjusted by setting the HUE register.
  # Related register: $16/HUE

Output Block

The output block performs output timing adjustment, picture sizing, output format conversion and other types of output conversion.

- Pixel Count Correction Function

  This function uses the internal FIFO to correct the total number of pixels in a line. It corrects the 1-line sampling error generated when in asynchronous sampling mode or PLL synchronization is lost, and fixes the pixel count for a line within the active screen. Refer to Active Pixel Timing for more on the pixel count for one line.
  # Related registers $03/MRD[7:6], $19/OMRB

  The internal FIFO can be set in the through mode by register $03/MRD[7:6].
  MRD[7:6] = "00" : FIFO-1 mode
  The standard value of the pixel count per horizontal (H) line is output by the internal FIFO.
  MRD[7:6] = "01" : FIFO-2 mode * (default)
  The standard value of the pixel count per horizontal (H) line is output by the internal FIFO. This mode is different from the FIFO-1 mode in the internal processing method. The FIFO-2 mode is more effective than the FIFO-1 mode for non-standard signals.
  MRD[7:6] = "10" : FIFO through mode
  This is the mode in which the value of the decoded result of an input signal is output without correcting the pixel count by the internal FIFO.
  MRD[7:6] = "11" : Undefined

• Output Format Conversion Function

This function converts the output data to the desired output format.
The following output formats are possible.
Related registers: $00/MRA, $01/MRC

Output Formats

Output mode (i): interlace	Register MRA[0]=0	Register MRA[0]=1	Register
	Control pin (Pin 57)	Register	
	MODE[2]	MRA[7:6]	MRC[5]
ITU-R BT.656 (i) 4:2:2	[0]	[00]	0
Y/CbCr 8-bit multiplex(i) 4:2:2	[1]	*[01]	0

Synchronization Block

This block controls the sync signals for internal operation, output sync signals, and the timing for each block. Synchronization detection levels, output timing, and various other functions can be adjusted by the registers listed below.

Related registers: $03/MRD, $04/SYDR, $05/HSYT, $06/STHR, $07/VSTHR, $08/HSDL, $09/HVALT, $0A/VVALT1, $0B/VVALT2, $12/CHRCA, $13/CHRCB, $17/BBHC, $18/OMRA, $1A/OMRC, $1B/OMRD

• PLL Function

The digital PLL circuit generates an operating clock synchronized with the horizontal sync signals of the video signals. With the input of a 25 MHz or 32 MHz standard clock, the double-speed sampling clock for each mode is provided as a line lock clock and used as the system clock.
The asynchronous sampling mode, which uses an asynchronous clock directly, can be used without using PLL.
Related registers: $20/PLLR1, $21/PLLR2

Input Clock Settings

PLL ON/OFF Register $20/PLLR[7]		Input clock		
		PLL reference clock		Asynchronous clock
PLLR1[7]=0	PLLR1[7]=1	PLLR1[6]=0	PLLR1[6]=1	
PLL ON	-	32MHz	25MHz	—
—	PLL OFF	—	—	Sampling clock input according to the operating mode (See the table on the next page.)

In the PLL mode, a double-speed line lock clock is generated by setting the operating mode.

Operating Modes/Sampling Clock Settings

Operating mode	$00/MRA[0]=0 *	$00/MRA[0]=1	Sampling clock (double-speed)
	Control pin (Pins 55, 56)	Register	
	MODE[1:0]	$00/MRA[5:3]	Pin 51 CLKX2
NTSC ITU-R BT.601 13.5 MHz	[00]	*[000]	27 MHz
NTSC Square pixel 12.272727 MHz	[01]	[001]	24.545454 MHz
NTSC 4fsc 14.31818 MHz	—	[010]	28.63636 MHz
—	—	[011]	—
PAL ITU-R BT.601 13.5 MHz	[10]	[100]	27 MHz
PAL Square pixel 14.75 MHz	[11]	[101]	29.5 MHz
—	—	[110]	—
—	—	[111]	—

— : Not used *: Default

VBID Detection Block

This block detects data information and copy protection information from the VBI (Vertical Blanking Interval) of the input luminance signals. The following four types of VBID data can be detected, and the detection line and detection level can be changed by altering register settings.
*Note: VBID detection may not provide the detection rate of 100% depending on signal status.

- VBID Detection Function

(1) AGC copy protection
Detects whether specified lines include a macrovision AGC pulse (NTSC/PAL) and sets a flag.
Related registers: $27/AGCD1, $28/AGCD2, $2A/VBIDM, $2B/AIREG, $2D/VFLAG

(2) C. C. (Closed Caption)
Detects whether specified lines include closed caption data (NTSC/PAL), keeps separately the data of even and odd lines, and sets individual flags.
Related registers: $23/CCD1, $24/CCD2, $2A/VBIDM, $2B/AIREG, $2D/VFLAG, $2E/CCD00, $2F/CCD01, $30/CCDE0, $31/CCDE1

(3) WSS (Wide Screen Signaling)
Detects the WSS data in the lines specified by ETSI (European Telecommunications Standards Institute) and sets a flag (PAL only).
Related registers: $29/WSSD, $2A/VBIDM, $2B/AIREG, $2D/VFLAG, $38/WSSD0, $39/WSSD1

(4) CGMS (Copy Generation Management System)
Detects the CGMS data in the lines specified by IEC61880 and sets a flag (NTSC only).
Related registers: $25/CGMS1, $26/CGMS2, $2A/VBIDM, $2B/AIREG, $2D/VFLAG, $32/CGMS00, $33/CGMS01, $34/CGMS02, $35/CGMSE0, $36/CGMSE1, $37/CGMSE2

(5) Other copy protection detection functions
Detects the color stripes, false pulses, and MV protection and sets flags.
Related registers: $2B/AIREG, $2C/STATUS, $2D/VFLAG

I²C-bus Control Block

This serial interface block is based on the I²C standard of the Phillips Corporation. The registers at up to subaddress 2Bh are write/read, while the registers from 2Ch on are read-only.

Normally, a license from the Phillips Corporation allowing the use of its I²C patent is required to use an I²C bus. However, the license to use this LSI chip as a slave is granted by the Phillips Corporation upon purchasing this LSI chip. There is no need for a license if the decoder is used alone, without I²C control, but if this I²C-bus is used to control this LSI, a license for use as a master is required.

As of 2001, the I²C patent expired in Japan and the rest of the Asian region, so there have been no costs with regard to license fees. However, in the USA and Canada, there is still a requirement for the payment of license fees, so if this product is intended for overseas trade, it may be necessary to pay the Phillips Corporation license fees for the use of its patent. For more information, contact the Phillips Corporation.

Test Control Block

This block is used to test the LSI chip. It is not intended for user use.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to +4.5	V
Input voltage	Vi	V_{DD} = 3.3 V	–0.3 to +5.5	V
Power consumption	Pw	—	1	W
Storage temperature	Tstg	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	—	3.0	3.3	3.6	V
Power supply voltage	GND	—	—	0	—	V
Analog video signal input	Avin	SYNC tip to white peak level	0.8		1.1	Vp-p
Operating temperature (*)	Ta	—	–40	—	+85	°C

(*): The operating temperature is an ambient temperature (not an IC surface temperature).
The power application sequence should be made to apply the digital, analog, and PLL power supplies at the same time.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, VDD (DVDD, ADVDD, AVDD) = 3.0 to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage (*3)	Vih1	—	2.2	—	VDD (*2)	V
	Vih2 (*1)	—	0.8VDD	—	VDD (*2)	V
"L" level input voltage (*3)	Vil	—	0	—	0.8	V
"H" level output voltage	Voh	Ioh = –2 mA (*4)	0.7VDD	—	VDD	V
		Ioh = –4 mA (*5)				
"L" level output voltage	Vol	Iol = 2 mA (*4)	0	—	0.6	V
		Iol = 4 mA (*5)				
Input leakage current	Ii	Vi = GND to VDD	–10	—	+10	μA
Output leakage current	Io	Vi = GND to VDD	–10	—	+10	μA
VIN input	Avin	C Coupling	0.4	—	1.3	Vp-p

*1: SDA, CLKX2
*2: 5 V can be input since 5 V tolerance is specified for the input voltage.
*3: Place input pins at a "H" or "L" level since they are not pulled down. It is recommended that the pins be placed at a "L" level.
*4: Y[7:0], HSYNC_L, VSYNC_L, HVALID, VVALID, STATUS1, STATUS2, STATUS3, STATUS4
*5: CLKX2O

(Ta = –40 to +85°C, VDD (DVDD, ADVDD, AVDD) = 3.0 to 3.6 V, GND = 0 V)

Parameter	Symbol	Condition	Operating clock	Min. VDD=3.0V	Typ. VDD=3.3V	Max. VDD=3.6V	Unit
Digital power supply current (DVDD)	IDD1	PLL Mode CLKX2= 32MHx	24.545454 MHz	40	55	70	mA
			27 MHz	45	60	75	
			28.63636 MHz	45	65	75	
			29.5 MHz	50	70	80	
Analog power supply current (AVDD+ADVDD)	IDA1		24.545454 MHz	25	35	50	mA
			27 MHz	25	35	50	
			28.63636 MHz	25	35	50	
			29.5 MHz	25	35	50	
Digital power supply current (DVDD)	IDD1	Fixed Clock Mode	24.545454 MHz	40	55	70	mA
			27 MHz	45	60	75	
			28.63636 MHz	45	65	75	
			29.5 MHz	50	70	80	
Analog power supply current (AVDD+ADVDD)	IDA1		24.545454 MHz	25	35	50	mA
			27 MHz	25	35	50	
			28.63636 MHz	25	35	50	
			29.5 MHz	25	35	50	
Power supply current (inactive)	IDoff	—		0	—	10	mA

AC Characteristics

(Ta = –40 to +85°C, VDD (DVDD, ADVDD, AVDD) = 3.0 to 3.6 V, GND = 0 V)

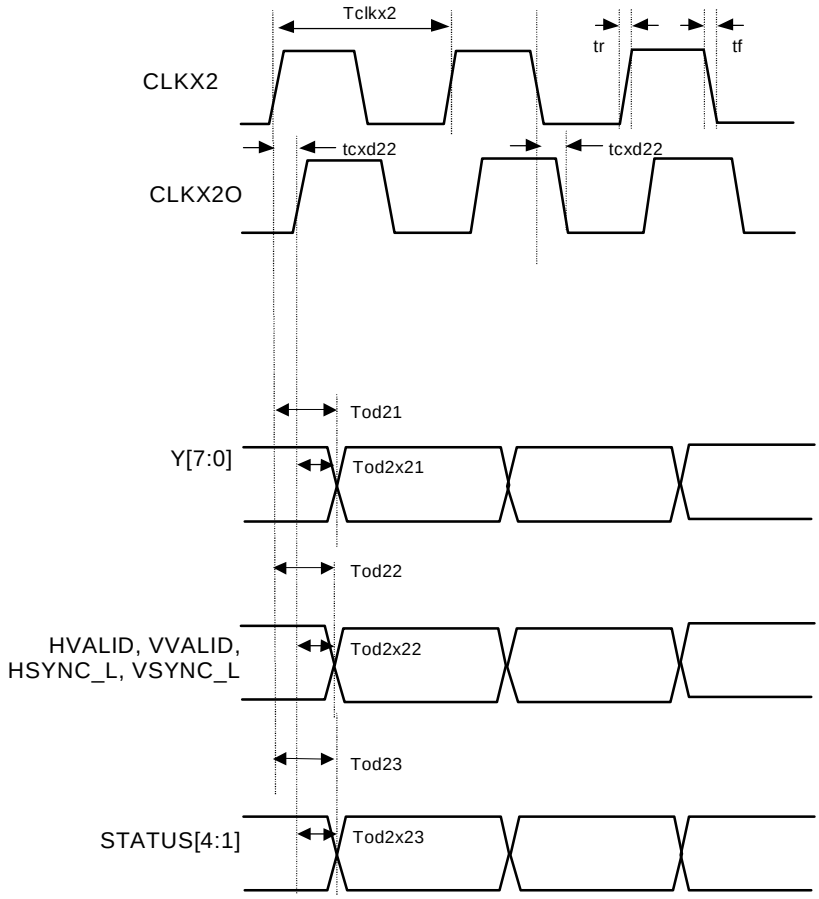
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 cycle frequency	1/tclkx2	ITU-R BT.601	—	27.0	—	MHz
		NTSC 4Fsc	—	28.63636	—	MHz
		NTSC Square Pixel	—	24.545454	—	MHz
		PAL Square Pixel	—	29.5	—	MHz
Input frequency accuracy (**)	—	—	—	—	±100	ppm
CLKX2 duty	td_d2	—	45	—	55	%
CLKX2 rise/fall time	tr, tf	CLKSEL: L	—	—	4	ns
Output data delay time 1 (*)	tod21	CLKSEL: L	7	—	24	ns
Output data delay time 2 (*)	tod22	CLKSEL: L	7	—	22	ns
Output data delay time 3 (*)	tod23	CLKSEL: L	5	—	25	ns
Output data delay time 2x1 (*)	tod2x21	CLKSEL: L	1	—	9	ns
Output data delay time 2x2 (*)	tod2x22	CLKSEL: L	1	—	8	ns
Output data delay time 2x3 (*)	tod2x23	CLKSEL: L	1	—	11	ns
Output clock delay time (*) (CLKX2-CLKX2O)	tcxd22	CLKSEL: L	4	—	16	ns
SCL clock cycle time	tc_scl	Pull up = 4.7kΩ	200	—	—	ns
Low level cycle	tl_scl	Pull up = 4.7kΩ	100	—	—	ns
RESET_L width	rst_w		200	—	—	ns

(*) Output load: 10 pF

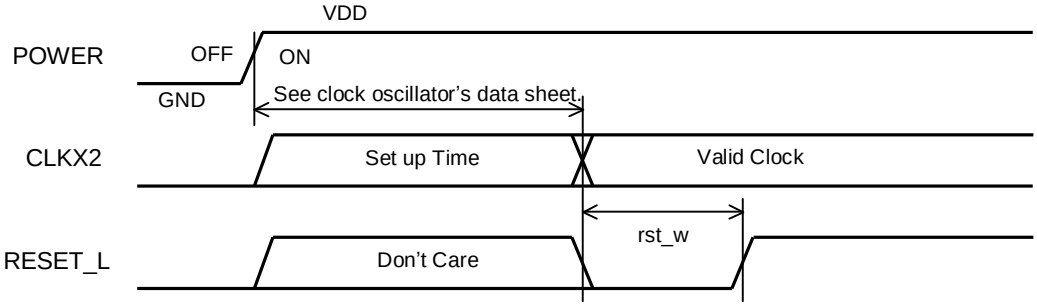
(**) Use a frequency accuracy of ±50 ppm for a vector waveform whose characteristics are important. If a frequency accuracy of ±100 ppm is used, degradation of accuracy with temperature can cause larger jitter of vector waveform.

INPUT AND OUTPUT TIMING DIAGRAMS

Data Output Timing

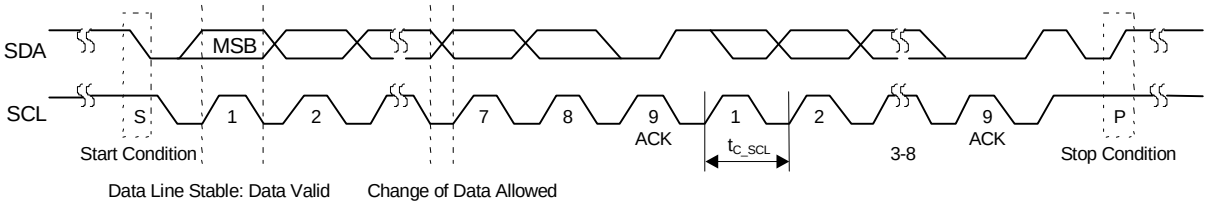


Reset Timing

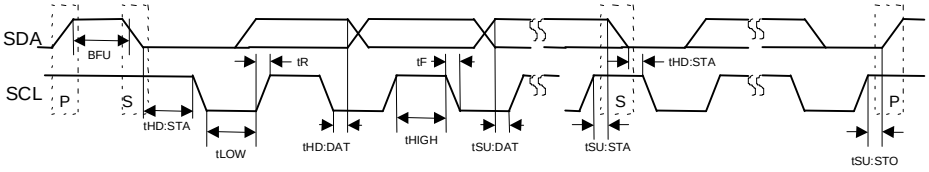


(*) Output data is "don't care" at reset.

I²C-bus Interface Timing



I²C-bus Timing

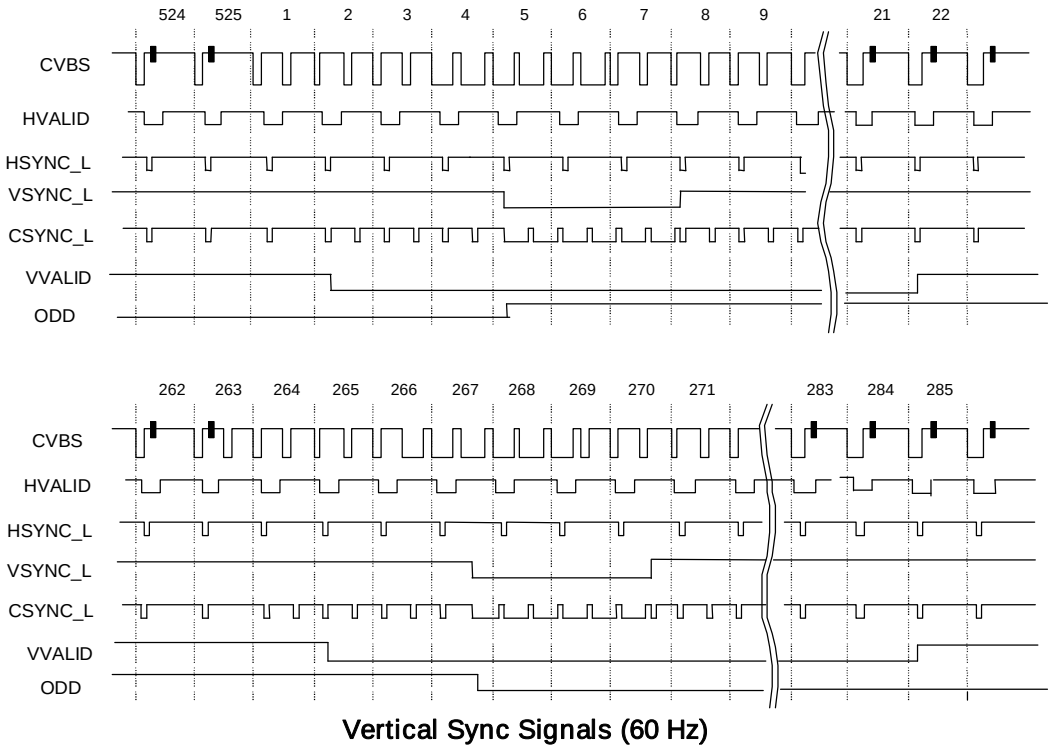


Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL frequency	0	100	400	KHz
tBUF	Bus open time	4.7			µs
tHD:STA	Start condition hold time	4.0			µs
tLOW	Clock LOW period	4.7			µs
tHIGH	Clock HIGH period	4.0			µs
tSU:STA	Start condition setup time	4.7			µs
tHD:DAT	Data hold time	300			ns
tSU:DAT	Data setup time	250			ns
tR	Line rise time			1	µs
tF	Line fall time			300	ns
tSU:STO	Stop condition setup time	4.7			µs

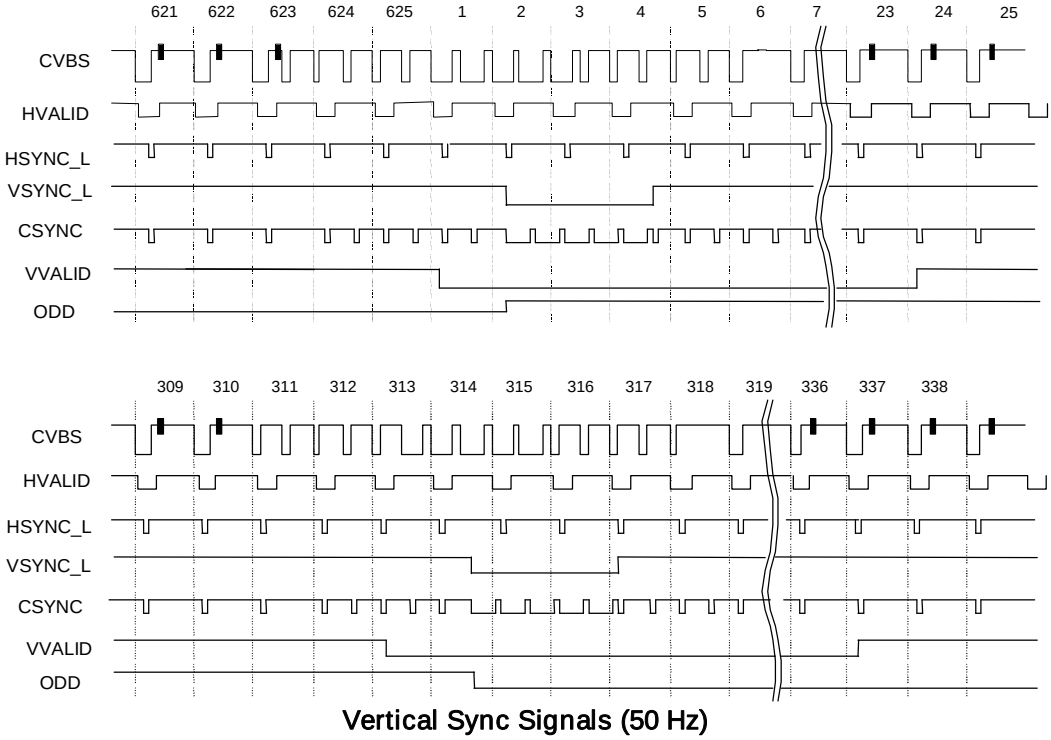
The I²C-bus timing should be designed based on the table above.

Sync Signal Input and Output Timing (Default)

The following illustrations show the timing of vertical sync signals. The internal processing of the sync signal is performed before 1H.



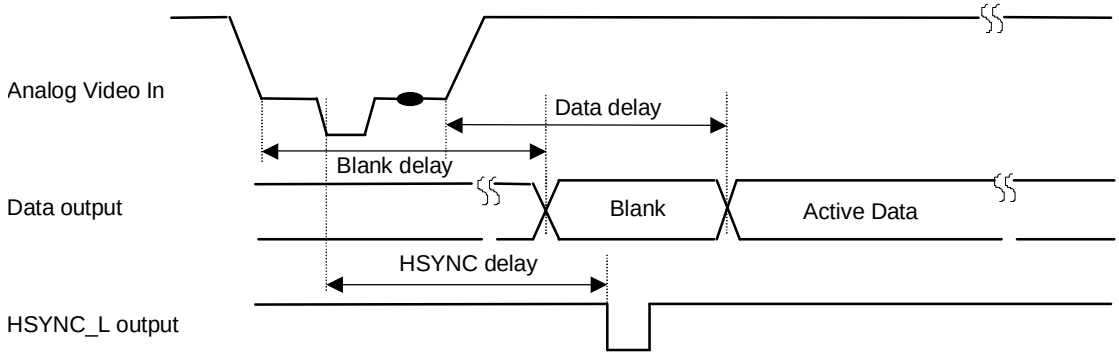
Vertical Sync Signals (60 Hz)



Vertical Sync Signals (50 Hz)

Input/Output Delays (at Standard Signal Input)

The illustration below shows the time delay between the input of a video signal and the output of digital data.

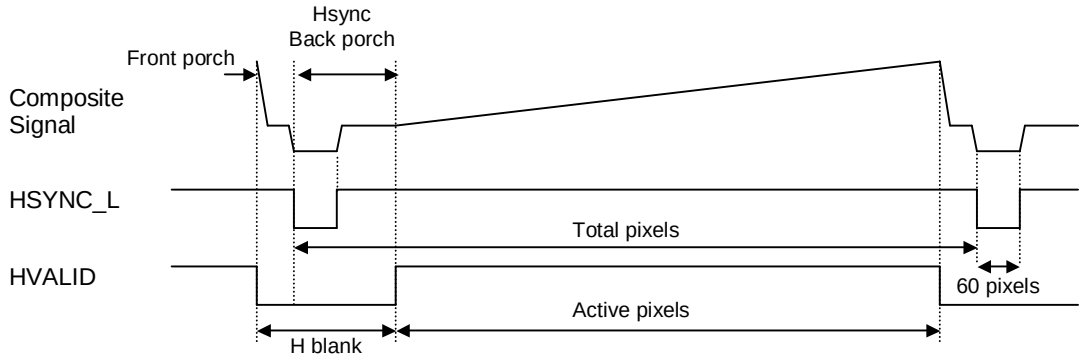


Absorption difference by T = 1 Pixel rate, α = FIFO

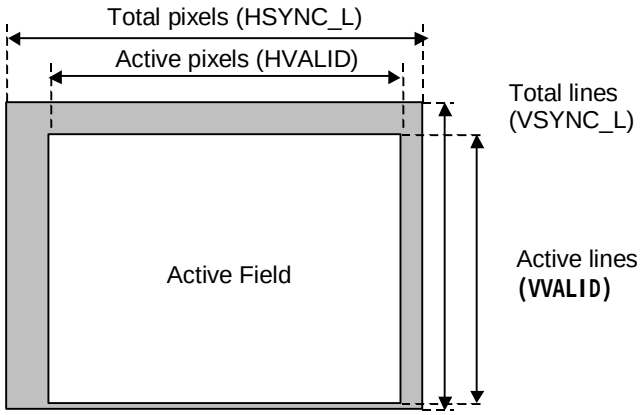
Video mode	Input signal	FIFO/FM mode	Delay
NTSC	Composite	FIFO-1	1.5H
NTSC	Composite	FM	1.5H
PAL	Composite	FIFO-1	1.5H
PAL	Composite	FM	1.5H

The data delay, blank delay, and sync signal delay are the same length.
1H varies with the sampling mode.
Depending on the signal status, the numeric value (T value) may vary.
In the FIFO mode, the output cycle is fixed, so the delay varies.
In the PAL mode, where Y/C separation is performed by trap filter, 1H is not added.

Active Pixel Timing



Note: Actually, there is an output delay of about 1H after video signal input.



Video Modes and Pixel/Line Counts (at Standard Signal Input)

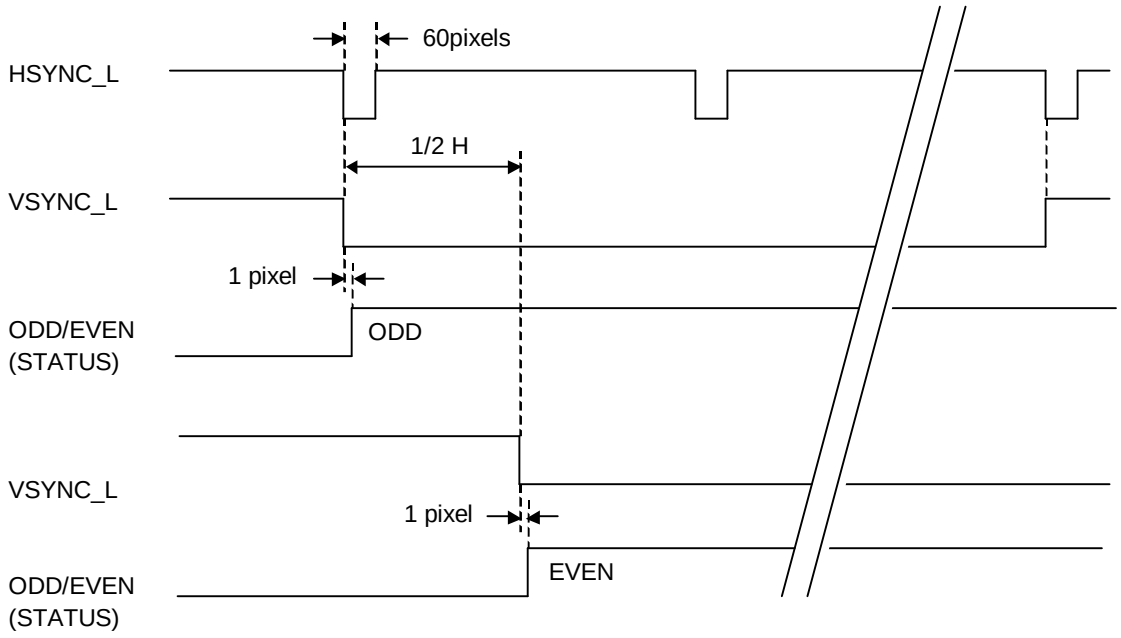
Video mode	Sampling Pixel mode	Output Pixel rate (MHz)	H					V		
			Front porch	Hsync Back porch	H blank	Active pixels	Total pixels	V blank	Active lines	Total lines
NTSC	ITUR.601	13.5	16	122	138	720	858	Odd/20 Even/20	Odd/243 Even/242	Odd/263 Even/262
	Square pixel	12.272727	22	118	140	640	780			
	4fsc	14.31818	16	126	142	768	910			
PAL	ITUR.601	13.5	14	130	144	720	864	Odd/23 Even/24	Odd/289 Even/289	Odd/312 Even/313
	Square pixel	14.75	34	142	176	768	944			

Note: Where the FIFO mode is used in asynchronous sampling operations with fixed clock, the 1-field sampling error accumulated in the line immediately following the fall of VVALID is reset. Therefore, the pixel count for the line that was reset will change. In addition, where the condition of VTR and other signals is poor in the FIFO-2 mode, the FIFO reset line might break in before the fall of VVALID.

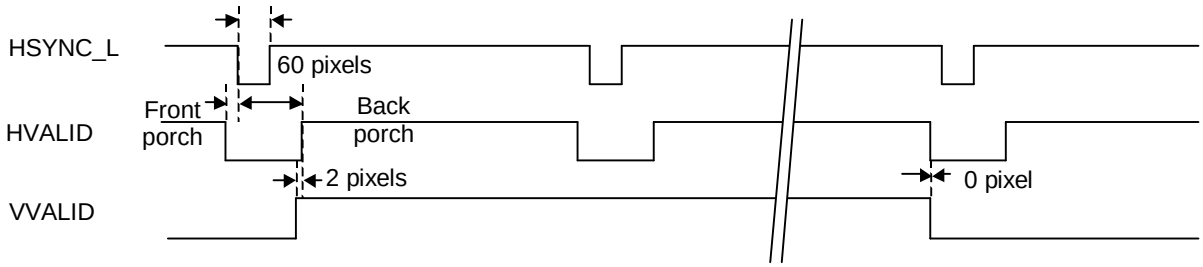
Sync Signals Output Timing (at Default/Standard Signal Input)

Each VALID signal and the ODD/EVEN signal are selected by the STATUS signal.

VSYNC_L, ODD/EVEN

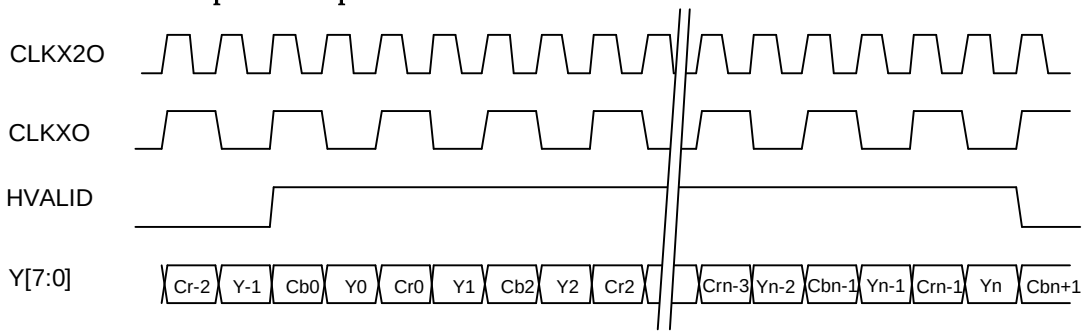


VALID Signal



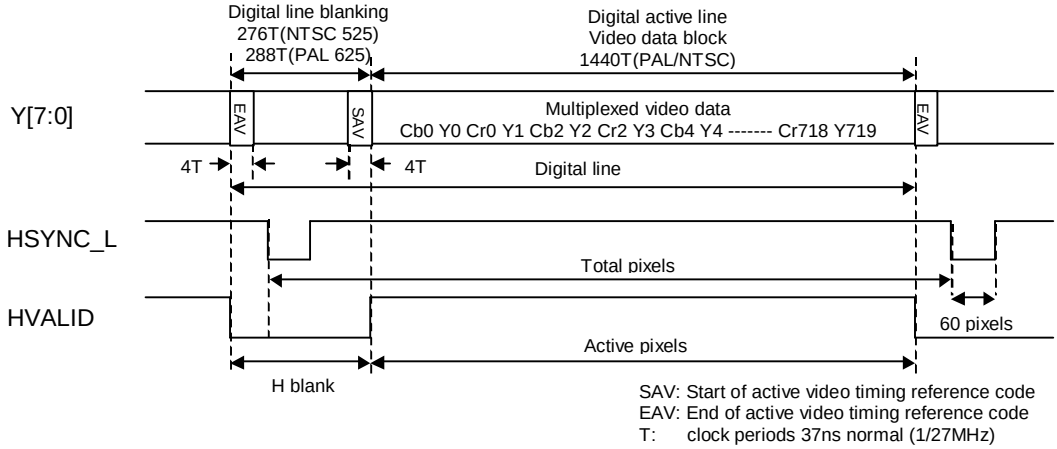
Output Timing by Mode

8-bit Y/CbCr Multiplexed Output



ITU-R BT.656-4 output:

Output is performed based on BT.656 of the ITU standards. Since sync signal information (SAV, EAV) is multiplexed with video data, for the interface that complies with BT.656, data can be transferred by connecting to 8-bit data lines, without connecting to the sync signal.



The data in the blanking period is masked, but the Y data can be output.

Note: When operating in the asynchronous sampling mode, digital lines 1716T (NTSC,525) and 1728T (PAL, 625) will change due to the sampling error.
In the FIFO mode, the pixels count correction function ensures that there is no fluctuation in the pixel count between active lines, but the line immediately following the fall of VVALID will change due to the FIFO reset.
In particular, when non-standard signals such as VTR signals are input, the line immediately following the fall of VVALID will vary greatly in accordance with the degree of the instability of the input signal. Where the sampling error is large, the line will change immediately before the fall of VVALID.
In some cases where the line count increases or decreases with respect to the reference, such as non-standard signals, EAV and SAV may not be guaranteed.

INTERNAL REGISTERS

The following is a list of registers.
Refer to the User's Manual for details of each register.

	W/R	Sub address	Register Bits								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
MRA	W/R	00	0	1	0	0	0	0	0	0	40
MRB	W/R	01	0	0	0	0	0	0	0	0	00
MRC	W/R	02	1	0	0	0	0	0	0	1	81
MRD	W/R	03	0	1	0	0	0	0	0	0	40
SYDR	W/R	04	0	0	0	0	1	0	0	0	08
HSYT	W/R	05	1	1	1	1	0	0	1	1	F3
STHR	W/R	06	1	0	1	0	1	1	0	1	AD
VSTHR	W/R	07	0	0	0	0	0	0	0	0	00
HSDL	W/R	08	0	0	0	0	0	0	0	0	00
HVALT	W/R	09	0	0	0	0	0	0	0	0	00
VVALT1	W/R	0A	0	0	0	0	0	0	0	0	00
VVALT2	W/R	0B	0	0	0	0	0	0	0	0	00
LUMC	W/R	0C	0	0	0	0	0	0	0	0	00
AGCLA	W/R	0D	0	1	0	0	0	0	0	0	40
AGCLB	W/R	0E	0	0	0	0	0	0	1	0	02
AGCRC	W/R	0F	0	0	0	0	0	0	0	0	00
CLC	W/R	10	1	0	0	0	0	0	0	0	80
SSEPL	W/R	11	0	0	0	0	0	0	0	0	00
CHRCA	W/R	12	0	0	1	0	0	0	0	0	20
CHRCB	W/R	13	0	0	0	0	0	0	0	0	00
ACCC	W/R	14	0	1	0	0	0	0	0	0	40
ACCRC	W/R	15	0	0	0	0	0	0	0	0	00
HUE	W/R	16	0	0	0	0	0	0	0	0	00
BBHC	W/R	17	1	0	0	1	0	1	0	0	94
OMRA	W/R	18	1	0	0	0	0	0	0	0	80
OMRB	W/R	19	0	0	1	0	1	0	1	0	2A
OMRC	W/R	1A	0	0	0	0	0	0	0	1	01
OMRD	W/R	1B	0	0	1	0	1	0	0	0	28
OMRE	W/R	1C	0	0	0	0	0	0	0	0	00
OMRF	W/R	1D	0	0	0	0	0	0	0	0	00
ADC1	W/R	1E	0	1	1	0	0	0	0	0	60
ADC2	W/R	1F	1	0	0	1	0	0	0	1	91
PLLR1	W/R	20	0	0	1	1	1	1	0	1	3D
PLLR2	W/R	21	0	0	0	1	1	0	1	1	1B
PLLR3	W/R	22	1	0	0	0	0	0	1	0	82
CCD1	W/R	23	0	0	0	0	0	0	0	0	00
CCD2	W/R	24	0	0	0	0	0	0	0	0	00

	W/R	Sub address	Register Bits								HEX
			MSB	Default Value						LSB	
			[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
CGMS1	W/R	25	0	0	0	0	0	0	0	0	00
CGMS2	W/R	26	0	0	0	0	0	0	0	0	00
AGCD1	W/R	27	0	0	0	0	0	0	0	0	00
AGCD2	W/R	28	0	0	0	0	0	0	0	0	00
WSSD	W/R	29	0	0	0	0	0	0	0	0	00
VBIDM	W/R	2A	1	0	0	0	0	1	1	0	86
AIREG	W/R	2B	0	0	0	0	0	0	0	0	00
STATUS	R	2C	—	—	—	—	—	—	—	—	—
VFLAG	R	2D	—	—	—	—	—	—	—	—	—
CCDO0	R	2E	—	—	—	—	—	—	—	—	—
CCDO1	R	2F	—	—	—	—	—	—	—	—	—
CCDE0	R	30	—	—	—	—	—	—	—	—	—
CCDE1	R	31	—	—	—	—	—	—	—	—	—
CGMSO0	R	32	—	—	—	—	—	—	—	—	—
CGMSO1	R	33	—	—	—	—	—	—	—	—	—
CGMSO2	R	34	—	—	—	—	—	—	—	—	—
CGMSE0	R	35	—	—	—	—	—	—	—	—	—
CGMSE1	R	36	—	—	—	—	—	—	—	—	—
CGMSE2	R	37	—	—	—	—	—	—	—	—	—
WSSD0	R	38	—	—	—	—	—	—	—	—	—
WSSD1	R	39	—	—	—	—	—	—	—	—	—

NOTES ON USE

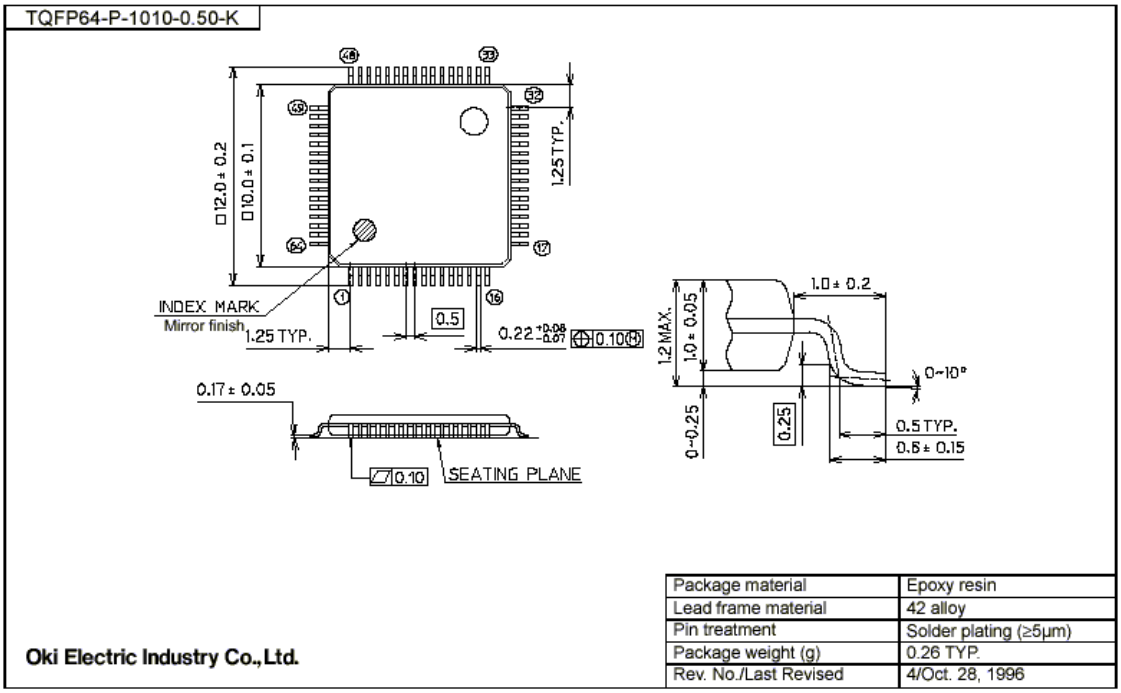
The ML86V7667 Video Decoder is being developed based on standard signals. Improvements are being made to ensure stable operation even with non-standard signals. However, the signal conditions and usage environments differ widely for signals such as those having a weak electromagnetic field, VTR playback signals, signals with numerous signal switching or a large amount of noise, and simple video signals from various cameras. As a result, stable operation for all signals has not yet been confirmed. Before using the decoder, please carefully evaluate and consider the signal conditions and usage environment of the intended use.

In addition to this Data Sheet, a ML86V7667 User's Manual is also available. The User's Manual explains each register and provides examples of adapted circuits as well as other information helpful in the design phase. Please read the User's Manual before embarking on design work.

Users are also requested to regularly download the most recent versions of this Data Sheet and the User's Manual from the Oki web site. As the newest information, not included in printed materials, and the answers to frequently asked questions are published on the web site, users are recommended to check the site regularly for updates.

PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.26 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL86V7667-00	Oct. 20, 2004	–	–	Preliminary edition 1

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

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