TB-6V-LX760-LSI
Hardware User Manual

Rev.3.00

Revision History

Version	Date	Description	Publisher
Rev.1.xx	2009/xx/xx	Preliminary	
Rev.2.00	2010/05/06	Initial release	Sen Odajima
Rev.2.01	2010/06/25	-Added J66, J53 to figure 12-1 -Modified table 12-1 Added J66,J53 Separate SW5,SW6 Changed initial settings : No1, 6 ,7 ,18, 20.21	Yoshioka
Rev.2.02	2010/07/07	- Modified table 6-1, table 6-2, table 6-3 - Modified figure 6-1, figure 7-3 - Delete wrong information on 8-3 FMC connector - Modified explaining of clock signal of each FMC connectors - Modified figure 9-1 - Add DIP SW pin number on table 9-1 and 9-2 - Changed connector for FAN on 6.5 Power supply for FAN	Yoshioka
Rev.2.03	2012/04/24	-Modified Q'ty of TB-FMCH-STACK and Q'ty of TB-FMCH-CONNECTRO	Yoshioka
Rev.3.00	2012/07/17	- Modified revision of pin assign table - Modified PCB dimension and surface coating - Modified External view - Modified Table 8-1 LA06_P/N, LA33_P/N, CLK1_M2C_P/N and CLK0_M2C_P/N - Add comment to Table 8-1, 8-2, 8-6, 8-7: LA33_P/N. these are not differential pair - Modified Table 8-2 LA15_P/N, LA19_P/N, LA33_P/N, CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-4 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-5 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-6 LA11_P/N, LA33_P/N, CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-7 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-8 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-9 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Table 8-10 CLK1_M2C_P/N and CLK0_M2C_P/N - Modified Figure 1-3 Power Supply Arrangement for FPGA Banks - Modified Spec of FAN - Added 11-4 Pin header and Table 11-4 pin assign of pin header - Modified Figure 12-1 Default settings - Modified Table 12-1 Initial Settings (removed J66)	Yoshioka

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Introduction

Thank you for purchasing the TB-6V-LX760-LSI board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions

Observe the precautions listed below to prevent injuries to you, other personnel or damage to property.

Before using the product, read these safety precautions carefully to assure safe use.
These precautions contain serious safety instructions that must be observed.
After reading through this manual, be sure to always keep it handy.

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with property if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact technical support.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates at high speed, do not put your hand close to it or touch it. Otherwise, it may cause injury.
	**Do not place the product in an unstable position.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash on it.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may be damaged and break down or it may cause a fire or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Static locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is a Xilinx Virtex6 FPGA evaluation board. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please see attached "Welcome latter" on the products.

Board accessories:

- FMC spacer set

2. Overview

This document describes the design specification of the TB-6V-LX760-LSI board.

The design covers the TB-6V-LX760-LSI board and two FMC option boards (TB-FMCH-STACK and TB-FMCH-CONNECTOR).

3. Feature

FPGA Devices	:	XC6VLX760-2FFG1760
	:	XC3S700AN-4FGG484C (It is only for Virtex-6 Configuration)
Memory		
DDR3 SDRAM CH1	:	1Gbit (8Meg x 16bit x 8Bank) x 2
DDR3 SDRAM CH2	:	1Gbit (8Meg x 16bit x 8Bank) x 2
NAND FLASH	:	4G (16bit) x 1 (for FPGA Configuration)
SPI Flash	:	64MBit x 1 (for MicroBlaze)
BPI Flash	:	256MBit x 1 (for test)
Interface		
FMC (LPC)	:	Connectors for component side x 10
FMC (LPC)	:	Connectors for solder side x 10
USB	:	Type B Hi-speed USB (target)
SD CARD	:	MicroSD (It is only for Virtex-6 Configuration)
Expansion Connector	:	x 1 (30-bit) connecting to XC6VLX760
Others		
LTC2978CUP	:	Onboard power source monitor
Clock	:	OSC 24MHz for USB (mounted)
	:	50MHz for XC3S700AN (mounted)
	:	266MHz for DDR3 (mounted)
	:	16MHz for PLL (mounted)
I2C	:	4pin Header
FAN	:	3pin Header connecting to XC3S700AN
LED	:	Green color LED for XC6VLX760 configuration DONE
	:	14 general purpose green color LEDs connecting to XC6VLX760
	:	2 general purpose red LEDs connecting to XC6VLX760
	:	Green color LED for XC3S700AN configuration DONE
	:	3 general purpose red LEDs connected to XC3S700AN
SW	:	Pushbutton switch to initiate configuration
	:	General purpose 16-bit DIP switch connected to XC6VLX760
	:	General purpose 4-bit pushbutton switch connected to XC6VLX760
Rotary SW	:	2 switches connected to XC3S700AN

Power Supply: The +12 volt power supply can be derived either from the Molex 39-29-1048 connector or from the 39-30-0060. A dedicated power supply is attached.
Onboard power supply module: Various Linear modules (LTM4601A, LTM4606, LTM8025 etc.)

Holes for fixing an FPGA radiator, dedicated heat sink and FAN
Spacers and screws for attaching option boards

5 TB-FMCH-STACK boards and 3 TB-FMCH-CONNECTERs
Warning Virtex-6 FPGA does not support 3.3V IO.

4. Block Diagram

The following figure represents the block diagram of the TB-6V-LX760-LSI and illustrates the assignment of various blocks and connectors to IO banks on the FPGA.

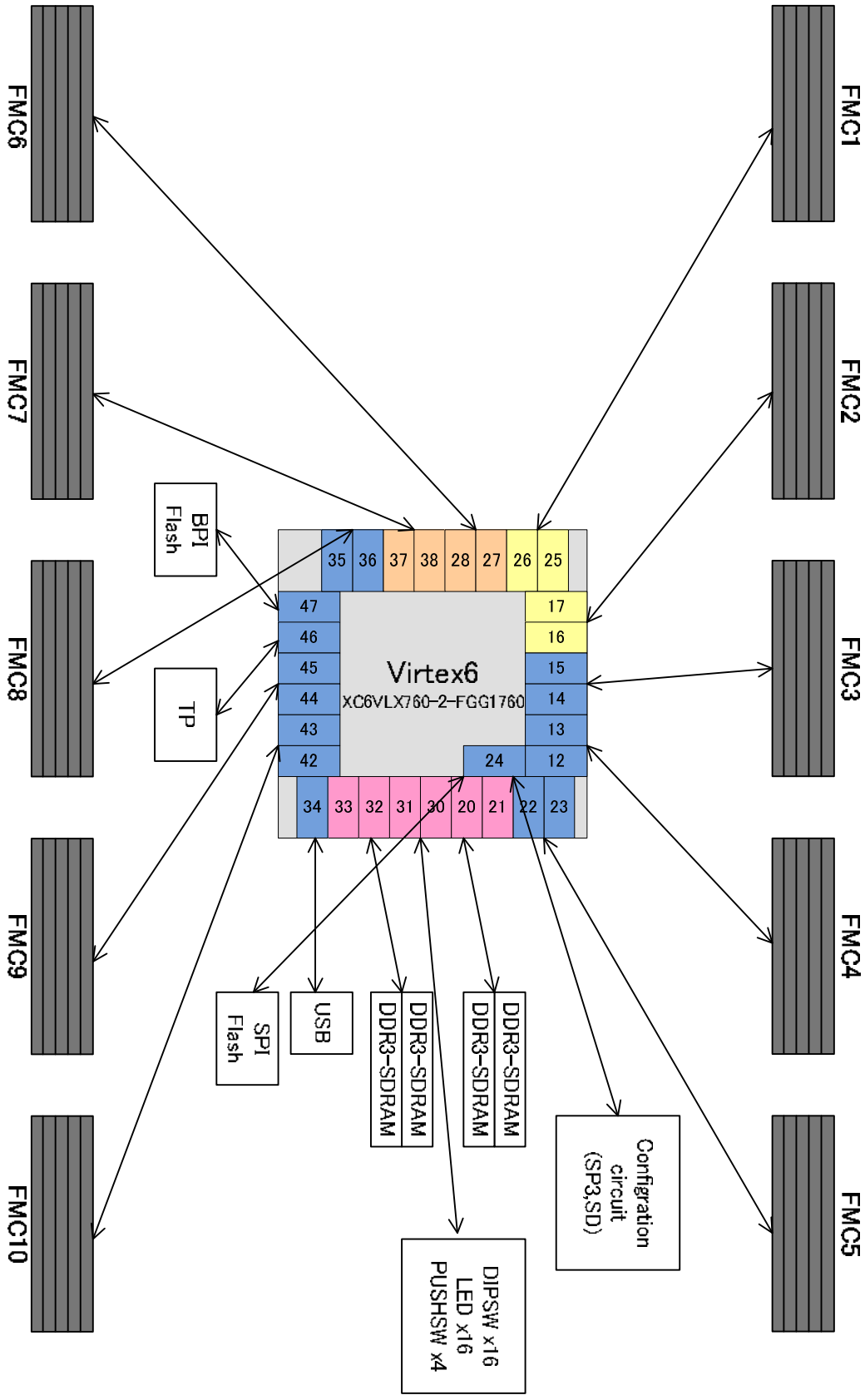

Figure4-1 Block Diagram

5. External View of the Board

5.1. TB-6V-LX760-LSI

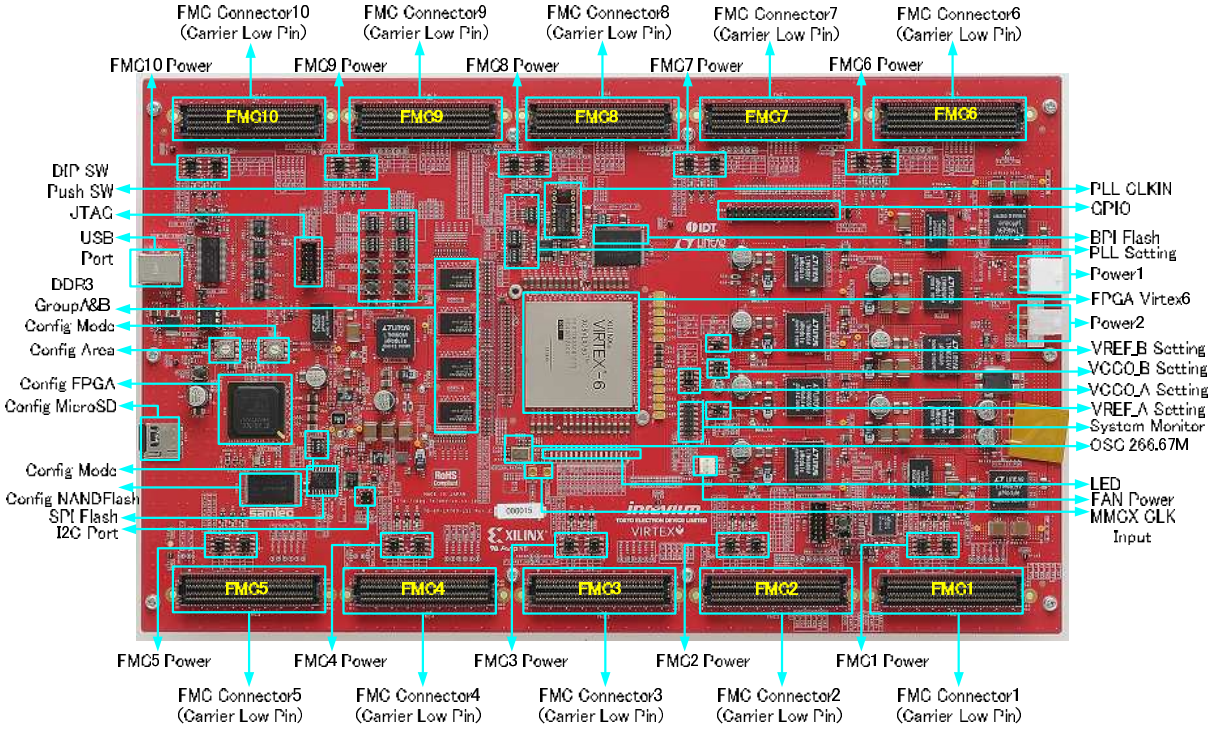

Figure5-1 Component Side

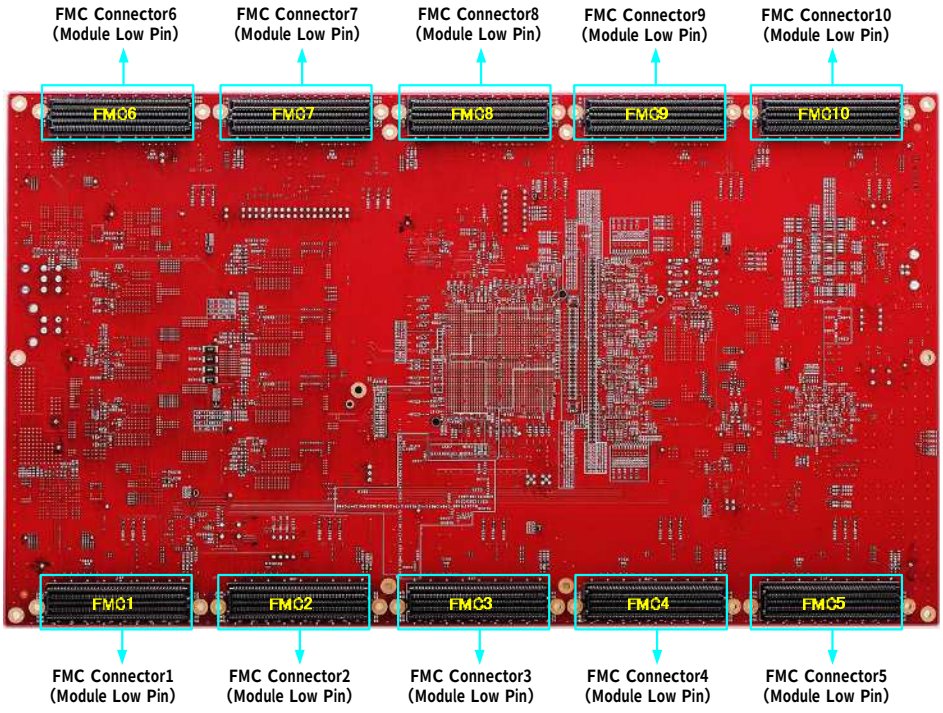

Figure5-2 Solder Side

5.2. TB-FMCH-STACK and TB-FMCH-CONNECTOR

The TB-FMCH-STACK and the TB-FMCH-CONNECTOR permit the interconnection of multiple TB-6V-LX760T-LSI boards in either a horizontal or vertical configuration.

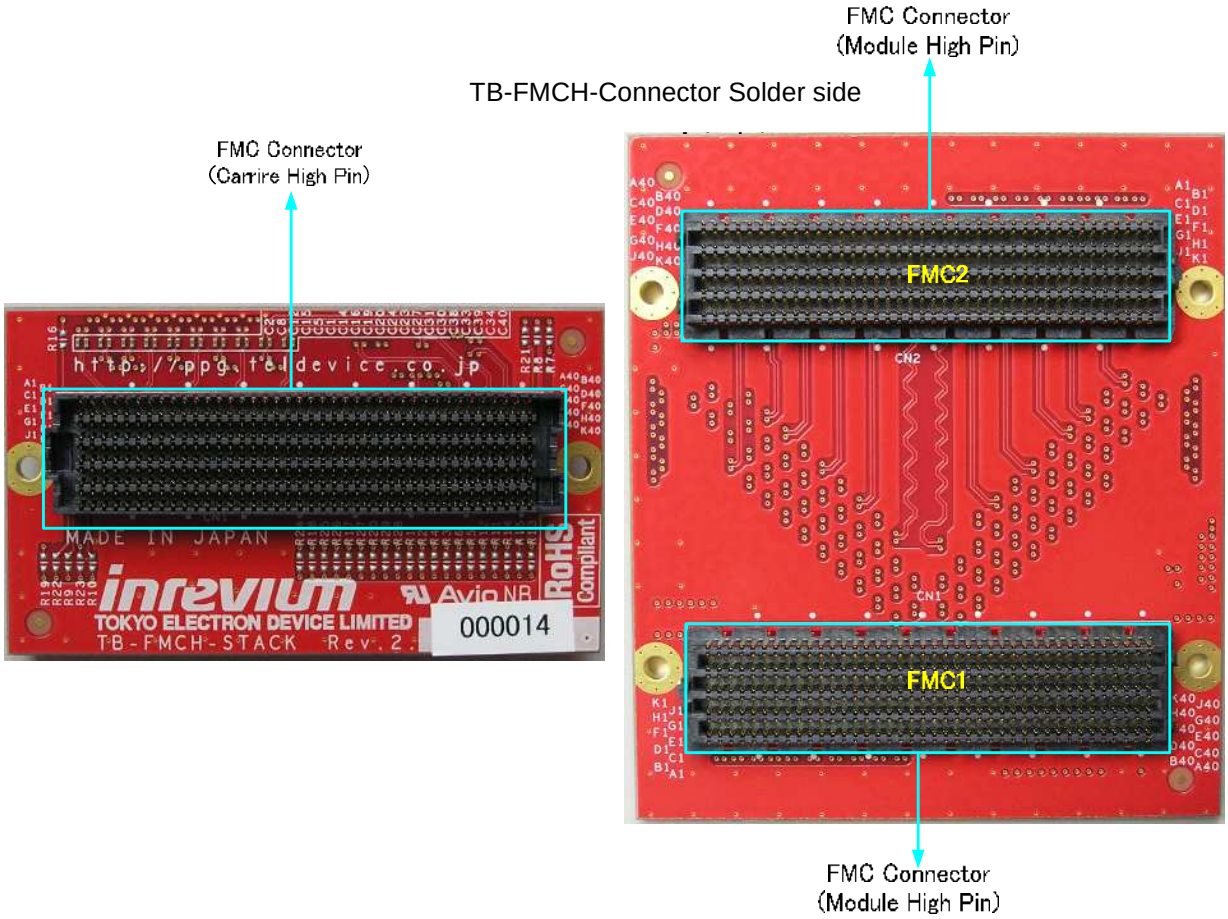

Figure5-3 External view of the TB-FMCH-STACK and TB-FMCH-CONNECTOR

6. Board Specifications

6.1. TB-6V-LX760-LSI Board Structure

The following table shows the board structure and the specifications.
For details about connector locations, refer to the board layout drawing.
For details about clock structure and operational frequency, refer to the clock system diagram.

Table6-1 TB-6V-LX760-LSI Board Structure

Item	Category-I	Category-II	Specification	Remarks
1	Board Structure	Number of Layers	16	
2		Dimensions	369mm x 225mm	
3		Thickness	3mm	
4		Resist Color	Red	
5		Material	FR-4	
6	Height	Component Side	13.0mm (without FAN and power connector)	
7		Solder Side	7.1mm	
8	Impedance Control	Single Signal	50 Ohm	
9		Differential Signal	90 Ohm, 100 Ohm	
10	RoHS/Pbfree	RoHS/Pbfree	RoHS, lead-free solder	
11	Surface Coating	-	Gold plating	

6.2. TB-FMCH-STACK Board Structure

The following table shows the board structure and the specifications.
For details about connector locations, refer to the board layout drawing.

Table6-2 TB-FMCH-STACK Board Structure

Item	Category-I	Category-II	Specification	Remarks
1	Board Structure	Number of Layers	16	
2		Dimensions	69mm x 40mm	
3		Thickness	3mm	
4		Resist Color	Red	
5		Material	FR-4	
6	Height	Component Side	6.5mm	
7		Solder Side	7.1mm	
8	Impedance Control	Single Signal	50 Ohm	
9		Differential Signal	100 Ohm	
10	RoHS/Pbfree	RoHS/Pbfree	RoHS, lead-free solder	
11	Surface Coating	-	Gold plating	

6.3. TB-FMCH-CONNECTER Board Structure

The following table shows the board structure and the specifications.

For details about connector locations, refer to the board layout drawing.

Table6-3 TB-FMCH-CONNECTER Board Structure

Item	Category-I	Category-II	Specification	Remarks
1	Board Structure	Number of Layers	16	
2		Dimensions	69mm x 80mm	
3		Thickness	3mm	
4		Resist Color	Red	
5		Material	FR-4	
6	Height	Component Side	2mm	
7		Solder Side	7.1mm	
8	Impedance Control	Single Signal	50 Ohm	
9		Differential Signal	100 Ohm	
10	RoHS/Pbfree	RoHS/Pbfree	RoHS, lead-free solder	
11	Surface Coating	-	Gold plating	

6.4. Layout of TB-6V-LX760-LSI Board Components

The following figure shows the dimensions of the TB-6V-LX760-LSI.

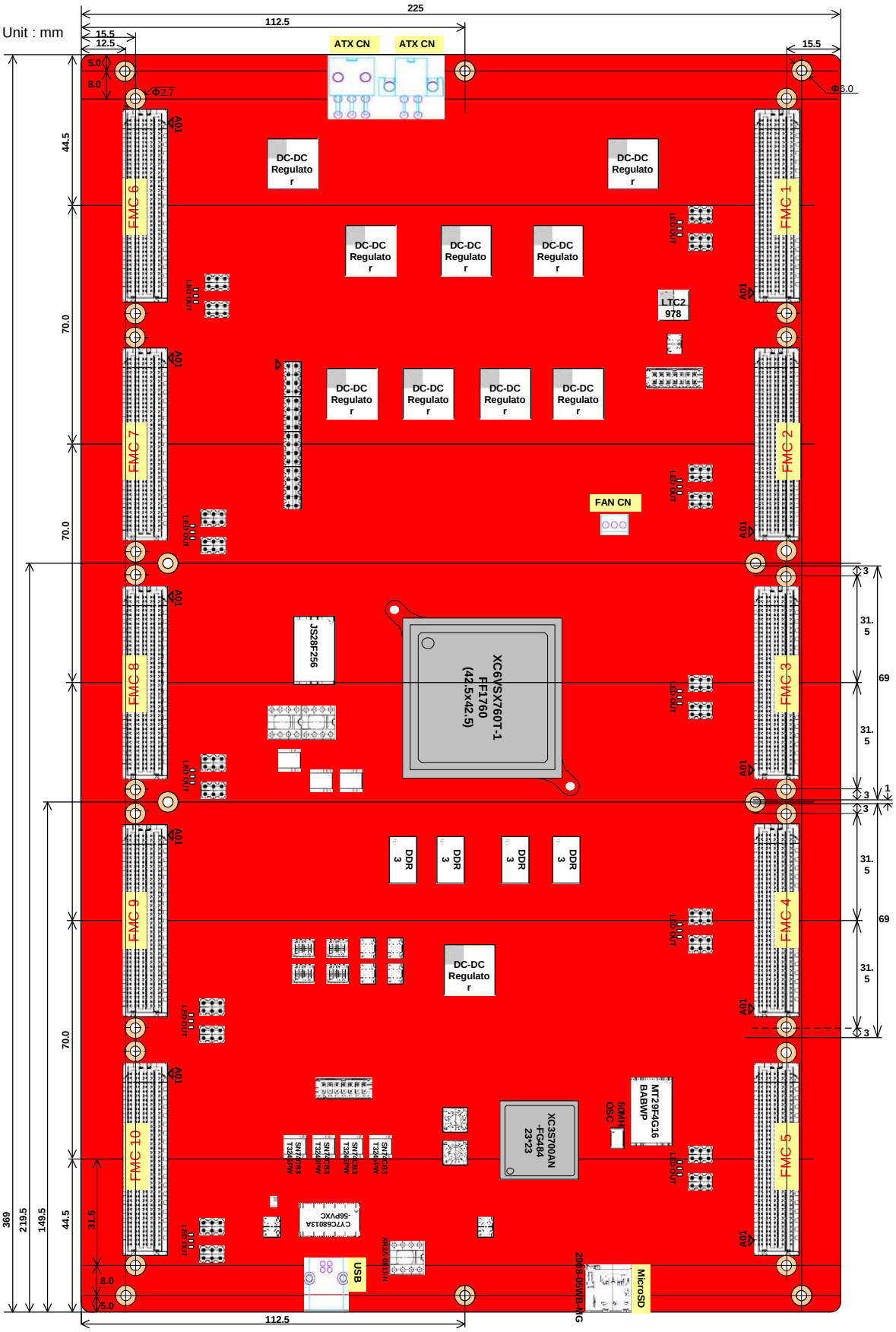

Figure6-1 Layout of TB-6V-LX760-LSI Board Components

6.5. Layout of the TB-FMCH-STACK Board Components

The following figure shows the dimensions of the TB-FMCH-STACK board and locations of its connectors.

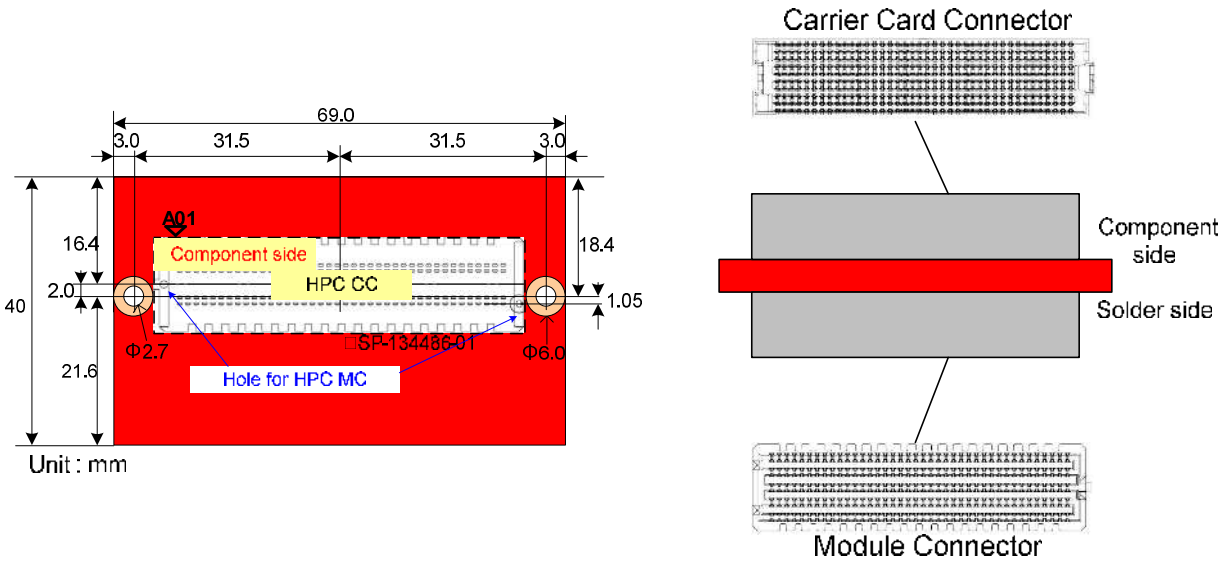

Figure6-2 Layout of the TB-FMCH-STACK Board Components

6.6. Layout of the TB-FMCH-CONNECTER Board Components

The following figure shows the dimensions of the TB-FMCH-CONNECTER board and locations of its connectors.

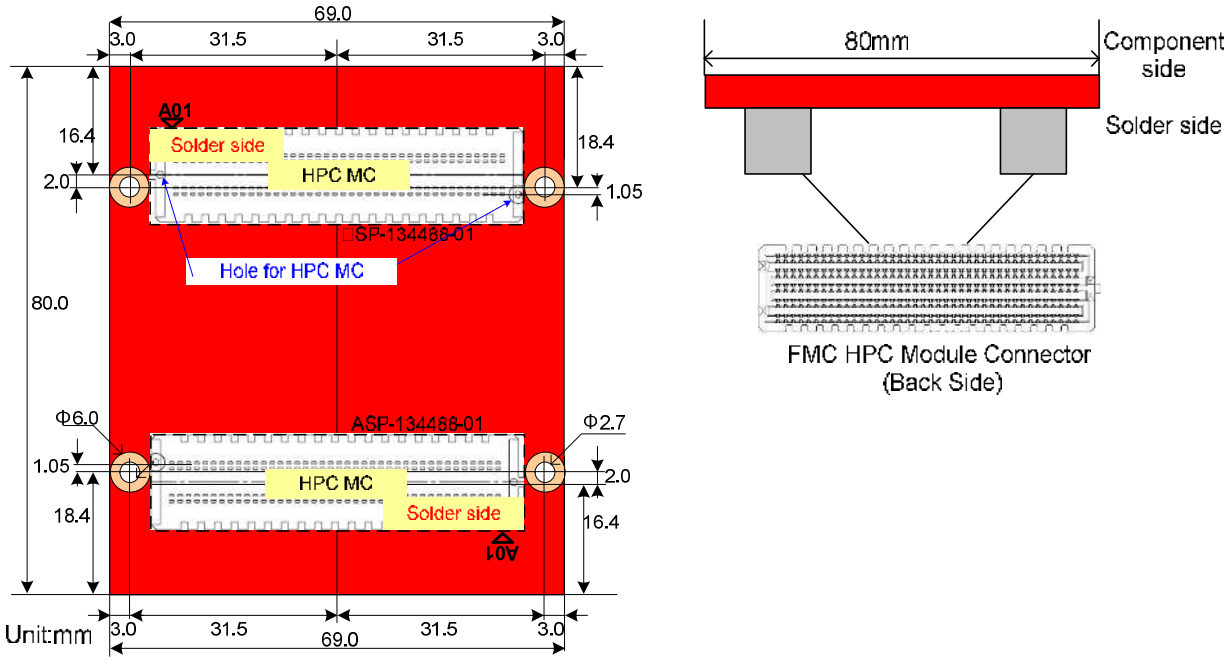

Figure6-3 Layout of the TB-FMCH-CONNECTER Board Components

7. Description of Components

7.1. DDR3 SDRAM

The TB-6V-LX760-LSI board has four DDR3 SDRAM chips.
Device: MT41J64M16LA-15E:B (Micron) 1-Gbit (8Meg x 16bit x 8Bank) x 4 or equivalents

The DDR3 memory device can be divided into two groups as shown in following figure.

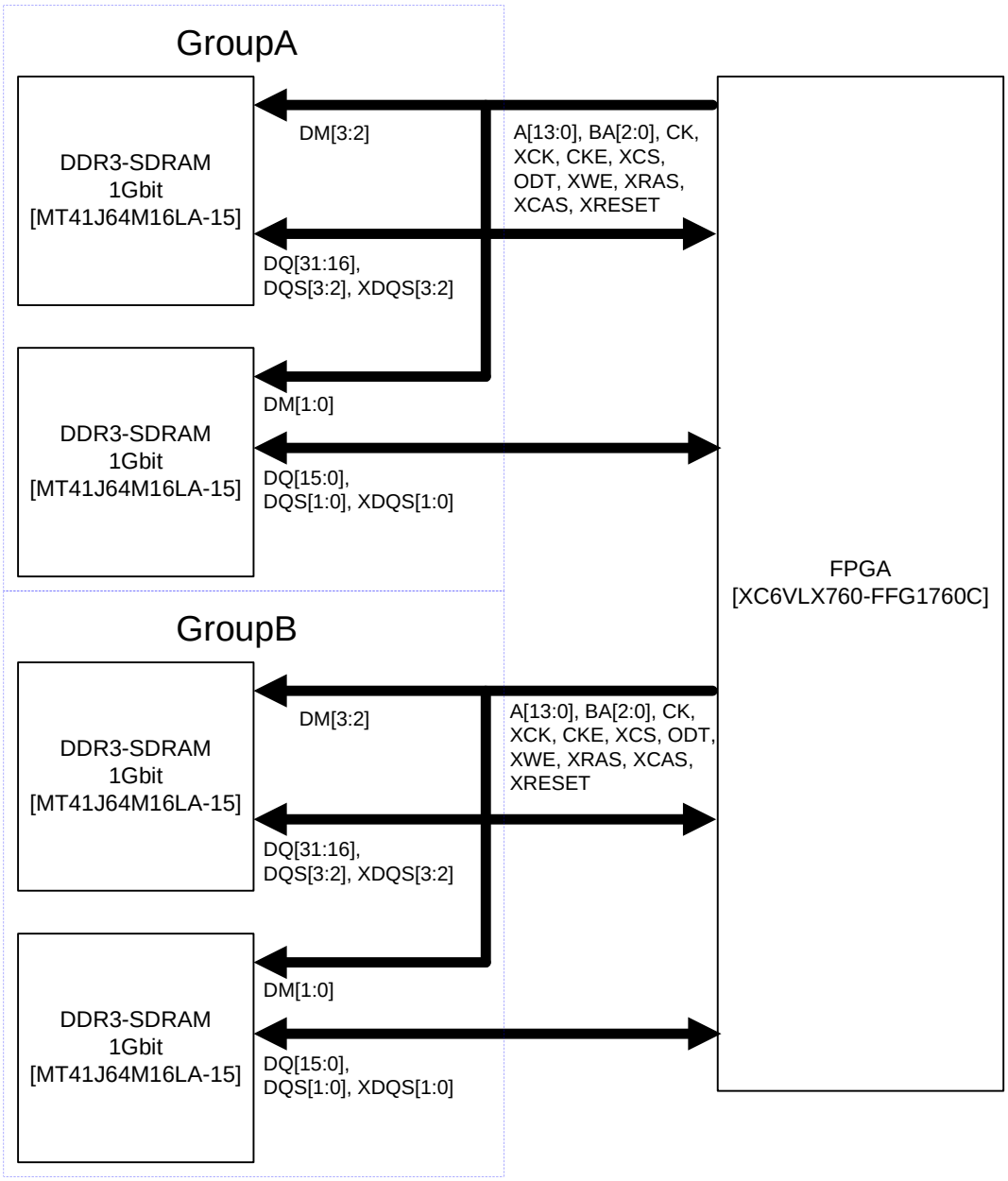

Figure7-1 DDR3 Peripheral Connections

7.2. SPI FLASH

The TB-6V-LX760-LSI board has one SPI Flash memory device.

Device: M25P64-VMF6TP (Numonyx) 64-MBit

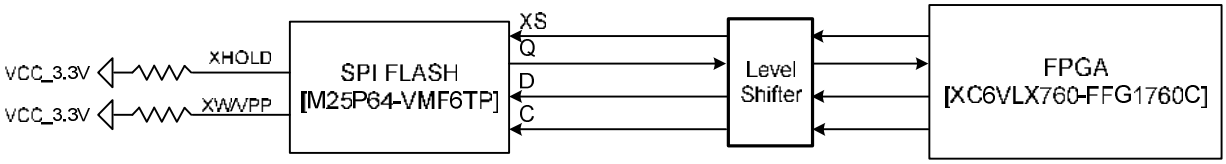

Figure7-2 SPI Flash Peripheral Connections

7.3. BPI FLASH

The TB-6V-LX760-LSI board has one BPI Flash memory device.

Device: JS28F256P30TF (Numonyx) 256-MBit

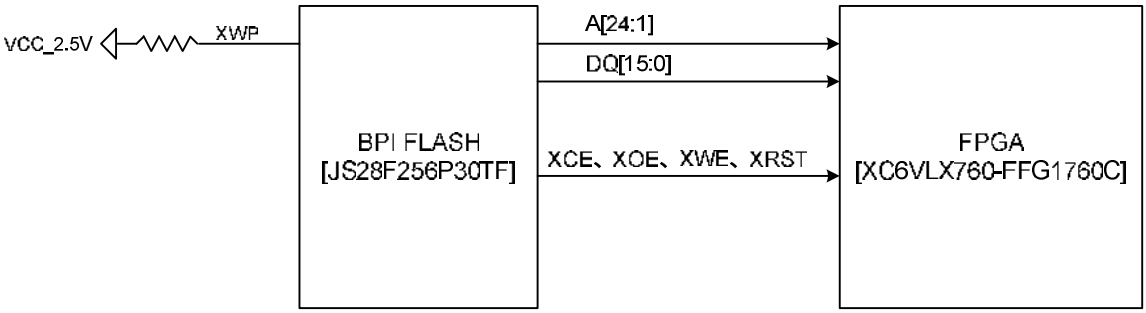

Figure7-3 BPI Flash Peripheral Connections

7.4. MicroSD/NAND FLASH (these are only for Virtex-6 configuration)

The TB-6V-LX760-LSI board has one NAND Flash for storing Virtex-6 configuration files and one MicroSD socket.

The Spartan-3AN reads the data stored in the Micro SD/NAND Flash memory device to configure the Virtex-6 device.

Device: NAND Flash: MT29F4G16BABWP (Micron) 4-G (16-bit)

For more information, refer to the related document “Configuration Method Using SD and XC3S700AN” (uSD_CONF_UserManual_V6LSI_x.xxe.pdf).

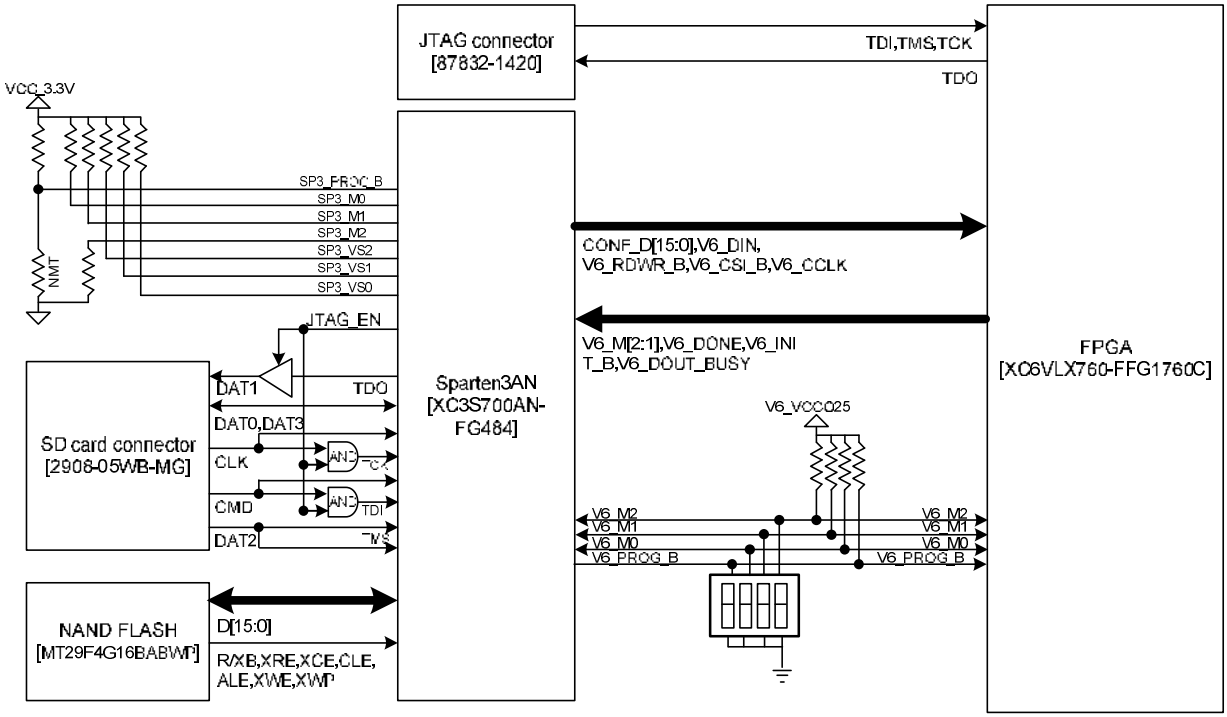

Figure7-4 CONFIG Peripheral Connections

The following figure shows the JTAG chain of Virtex-6 and Spartan-3AN.

The Spartan-3AN comes with burned ROM data for configuration.

No need to change it, if it is used in an ordinary way.

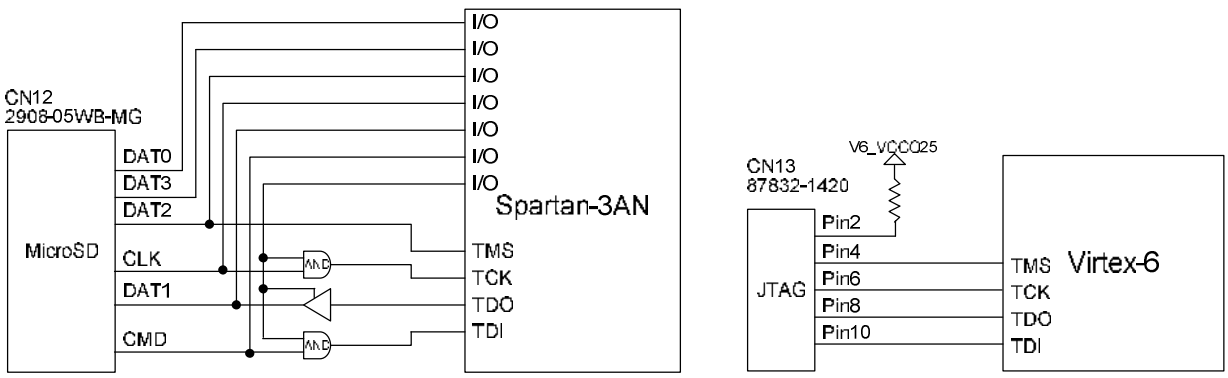

Figure7-5 JTAG Chain

8. Interfaces

8.1. USB and I2C

USB Connector Type B: 67068-8000

USB PHY: CY7C68013A-56PVXC

I2C Connector Pin Header: A2-2PA-2.54DSA

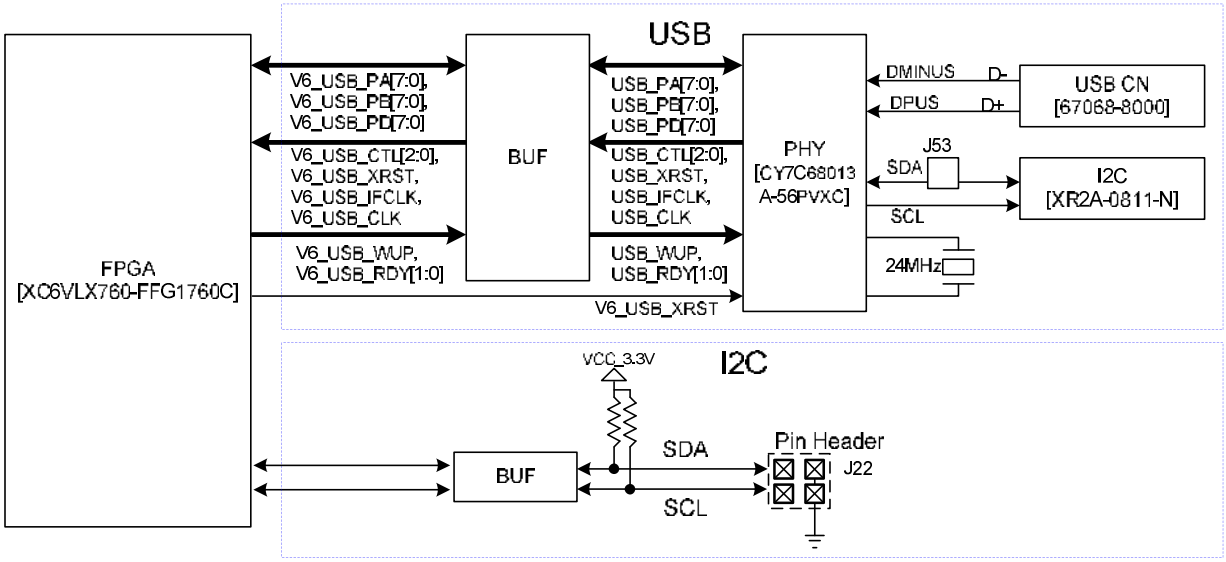

Figure8-1 USB and I2C Peripheral Connections

8.2. Method of Rewriting an EEPROM for USB PHY

Free software “EzMr.exe” is available from Cypress Semiconductor Corporation for rewriting the CY7C68013 EEPROM. The following procedure describes how to rewrite an EEPROM. (Contact Cypress Semiconductor for more information if necessary.)

1. Remove the J53 jumper
2. Connect the board to a PC using a USB cable.
3. Run EzMr.exe.
4. Reinstall jumper J53.
5. On the EzMr.exe panel select the EEPROM Erase File (.hex) to erase the EEPROM data.
6. After completion of downloading, disconnect the USB cable.
7. Connect it again to get the PC to recognize the board once more.
8. On the EzMr.exe panel select the target firm binary data (.iic) and download it.
9. Again, disconnect and reconnect the USB cable to get the PC recognize it.
10. That’s all.

8.3. FMC Connector

The TB-6V-LX760-LSI board has 10 FMC LPC connectors (Carrier type) on its component side and 10 FMC LPC connectors (Module type) on its solder side. The following figure shows the FPGA to FMC connections. For details about FPGA pinouts, refer to the board circuit diagram. A Microsoft Excel spreadsheet document, defining the pinouts, is also available as a published reference.

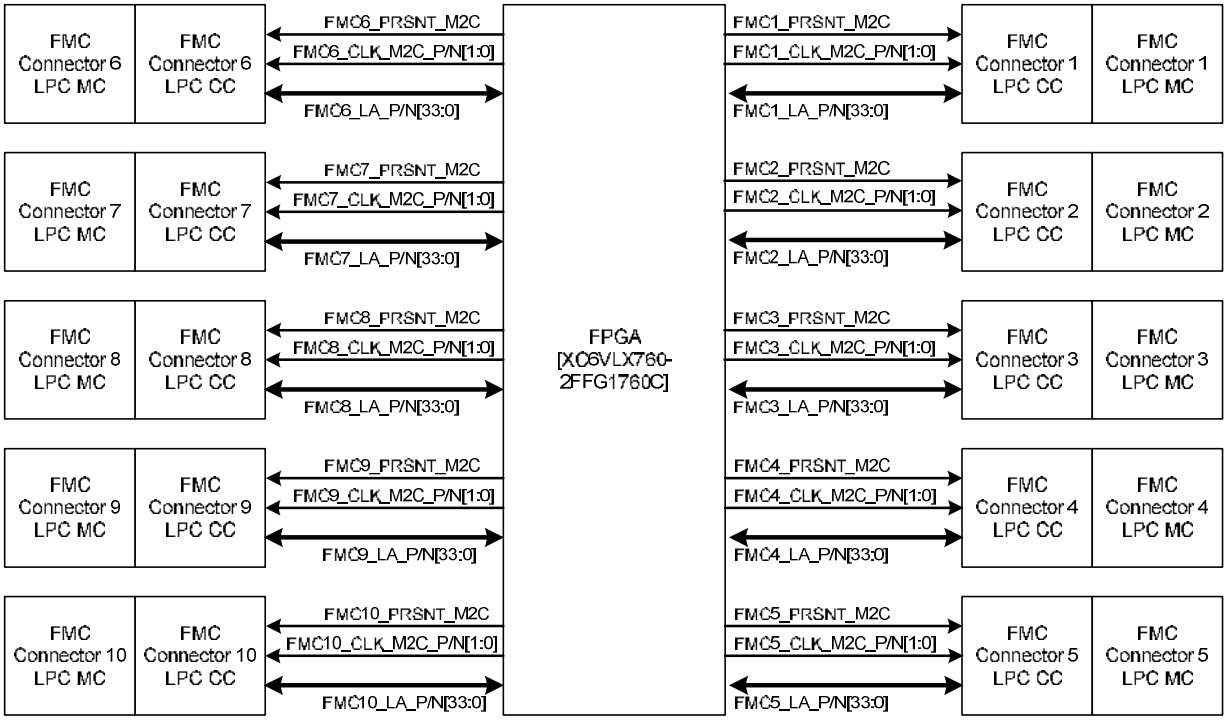

Figure8-2 FMC Connector Peripheral Connections

The following figure shows the FMC connector pinout.

Note that not all LPC (Low-Pin Count) are connected to the FPGA.

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure8-3 Low-Pin Count Pinouts

8.3.1. FMC1 LPC MC / CC Connector

The FMC connector (J43/J67) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 1 pair is assigned to the GC pin and 1 pair is assigned to the MRCC pins of the FPGA. Also, LA33_P and LA33_N is not FPGA deferential signal pair pin. So, LA33_P/N cannot use for differential signal interface. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-1 FMC1 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	* 4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	A39	26
		GND	9	LA01_N_CC	B38	26
26	P25	LA06_P	10	GND		
26	R25	LA06_N	11	LA05_P	H35	26
		GND	12	LA05_N	H34	26
		GND	13	GND		
25	D38	LA10_P	14	LA09_P	D35	25
25	C38	LA10_N	15	LA09_N	E34	25
		GND	16	GND		
		GND	17	LA13_P	C35	25
25	G34	LA14_P	18	LA13_N	B34	25
25	H33	LA14_N	19	GND		
		GND	20	LA17_P_CC	M29	26
		GND	21	LA17_N_CC	N28	26
26	K30	LA18_P_CC	22	GND		
26	J31	LA18_N_CC	23	LA23_P	C33	25
		GND	24	LA23_N	D32	25
		GND	25	GND		
26	G33	LA27_P	26	LA26_P	A36	25
26	G32	LA27_N	27	LA26_N	B36	25
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
25	N31	CLK1_M2C_P	2	*6 PRSNT_M2C_L	G31	26
25	M32	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	D33	26
		GND	5	CLK0_M2C_N	E33	26
25	N30	LA00_P_CC	6	GND		
25	P31	LA00_N_CC	7	LA02_P	M31	25
		GND	8	LA02_N	L32	25
25	G36	LA03_P	9	GND		
25	F36	LA03_N	10	LA04_P	F34	25
		GND	11	LA04_N	F35	25
25	B37	LA08_P	12	GND		
25	A37	LA08_N	13	LA07_P	F37	25
		GND	14	LA07_N	E37	25
26	B33	LA12_P	15	GND		
26	C34	LA12_N	16	LA11_P	C36	25
		GND	17	LA11_N	D37	25
25	P30	LA16_P	18	GND		
25	N29	LA16_N	19	LA15_P	K32	25
		GND	20	LA15_N	J32	25
26	E32	LA20_P	21	GND		
26	F32	LA20_N	22	LA19_P	H29	26
		GND	23	LA19_N	H30	26
26	M28	LA22_P	24	GND		
26	L29	LA22_N	25	LA21_P	K28	26
		GND	26	LA21_N	J28	26
26	L27	LA25_P	27	GND		
26	M27	LA25_N	28	LA24_P	A35	26
		GND	29	LA24_N	A34	26
25	R28	LA29_P	30	GND		
25	P28	LA29_N	31	LA28_P	P26	26
		GND	32	LA28_N	N26	26
26	P27	LA31_P	33	GND		
26	R27	LA31_N	34	LA30_P	A32	26
		GND	35	LA30_N	B32	26
25	K33	LA33_P	36	GND		
25	L31	LA33_N	37	LA32_P	F31	26
		GND	38	LA32_N	F30	26
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.2. FMC2 LPC MC / CC Connector

The FMC connector (J44/J68) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. Also, LA33_P and LA33_N is not FPGA deferential signal pair pin. So, LA33_P/N cannot use for differential signal interface. The following table shows the pin mapping assignments between the FPC connector and the FPGA.

Table8-2 FMC2 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	T31	16
		GND	9	LA01_N_CC	T32	16
16	J40	LA06_P	10	GND		
16	K39	LA06_N	11	LA05_P	N33	17
		GND	12	LA05_N	P32	17
		GND	13	GND		
17	G37	LA10_P	14	LA09_P	P33	17
17	H36	LA10_N	15	LA09_N	N34	17
		GND	16	GND		
		GND	17	LA13_P	J36	17
17	H39	LA14_P	18	LA13_N	K35	17
17	G39	LA14_N	19	GND		
		GND	20	LA17_P_CC	J42	16
		GND	21	LA17_N_CC	H41	16
16	L42	LA18_P_CC	22	GND		
16	L41	LA18_N_CC	23	LA23_P	F41	17
		GND	24	LA23_N	E42	17
		GND	25	GND		
17	C41	LA27_P	26	LA26_P	D42	17
17	C40	LA27_N	27	LA26_N	D41	17
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
16	M38	CLK1_M2C_P	2	*6 PRSNT_M2C_L	D40	17
16	M37	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	J38	17
		GND	5	CLK0_M2C_N	J37	17
16	M36	LA00_P_CC	6	GND		
16	N35	LA00_N_CC	7	LA02_P	L40	16
		GND	8	LA02_N	K40	16
16	U33	LA03_P	9	GND		
16	T34	LA03_N	10	LA04_P	K38	16
		GND	11	LA04_N	L37	16
17	K37	LA08_P	12	GND		
17	L36	LA08_N	13	LA07_P	R33	16
		GND	14	LA07_N	R32	16
17	L35	LA12_P	15	GND		
17	M34	LA12_N	16	LA11_P	M33	17
		GND	17	LA11_N	L34	17
17	K34	LA16_P	18	GND		
17	J35	LA16_N	19	LA15_P	A41	17
		GND	20	LA15_N	A40	17
16	K42	LA20_P	21	GND		
16	J41	LA20_N	22	LA19_P	F40	17
		GND	23	LA19_N	F39	17
16	G42	LA22_P	24	GND		
16	F42	LA22_N	25	LA21_P	P38	16
		GND	26	LA21_N	P37	16
16	H40	LA25_P	27	GND		
16	G41	LA25_N	28	LA24_P	R34	16
		GND	29	LA24_N	P35	16
17	B41	LA29_P	30	GND		
17	B42	LA29_N	31	LA28_P	P36	16
		GND	32	LA28_N	N36	16
17	E39	LA31_P	33	GND		
17	E38	LA31_N	34	LA30_P	T35	16
		GND	35	LA30_N	R35	16
16	U31	LA33_P	36	GND		
16	M39	LA33_N	37	LA32_P	B39	17
		GND	38	LA32_N	C39	17
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.3. FMC3 LPC MC / CC Connector

The FMC connector (J45/J69) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-3 FMC3 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	Y38	14
		GND	9	LA01_N_CC	Y37	14
15	U37	LA06_P	10	GND		
15	T37	LA06_N	11	LA05_P	U41	15
		GND	12	LA05_N	V40	15
		GND	13	GND		
14	Y35	LA10_P	14	LA09_P	AD33	14
14	Y34	LA10_N	15	LA09_N	AD32	14
		GND	16	GND		
		GND	17	LA13_P	AC33	14
15	R40	LA14_P	18	LA13_N	AB32	14
15	P40	LA14_N	19	GND		
		GND	20	LA17_P_CC	AB34	14
		GND	21	LA17_N_CC	AA34	14
14	V41	LA18_P_CC	22	GND		
14	W40	LA18_N_CC	23	LA23_P	AB41	14
		GND	24	LA23_N	AC40	14
		GND	25	GND		
14	AA40	LA27_P	26	LA26_P	W38	15
14	Y40	LA27_N	27	LA26_N	W37	15
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
15	V38	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AB42	14
15	U38	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AB37	14
		GND	5	CLK0_M2C_N	AA37	14
14	AC38	LA00_P_CC	6	GND		
14	AC39	LA00_N_CC	7	LA02_P	AB39	14
		GND	8	LA02_N	AB38	14
14	AA39	LA03_P	9	GND		
14	Y39	LA03_N	10	LA04_P	AD42	14
		GND	11	LA04_N	AC41	14
15	U42	LA08_P	12	GND		
15	T42	LA08_N	13	LA07_P	AA36	14
		GND	14	LA07_N	AA35	14
15	T40	LA12_P	15	GND		
15	T39	LA12_N	16	LA11_P	AC34	14
		GND	17	LA11_N	AC35	14
15	Y32	LA16_P	18	GND		
15	Y33	LA16_N	19	LA15_P	P41	15
		GND	20	LA15_N	P42	15
14	AA32	LA20_P	21	GND		
14	AB33	LA20_N	22	LA19_P	V35	15
		GND	23	LA19_N	V34	15
15	W32	LA22_P	24	GND		
15	W33	LA22_N	25	LA21_P	R37	15
		GND	26	LA21_N	T36	15
14	AA41	LA25_P	27	GND		
14	Y42	LA25_N	28	LA24_P	V36	15
		GND	29	LA24_N	U36	15
15	N41	LA29_P	30	GND		
15	N40	LA29_N	31	LA28_P	W41	14
		GND	32	LA28_N	W42	14
15	W35	LA31_P	33	GND		
15	W36	LA31_N	34	LA30_P	U34	15
		GND	35	LA30_N	V33	15
15	M42	LA33_P	36	GND		
15	M41	LA33_N	37	LA32_P	R39	15
		GND	38	LA32_N	R38	15
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.4. FMC4 LPC MC / CC Connector

The FMC connector (J46/J70) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-4 FMC4 Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AV40	12
		GND	9	LA01_N_CC	AW41	12
12	AW42	LA06_P	10	GND		
12	AV41	LA06_N	11	LA05_P	AT40	12
		GND	12	LA05_N	AR40	12
		GND	13	GND		
12	AT42	LA10_P	14	LA09_P	AR42	12
12	AU42	LA10_N	15	LA09_N	AP42	12
		GND	16	GND		
		GND	17	LA13_P	AP41	12
13	AJ40	LA14_P	18	LA13_N	AN40	12
13	AH40	LA14_N	19	GND		
		GND	20	LA17_P_CC	AG36	13
		GND	21	LA17_N_CC	AG37	13
13	AL42	LA18_P_CC	22	GND		
13	AK42	LA18_N_CC	23	LA23_P	AF34	13
		GND	24	LA23_N	AF35	13
		GND	25	GND		
13	AJ41	LA27_P	26	LA26_P	AE40	13
13	AJ42	LA27_N	27	LA26_N	AF40	13
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
12	AK37	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AU41	12
12	AJ36	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AF36	13
		GND	5	CLK0_M2C_N	AF37	13
12	AG32	LA00_P_CC	6	GND		
12	AG37	LA00_N_CC	7	LA02_P	AN39	12
		GND	8	LA02_N	AP40	12
12	AE33	LA03_P	9	GND		
12	AE32	LA03_N	10	LA04_P	AM39	12
		GND	11	LA04_N	AL39	12
12	AG34	LA08_P	12	GND		
12	AG33	LA08_N	13	LA07_P	AK35	12
		GND	14	LA07_N	AJ35	12
12	AH36	LA12_P	15	GND		
12	AH35	LA12_N	16	LA11_P	AK38	12
		GND	17	LA11_N	AJ37	12
13	AH38	LA16_P	18	GND		
13	AH39	LA16_N	19	LA15_P	AN41	12
		GND	20	LA15_N	AM41	12
13	AM42	LA20_P	21	GND		
13	AL41	LA20_N	22	LA19_P	AK39	12
		GND	23	LA19_N	AJ38	12
13	AE37	LA22_P	24	GND		
13	AE38	LA22_N	25	LA21_P	AG38	13
		GND	26	LA21_N	AG39	13
13	AH41	LA25_P	27	GND		
13	AG41	LA25_N	28	LA24_P	AG42	13
		GND	29	LA24_N	AF41	13
13	AF39	LA29_P	30	GND		
13	AE39	LA29_N	31	LA28_P	AD37	13
		GND	32	LA28_N	AD38	13
13	AF42	LA31_P	33	GND		
13	AE42	LA31_N	34	LA30_P	AD40	13
		GND	35	LA30_N	AD41	13
12	AH33	LA33_P	36	GND		
12	AH34	LA33_N	37	LA32_P	AD36	13
		GND	38	LA32_N	AD35	13
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.5. FMC5 LPC MC / CC Connector

The FMC connector (J47/J71) is interfaced to the FPGA over 36 pairs of signals pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-5 FMC5 Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AV30	22
		GND	9	LA01_N_CC	AW31	22
22	BB33	LA06_P	10	GND		
22	BB34	LA06_N	11	LA05_P	AP33	23
		GND	12	LA05_N	AN33	23
		GND	13	GND		
23	BA40	LA10_P	14	LA09_P	BB37	23
23	BB39	LA10_N	15	LA09_N	BB38	23
		GND	16	GND		
		GND	17	LA13_P	BA42	23
23	AY38	LA14_P	18	LA13_N	AY42	23
23	AW38	LA14_N	19	GND		
		GND	20	LA17_P_CC	BA41	23
		GND	21	LA17_N_CC	BB41	23
22	AY35	LA18_P_CC	22	GND		
22	AW35	LA18_N_CC	23	LA23_P	AV36	23
		GND	24	LA23_N	AW37	23
		GND	25	GND		
23	AT35	LA27_P	26	LA26_P	AR30	22
23	AR34	LA27_N	27	LA26_N	AT31	22
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
22	AW32	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AN28	22
22	AW33	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AU36	23
		GND	5	CLK0_M2C_N	AU37	23
23	AW36	LA00_P_CC	6	GND		
23	AV35	LA00_N_CC	7	LA02_P	AV33	22
		GND	8	LA02_N	AU32	22
22	AV34	LA03_P	9	GND		
22	AU34	LA03_N	10	LA04_P	BA34	22
		GND	11	LA04_N	BA35	22
23	BA39	LA08_P	12	GND		
23	AY39	LA08_N	13	LA07_P	BB36	23
		GND	14	LA07_N	BA36	23
23	AV38	LA12_P	15	GND		
23	AU38	LA12_N	16	LA11_P	AP31	22
		GND	17	LA11_N	AP30	22
23	AU39	LA16_P	18	GND		
23	AV39	LA16_N	19	LA15_P	AY40	23
		GND	20	LA15_N	AW40	23
22	AY33	LA20_P	21	GND		
22	AY34	LA20_N	22	LA19_P	AV31	22
		GND	23	LA19_N	AU31	22
22	AT30	LA22_P	24	GND		
22	AR29	LA22_N	25	LA21_P	AR28	22
		GND	26	LA21_N	AT29	22
22	AN30	LA25_P	27	GND		
22	AN31	LA25_N	28	LA24_P	AM29	22
		GND	29	LA24_N	AN29	22
23	AP32	LA29_P	30	GND		
23	AR32	LA29_N	31	LA28_P	AM31	23
		GND	32	LA28_N	AM32	23
22	AL27	LA31_P	33	GND		
22	AM28	LA31_N	34	LA30_P	AL26	22
		GND	35	LA30_N	AM27	22
22	AJ28	LA33_P	36	GND		
22	AK28	LA33_N	37	LA32_P	AK27	22
		GND	38	LA32_N	AJ27	22
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.6. FMC6 LPC MC / CC Connector

The FMC connector (J48/J72) is interfaced to the FPGA over 38 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. Also, LA33_P and LA33_N is not FPGA deferential signal pair pin. So, LA33_P/N cannot use for differential signal interface. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-6 FMC6 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	A31	27
		GND	9	LA01_N_CC	B31	27
27	H28	LA06_P	10	GND		
27	J27	LA06_N	11	LA05_P	B28	27
		GND	12	LA05_N	B29	27
		GND	13	GND		
27	D30	LA10_P	14	LA09_P	L25	27
27	E29	LA10_N	15	LA09_N	M24	27
		GND	16	GND		
		GND	17	LA13_P	G27	27
27	H26	LA14_P	18	LA13_N	G26	27
27	J26	LA14_N	19	GND		
		GND	20	LA17_P_CC	K23	28
		GND	21	LA17_N_CC	J23	28
28	D26	LA18_P_CC	22	GND		
28	D25	LA18_N_CC	23	LA23_P	A25	28
		GND	24	LA23_N	A24	28
		GND	25	GND		
28	E24	LA27_P	26	LA26_P	H24	28
28	E25	LA27_N	27	LA26_N	H25	28
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
28	F26	CLK1_M2C_P	2	*6 PRSNT_M2C_L	C31	27
28	F25	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	D28	27
		GND	5	CLK0_M2C_N	E28	27
27	D31	LA00_P_CC	6	GND		
27	E30	LA00_N_CC	7	LA02_P	G29	28
		GND	8	LA02_N	F29	28
27	A30	LA03_P	9	GND		
27	A29	LA03_N	10	LA04_P	P23	27
		GND	11	LA04_N	N24	27
27	N25	LA08_P	12	GND		
27	M26	LA08_N	13	LA07_P	C29	27
		GND	14	LA07_N	C28	27
27	G28	LA12_P	15	GND		
27	F27	LA12_N	16	LA11_P	L26	27
		GND	17	LA11_N	K27	27
28	E27	LA16_P	18	GND		
28	D27	LA16_N	19	LA15_P	K24	28
		GND	20	LA15_N	J25	28
28	A27	LA20_P	21	GND		
28	A26	LA20_N	22	LA19_P	G23	28
		GND	23	LA19_N	H23	28
28	F22	LA22_P	24	GND		
28	G22	LA22_N	25	LA21_P	C23	28
		GND	26	LA21_N	B23	28
27	M22	LA25_P	27	GND		
27	M21	LA25_N	28	LA24_P	B22	28
		GND	29	LA24_N	A22	28
28	B24	LA29_P	30	GND		
28	C24	LA29_N	31	LA28_P	E23	28
		GND	32	LA28_N	D23	28
28	G24	LA31_P	33	GND		
28	F24	LA31_N	34	LA30_P	N21	27
		GND	35	LA30_N	P22	27
28	B27	LA33_P	36	GND		
28	L24	LA33_N	37	LA32_P	E22	28
		GND	38	LA32_N	D22	28
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.7. FMC7 LPC MC / CC Connector

The FMC connector (J49/J73) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. Also, LA33_P and LA33_N is not FPGA deferential signal pair pin. So, LA33_P/N cannot use for differential signal interface. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-7 FMC7 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	F20	38
		GND	9	LA01_N_CC	E19	38
38	B21	LA06_P	10	GND		
38	A21	LA06_N	11	LA05_P	A19	38
		GND	12	LA05_N	A20	38
		GND	13	GND		
38	K22	LA10_P	14	LA09_P	C16	37
38	L22	LA10_N	15	LA09_N	D16	37
		GND	16	GND		
		GND	17	LA13_P	G21	38
38	K20	LA14_P	18	LA13_N	H21	38
38	J20	LA14_N	19	GND		
		GND	20	LA17_P_CC	A14	37
		GND	21	LA17_N_CC	A15	37
37	H18	LA18_P_CC	22	GND		
37	G17	LA18_N_CC	23	LA23_P	C15	37
		GND	24	LA23_N	D15	37
		GND	25	GND		
37	F15	LA27_P	26	LA26_P	K19	28
37	F14	LA27_N	27	LA26_N	L19	37
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
37	G16	CLK1_M2C_P	2	*6 PRSNT_M2C_L	B18	38
37	F16	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	D17	38
		GND	5	CLK0_M2C_N	D18	38
38	D21	LA00_P_CC	6	GND		
38	C21	LA00_N_CC	7	LA02_P	C20	38
		GND	8	LA02_N	D20	38
38	F19	LA03_P	9	GND		
38	E18	LA03_N	10	LA04_P	A16	38
		GND	11	LA04_N	A17	38
38	F21	LA08_P	12	GND		
38	E20	LA08_N	13	LA07_P	C18	38
		GND	14	LA07_N	C19	38
38	B16	LA12_P	15	GND		
38	B17	LA12_N	16	LA11_P	E17	38
		GND	17	LA11_N	F17	38
38	G19	LA16_P	18	GND		
38	H20	LA16_N	19	LA15_P	J22	38
		GND	20	LA15_N	J21	38
37	B13	LA20_P	21	GND		
37	B14	LA20_N	22	LA19_P	H15	37
		GND	23	LA19_N	H16	37
37	K17	LA22_P	24	GND		
37	J17	LA22_N	25	LA21_P	K18	37
		GND	26	LA21_N	J18	37
38	L21	LA25_P	27	GND		
38	L20	LA25_N	28	LA24_P	M18	37
		GND	29	LA24_N	M19	37
37	P17	LA29_P	30	GND		
37	N18	LA29_N	31	LA28_P	E14	37
		GND	32	LA28_N	E15	37
37	R17	LA31_P	33	GND		
37	P18	LA31_N	34	LA30_P	P21	37
		GND	35	LA30_N	N20	37
37	M17	LA33_P	36	GND		
37	P20	LA33_N	37	LA32_P	D13	37
		GND	38	LA32_N	E13	37
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.8. FMC8 LPC MC / CC Connector

The FMC connector (J50/J74) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 1 pair is assigned to the GCLK pins and 1 pair is assigned to the MRCC pin of FPGA. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-8 FMC8 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	E9	36
		GND	9	LA01_N_CC	E10	36
36	E8	LA06_P	10	GND		
36	D8	LA06_N	11	LA05_P	C6	36
		GND	12	LA05_N	B6	36
		GND	13	GND		
36	B12	LA10_P	14	LA09_P	F10	35
36	B11	LA10_N	15	LA09_N	F9	35
		GND	16	GND		
		GND	17	LA13_P	D10	36
36	G11	LA14_P	18	LA13_N	D11	36
36	G12	LA14_N	19	GND		
		GND	20	LA17_P_CC	G6	35
		GND	21	LA17_N_CC	F6	35
35	J8	LA18_P_CC	22	GND		
35	H8	LA18_N_CC	23	LA23_P	H11	35
		GND	24	LA23_N	H10	35
		GND	25	GND		
35	J10	LA27_P	26	LA26_P	N14	35
35	J11	LA27_N	27	LA26_N	N15	35
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
35	K8	CLK1_M2C_P	2	*6 PRSNT_M2C_L	M13	35
35	J7	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	J15	36
		GND	5	CLK0_M2C_N	J16	36
36	A11	LA00_P_CC	6	GND		
36	A12	LA00_N_CC	7	LA02_P	E12	36
		GND	8	LA02_N	D12	36
36	B7	LA03_P	9	GND		
36	A7	LA03_N	10	LA04_P	D6	35
		GND	11	LA04_N	D7	35
36	A9	LA08_P	12	GND		
36	A10	LA08_N	13	LA07_P	B8	36
		GND	14	LA07_N	B9	36
36	C11	LA12_P	15	GND		
36	C10	LA12_N	16	LA11_P	F7	35
		GND	17	LA11_N	E7	35
36	G13	LA16_P	18	GND		
36	H13	LA16_N	19	LA15_P	F11	36
		GND	20	LA15_N	F12	36
35	H9	LA20_P	21	GND		
35	G9	LA20_N	22	LA19_P	G7	35
		GND	23	LA19_N	G8	35
35	K10	LA22_P	24	GND		
35	L11	LA22_N	25	LA21_P	M16	35
		GND	26	LA21_N	L15	35
35	L10	LA25_P	27	GND		
35	K9	LA25_N	28	LA24_P	M16	35
		GND	29	LA24_N	L15	35
35	K13	LA29_P	30	GND		
35	J12	LA29_N	31	LA28_P	N16	35
		GND	32	LA28_N	P16	35
35	R15	LA31_P	33	GND		
35	P15	LA31_N	34	LA30_P	J13	36
		GND	35	LA30_N	K14	36
35	H14	LA33_P	36	GND		
35	G14	LA33_N	37	LA32_P	L16	36
		GND	38	LA32_N	K15	36
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.9. FMC9 LPC MC / CC Connector

The FMC connector (J51/J75) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. The following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-9 FMC9 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	N1	45
		GND	9	LA01_N_CC	M1	45
44	Y3	LA06_P	10	GND		
44	Y2	LA06_N	11	LA05_P	T6	45
		GND	12	LA05_N	T7	45
		GND	13	GND		
45	U11	LA10_P	14	LA09_P	W8	45
45	V11	LA10_N	15	LA09_N	W7	45
		GND	16	GND		
		GND	17	LA13_P	V1	45
45	V8	LA14_P	18	LA13_N	U1	45
45	U7	LA14_N	19	GND		
		GND	20	LA17_P_CC	Y5	44
		GND	21	LA17_N_CC	Y4	44
44	AA1	LA18_P_CC	22	GND		
44	AA2	LA18_N_CC	23	LA23_P	Y7	44
		GND	24	LA23_N	Y8	44
		GND	25	GND		
44	AC3	LA27_P	26	LA26_P	AB1	44
44	AB3	LA27_N	27	LA26_N	AB2	44
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
44	AC4	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AD3	44
44	AB4	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	V5	45
		GND	5	CLK0_M2C_N	V6	45
45	R4	LA00_P_CC	6	GND		
45	R5	LA00_N_CC	7	LA02_P	U6	45
		GND	8	LA02_N	T5	45
45	T1	LA03_P	9	GND		
45	T2	LA03_N	10	LA04_P	W6	45
		GND	11	LA04_N	W5	45
44	AA6	LA08_P	12	GND		
44	AA7	LA08_N	13	LA07_P	P2	45
		GND	14	LA07_N	P4	45
45	P1	LA12_P	15	GND		
45	E2	LA12_N	16	LA11_P	R3	45
		GND	17	LA11_N	T4	45
44	AB7	LA16_P	18	GND		
44	AB6	LA16_N	19	LA15_P	W3	45
		GND	20	LA15_N	V3	45
44	W1	LA20_P	21	GND		
44	W2	LA20_N	22	LA19_P	AA4	44
		GND	23	LA19_N	AA5	44
44	AA9	LA22_P	24	GND		
44	Y9	LA22_N	25	LA21_P	U8	45
		GND	26	LA21_N	U9	45
44	AB9	LA25_P	27	GND		
44	AB8	LA25_N	28	LA24_P	AC9	44
		GND	29	LA24_N	AC8	44
44	AD1	LA29_P	30	GND		
44	AC1	LA29_N	31	LA28_P	AE3	44
		GND	32	LA28_N	AE2	44
44	Y10	LA31_P	33	GND		
44	AA11	LA31_N	34	LA30_P	V9	45
		GND	35	LA30_N	V10	45
45	W11	LA33_P	36	GND		
45	W10	LA33_N	37	LA32_P	AA10	44
		GND	38	LA32_N	AB11	44
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

8.3.10. FMC10 LPC MC / CC Connector

The FMC connector (J52/J76) is interfaced to the FPGA over 36 pairs of signal pins. Of them, 2 pairs are assigned to the MRCC pins of the FPGA. Following table shows the pin mapping assignments between the FMC connector and the FPGA.

Table8-10 FMC10 Connector Pinouts on Component and Solder Sides

Bank No.	Pin No.	C		D	PinNo.	Bank No.
		GND	1	*4 PG_C2M		
		DP0_C2M_P	2	GND		
		DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P		
		GND	5	GBTCLK0_M2C_N		
		DP0_M2C_P	6	GND		
		DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AE7	43
		GND	9	LA01_N_CC	AD7	43
43	AD8	LA06_P	10	GND		
43	AE8	LA06_N	11	LA05_P	AH1	43
		GND	12	LA05_N	AJ1	43
		GND	13	GND		
42	AL1	LA10_P	14	LA09_P	AJ8	42
42	AK2	LA10_N	15	LA09_N	AK7	42
		GND	16	GND		
		GND	17	LA13_P	AP1	42
42	AL4	LA14_P	18	LA13_N	AN1	42
42	AK4	LA14_N	19	GND		
		GND	20	LA17_P_CC	AM6	42
		GND	21	LA17_N_CC	AL6	42
42	AN4	LA18_P_CC	22	GND		
42	AN5	LA18_N_CC	23	LA23_P	AM1	42
		GND	24	LA23_N	AM2	42
		GND	25	GND		
42	AM4	LA27_P	26	LA26_P	AU3	42
42	AM3	LA27_N	27	LA26_N	AU2	42
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	*7 3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		*7 12P0V	35	*2 GA1		
		GND	36	*7 3P3V		
		*7 12P0V	37	GND		
		GND	38	*7 3P3V		
		*7 3P3V	39	GND		
		GND	40	*7 3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*5 VREF_A_M2C		
42	AL5	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AH10	42
42	AK5	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AH4	43
		GND	5	CLK0_M2C_N	AG4	43
43	AD6	LA00_P_CC	6	GND		
43	AD5	LA00_N_CC	7	LA02_P	AG1	43
		GND	8	LA02_N	AF1	43
43	AG2	LA03_P	9	GND		
43	AF2	LA03_N	10	LA04_P	AF5	43
		GND	11	LA04_N	AE5	43
42	AH8	LA08_P	12	GND		
42	AJ7	LA08_N	13	LA07_P	AJ6	42
		GND	14	LA07_N	AJ5	42
43	AF7	LA12_P	15	GND		
43	AF6	LA12_N	16	LA11_P	AG7	43
		GND	17	LA11_N	AG6	43
42	AL2	LA16_P	18	GND		
42	AK3	LA16_N	19	LA15_P	AH6	42
		GND	20	LA15_N	AH5	42
42	AR2	LA20_P	21	GND		
42	AP2	LA20_N	22	LA19_P	AG9	42
		GND	23	LA19_N	AG8	42
42	AR4	LA22_P	24	GND		
42	AR3	LA22_N	25	LA21_P	AF10	43
		GND	26	LA21_N	AF9	43
43	AJ3	LA25_P	27	GND		
43	AJ2	LA25_N	28	LA24_P	AP3	42
		GND	29	LA24_N	AN3	42
43	AD10	LA29_P	30	GND		
43	AD11	LA29_N	31	LA28_P	AE10	43
		GND	32	LA28_N	AE9	43
42	AV1	LA31_P	33	GND		
42	AU1	LA31_N	34	LA30_P	AC10	43
		GND	35	LA30_N	AC11	43
43	AF12	LA33_P	36	GND		
43	AF11	LA33_N	37	LA32_P	AG12	43
		GND	38	LA32_N	AG11	43
		*7 VADJ	39	GND		
		GND	40	*7 VADJ		

*1 SCL/SDA

This has a test pad to perform the I2C communication with the FMC mezzanine card.

*2 GA[1:0]

This has a test pad to perform the ID notification function to the FMC mezzanine card.

*3 TDI/TDO/TCK/TMS/TRST_L

These have an onboard loopback function to enable JTAG communication from the FMC mezzanine card. (TCK, TMS and TRST_L are for test points only). By default the loopback connection is not enabled since a 0-ohm resistor is not mounted.

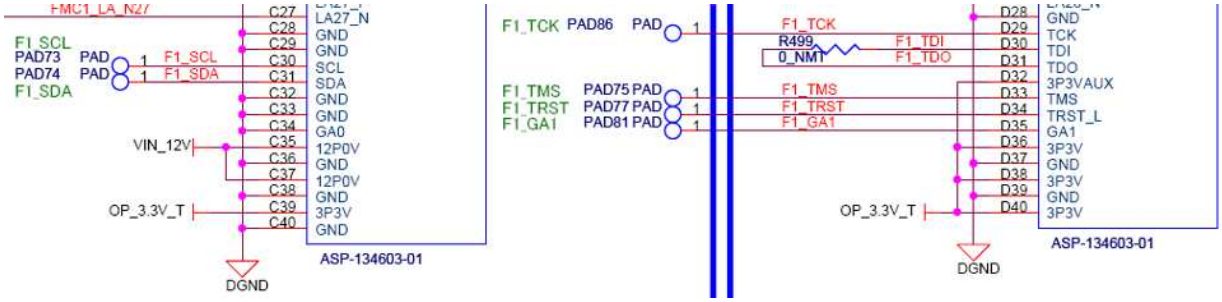

Figure8-4 SDA,SCL,GA1/0 TDI/TDO Circuit

*4 PG_C2M,

This has a test point and a pull-up function to enable level output to the FMC mezzanine card.

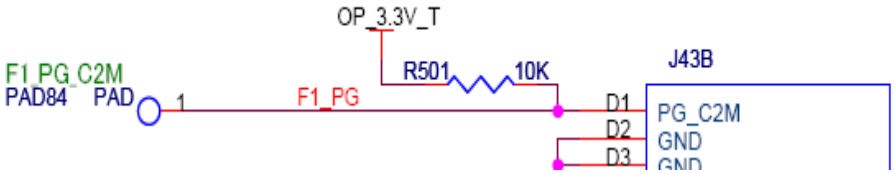

Figure8-5 PG_C2M Circuit

*5 VREF_A_M2C

This has a test pad to monitor the “H1” pin of each FMC3,4,5,8,9 and 10 connector.

Figure8-6 VREF_A_M2C Circuit

This connects the “H1” pin of the FMC1 and 2 connectors to the FMC_VREFA and the “H1” pin of the FMC6 and 7 connectors to the FMC_VREFB.
The following VREF circuit is enabled with J23 and J24 settings.
FMC_VREFA/B > V6_OPVREF_A/B
FP_OP_A/B > V6_OPVREF_A/B
FP_OP_A/B > FMC_VREFA/B,V6_OPVREF_A/B

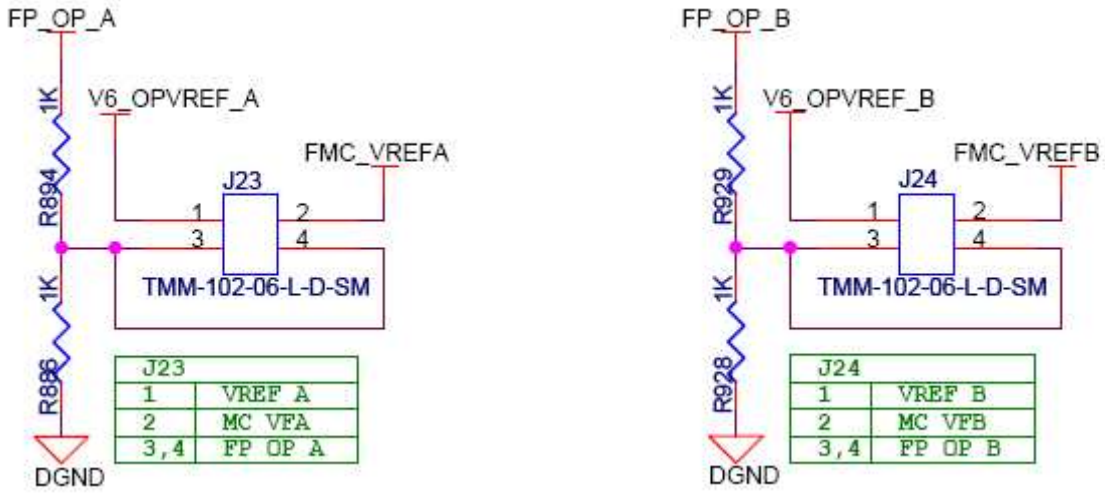

Figure8-7 FMC_VREF Select Circuit

*6 PRSNT_M2C_L
This connects the “H2” pin of the FMC connector to the FPGA.

*7 Power Supply
The board provides 12V to the 12P0V pin and 3.3V to the 3P3V and 3P3VAUX pins. The following circuit also allows the selection of 5V, 3.3V and 2.5V for the VADJ pins including E39, F40, G39 and H40. The voltage can be supplied by short-circuiting one of the jumpers JP7-16 and JP27-36 respectively. The supply voltage can be monitored with a neighboring LED.
Caution:
Do not short-circuit two or more positions of each JP7-16 and JP27-36.
Short-circuit the same position of each JP7-16 and JP27-36.

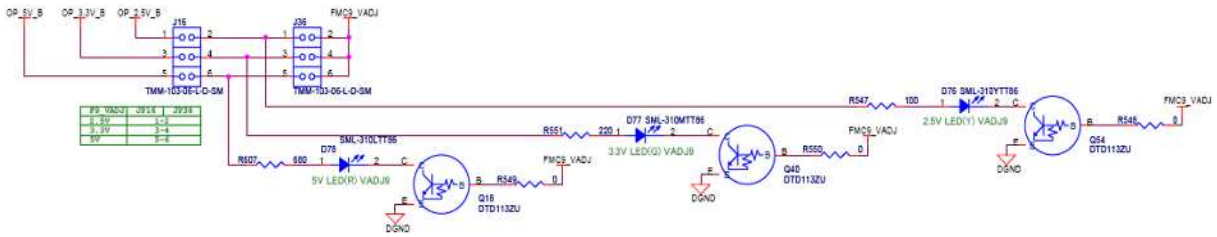

Figure8-8 VADJ Circuit

9. Clock System Diagram

The following figure shows the clock system diagram of the TB-6V-LX760-LSI board.

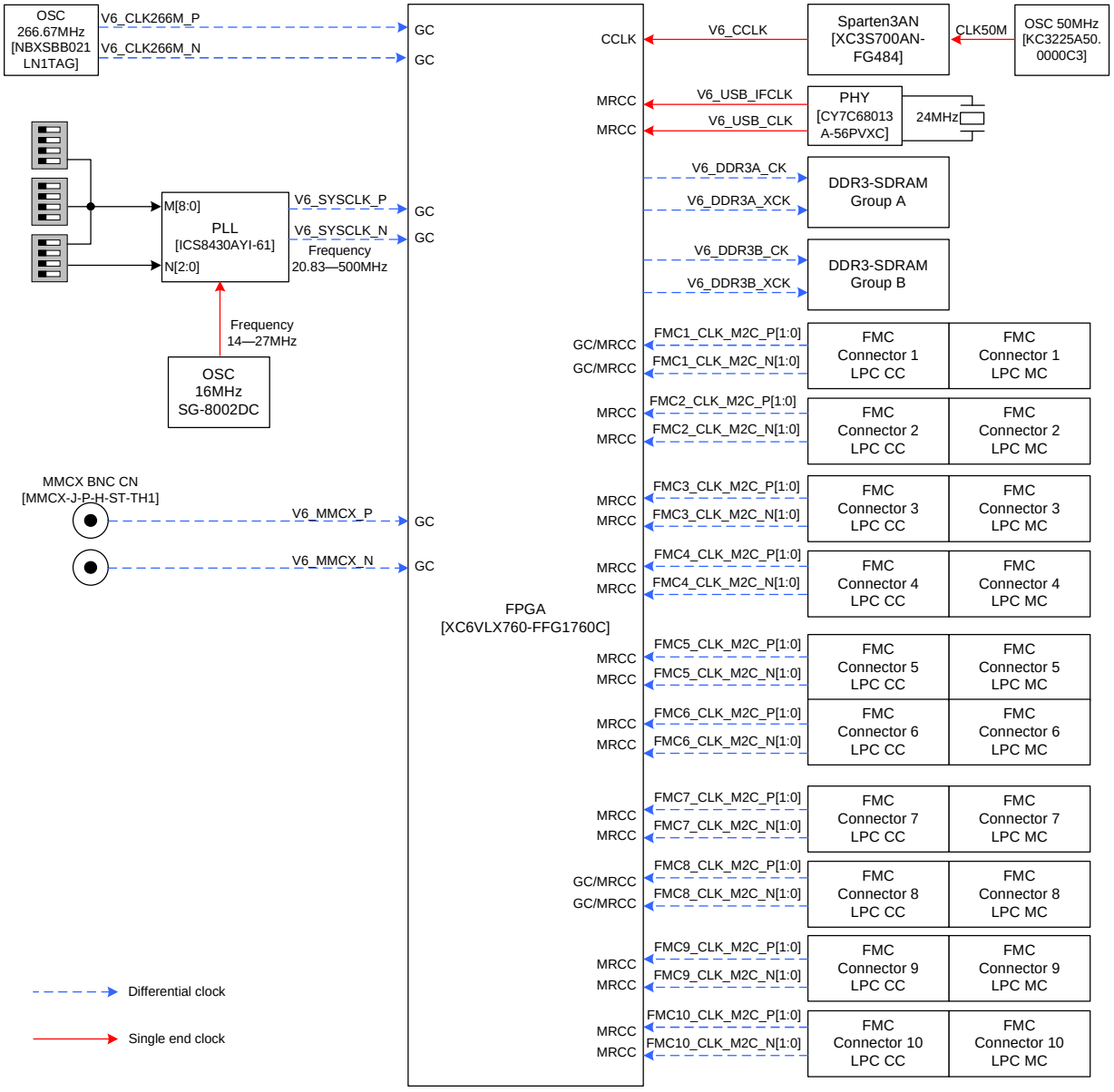

Figure9-1 Clock System Diagram

9.1. PLL Setting

The output clock frequency of an onboard PLL can be calculated using the following formula.
Fout is the output clock frequency in the range of 20.83MHz-500MHz, and
Fxtal is the input clock frequency in the range of 14MHz-27MHz.

$$Fout = \frac{Fvco}{N} = \frac{Fxtal}{16} x \frac{M}{N}$$

Fvco = (Fxtal / 16) x M must be set within the range of 250-500MHz.
Fout = (Fxtal / 16) x M / N

In case of outputting 125MHz:
Condition: Fxtal input clock: 16MHz
M[8:0]=0,1,1,1,1,1,0,1,0 (x 250)
N[2:0]=0,1,0 (divide-by-2)

The following table shows the mapping table between M value and DIP SW.

Table9-1 PLL's M Divide Setting Table

VCO Frequency (MHz)	M Divide	SW19-1	SW18-4	SW18-3	SW18-2	SW18-1	SW17-4	SW17-3	SW17-2	SW17-1
		256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	250	0	1	1	1	1	1	0	1	0
251	251	0	1	1	1	1	1	0	1	1
252	252	0	1	1	1	1	1	1	0	0
253	253	0	1	1	1	1	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
498	498	1	1	1	1	1	0	0	1	0
499	499	1	1	1	1	1	0	0	1	1
500	500	1	1	1	1	1	0	1	0	0

The following table shows the function corresponding to the N value.

Table9-2 PLL's N Divide Setting Table

Inputs			N Divider Value	Output Frequency(MHz)	
SW19-4	SW19-3	SW19-2		Minimum	Maximum
N2	N1	N0			
0	0	0	1	250	500
0	0	1	1.5	166.66	333.33
0	1	0	2	125	250
0	1	1	3	83.33	166.66
1	0	0	4	62.5	125
1	0	1	6	41.66	83.33
1	1	0	8	31.25	62.5
1	1	1	12	20.83	41.66

10. Power Supply System

10.1. Power Consumption Estimation

The following is the power consumption estimation of the main components:

XC6VLX760-2FFG1760C		
Vccint 1.0V	29.5W	
Vccaux 2.5V	7.5W	
Vcco2.5 2.5V	10.5W	
Vcco1.5 1.5V	2.5W	
XC3S700AN-4FGG484C		
Vccint 1.2V	0.6W	
Vccaux 3.3V	0.66W	
Vcco2.5 2.5V	0.75W	
DDR3 (Micron 1-Gbit x 4)		
VDD 1.5V	4W	
Vtt 0.75V	1W	(Note 0.75V / 50ohm x 60pin=1A)
SPI Flash (Numonyx M25P64 x 1)		
VDD 3.3V	0.5W	
USB (Cypress CY7C68013A x 1)		
VDD, VDDQ 3.3V	0.5W	
Option I/O x20 to FMC		
2.5V	20W	
3.3V	26.4W	
5.0V	20W	
12V	24W	

The following is the current value to the power consumption of the main components:

Vccint/Vccaux/Vcco:

1.0V 29.5W = 29.5A
1.2V 0.6W = 0.50A
2.5V 18.8W = 7.52A
3.3V 2.5W = 0.75A
1.5V 6.5W = 4.33A
0.75V 1.0W = 1.33A

Option Power

2.5V 20.0W = 3.20A
3.3V 26.4W = 3.55A
5.0V 20.0W = 7.22A
12V 24W = 2A

The board is designed assuming that the power consumption and the current value for 12V input power is 149.30W and 12.44A respectively.

10.2. Power Supply System Diagram

Power Supply: ATX12V

Power Supply Connector: Molex 39-29-1048 or 39-30-0060 connector

The following figure shows the power supply system diagram.

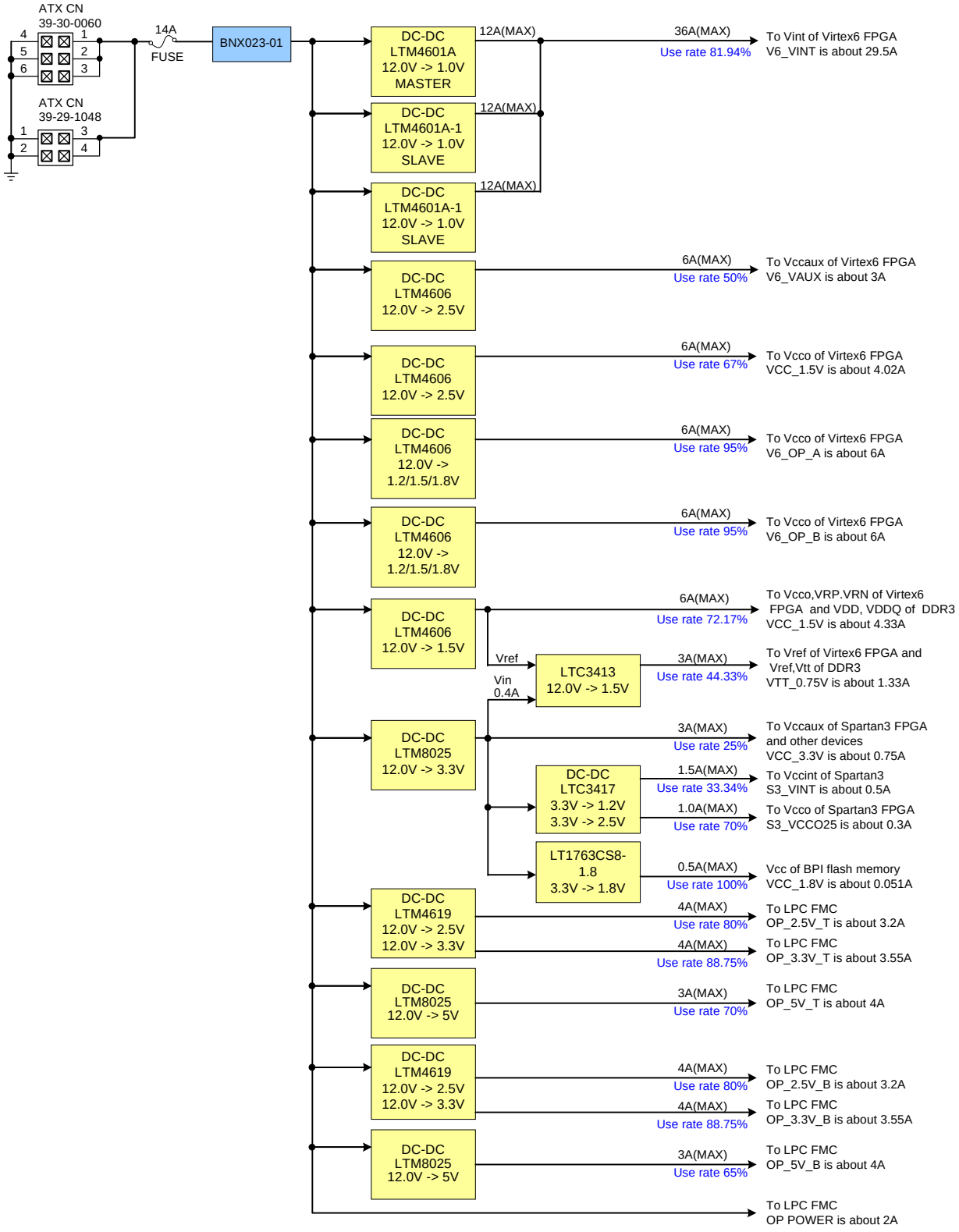

Figure10-1 Power Supply System Diagram

10.3. Power Supply Monitor

The board has a Linear Technology's LTC2978CUP to monitor the onboard power sources such as Core voltage, AUX voltage and VCCO (2.5V/1.5V) that use Virtex-6. The monitor information can be displayed on your PC through the onboard CN29 connector and the Linear Technology's USB conversion board. You can set various parameters for monitoring using dedicated application software. The following figure shows the connection diagram.

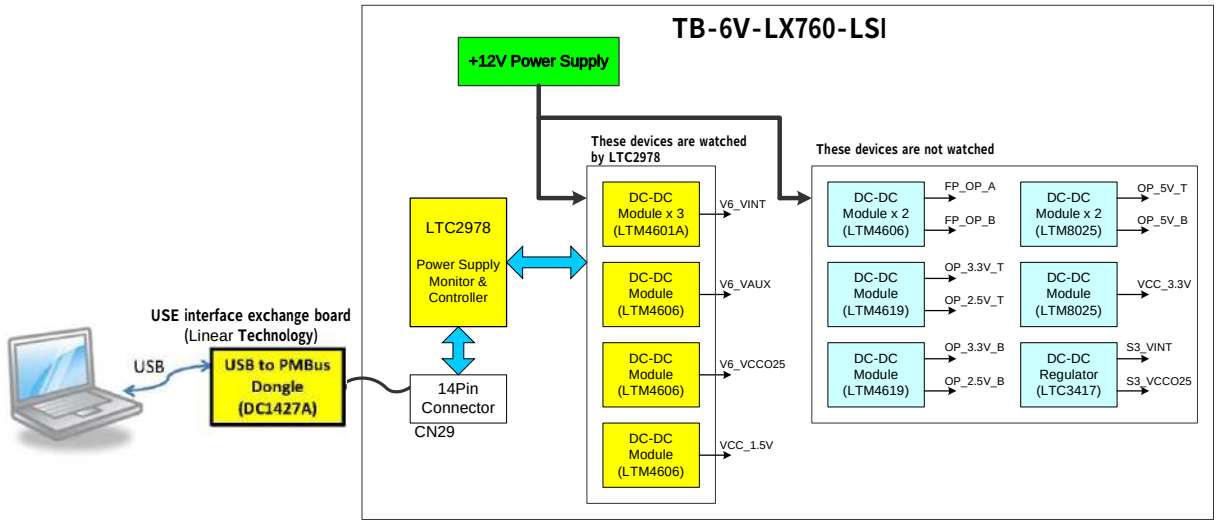

Figure10-2 Power Supply Monitor

For more information, please contact Linear Technology.

10.4. Power Supply Arrangement for FPGA Banks

Figure 6-3 shows the arrangement of the power supplies for Virtex-V6 FPGA Banks that are mounted on the TB-6V-LX760-LSI board.

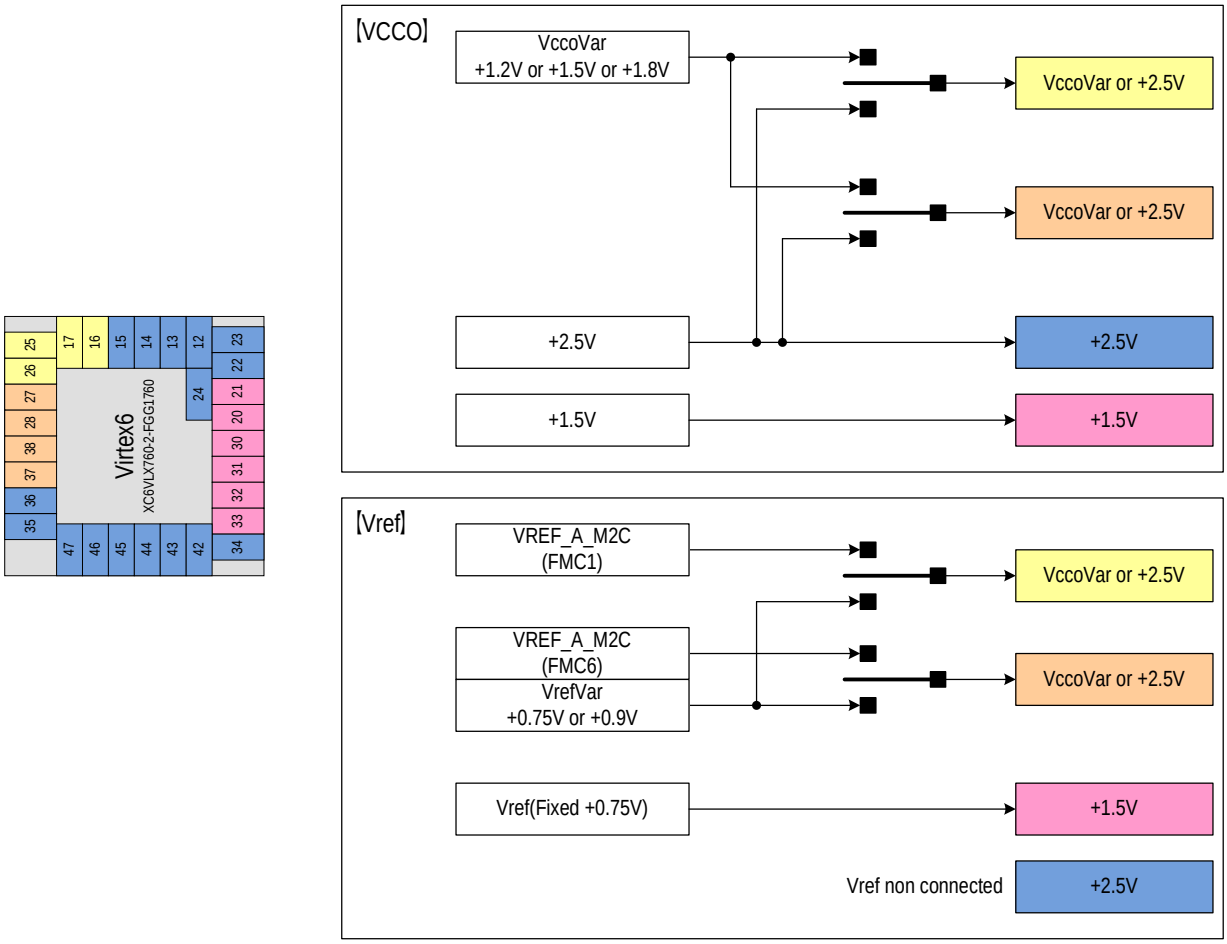

Figure10-3 Power Supply Arrangement for FPGA Banks

10.5. Power Supply for Fan

FAN Pin Header: MOLEX's 5045-03A-50PS (mounted)

FAN Specification (draft): Rotation speed 3800/min, rated current 0.11A and rated voltage +12V

The following figure shows the FAN pin header connection.

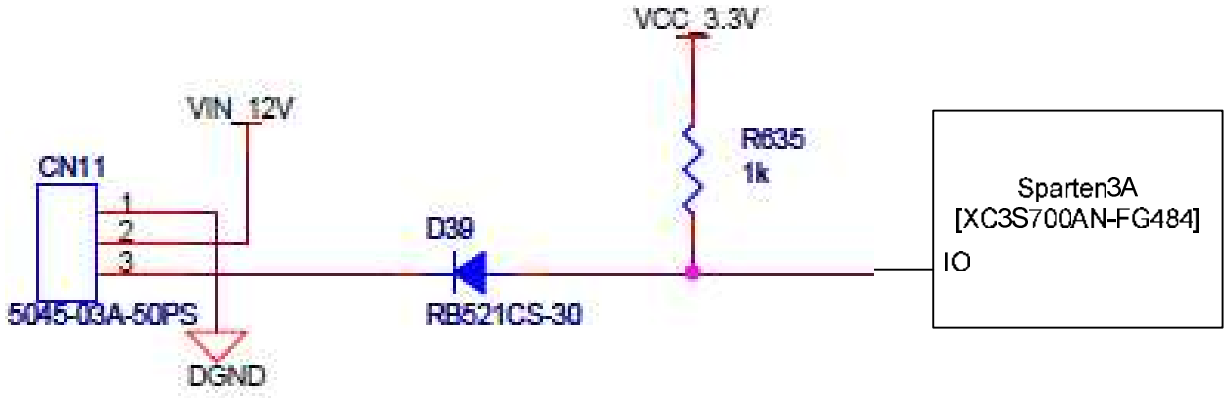

Figure10-4 Fan Connector Peripheral Circuit

11. LED/SW/JUMPER

11.1. LED

The following table describes the function of the onboard LEDs.

Table11-1 LED Functions

LED Name	Function	Remarks
D1 (Green)	Lights when +12V input power is ON.	1
D103(Green)	Lights when Virtex6_VINT (+1.0V) is OK.	1
D104(Green)	Lights when Virtex6_VAUX (+2.5V) is OK.	1
D106(Green)	Lights when Virtex6_VCCO25 (+2.5V) is OK.	1
D105(Green)	Lights when VCC_1.5V (+1.5V) is OK.	1
D109(Green)	Lights when VCC_3.3V (+3.3V) is OK.	1
D107(Green)	Lights when Spartan3_VINT (+1.2V) and S3_VCCO25 (+2.5V) is OK.	1
D108(Green)	Lights when VTT_0.75V(+0.75V) is OK.	1
D113(Green)	Lights when OP_3.3V_T (+3.3V) and OP_2.5V_T (+2.5V) is OK.	1
D112(Green)	Lights when OP_3.3V_B (+3.3V) and OP_2.5V_B (+2.5V) is OK.	1
D110(Green)	Lights when FP_OP_A (+1.2V/+1.5V/+1.8V) is OK.	1
D111(Green)	Lights when FP_OP_B (+1.2V/+1.5V/+1.8V) is OK.	1
D115(Green)	Lights when OP_5V_T (+5V) is OK.	1
D114(Green)	Lights when OP_5V_B (+5V) is OK.	1
D3 (Red)	Lights when Power Monitor is in an Alert state.	1
D34(Green)	Lights when Power (Monitor) is OK.	1
D32 (Green)	Lights when Sparten3 Config is completed.	1
D33 (Green)	Lights when Virtex6 Config is completed.	1
5V_VADJ1-10(Red)	Lights when FMC VADJ is 5V.	10
3.3V_VADJ1-10 (Green)	Lights when FMC VADJ is 3.3V.	10
2.5V_VADJ1-10 (Yellow)	Lights when FMC VADJ is 2.5V.	10
D[31:29] (Red)	Connects to Spartan3 for test.	3
D[60:57] (Green) D[98:91] (Green) D[102:101] (Green)	Connects to Virtex6 for test.	14
D[100:99] (Red)	Connects to Virtex6 for test.	2

11.2. Switch

The following table shows the destination of the onboard switch to be connected and its function.

Table11-2 Switch Functions

Switch Name	Function	DIP_SW Pin Order	Destination	Destination Pin Function
SW7	Slide Switch for Configuration	1	V6 FPGA/ SP3AN FPGA	V6_M0
		2		V6_M1
		3		V6_M2
		4	V6 FPGA	V6_PROG_B
SW5	Rotary Switch for Test	8-4-2-1	SP3AN FPGA	MODE[3:0]
SW6	Rotary Switch for Test	8-4-2-1	SP3AN FPGA	AREA[3:0]
SW8	Slide Switch for Test	[4:1]	V6 FPGA	V6_DIPSW[3:0]
SW14	Slide Switch for Test	[4:1]	V6 FPGA	V6_DIPSW[7:4]
SW15	Slide Switch for Test	[4:1]	V6 FPGA	V6_DIPSW[11:8]
SW16	Slide Switch for Test	[4:1]	V6 FPGA	V6_DIPSW[15:12]
SW9	Push Switch for Test	-	V6 FPGA	V6_PUSHSW0
SW10	Push Switch for Test	-	V6 FPGA	V6_PUSHSW1
SW11	Push Switch for Test	-	V6 FPGA	V6_PUSHSW2
SW13	Push Switch for Test	-	V6 FPGA	V6_PUSHSW3
SW17	Slide Switch for PLL Setting	[4:1]	ICS8430AYI	M[3:0]
SW18	Slide Switch for PLL Setting	[4:1]	ICS8430AYI	M[7:4]
SW19	Slide Switch for PLL Setting	[4:1]	ICS8430AYI	N[2:0], M8

11.3. JUMPER

The following figure shows the onboard jumper functions.

Table11-3 Jumper Functions

Jumper Name	Function	Remarks
J41, J42	NC/pull-up/pull-down setting for Monitor ASEL[1:0] pin	1: Pull-up 2: ASEL0/1 3: Pull-down
J54	VCCO_A power supply selection for Virtex-6 FPGA	1,2: FP_OP_A 3,4: V6_VCCO_A 5,6: 2.5V
J55	VCCO_B power supply selection for Virtex-6 FPGA	1,2: FP_OP_B 3,4: V6_VCCO_B 5,6: 2.5V
J23	V6_OPVREF_A power supply selection for Virtex-6 FPGA	1: V6_OPVREF_A 2: FMC_VREFA 3,4: FP_OP_A
J24	V6_OPVREF_B power supply selection for Virtex-6 FPGA	1: V6_OPVREF_B 2: FMC_VREFB 3,4: FP_OP_B
J12, J32	VADJ power supply selection for FMC1 LPC CC/MC	1: 2.5V 3: 3.3V 5: 5V 2,4,6: VADJ
J11, J31	VADJ power supply selection for FMC2 LPC CC/MC	
J14, J34	VADJ power supply selection for FMC3 LPC CC/MC	
J13, J33	VADJ power supply selection for FMC4 LPC CC/MC	
J7, J27	VADJ power supply selection for FMC5 LPC CC/MC	
J8, J28	VADJ power supply selection for FMC6 LPC CC/MC	
J10, J30	VADJ power supply selection for FMC7 LPC CC/MC	
J9, J29	VADJ power supply selection for FMC8 LPC CC/MC	
J16, J36	VADJ power supply selection for FMC9 LPC CC/MC	
J15, J35	VADJ power supply selection for FMC10 LPC CC/MC	

11.4. Pin Header

This pin header is used for general purpose. The connector is HIROSE A1-34PA-2.54DSA.

Table11-4 Pin assign of Pin header

Pin Number	Pin Name	Pin Number	Pin Name
1	+2.5V	2	+2.5V
3	V6_TP0	4	V6_TP15
5	V6_TP1	6	V6_TP16
7	V6_TP2	8	V6_TP17
9	V6_TP3	10	V6_TP18
11	V6_TP4	12	V6_TP19
13	V6_TP5	14	V6_TP20
15	V6_TP6	16	V6_TP21
17	V6_TP7	18	V6_TP22
19	V6_TP8	20	V6_TP23
21	V6_TP9	22	V6_TP24
23	V6_TP10	24	V6_TP25
25	V6_TP11	26	V6_TP26
27	V6_TP12	28	V6_TP27
29	V6_TP13	30	V6_TP28
31	V6_TP14	32	V6_TP29
33	GND	34	GND

12. Initial Settings

The following figure shows the Initial switch settings.
Look at the switches surrounded by a blue box.

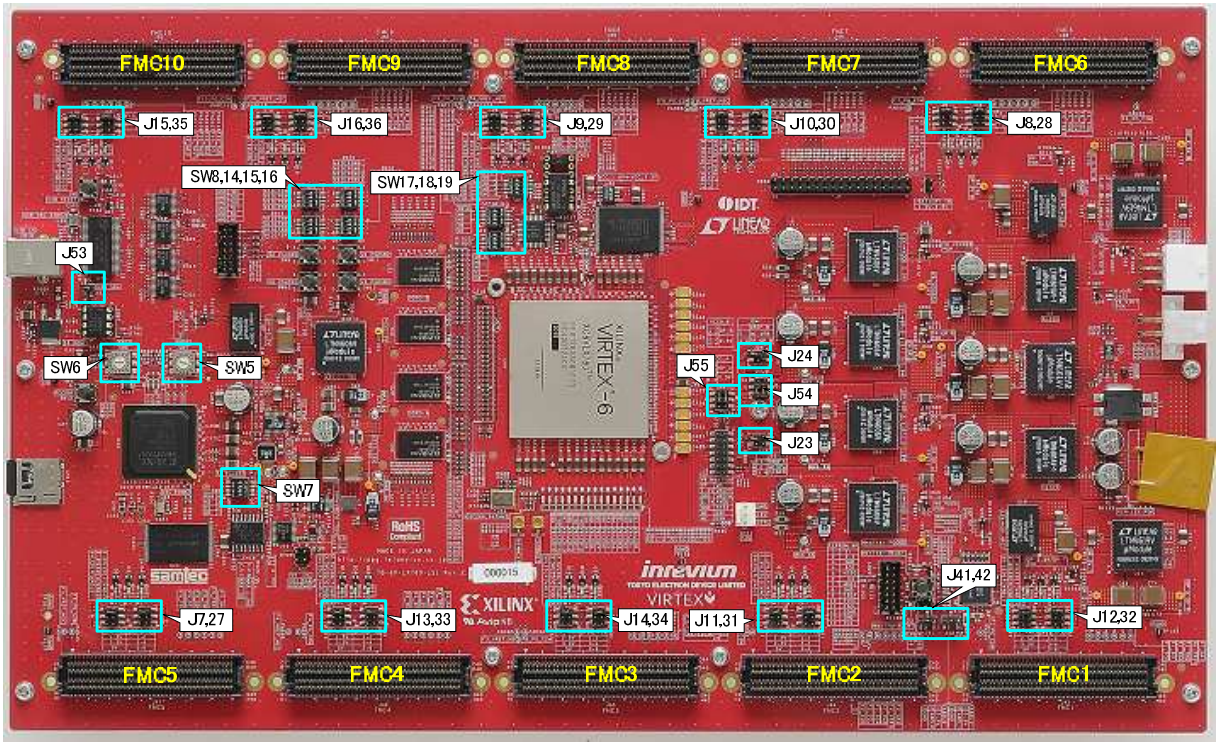

Figure12-1 Default Settings (component side)

The following table shows the initial settings.

Table12-1 Initial Settings

No.	Silk No.	Default Setting	Function
1	J41, J42	2-3	Address setting for voltage monitoring
2	J53	SHORT	Use for rewriting to EEPROM of USB-Chip
3	J54	3-5; 4-6	VCCO setting for Virtex6 Bank16/17/25/26 (**2.5V** / FP_OP_A / None)
4	J55	3-5; 4-6	VCCO setting for Virtex6 Bank27/28/37/38 (**2.5V** / FP_OP_B / None)
5	J23	OPEN	VREF setting for Virtex6 Bank16/17/25/26 (1.8V / FMC_VREFA / **None**)
6	J24	OPEN	VREF setting for Virtex6 Bank27/28/37/38 (1.8V / FMC_VREFB / **None**)
7	J12, J32	1-2	VADJ setting for FMC1 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
8	J11, J31	1-2	VADJ setting for FMC2 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
9	J14, J34	1-2	VADJ setting for FMC3 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
10	J13, J33	1-2	VADJ setting for FMC4 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
11	J7, J27	1-2	VADJ setting for FMC5 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
12	J8, J28	1-2	VADJ setting for FMC6 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
13	J10, J30	1-2	VADJ setting for FMC7 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
14	J9, J29	1-2	VADJ setting for FMC8 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
15	J16, J36	1-2	VADJ setting for FMC9 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
16	J15, J35	1-2	VADJ setting for FMC10 LPC CC/MC (**2.5V** / 3.3V / 5V / None)
17	SW7	All Off	FPGA Configuration Slave Select Map Mode setting FAN Alarm OFF
18	SW5	1	User Rotary Switch
19	SW6	0	User Rotary Switch
20	SW8,14.15.16	OFF	User Slide Switch
21	SW17,18,19	OFF	PLL Slide Switch

*The bold, red characters in the Function field indicate a default setting.

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