User Manual

November 1999

Version 3.2

FME/MS/SFDAC1/UM_1/4190

DK86060-3

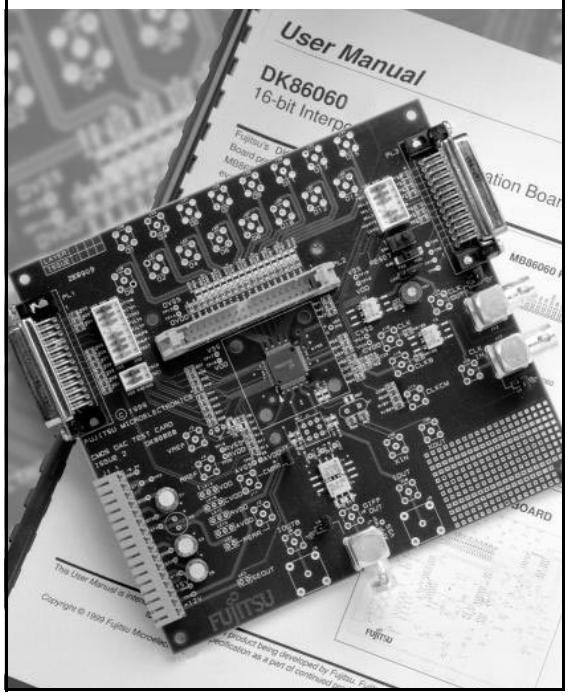
16-bit Interpolating DAC Evaluation Board

Fujitsu's DK86060-3 16-bit Interpolating DAC Evaluation Board provides a simple and effective means of evaluating the MB86060 16-bit Interpolating DAC. This enables faster device evaluation without incurring the time and cost penalties of in-house PCB design and manufacture.

The board provides a complete evaluation environment for the DAC device. A selectable single-ended or transformer-coupled differential analog output interface is provided on-board to simplify integration into target application and development environments. The clock can be sourced from either the internal crystal oscillator, or from a transformer-coupled RF source. 16-bit data is input via a 40way IDC header, or optional SMA/SMB connectors.

The MB86060 device is a single 16-bit DAC enclosed in a 80 pin LQFP package with a 0.5mm pin pitch.

EVALUATION BOARD



Features

- 16-bit data input via a choice of connectors
- Transformer-coupled differential output via BNC & SMA/SMB
- Internal oscillator with optional on-board crystal
- Transformer-coupled RF clock input via BNC & SMA/SMB
- Requires DC power supply of +3.3V

CAUTION

ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

This page left intentionally blank

1 Overview

The DK86060-3 evaluation board allows users to evaluate and demonstrate the different operational modes of the MB86060 16-bit Interpolating DAC. The evaluation board consists of a MB86060 device with support circuitry for single-ended or differential analog output interfaces, a clock input interface, and a clock output interface. This will enable simple connection of measurement equipment. For convenience, customer evaluation boards have been configured using soldered zero-ohm links for transformer-coupled differential output only.

The CMOS input data interface has a 40 way IDC header for connection via a flat ribbon cable. Separate SMA/SMB connectors for individual data bit connections are also available, but not normally fitted (SMA not recommended due to insufficient space to rotate the connectors body). The setup of the device is controlled by on-board DIP switches, but these controls can be accessed and overridden via two 25 way male D type connectors if remote control is required.

The evaluation board has been designed to address requirements of both automatic and conventional bench testing. Standard evaluation boards feature a simplified build state where certain components or connectors are omitted. These omissions are documented in Appendix A with the evaluation board schematics.

This User Manual is intended to document the DK86060-3 Development Kit PCB titled 'MB86060 DAC TEST CARD - ISSUE 3' only.

2 Evaluation Board

2.1 Power Supply

The DK86060-3 evaluation board requires a +3.3V supply, and a number of other low voltage DC supplies depending upon build configuration (marked †). A cable mounting socket suitable for mating with the PCB mounted power plug is supplied with the development board. Additional sockets, type Weidmuller BL3.6/16 may be obtained from RS Components (http://rswww.com), Stock no. 216-2683. The power should be connected to the board via this connector, as shown in Figure 2.1. Flexible cable of 16 - 28 AWG, 0.5 - 1.5mm^2 should be used.

The format of the power connector is common across Fujitsu's DAC Development Kit range. The result is that there are some un-necessary supplies (marked ‡). These supply pins are connected to test points for convenience if the user requires extra supplies for the prototype area

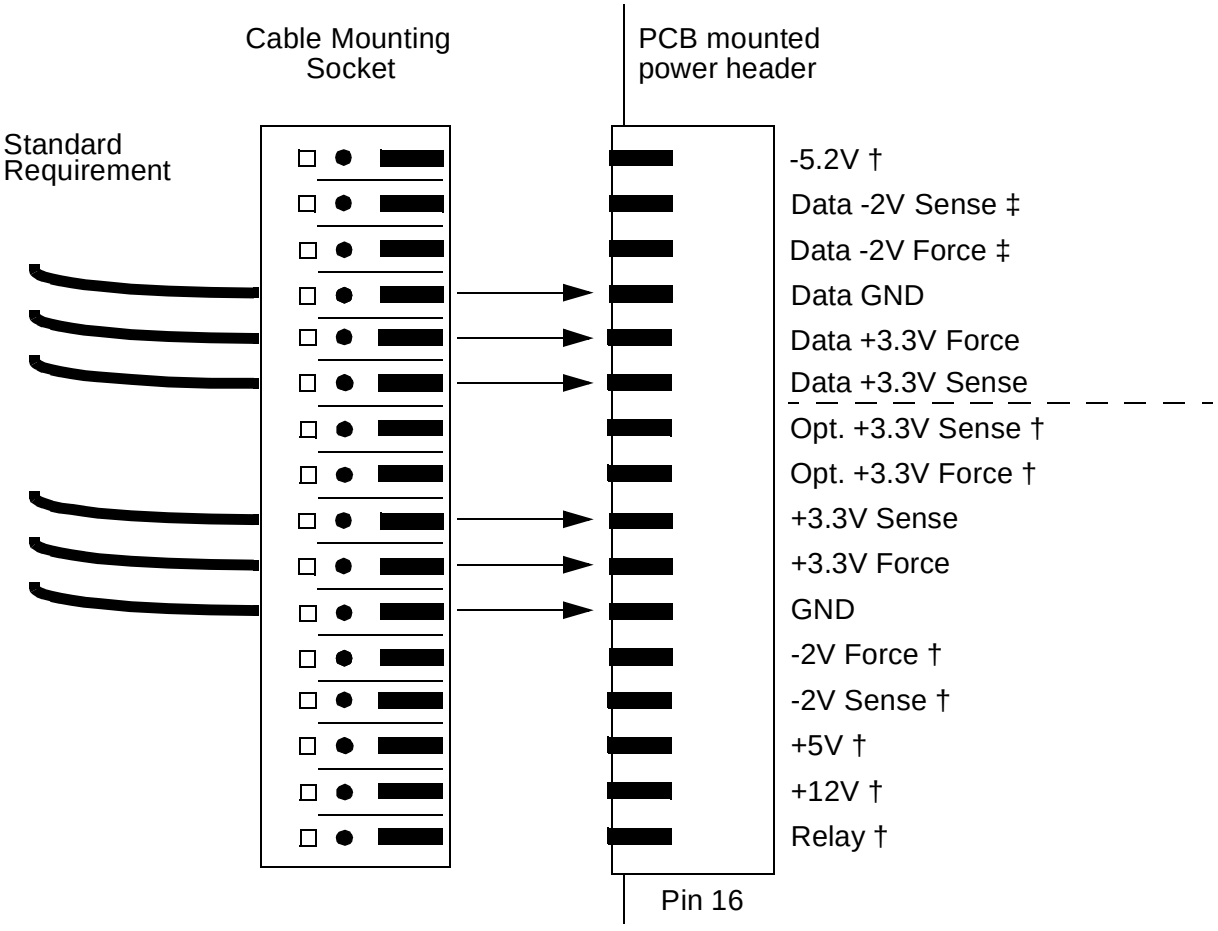


Figure 2.1: Power Connections

2.2 Board And Interface Controls

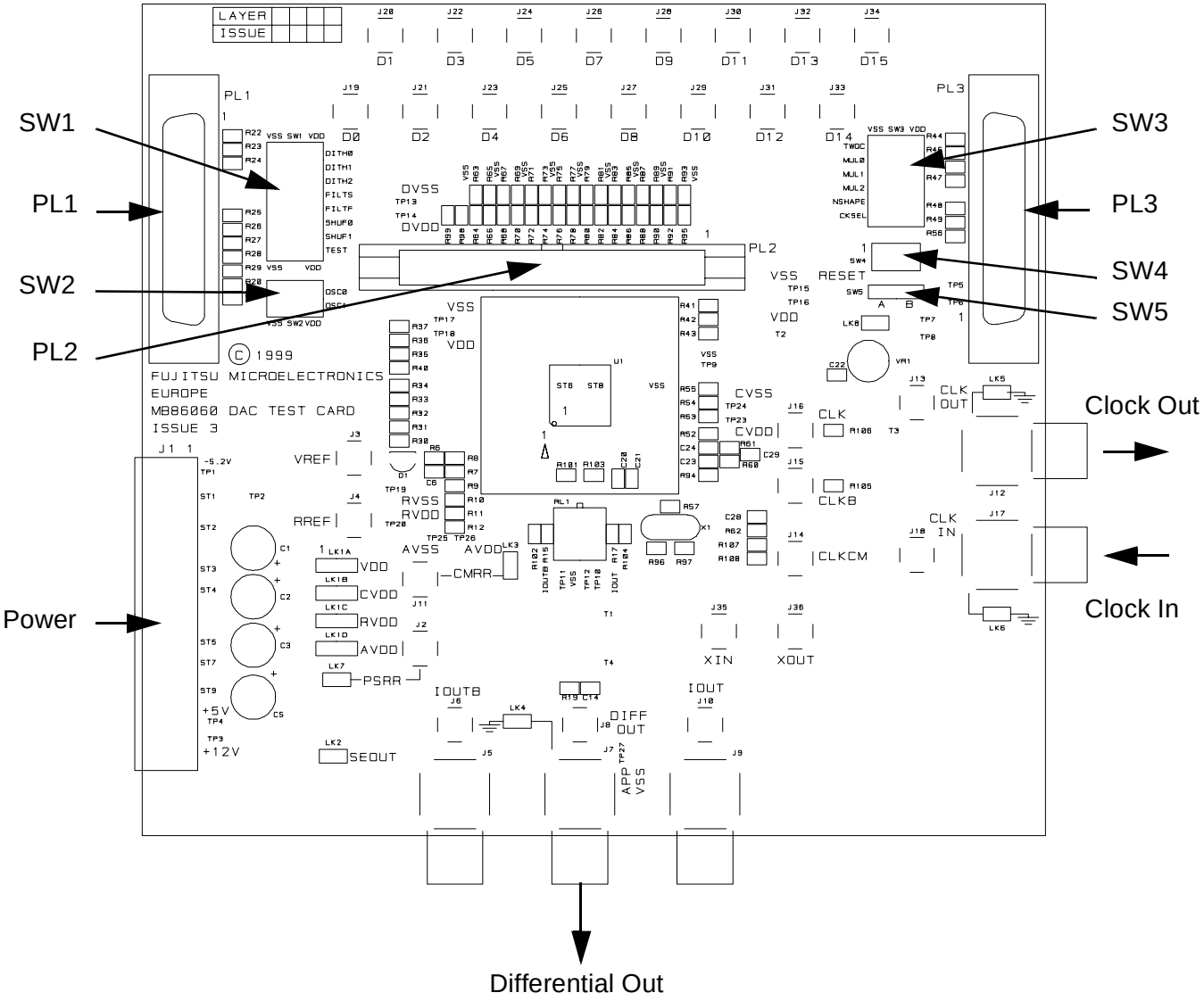


Figure 2.2: Evaluation Board Component Side Layout

2.2.1 Switches

There are several control switches on the evaluation board, as shown in Figure 2.2. Switch idents are marked on the board silkscreen.

Table 1: Switch 1 Settings

Switch	Mode / Function	Setting
SW1[1:3] (DITH0, DITH1, DITH2)	Dither disabled	**VSS, VSS, VSS**
	-27.0 dBFS pk Dither amplitude	VDD, VSS, VSS
	-21.0 dBFS pk Dither amplitude	VSS, VDD, VSS
	-15.0 dBFS pk Dither amplitude	VDD, VDD, VSS
	-9.0 dBFS pk Dither amplitude	VSS, VSS, VDD
	-3.0 dBFs pk Dither amplitude	VDD, VSS, VDD
	Factory use only	VSS, VDD, VDD
	Factory use only	VDD, VDD, VDD
SW1[4:5] (FILTS, FILTF)	Disabled	**VSS, VSS**
	x2 Slow	VDD, VSS
	x2 Fast	VSS, VDD
	x4	VDD, VDD
SW1[6:7] (SHUF0, SHUF1)	Segment Shuffling disabled	**VSS, VSS**
	Random - every 4 cycles	VDD, VSS
	Random - every 8 cycles	VSS, VDD
	Random - every 16 cycles	VDD, VDD
SW1[8] (TEST)	Factory use only	**VSS**

Table 2: Switch 2 Settings

Switch	Mode / Function	Setting
SW2[1:2] (OSC0, OSC1)	Multiplier fastest mode	**VSS, VSS**
		VDD, VSS
		VSS, VDD
	Multiplier slowest mode	VDD, VDD

Table 3: Switch 3 Settings

Switch	Mode / Function	Setting
SW3[1] (TWOC)	Offset binary input data	**VSS**
	2's Compliment input data	VDD
SW3[2:4] (MUL0, MUL1, MUL2)	Clock multiplier bypass	**VSS, VSS, VSS**
	Clock multiplier x1 mode	VDD, VSS, VSS
	Clock multiplier x2 mode	VSS, VDD, VSS
	Clock multiplier x3 mode	VDD, VDD, VSS
	Clock multiplier x4 mode	VSS, VSS, VDD
	Clock multiplier x5 mode	VDD, VSS, VDD
	Clock multiplier x6 mode	VSS, VDD, VDD
	Clock multiplier x8 mode	VDD, VDD, VDD
SW3[5] (NSHAPE)	Noise shaping disabled	**VSS**
	Noise shaping enabled	VDD
SW3[6]† (CKSEL)	On-board crystal	VSS
	External clock source	**VDD**

† Standard Evaluation Kits are not configured with an on-board crystal.

Table 4: Switch 4 Settings

Switch	Mode / Function	Setting	
SW3[1] & SW4	Part Reset†	SW3[1] VSS	Push to Reset
	Full Reset‡	SW3[1] VDD	Push to Reset

† With SW3[1] set to Offset binary, a 'Reset' will not reset the Clock Multiplier or the Reference circuits.
‡ With SW3[1] set to 2's compliment, a 'Reset' will reset the entire device.

Table 5: Switch 5 Settings

Switch	Mode / Function	Setting
SW5	Device in forced RESET mode	B
	Device in normal operating mode	**A**

Note: SW1, 2 & 3 may appear to malfunction if pressure is placed on the slider when in either the left or right position. In this case the DAC control pin will be floating.

2.2.2 Jumper Links

Table 6: Jumper Links

Link Name	Mode / Function	Setting
LK1A† (VDD)	Optional supply used for VDD	1 to 2 linked
	Common supply used for VDD	**2 to 3 linked**
LK1B† (CVDD)	Optional supply used for CVDD	1 to 2 linked
	Common supply used for CVDD	**2 to 3 linked**
LK1C† (RVDD)	Optional supply used for RVDD	1 to 2 linked
	Common supply used for RVDD	**2 to 3 linked**
LK1D† (AVDD)	Optional supply used for AVDD	1 to 2 linked
	Common supply used for AVDD	**2 to 3 linked**
LK2‡ (SEOUT)	Select single-ended output	Linked
	Select differential output	**Not linked**
LK3 (CMRR)	Centre tap of T1 (Pin 5) linked to AVSS	Linked
	Centre tap of T1 (Pin 5) decoupled to AVSS	**Not linked**
LK4	DIFF OUT Ground linked to AVSS	Linked
	DIFF OUT Ground floating	**Not Linked**
LK5	CLK OUT Ground linked to VSS	Linked
	CLK OUT Ground floating	**Not Linked**
LK6	CLK IN Ground linked to CVSS	Linked
	CLK IN Ground floating	**Not Linked**
LK7† (PSRR)	Power supply ripple rejection disabled	**Linked**
	Power supply ripple rejection enabled	Not Linked
LK8	CLK OUT biasing enabled	Linked
	CLK OUT biasing disabled	**Not Linked**

Note: Bold type indicates default jumper settings.
† Standard Evaluation Kits are not configured to use the optional supply. LK1 and LK7 are not used.
‡ Standard Evaluation Kits are configured for Differential output. LK2 is not used.

This page left intentionally blank

3 Getting Started

This Chapter documents the basic steps to powering up and starting to use the DK86060-3 Evaluation Board. Component references may be cross-referenced with the component overlay in Appendix B.

Step 1. Configure the board

The data input format must be configured to either Offset binary or 2's Compliment. Use configuration switch SW3[1] to select.

The device control signals should be set to the default conditions shown in Section 2.2. Use configuration switches SW1, SW2 and SW3 to select.

Jumper links LK3 to LK6 inclusive, and LK8, should be 'Not linked'. Switch SW5 should be set to position 'A'.

Step 2. Connect data input & analog output connectors to the board

The input data should be connected via the 40 way IDC header PL2, or if fitted the SMA/SMB connectors J19 to J34 inclusive. See Table C1: for the pin description of the IDC header.

The output is provided as a transformer-coupled differential signal, via a BNC connector.

- Differential Output signal (J7). (50Ω source resistance)
  The DAC is coupled to a single output connector using a transmission line and 1:1 balun transformer. Signal swing is ±0.5V with a high impedance load, or ±0.25V with an external 50Ω load. For sinusoidal signals, this corresponds to approximately -2dBm into a 50Ω external load.

Step 3. Connect clock

The clock input is provided to the device through a transmission line transformer, via a BNC connector.

- RF clock (J17). (50Ω input impedance)
  The DAC is coupled to a single input connector using a transmission line transformer. Sine wave or square wave input signals between -10dBm and +10dBm are acceptable, depending on clock frequency and required output jitter / phase noise.

Step 4. Connect power header to power supplies

Ensure that the power supply is connected according to Figure 2.1. Connect the power header to the board and turn the power supply on.

Step 5. Press Reset

Press the Reset button to ensure that the device is in the correct operating condition. Press Reset every time a configuration change is made.

4 Testing

This section provides a brief introduction to testing with the DK86060-3 16-bit Interpolating DAC Evaluation Board.

MB86060 incorporates a 12-bit, 400MSa/s digital to analog converter core with a 16-bit interpolation filtering front end, designed to give excellent SFDR performance. The use of novel techniques for the converter architecture have allowed high speed operation consistent with BiCMOS or bipolar devices, but with the low power consistent with CMOS.

In certain applications it is now possible to consider using the MB86060's DAC core at a full 400MSa/s DAC conversion rate, even though the generated signal band may only be, for example, up to 40MHz or less. Although, in theory, a 100MSa/s converter would be sufficient to reproduce this desired signal band, according to Nyquist, converter performance will tend to limit due to step-size and sinx/x roll-off as a result of the converters sample & hold output stage. 400MSa/s operation significantly reduces effects due to both of these - sinx/x roll-off is reduced from -4dB to -0.22dB, and the increased oversampling [DAC conversion rate / signal rate] reduces step sizes to give a direct improvement in spurious performance.

These issues should be considered when testing the MB86060 and measurements should be obtained at different conversion rates to establish the most appropriate operating conditions for the target application.

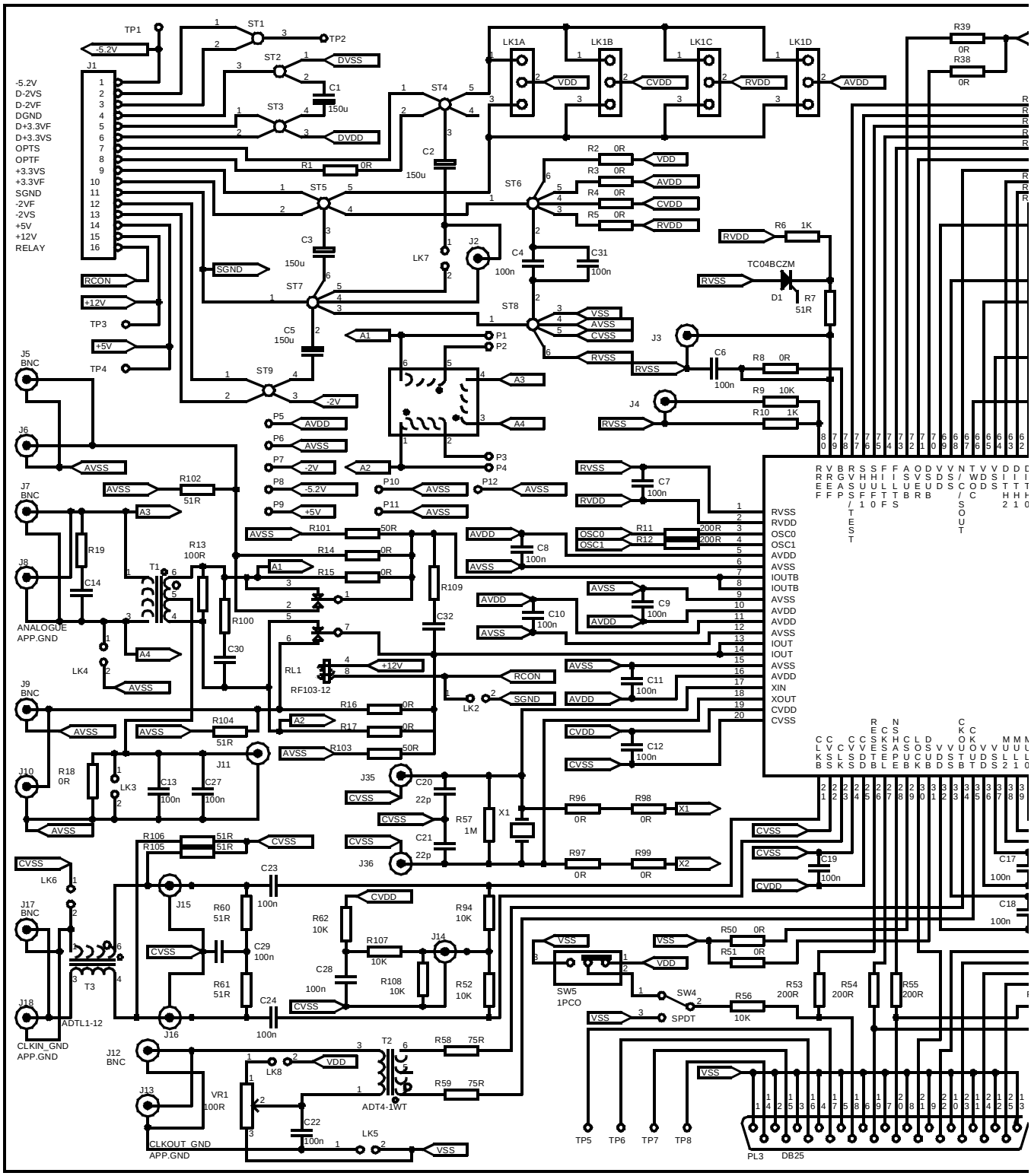
For convenience the board has been configured using soldered zero-ohm links as a transformer coupled differential output. To enable single-ended outputs changes to the soldered zero-ohm links would be required. For rise/fall time tests the transformer-coupled output should not be used since the transformer response will limit the dV/dt. The DAC current switches are designed to give the best possible differential performance, at the expense of some single ended performance, so there is a noticeable difference between the two configurations. The revised analog output circuit uses an additional transmission line transformer to improve rejection of common-mode distortion at the DAC output.

If a spectrum analyser is used to measure the output spectrum, it should have a very good noise and distortion, for example HP8562E or R&S FSEA30. In addition, the input attenuator setting should be chosen such that input mixer distortion does not limit the measurements (e.g. 30dB RF attenuation). This implies that narrow resolution bandwidths and/or averaging are required to obtain low enough measurement noise floor.

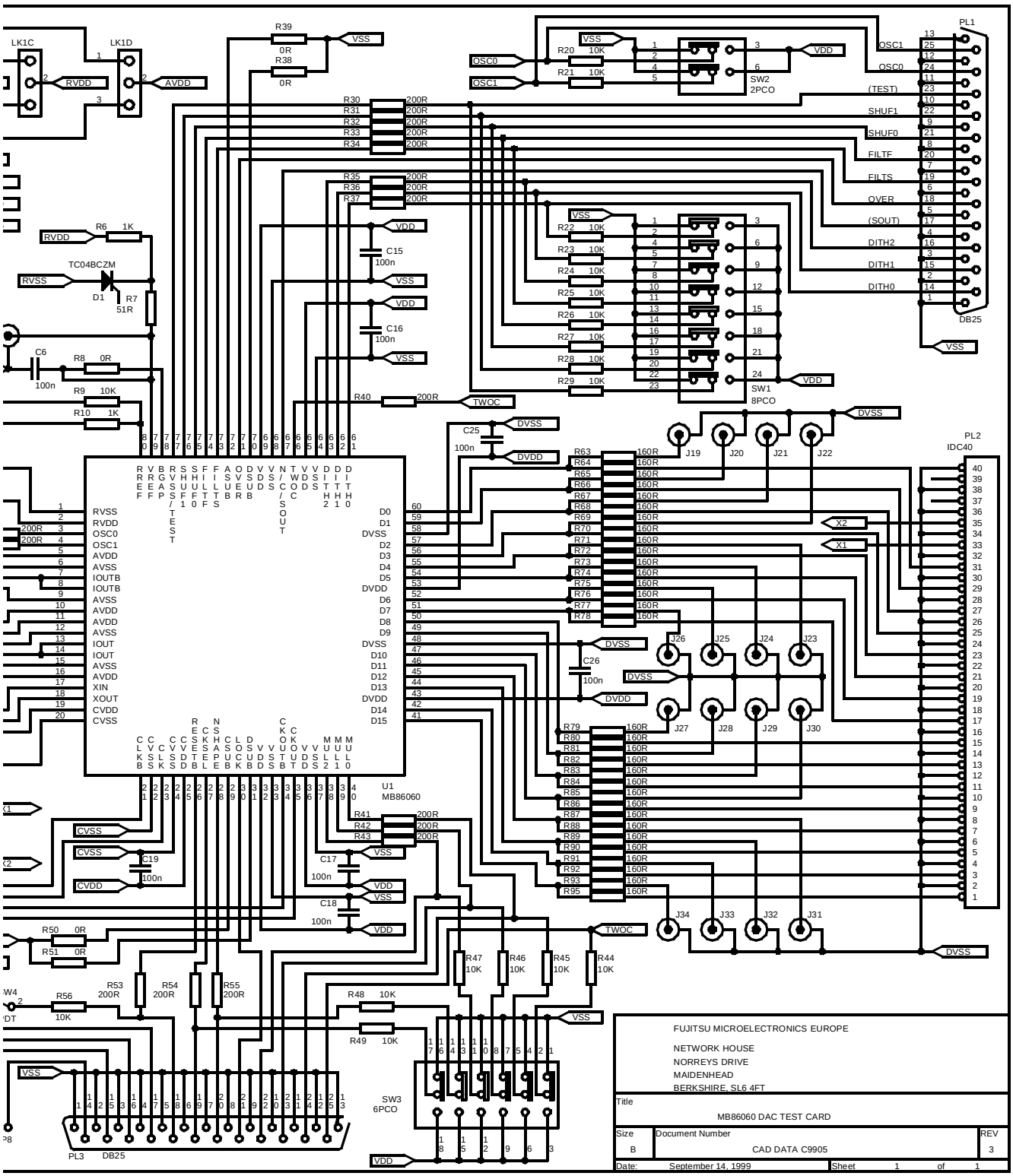
Appendix A Evaluation Board Circuit Diagrams

Appendix A shows the circuit diagrams of the DK86060-3 evaluation board. Note that these diagrams are for reference only and that some components fitted to the board may be of a different value to the schematics or not fitted at all. Fujitsu has undertaken to document these changes where possible. The schematic is divided over two pages for clarity.

- Sheet 1 - DAC support circuitry, including analog output interfaces [covers 2 pages]



DK86060-3 16-bit Interpolating DAC Evaluation Board



A.1 Components Not Fitted to the PCB

Table A1: Components Not Fitted

Reference	Value	Description
LK1a, b, c, d	-	Power supply selection jumper links
LK2	-	Single-ended output selection jumper link
LK7	-	PSRR jumper link
J2 to J6, J8, J10, J11, J13 to J16, J18 to J36	-	SMA/SMB connectors
J5, J9	-	BNC connectors
D1	TC04BCZM	Reference diode
RL1	RF103-12	Output selection relay
X1	-	Crystal
C2	150uF	Optional power supply decoupling capacitor
C14, C32	-	Analog output RC network capacitors
C20, C21	22pF	Crystal capacitors
R1	0R	Optional power supply PSRR series resistor
R6	1K	Reference current limit resistor
R7	51R	Reference series resistor
R14, R16	0R	Single-ended output relay bypass resistors
R18	0R	CMRR jumper link bypass resistor
R19, R109	-	Analog output RC network resistors
R57	1M	Crystal shunt resistor
R63, R65, R67, R69, R71, R73, R75, R77, R79, R81, R83, R85, R87, R89, R91, R93	0R	Data input series resistors (for SMA/SMB connectors)
R102, R104	51R	Analog output termination resistors
T4	-	Optional analog output circuit transformer

A.2 Changes to the PCB Schematics

Table A2: Schematic Changes

Reference	Old Value	New Value	Description
R100	-	51R	Analog output RC network resistor
C30	-	22pF	Analog output RC network capacitor
T1(a)	-	ADTT1-1	Mini-Circuits 1:1 analog output transformer
T1(b)		ADTL1-12	Mini-Circuits transmission line transformer

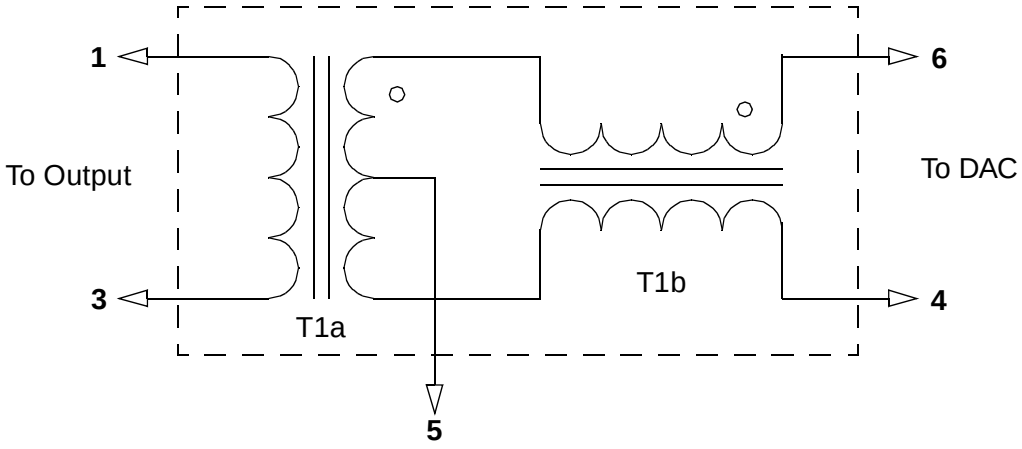


Figure A1 Replacement Schematic For T1 (Pin Numbers Refer To T1)

Appendix B Component Overlays

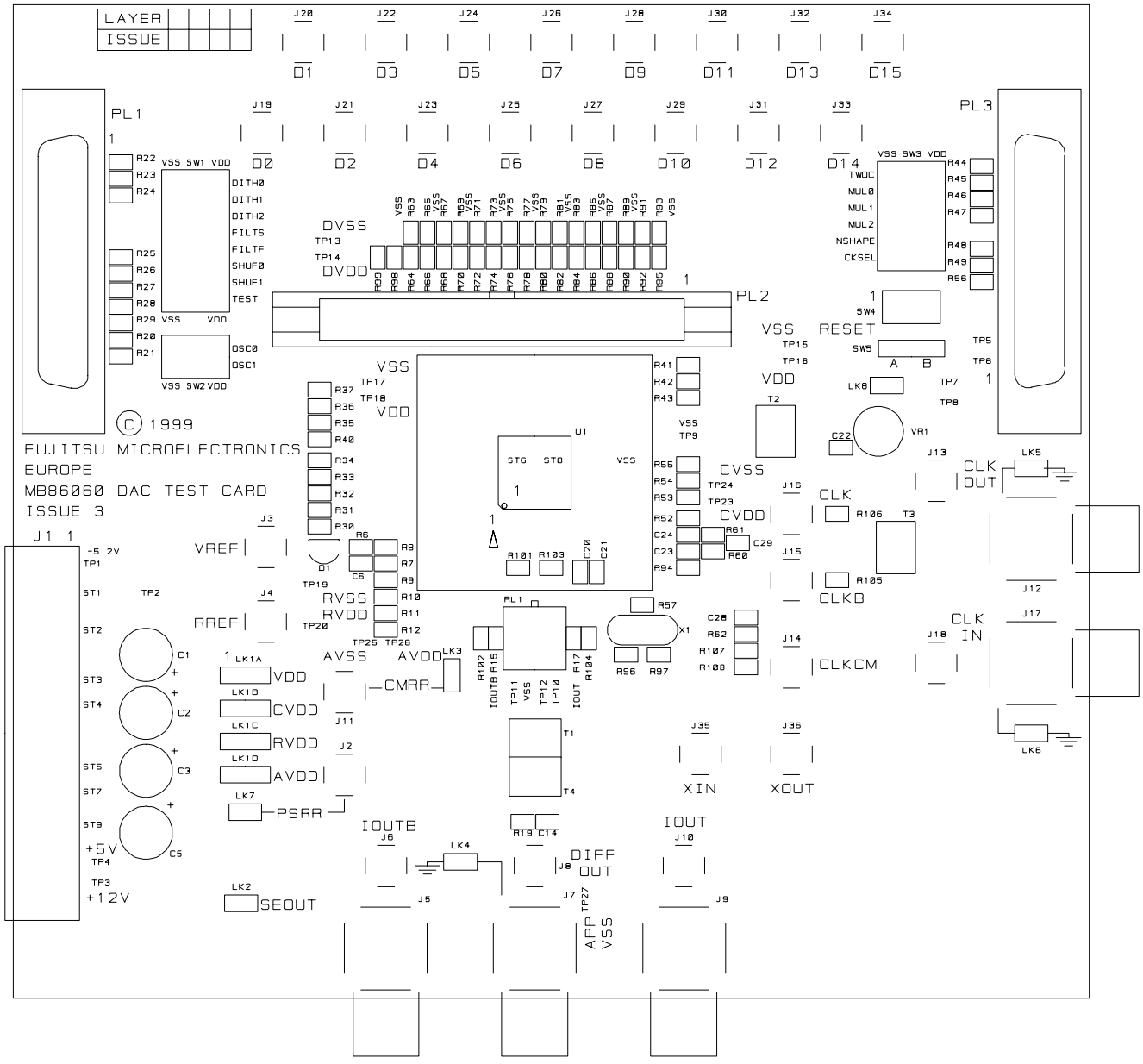


Figure B1 Component Overlay For Layer 1, (Component Side)

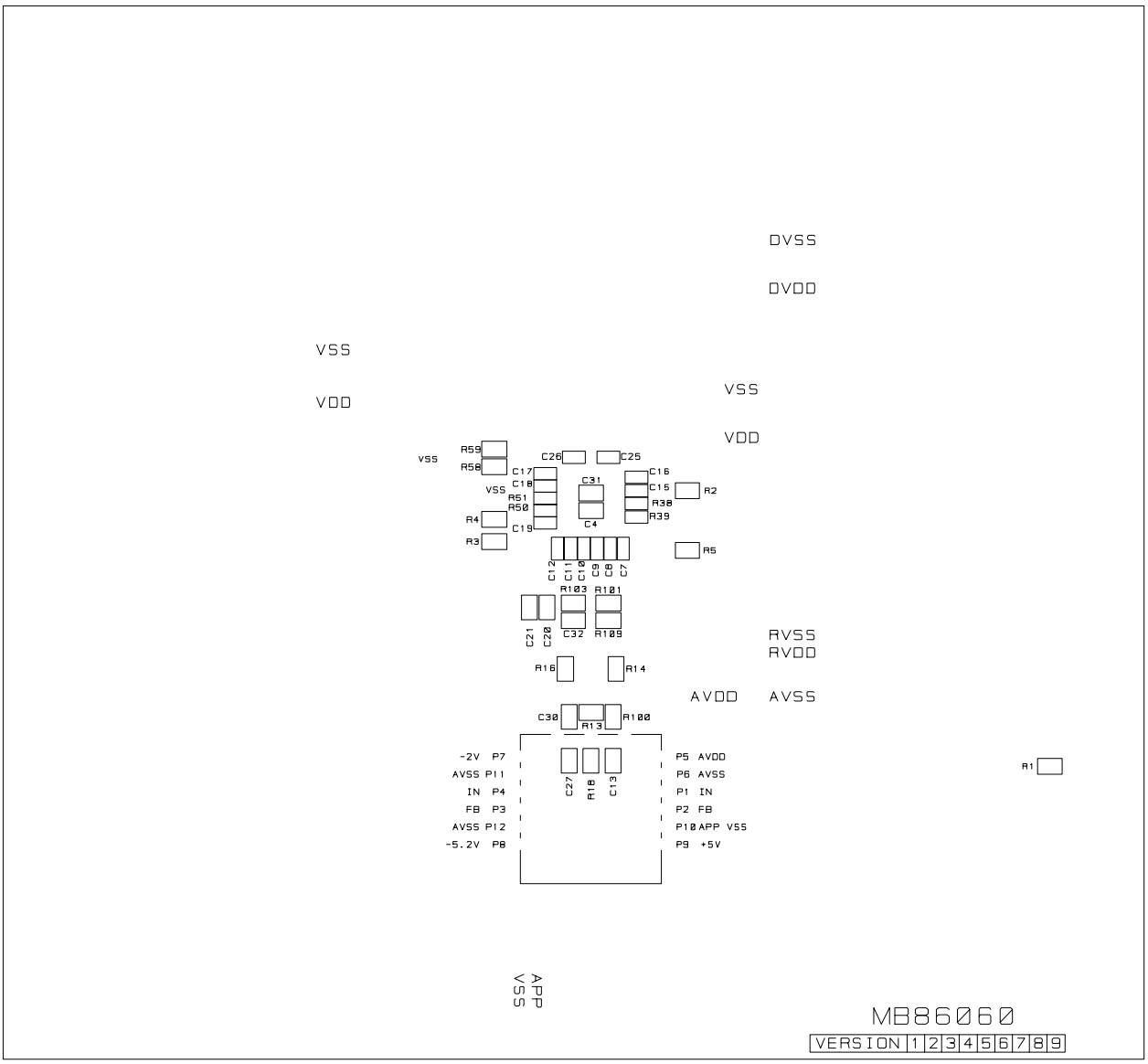


Figure B2 Component Overlay For Layer 4 (Solder Side)

Appendix C Connector Pin Functions

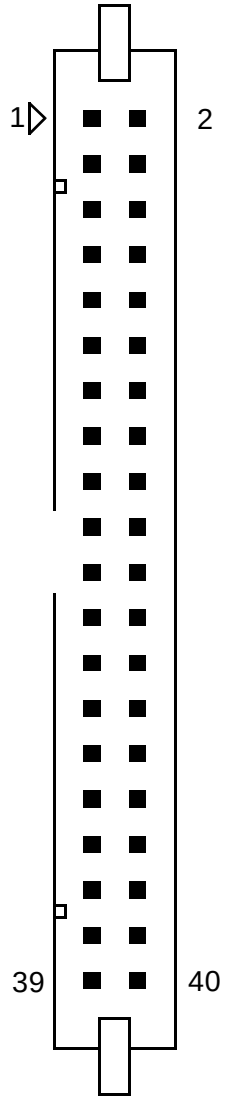


Table C1: Data Connector PL2 Pin Functions

Pin	Function
1	Data Bit 15 (MSB)
3	Data Bit 14
5	Data Bit 13
7	Data Bit 12
9	Data Bit 11
11	Data Bit 10
13	Data Bit 9
15	Data Bit 8
17	Data Bit 7
19	Data Bit 6
21	Data Bit 5
23	Data Bit 4
25	Data Bit 3
27	Data Bit 2
29	Data Bit 1
31	Data Bit 0 (LSB)
33	XIN
35	XOUT
37	Not Used
39	Not Used
2 to 40 (Even numbers only)	Data Ground (DVSS)

Table C2: Control Connector PL1 Pin Functions

Pin	Function
1 to 13	Digital Ground (VSS)
14	DITH0
15	DITH1
16	DITH2
17†	SOUT (O/P)
18	OVER (O/P)
19	FILTS
20	FILTF
21	SHUF0
22	SHUF1
23†	TEST
24	OSC0
25	OSC1

† These pins are for factory test purposes only.

Table C3: Control Connector PL3 Pin Functions

Pin	Function
1 to 13	Digital Ground (VSS)
14†	Test Point 8
15†	Test Point 7
16†	Test Point 6
17†	Test Point 5
18	RESETB
19	CKSEL
20	NSHAPE
21	LOCK (O/P)
22	MUL2
23	MUL1
24	MUL0
25	TWOC

† These pins are connected to test points so that connections to the prototype area can be made via the control connector.

Appendix D Prototype Area

A prototype area has been introduced into the DK86060-3 development kit PCB. This area takes the form of a matrix of pads with plated through holes on a 2.54mm pitch. The pads are made square to allow for 0805 format surface mount devices to be fitted between adjacent pads. The matrix area has four rows individually linked together to act as power rails. These rows are arranged as two pairs, with connections to the internal planes (layers 2 and 3) made to each of the rows. The internal plane regions only occupy the prototype area, and are not linked to any other area of the PCB. The prototype area layout is shown in Figure D1.

Layer 2 would typically be used as the ground plane, and layer 3 as the power plane, with signals routed on layer 1. However the choice in the prototype area is free as the planes are entirely separate to the rest of the PCB.

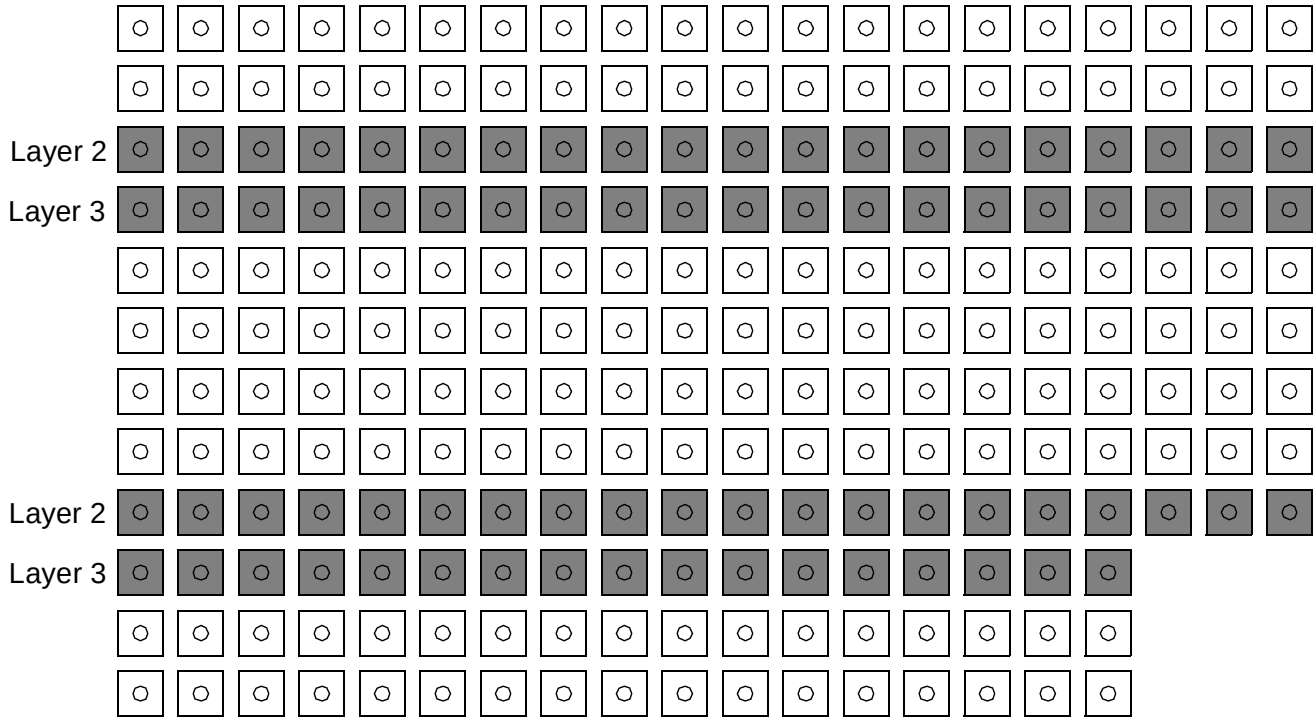


Figure D1 Prototype Area Layout

This page left intentionally blank

Notes:

FUJITSU

DK86060-3 16-bit Interpolating DAC Evaluation Board

Worldwide Headquarters

Japan

Fujitsu Limited

Tel: +81 44 754 3753
Fax: +81 44 754 3329

1015 Kamikodanaka 4-1-1
Nakahara-ku
Kawasaki-shi
Kanagawa-ken 211-88
Japan

http://www.fujitsu.co.jp/

Asia

Fujitsu Microelectronics Asia Pte Limited

Tel: +65 281 0770
Fax: +65 281 0220

151 Lorong Chuan
#05-08 New Tech Park
Singapore 556741

http://www.fmap.com.sg/

USA

Fujitsu Microelectronics Inc

Tel: +1 408 922 9000
Fax: +1 408 922 9179

3545 North First Street
San Jose CA 95134-1804
USA

Tel: +1 800 866 8608
Fax: +1 408 922 9179

Customer Response Center
Mon-Fri: 7am-5pm (PST)

http://www.fujitsumicro.com/

Europe

Fujitsu Microlectronics Europe GmbH

Tel: +49 6103 6900
Fax: +49 6103 690122

Am Siebenstein 6-10
D-63303 Dreieich-Buchschlag
Germany

http://www.fujitsu-fme.com/