GE864 Hardware User Guide

1vv0300694 Rev.10 - 10/06/08

Making machines talk.

This document is relating to the following products:

GE864-QUAD 3990250648
GE864-PY 3990250650

Contents

DISCLAIMER

The information contained in this document is the proprietary information of Telit Communications S.p.A. and its affiliates ("TELIT"). The contents are confidential and any disclosure to persons other than the officers, employees, agents or subcontractors of the owner or licensee of this document, without the prior written consent of Telit, is strictly prohibited.

Telit makes every effort to ensure the quality of the information it makes available. Notwithstanding the foregoing, Telit does not make any warranty as to the information contained herein, and does not accept any liability for any injury, loss or damage of any kind incurred by use of or reliance upon the information.

Telit disclaims any and all responsibility for the application of the devices characterized in this document, and notes that the application of the device must comply with the safety standards of the applicable country, and where applicable, with the relevant wiring rules.

Telit reserves the right to make modifications, additions and deletions to this document due to typographical errors, inaccurate information, or improvements to programs and/or equipment at any time and without notice. Such changes will, nevertheless be incorporated into new editions of this application note.

1 Overview

The aim of this document is the description of some hardware solutions useful for developing a product with the **Telit GE864-QUAD / PY module**.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the **Telit GE864-QUAD / PY module**.
For further hardware details that may not be explained in this document refer to the Telit GE864-QUAD / PY Product Description document where all the hardware information is reported.

NOTICE

(EN) The integration of the GSM/GPRS GE864-QUAD / PY cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare GSM/GPRS GE864-QUAD / PY all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die integration des GE864-QUAD / PY GSM/GPRS Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen

(SL) Integracija GSM/GPRS GE864-QUAD / PY modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem piročniku.

(SP) La utilización del modulo GSM/GPRS GE864-QUAD / PY debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire GSM/GPRS GE864-QUAD / PY dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

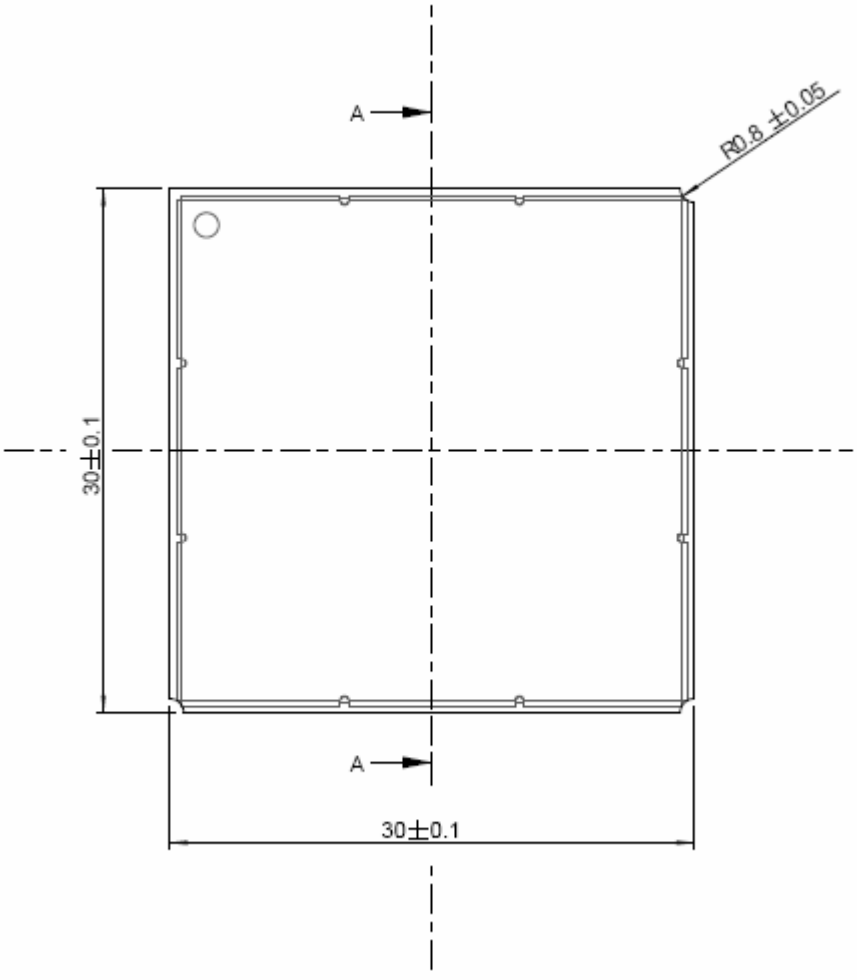
(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי GE864-QUAD / PY עם המוצר.

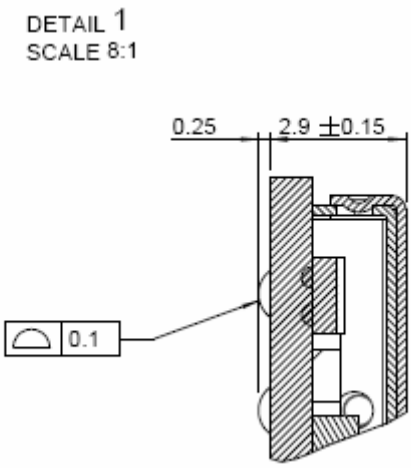
The information presented in this document is believed to be accurate and reliable. However, no responsibility is assumed by Telit Communications S.p.A. for its use, nor any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent rights of Telit Communications S.p.A. other than for circuitry embodied in Telit products. This document is subject to change without notice.

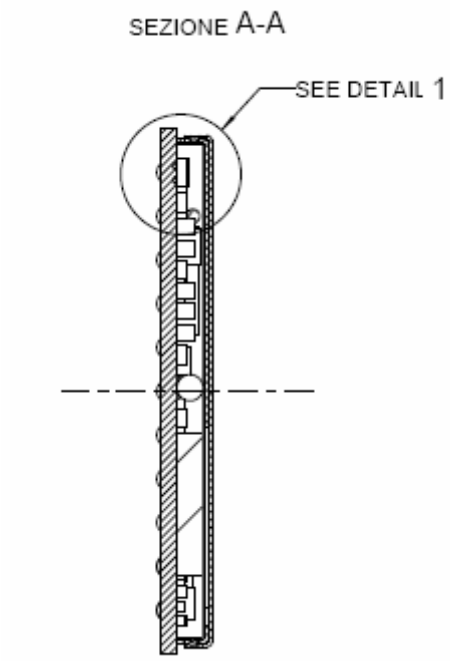
2 GE864 Mechanical Dimensions

The **Telit GE864 module** overall dimension are:

- **Length:** **30 mm**
- **Width:** **30 mm**
- **Thickness:** **2.9 mm**







3 GE864 module connections

3.1 PIN-OUT

Ball	Signal	I/O	Function	Internal PULL UP	Type
Audio					
H9	EAR_MT-	AO	Handset earphone signal output, phase -		Audio
G10	EAR_MT+	AO	Handset earphone signal output, phase +		Audio
H10	EAR_HF+	AO	Handsfree ear output, phase +		Audio
J10	EAR_HF-	AO	Handsfree ear output, phase -		Audio
J8	MIC_MT+	AI	Handset mic.signal input; phase+		Audio
G9	MIC_MT-	AI	Handset mic.signal input; phase-		Audio
G8	MIC_HF+	AI	Handsfree mic. input; phase +		Audio
J9	MIC_HF-	AI	Handsfree mic.input; phase -		Audio
F9	AXE	I	Handsfree switching	100K	CMOS 2.8V
SIM card interface					
C10	SIMCLK	O	External SIM signal – Clock		1,8 / 3V
E9	SIMRST	O	External SIM signal – Reset		1,8 / 3V
D10	SIMIO	I/O	External SIM signal – Data I/O		1,8 / 3V
C11	SIMIN	I	External SIM signal – Presence (active low)	47K	1,8 / 3V
D4[1]	SIMVCC	-	External SIM signal – Power supply for the SIM		1,8 / 3V
Trace					
D11	TX_TRACE	O	TX Data for debug monitor		CMOS 2.8V
F10	RX_TRACE	I	RX Data for debug monitor		CMOS 2.8V
Prog. / Data + HW Flow Control					
E7	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 2.8V
H8	C104/RXD	O	Serial data output to DTE		CMOS 2.8V
B7	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE		CMOS 2.8V
F7	C105/RTS	I	Input for Request to send signal (RTS) from DTE		CMOS 2.8V
F6	C106/CTS	O	Output for Clear to send signal (CTS) to DTE		CMOS 2.8V
D9	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE		CMOS 2.8V
E11	C107/DSR	O	Output for Data set ready signal (DSR) to DTE		CMOS 2.8V
B6	C125/RING	O	Output for Ring indicator signal (RI) to DTE		CMOS 2.8V
DAC and ADC					

[1] On this line a maximum of 10nF bypass capacitor is allowed

Ball	Signal	I/O	Function	Internal PULL UP	Type
C7	DAC_OUT	AO	Digital/Analog converter output		D/A
J11	ADC_IN1	AI	Analog/Digital converter input		A/D
H11	ADC_IN2	AI	Analog/Digital converter input		A/D
G11	ADC_IN3	AI	Analog/Digital converter input		A/D
Miscellaneous Functions					
A2	RESET*	I	Reset input		
E2	VRTC	AO	VRTC Backup capacitor		Power
D8	STAT_LED	O	Status indicator led		**CMOS 1.8V**
G1	CHARGE	AI	Charger input		Power
G2	CHARGE	AI	Charger input		Power
J5	ON_OFF*	I	Input command for switching power ON or OFF (toggle command).	47K	Pull up to VBATT
D5	VAUX1	-	Power output for external accessories		-
L8	PWRMON	O	Power ON Monitor		CMOS 2.8V
L4	Antenna	O	Antenna output – 50 ohm		RF
D7	DVI2_CLK	-	DVI2_CLK (Digital Voice Interface)	4.7K	CMOS 2.8
GPIO					
G4	TGPIO_12	I/O	Telit GPIO12 Configurable GPIO		CMOS 2.8V
C2	TGPIO_03	I/O	Telit GPIO03 Configurable GPIO		CMOS 2.8V
B3	TGPIO_04	I/O	Telit GPIO04 Configurable GPIO / RF Transmission Control		CMOS 2.8V
C3	TGPIO_20	I/O	Telit GPIO20 Configurable GPIO		CMOS 2.8V
B4	TGPIO_14	I/O	Telit GPIO14 Configurable GPIO		CMOS 2.8V
D1	TGPIO_11	I/O	Telit GPIO11 Configurable GPIO		CMOS 2.8V
B1	TGPIO_19	I/O	Telit GPIO19 Configurable GPIO		CMOS 2.8V
C1	TGPIO_01	I/O	Telit GPIO01 Configurable GPIO		CMOS 2.8V
K7	TGPIO_18	I/O	Telit GPIO18 Configurable GPIO/ DVI2_RX (Digital Voice Interface)		CMOS 2.8V
H5	TGPIO_17	I/O	Telit GPIO17 Configurable GPIO / DVI2_WA (Digital Voice Interface)		CMOS 2.8V
F5	TGPIO_15	I/O	Telit GPIO15 Configurable GPIO		CMOS 2.8V
K11	TGPIO_08	I/O	Telit GPIO08 Configurable GPIO		CMOS 2.8V
B5	TGPIO_06 / ALARM	I/O	Telit GPIO06 Configurable GPIO / ALARM		CMOS 2.8V
C9	TGPIO_09	I/O	Telit GPIO09 GPIO I/O pin		CMOS 2.8V
E6	TGPIO_02 / JDR	I/O	Telit GPIO02 I/O pin / Jammer detect report		CMOS 2.8V
L9	TGPIO_07 / BUZZER	I/O	Telit GPIO07 Configurable GPIO / Buzzer		CMOS 2.8V
H6	TGPIO_16	I/O	Telit GPIO16 Configurable GPIO		CMOS 2.8V
K10	TGPIO_13	I/O	Telit GPIO13 Configurable GPIO		CMOS 2.8V
K8	TGPIO_05 / RFTXMON	I/O	Telit GPIO05 Configurable GPIO / Transmitter ON monitor		CMOS 2.8V
L10	TGPIO_21	I/O	Telit GPIO21 Configurable GPIO		CMOS 2.8V
E8	TGPIO_22	I/O	Telit GPIO22 Configurable GPIO		**CMOS 1.8V (not 2.8V !!)**
H3	TGPIO_10	I/O	Telit GPIO10 Configurable GPIO / DVI2_TX (Digital Voice Interface)		CMOS 2.8V
Power Supply					

Ball	Signal	I/O	Function	Internal PULL UP	Type
J1	VBATT	-	Main power supply		Power
K1	VBATT	-	Main power supply		Power
J2	VBATT	-	Main power supply		Power
K2	VBATT	-	Main power supply		Power
A1	GND	-	Ground		Power
F1	GND	-	Ground		Power
H1	GND	-	Ground		Power
L1	GND	-	Ground		Power
H2	GND	-	Ground		Power
L2	GND	-	Ground		Power
J3	GND	-	Ground		Power
K3	GND	-	Ground		Power
L3	GND	-	Ground		Power
K4	GND	-	Ground		Power
K5	GND	-	Ground		Power
D6	GND	-	Ground		Power
K6	GND	-	Ground		Power
L6	GND	-	Ground		Power
A11	GND	-	Ground		Power
F11	GND	-	Ground		Power
L11	GND	-	Ground		Power
RESERVED					
A10		-			
A3		-			
A4		-			
A5		-			
A6		-			
A7		-			
A8		-			
A9		-			
B10		-			
B11		-			
B2		-			
B8		-			
B9		-			
C4		-			
C8		-			
D2		-			
D3		-			
E1		-			
E10		-			
E3		-			
E4		-			

Ball	Signal	I/O	Function	Internal PULL UP	Type
F2		-			
F3		-			
F4		-			
G6		-			
G7		-			
H4		-			
H7		-			
J4		-			
J6		-			
J7		-			
K9		-			
L5		-			
E5		-			
L7		-			
G5		-			
G3		-			
C6		-			
F8		-			
C5		-			

NOTE: RESERVED pins must not be connected

NOTE: If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

pin	signal
J1,K1,J2,K2	VBATT
A1,F1,H1,L1,H2,L2,J3,K3,L3, K4,K5,D6,K6,L6,A11,F11,L11	GND
J5	ON/OFF*
E7	TXD
A2	RESET*
H8	RXD
F7	RTS[2]

[2] RTS should be connected to the GND (on the module side) if flow control is not used

3.1.1 BGA Balls Layout

TOP VIEW

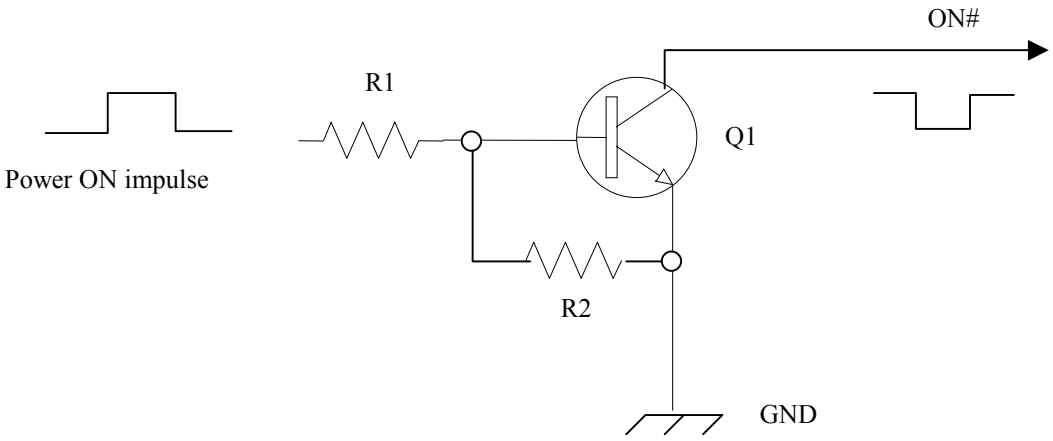
	A	B	C	D	E	F	G	H	J	K	L
1	GND	TGPIO_19	TGPIO_01	TGPIO_11	-	GND	CHARGE	GND	VBATT	VBATT	GND
2	RESET*	-	TGPIO_03	-	VRTC	-	CHARGE	GND	VBATT	VBATT	GND
3	-	TGPIO_04	TGPIO_20	-	-	-	VMICN	TGPIO_10	GND	GND	GND
4	-	TGPIO_14	-	SIMVCC	-	-	TGPIO_12	-	-	GND	Antenna
5	-	TGPIO_06 / ALARM		VAUX1	-	TGPIO_15	VMICP	TGPIO_17	ON_OFF*	GND	-
6	-	C125/RING		GND	TGPIO_02 / JDR	C106 / CTS	-	TGPIO_16	-	GND	GND
7	-	C108 / DTR	DAC_OUT	DVI2_CLK	C103 / TXD	C105 / RTS	-	-	-	TGPIO_18	-
8	-	-	-	STAD_LED	TGPIO_22	-	MIC_HF+	C104 / RXD	MIC_MT+	TGPIO_05 / RFTXMON	PWRMON
9	-	-	TGPIO_09	C109 / DCD	SIMRST	AXE	MIC_MT-	EAR_MT-	MIC_HF-	-	TGPIO_07 / BUZZER
10	-	-	SIMCLK	SIMIO	-	RX_TRACE	EAR_MT+	EAR_HF+	EAR_HF-	TGPIO_13	TGPIO_21
11	GND	-	SIMIN	TX_TRACE	C107 / DSR	GND	ADC_IN3	ADC_IN2	ADC_IN1	TGPIO_08	GND

	AUDIO Signals balls
	SIM CARD interface balls
	TRACE Signals balls
	Prog. / data + Hw Flow Control signals balls
	DAC and ADC signals balls
	MISCELLANEOUS functions signals balls
	TELIT GPIO balls
	POWER SUPPLY VBATT balls
	POWER SUPPLY GND balls
	RESERVED

4 Hardware Commands

4.1 Turning ON the GE864-QUAD / PY

To turn on the GE864-QUAD / PY the pad ON# must be tied low for at least 1 second and then released.
The maximum current that can be drained from the ON# pad is 0,1 mA.
A simple circuit to do it is:



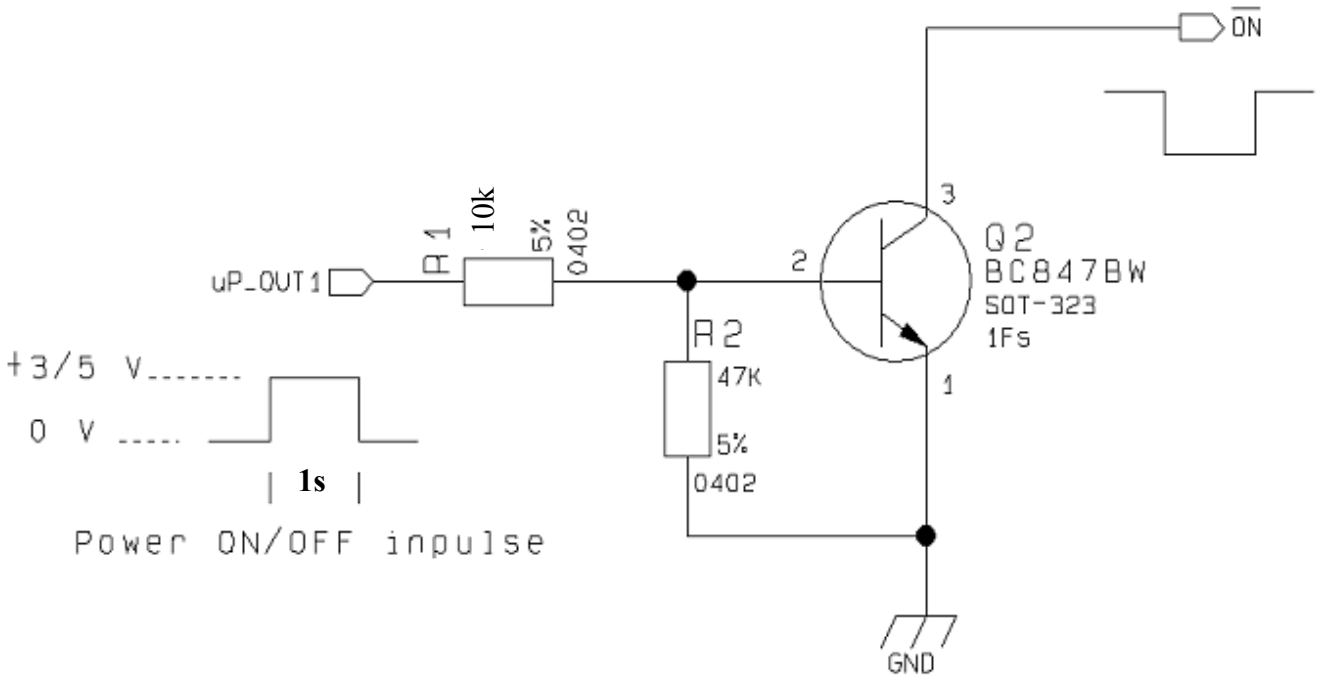
NOTE: don't use any pull up resistor on the ON# line, it is internally pulled up. Using pull up resistor may bring to latch up problems on the GE864-QUAD / PY power regulator and improper power on/off of the module. The line ON# must be connected only in open collector configuration.

NOTE: In this document all the lines that are inverted, hence have active low signals are labeled with a name that ends with a "#" or with a bar over the name.

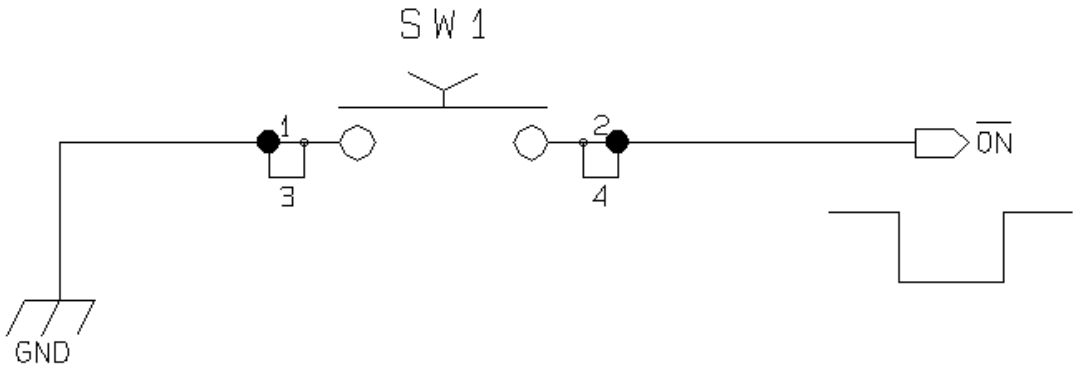
NOTE: The GE864-QUAD / PY turns fully on also by supplying power to the Charge pad (Module provided with a battery on the VBATT pads).

TIP: To check if the device has powered on, the hardware line PWRMON should be monitored. After 900ms the line raised up the device could be considered powered on.
PWRMON line rises up also when supplying power to the Charge pad

For example:
Let's assume you need to drive the ON# pad with a totem pole output of a +3/5 V micro controller (uP_OUT1):



Let's assume you need to drive the ON# pad directly with an ON/OFF button:



4.2 Turning OFF the GE864-QUAD / PY

The turning off of the device can be done in three ways:

- by software command (see GE864-QUAD / PY Software User Guide)
- by hardware shutdown
- by Hardware Unconditional Restart

When the device is shut down by software command or by hardware shutdown, it issues to the network a detach request that informs the network that the device will not be reachable any more.

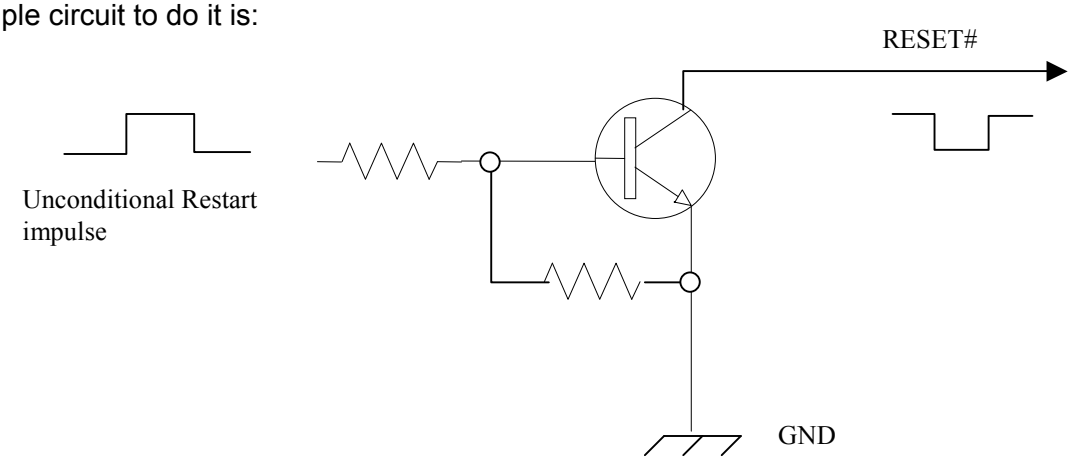
4.2.1 Hardware shutdown

To turn OFF the GE864-QUAD / PY the pad ON# must be tied low for at least 2 seconds and then released.
The same circuitry and timing for the power on shall be used.
The device shuts down after the release of the ON# pad.

TIP: To check if the device has powered off, the hardware line PWRMON should be monitored. When PWRMON goes low, the device has powered off.

4.2.2 Hardware Unconditional Restart

To unconditionally Restart the GE864-QUAD / PY, the pad RESET# must be tied low for at least 200 milliseconds and then released.
The maximum current that can be drained from the ON# pad is 0,15 mA.
A simple circuit to do it is:

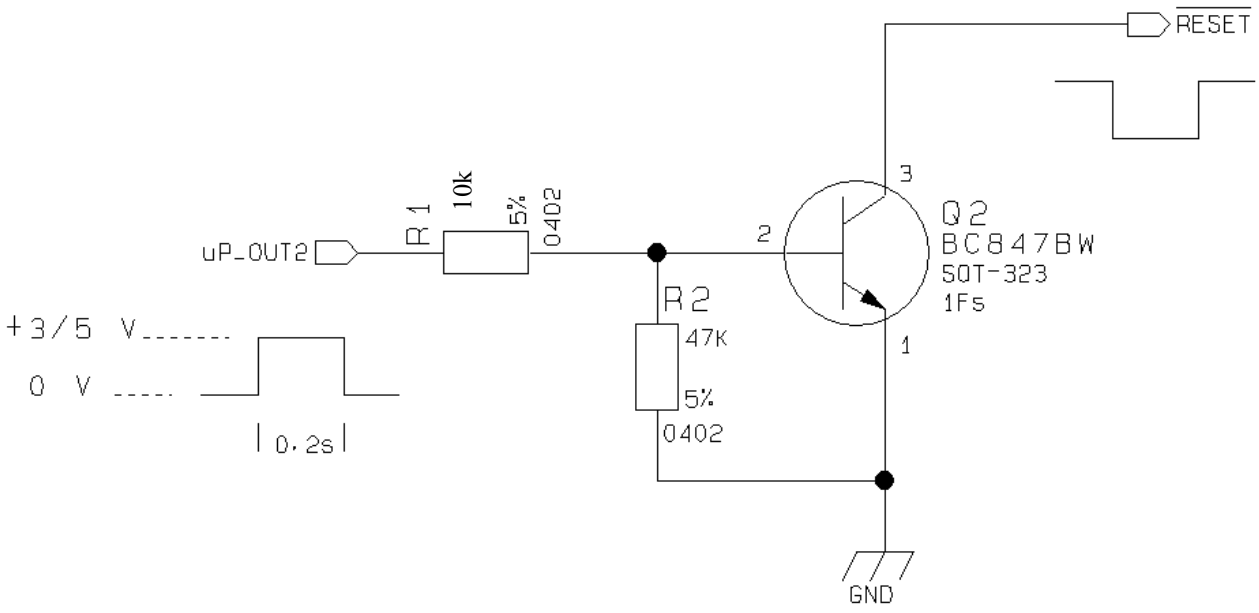


NOTE: don't use any pull up resistor on the RESET# line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the GE864-QUAD / PY power regulator and improper functioning of the module. The line RESET# must be connected only in open collector configuration.

TIP: The unconditional hardware Restart should be always implemented on the boards and software should use it as an emergency exit procedure.

For example:

Let's assume you need to drive the RESET# pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



This signal is internally pulled up so the pin can be left floating if not used.

5 Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

5.1 Power Supply Requirements

POWER SUPPLY	
Nominal Supply Voltage	3.8V
Max Supply Voltage	4.2
Supply Voltage Range	3.4 – 4.2

The GE864-QUAD / PY power consumptions are:

GE864-QUAD/PY		
Mode	**Average (mA)**	**Mode description**
IDLE mode		Stand by mode; no call in progress
AT+CFUN=1	23,9	Normal mode: full functionality of the module
AT+CFUN=4	22	Disabled TX and RX; module is not registered on the network
AT+CFUN=0 or AT+CFUN=5	7,20 / 3,56[3]	Power saving: CFUN=0 module registered on the network and can receive voice call or an SMS; but it is not possible to send AT commands; module wakes up with an unsolicited code (call or SMS) or rising RTS line. CFUN=5 full functionality with power saving; module registered on the network can receive incoming calls and SMS
RX mode		GSM Receiving data mode
1 slot in downlink	52,3	
2 slot in downlink	65,2	
3 slot in downlink	78,6	
4 slot in downlink	88,4	
GSM TX and RX mode		GSM Sending data mode
Min power level	78,1	
Max power level	200,1	
GPRS (class 10) TX and RX mode		GPRS Sending data mode
Min power level	123,7	
Max power level	370,8	

[1] Worst/best case depends on network configuration and is not under module control

The GSM system is made in a way that the RF transmission is not continuous, else it is packed into bursts at a base frequency of about 216 Hz, the relative current peaks can be as high as about 2A. Therefore the power supply has to be designed in order to withstand with these current peaks without big voltage drops; this means that both the electrical design and the board layout must be designed for this current flow.
If the layout of the PCB is not well designed a strong noise floor is generated on the ground and the supply; this will reflect on all the audio paths producing an audible annoying noise at 216 Hz; if the voltage drop during the peak current absorption is too much, then the device may even shutdown as a consequence of the supply voltage drop.

TIP: The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 2 A.

5.2 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

5.2.1 Electrical Design Guidelines

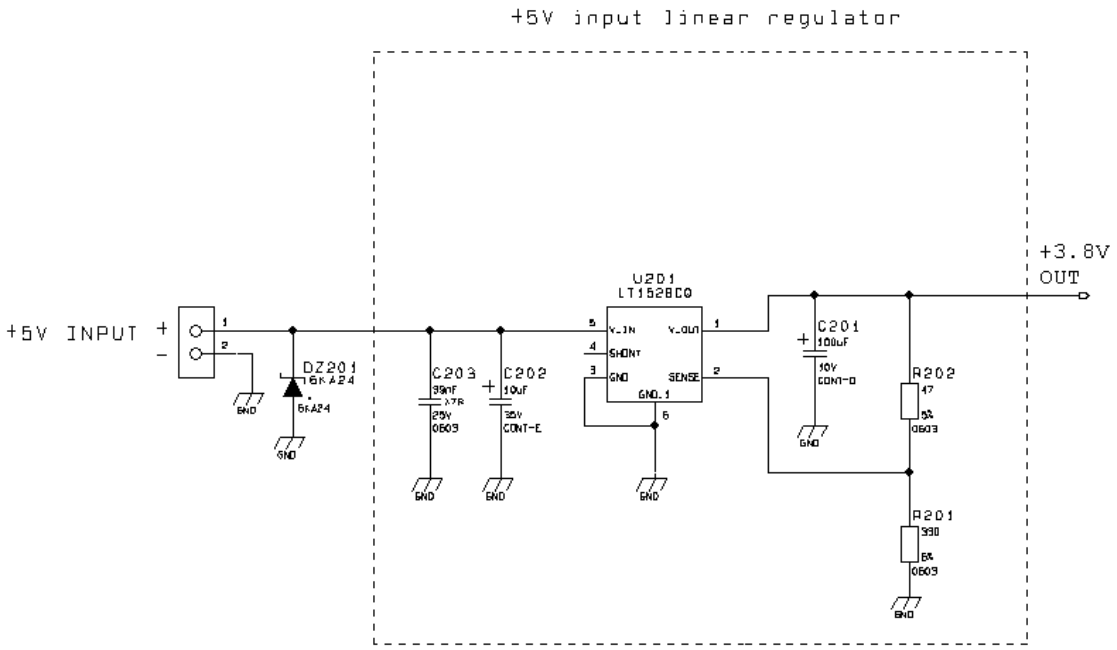
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.2.1.1 + 5V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the GE864-QUAD / PY, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GE864-QUAD / PY from power polarity inversion.

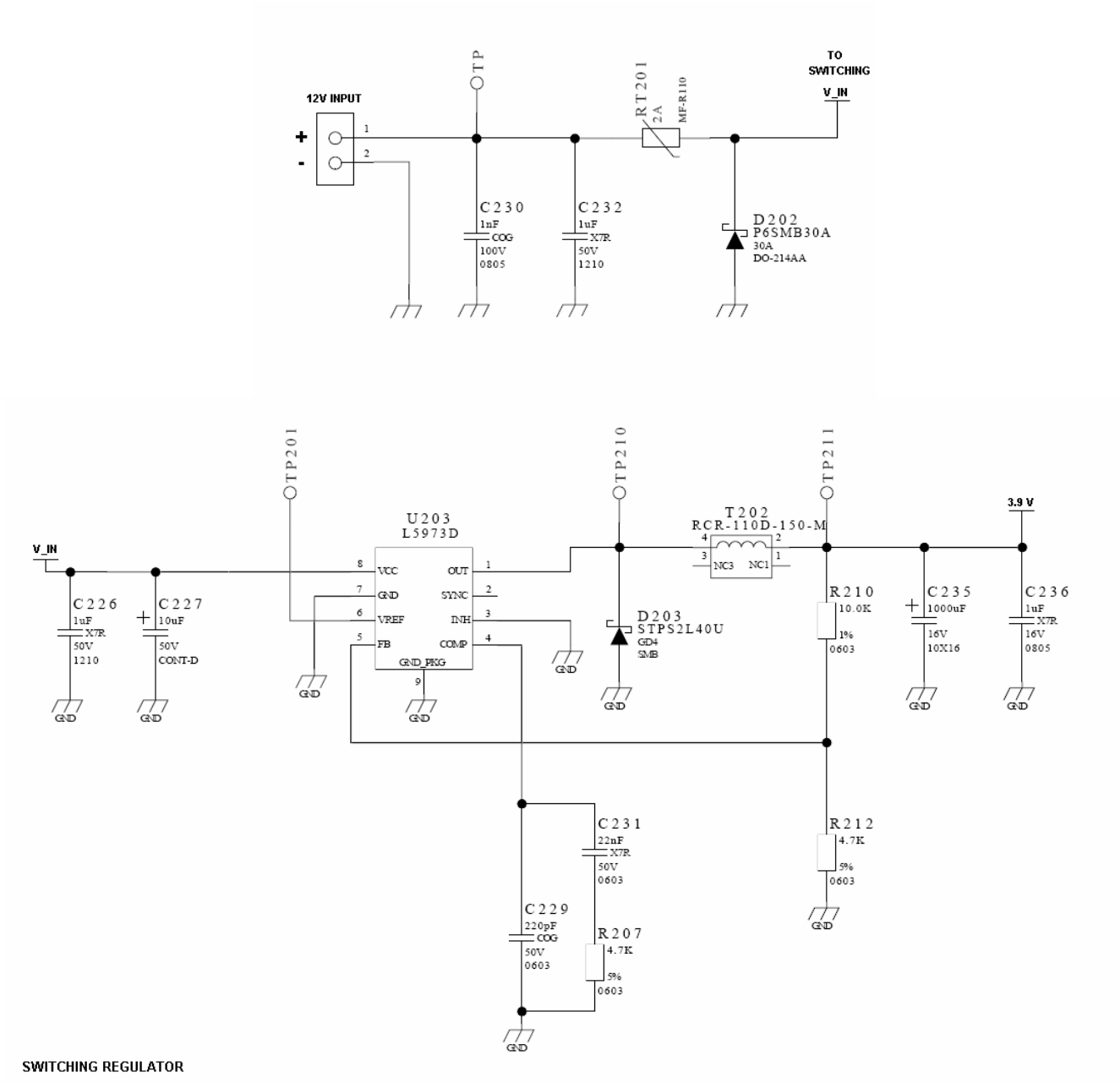
An example of linear regulator with 5V input is:



5.2.1.2 + 12V input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V; hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency especially with the 2A peak current load represented by the GE864-QUAD/PY.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the GE864-QUAD/PY from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic (it is split in 2 parts):



SWITCHING REGULATOR

5.2.1.3 Battery Source Power Supply Design Guidelines

- The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit GE864-QUAD/PY module.

  The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the GE864-QUAD/PY and damage it.

NOTE: DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with GE864-QUAD/PY. Their use can lead to overvoltage on the GE864-QUAD/PY and damage it. USE ONLY Li-Ion battery types.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the GE864-QUAD/PY from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

5.2.1.4 Battery Charge control Circuitry Design Guidelines

The charging process for Li-Ion Batteries can be divided into 4 phases:

- Qualification and trickle charging
- Fast charge 1 – constant current
- Final charge – constant voltage or pulsed charging
- Maintenance charge

The qualification process consists in a battery voltage measure, indicating roughly its charge status. If the battery is deeply discharged, that means its voltage is lower than the trickle charging threshold, then the charge must start slowly possibly with a current limited pre-charging process where the current is kept very low with respect to the fast charge value: the trickle charging.
During the trickle charging the voltage across the battery terminals rises; when it reaches the fast charge threshold level the charging process goes into fast charge phase.
During the fast charge phase the process proceeds with a current limited charging; this current limit depends on the required time for the complete charge and from the battery pack capacity. During this phase the voltage across the battery terminals still raises but at a lower rate.
Once the battery voltage reaches its maximum voltage then the process goes into its third state: Final charging. The voltage measure to change the process status into final charge is very important. It must be ensured that the maximum battery voltage is never exceeded, otherwise the battery may be damaged and even explode. Moreover for the constant voltage final chargers, the constant voltage phase (final charge) must not start before the battery voltage has reached its maximum value, otherwise the battery capacity will be highly reduced.
The final charge can be of two different types: constant voltage or pulsed. GE864-QUAD/PY uses constant voltage.
The constant voltage charge proceeds with a fixed voltage regulator (very accurately set to the maximum battery voltage) and hence the current will decrease while the battery is becoming charged. When the charging current falls below a certain fraction of the fast charge current value, then the battery is considered fully charged, the final charge stops and eventually starts the maintenance.
The pulsed charge process has no voltage regulation, instead the charge continues with pulses. Usually the pulse charge works in the following manner: the charge is stopped for some time, let's say few hundreds of ms, then the battery voltage will be measured and when it drops below its maximum value a fixed time length charging pulse is issued. As the battery approaches its full charge the off time will become longer, hence the duty-cycle of the pulses will decrease. The battery is considered fully charged when the pulse duty-cycle is less than a threshold value, typically 10%, the pulse charge stops and eventually the maintenance starts.
The last phase is not properly a charging phase, since the battery at this point is fully charged and the process may stop after the final charge. The maintenance charge provides an additional charging process to compensate for the charge leak typical of a Li-Ion battery. It is done by issuing pulses with a fixed time length, again few hundreds of ms, and a duty-cycle around 5% or less.
This last phase is not implemented in the GE864-QUAD/PY internal charging algorithm, so that the battery once charged is left discharging down to a certain threshold so that it is cycled from full charge to slight discharge even if the battery charger is always inserted. This guarantees that anyway the remaining charge in the battery is a good percentage and that the battery is not damaged by keeping it always fully charged (Li-Ion rechargeable battery usually deteriorate when kept fully charged).

Last but not least, in some applications it is highly desired that the charging process restarts when the battery is discharged and its voltage drops below a certain threshold, GE864-QUAD/PY internal charger does it.

As you can see, the charging process is not a trivial task to be done; moreover all these operations should start only if battery temperature is inside a charging range, usually 5°C – 45°C.
The GE864-QUAD/PY measures the temperature of its internal component, in order to satisfy this last requirement, it's not exactly the same as the battery temperature but in common application the two temperature should not differ too much and the charging temperature range should be guaranteed.

NOTE: For all the threshold voltages, inside the GE864-QUAD/PY all thresholds are fixed in order to maximize Li-Ion battery performances and do not need to be changed.

NOTE: In this application the battery charger input current must be limited to less than 400mA. This can be done by using a current limited wall adapter as the power source.

NOTE: When starting the charger from Module powered off the startup will be in CFUN4; to activate the normal mode a command AT+CFUN=1 has to be provided. This is also possible using the POWER ON.
There is also the possibility to activate the normal mode using the ON_OFF* signal.
In this case, when HW powering off the module with the same line (ON_OFF*) and having the charger still connected, the module will go back to CFUN4.

NOTE: It is important having a 100uF Capacitor to VBAT in order to avoid instability of the charger circuit if the battery is accidentally disconnected during the charging activity.

5.2.2 Thermal Design Guidelines

The thermal design for the power supply heat sink should be done with the following specifications:

- *Average current consumption during transmission @PWR level max:* *500mA*
- *Average current consumption during transmission @ PWR level min:* *100mA*
- *Average current during Power Saving (CFUN=5):* *4mA*
- *Average current during idle (Power Saving disabled)* *24mA*

NOTE: The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.
If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 500mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 500mA, being usually around 150mA.
For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.
For the heat generated by the GE864-QUAD / PY, you can consider it to be during transmission 1W max during CSD/VOICE calls and 2W max during class10 GPRS upload.
This generated heat will be mostly conducted to the ground plane under the GE864-QUAD / PY; you must ensure that your application can dissipate it.

5.2.3 Power Supply PCB layout Guidelines

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit GE864-QUAD / PY power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the GE864-QUAD / PY is wide enough to ensure a dropless connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 2A current peaks are absorbed. Note that this is not made in order to save power loss but especially to avoid the voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to that supply, introducing the noise floor at the burst base frequency. For this reason while a voltage drop of 300-400 mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If your application doesn't have audio interface but only uses the data feature of the Telit GE864-QUAD / PY, then this noise is not so disturbing and power supply layout design can be more forgiving.
- The PCB traces to the GE864-QUAD / PY and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 2A current peaks are absorbed. This is for the same reason as previous point. Try to keep this trace as short as possible.
- The PCB traces connecting the Switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.

6 Antenna

The antenna connection and board layout design are the most important part in the full product design and they strongly reflect on the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.

6.1 GSM Antenna Requirements

As suggested on the Product Description the antenna and antenna line on PCB for a Telit GE864-QUAD / PY device shall fulfill the following requirements:

ANTENNA REQUIREMENTS	
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	70 MHz in GSM850, 80 MHz in GSM900, 170 MHz in DCS & 140 MHz PCS band
Gain	Gain < 3dBi
Impedance	50 ohm
Input power	> 2 W peak power
VSWR absolute max	<= 10:1
VSWR recommended	<= 2:1

When using the Telit GE864-QUAD / PY, since there's no antenna connector on the module, the antenna must be connected to the GE864-QUAD / PY through the PCB with the antenna pad.

In the case that the antenna is not directly developed on the same PCB, hence directly connected at the antenna pad of the GE864-QUAD / PY, then a PCB line is needed in order to connect with it or with its connector.

This line of transmission shall fulfill the following requirements:

ANTENNA LINE ON PCB REQUIREMENTS	
Impedance	50 ohm
Max Attenuation	0,3 dB
No coupling with other signals allowed	
Cold End (Ground Plane) of antenna shall be equipotential to the GE864-QUAD / PY ground pins	

Furthermore if the device is developed for the US market and/or Canada market, it shall comply to the FCC and/or IC approval requirements:
This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the GE864-QUAD / PY module. Antennas used for this OEM module must not exceed 3dBi gain for mobile and fixed operating configurations.

6.2 GSM Antenna – PCB line Guidelines

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias once per 2mm at least;
- Place EM noisy devices as far as possible from GE864-QUAD / PY antenna line;
- Keep the antenna line far away from the GE864-QUAD / PY power supply lines;
- If you have EM noisy devices around the PCB hosting the GE864-QUAD / PY, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you don't have EM noisy devices around the PCB of GE864-QUAD / PY, by using a strip-line on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

6.3 GSM Antenna – Installation Guidelines

- Install the antenna in a place covered by the GSM signal.
- The Antenna must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter;
- Antenna shall not be installed inside metal cases
- Antenna shall be installed also according Antenna manufacturer instructions.

7 Logic level specifications

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels. The following table shows the logic level specifications used in the **Telit GE864-QUAD / PY** interface circuits:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1.8V signals:

Operating Range – Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.6V	3.3V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

Current characteristics

Level	Typical
Output Current	1mA
Input Current	1uA

7.1 Reset signal

Signal	Function	I/O	Bga Ball
RESET	Phone reset	I	A2

RESET is used to reset the **GE864-QUAD / PY modules**. Whenever this signal is pulled low, the GE864-QUAD / PY is reset. When the device is reset it stops any operation. After the release of the reset GE864-QUAD / PY is unconditionally shut down, without doing any detach operation from the network where it is registered. This behaviour is not a proper shut down because any GSM device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.
The RESET is internally controlled on start-up to achieve always a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

***NOTE**: do not use this signal to power off the **GE864-QUAD / PY**. Use the ON/OFF signal to perform this function or the AT#SHDN command.*

Reset Signal Operating levels:

Signal	Min	Max
RESET Input high	2.0V*	2.2V
RESET Input low	0V	0.2V

this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it **must always be connected with an open collector transistor**, to permit to the internal circuitry the power on reset and under voltage lockout functions.

8 Serial Ports

The serial port on the Telit GE864-QUAD/PY is the core of the interface between the module and OEM hardware.
2 serial ports are available on the module:

- MODEM SERIAL PORT
- MODEM SERIAL PORT 2 (DEBUG)

8.1 MODEM SERIAL PORT

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- Micro controller UART @ 2.8V – 3V (Universal Asynchronous Receive Transmit)
- Micro controller UART@ 5V or other voltages different from 2.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work. The only configuration that doesn't need a level translation is the 2.8V UART.
The serial port on the GE864-QUAD/PY is a +2.8V UART with all the 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. The levels for the GE864-QUAD/PY UART are the CMOS levels:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pad when on	-0.3V	+3.6V
Input voltage on analog pads when on	-0.3V	+3.0 V

Operating Range – Interface levels (2.8V CMOS)

Level		Min	Max
Input high level	V_{IH}	2.1V	3.3V
Input low level	V_{IL}	0V	0.5V
Output high level	V_{OH}	2.2V	3.0V
Output low level	V_{OL}	0V	0.35V

The signals of the GE864 serial port are:

RS232 Pin Number	Signal	GE864-QUAD / PY Pad Number	Name	Usage
1	DCD – dcd_uart	D9	Data Carrier Detect	Output from the GE864-QUAD / PY that indicates the carrier presence
2	RXD – tx_uart	H8	Transmit line *see Note	Output transmit line of GE864-QUAD / PY UART
3	TXD – rx_uart	E7	Receive line *see Note	Input receive of the GE864-QUAD / PY UART
4	DTR – dtr_uart	B7	Data Terminal Ready	Input to the GE864-QUAD / PY that controls the DTE READY condition
5	GND	A1,F1,H1,L1 , H2, L2, J3, K3….	Ground	ground
6	DSR – dsr_uart	E11	Data Set Ready	Output from the GE864-QUAD / PY that indicates the module is ready
7	RTS – rts_uart	F7	Request to Send	Input to the GE864-QUAD / PY that controls the Hardware flow control
8	CTS – cts_uart	F6	Clear to Send	Output from the GE864-QUAD / PY that controls the Hardware flow control
9	RI – ri_uart	B6	Ring Indicator	Output from the GE864-QUAD / PY that indicates the incoming call condition

NOTE: According to V.24, RX/TX signal names are referred to the application side, therefore on the GE864 side these signal are on the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx_uart) of the GE864 serial port and viceversa for RX.

TIP: For a minimum implementation, only the TXD and RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

TIP: In order to avoid noise or interferences on the RXD lines it is suggested to add a pull up resistor (100Kohm to 2.8V)

8.2 RS232 level translation

In order to interface the Telit GE864 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must

- invert the electrical signal in both directions
- change the level from 0/3V to +15/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562) , allowing for a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of driver and receiver and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-3V UART level to the RS232 level, while the receiver is the translator from RS232 level to 0-3V UART.

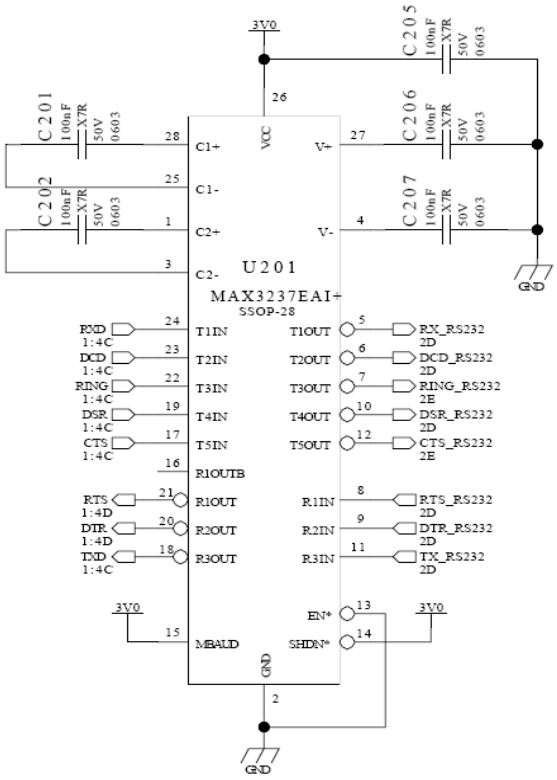
In order to translate the whole set of control lines of the UART you will need:

- 5 driver
- 3 receiver

NOTE: The digital input lines working at 2.8VCMOS have an absolute maximum input voltage of 3,75V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead it shall be powered from a +2.8V / +3.0V (dedicated) power supply.
This is because in this way the level translator IC outputs on the module side (i.e. GE864 inputs) will work at +3.8V interface levels, stressing the module inputs at its maximum input voltage.
This can be acceptable for evaluation purposes, but not on production devices.

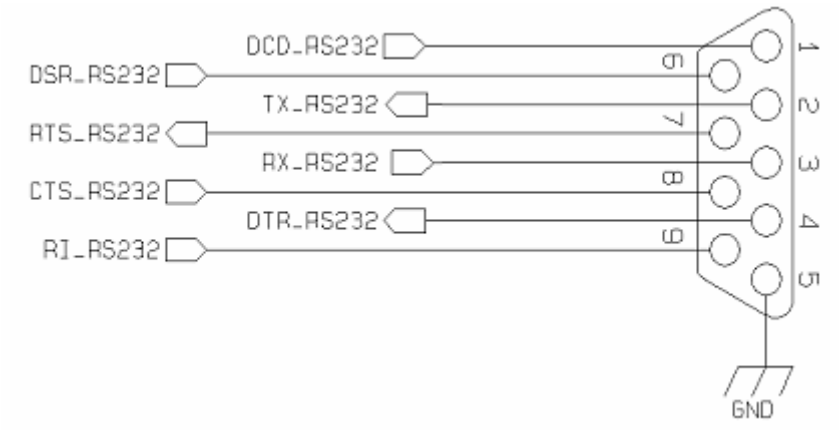
NOTE: In order to be able to do in circuit reprogramming of the GE864 firmware, the serial port on the Telit GE864 shall be available for translation into RS232 and either it's controlling device shall be placed into tristate, disconnected or as a gateway for the serial data when module reprogramming occurs.
Only RXD, TXD, GND and the On/off module turn on pad are required to the reprogramming of the module, the other lines are unused.
All applicator shall include in their design such a way of reprogramming the GE864.

An example of level translation circuitry of this kind is:



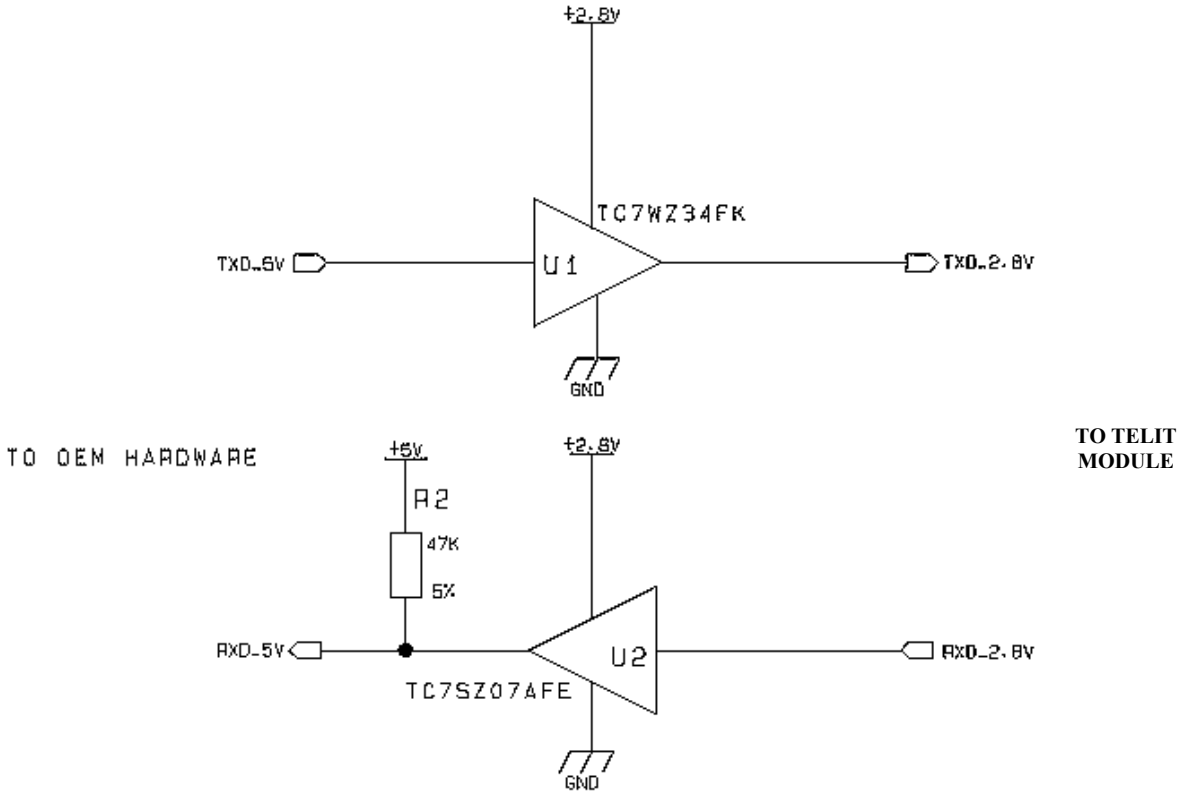
RS232 LEVEL TRSANSLATOR

The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



8.3 5V UART level translation

If the OEM application uses a microcontroller with a serial port (UART) that works at a voltage different from 2.8 – 3V, then a circuitry has to be provided to adapt the different levels of the two sets of signals. As for the RS232 translation there are a multitude of single chip translators. For example a possible translator circuit for a 5V TRANSMITTER/RECEIVER can be:



TIP: This logic IC for the level translator and 2.8V pull-ups (not the 5V one) can be powered directly from VAUX line of the GE864-QUAD / PY. Note that the TC7SZ07AE has open drain output; therefore the resistor R2 is mandatory.

NOTE: The UART input line TXD (rx_uart) of the GE864-QUAD / PY is NOT internally pulled up with a resistor, so there may be the need to place an external 47KΩ pull-up resistor, either the DTR (dtr_uart) and RTS (rts_uart) input lines are not pulled up internally, so an external pull-up resistor of 47KΩ may be required.

A power source of the internal interface voltage corresponding to the 2.8VCMOS high level is available at the VAUX pin on the connector,
A maximum of 9 resistors of 47 KΩ pull-up can be connected to the PWRMON pin, provided no other devices are connected to it and the pulled-up lines are GE864-QUAD / PY input lines connected to open collector outputs in order to avoid latch-up problems on the GE864-QUAD / PY.
Care must be taken to avoid latch-up on the GE864-QUAD / PY and the use of this output line to power electronic devices shall be avoided, especially for devices that generate spikes and noise such as switching level translators, micro controllers, failure in any of these condition can severely compromise the GE864-QUAD / PY functionality.

NOTE: The input lines working at 2.8VCMOS can be pulled-up with 47KΩ resistors that can be connected directly to the VAUX line provided they are connected as in this example.

In case of reprogramming of the module has to be considered the use of the RESET line to start correctly the activity.

The preferable configuration is having an external supply for the buffer.

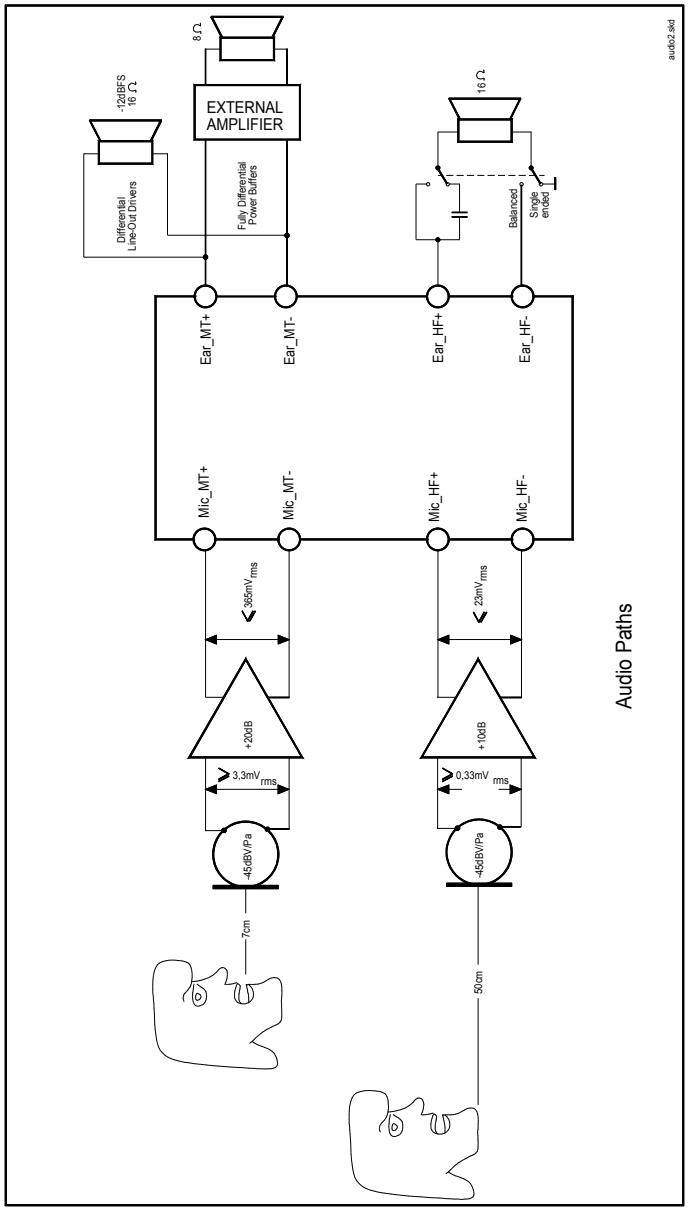
9 Audio Section Overview

The Base Band Chip of the GE864-QUAD / PY Telit Module provides two different audio blocks; both in transmit (*Uplink*) and in receive (*Downlink*) direction:

"*MT lines*" should be used for handset function,

"*HF lines*" is suited for hands –free function (car kit).

These two blocks can be active only one at a time, selectable by *AXE* hardware line or by AT command. The audio characteristics are equivalent in transmit blocks, but are different in the receive ones and this should be kept in mind when designing.



9.1 INPUT LINES (Microphone)

9.1.1 Short description

The Telit GE864-QUAD / PY provides two audio paths in transmit section. Only one of the two paths can be active at a time, selectable by *AXE* hardware line or by AT command.

You must keep in mind the different audio characteristics of the transmit blocks when designing:

The *"**MIC_MT**"* audio path should be used for handset function, while the "***MIC_HF**"* audio path is suited for hands-free function (car kit).

TIP: being the microphone circuitry the more noise sensitive, its design and layout must be done with particular care. Both microphone paths are balanced and the OEM circuitry should be balanced designed to reduce the common mode noise typically generated on the ground plane. However also an unbalanced circuitry can be used for particular OEM application needs.

TIP: due to the difference in the echo canceller type, the "Mic_MT" audio path is suited for Handset applications, while the "Mic_HF"audio path is suited for hands-free function (car kit). The Earphone applications should be made using the "Mic_HF" audio path but DISABLING the echo canceller by software AT command. If the echo canceller is left active with the Earphone, then some echo might be introduced by the echo cancel algorithm.

9.1.2 Input Lines Characteristics

"MIC_MT" 1st differential microphone path	
Line Coupling	AC*
Line Type	Balanced
Coupling capacitor	≥ 100nF
Differential input resistance	50kΩ
Differential input voltage	≤ 1,03V_{pp} (365mV_{rms})
Microphone nominal sensitivity	-45 dBV_{rms}/Pa
Analog gain suggested	+ 20dB
Echo canceller type	Handset

"MIC_HF" 2nd differential microphone path	
Line Coupling	AC*
Line Type	Balanced
Coupling capacitor	≥ 100nF
Differential input resistance	50kΩ
Differential input voltage	≤ 65mV_{pp} (23mV_{rms})
Microphone nominal sensitivity	-45 dBV_{rms}/Pa
Analog gain suggested	+10dB
Echo canceller type	Car kit hands-free

(*) WARNING: AC means that the signals from microphone has to be connected to input lines of the module by a *CAPACITOR*, which value must be ≥ 100nF. Not respecting this constraint, the input stage will be damaged.

9.2 OUTPUT LINES (Speaker)

9.2.1 Short description

The Telit GE864-QUAD / PY provides two audio paths in receive section. Only one of the two paths can be active at a time, selectable by *AXE* hardware line or by AT command.

You must keep in mind the different audio characteristics of the receive blocks when designing:

→ the *"**EAR_MT**"* lines *EPN1* and *EPP1* are the *Differential Line-Out Drivers* ; they can drive an external amplifier or directly a ***16 Ω earpiece*** at –12dBFS (*) ;
→ the "***EAR_HF***" lines *EPPA1_2* and *EPPA2* are the *Fully Differential Power Buffers ;* they can directly drive a *16**Ω** speaker* in differential (*balanced*) or single ended (*unbalanced*) operation mode .

(*) *FS* : acronym of *Full Scale.* It is equal to 0dB, the maximum Hardware Analog Receive Gain of BaseBand Chip.

The *"**EAR_MT**"* audio path should be used for handset function, while the "***EAR_HF***" audio path is suited for hands-free function (car kit).

Both receiver outputs are B.T.L. type (Bridged Tie Load) and the OEM circuitry shall be designed bridged to reduce the common mode noise typically generated on the ground plane and to get the maximum power output from the device; however also a single ended circuitry can be designed for particular OEM application needs.

9.2.2 Output Lines Characteristics

"EAR_MT" Differential Line-out Drivers Path	
Line Coupling	DC
Line Type	Bridged
Output load resistance	≥ 14 Ω
Internal output resistance	4 Ω (typical)
Signal bandwidth	150 – 4000 Hz @ -3 dB
Differential output voltage	328mVrms /16 Ω @ -12dBFS
SW volume level step	- 2 dB
Number of SW volume steps	10

"EAR_HF" Power Buffers Path	
Line Coupling	DC
Line Type	Bridged
Output load resistance	≥ 14 Ω
Internal output resistance	4 Ω (>1,7 Ω)
Signal bandwidth	150 – 4000 Hz @ -3 dB
Max Differential output voltage	1310 mV_{rms} (typ, open circuit)
Max Single Ended output voltage	656 mV_{rms} (typ, open circuit)
SW volume level step	- 2 dB
Number of SW volume steps	10

For more detailed information about audio please refer to the Audio Settings Application Note 80000NT10007a.

9.3 External SIM Holder Implementation

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a)

10 General Purpose I/O

The general purpose I/O pads can be configured to act in three different ways:

- input
- output
- alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time; output pads can only be written or queried and set the value of the pad output; an alternate function pad is internally controlled by the GE864-QUAD / PY firmware and acts depending on the function implemented. For Logic levels please refer to chapter 7.

The following GPIO are available on the GE864-QUAD and GE864-PY:

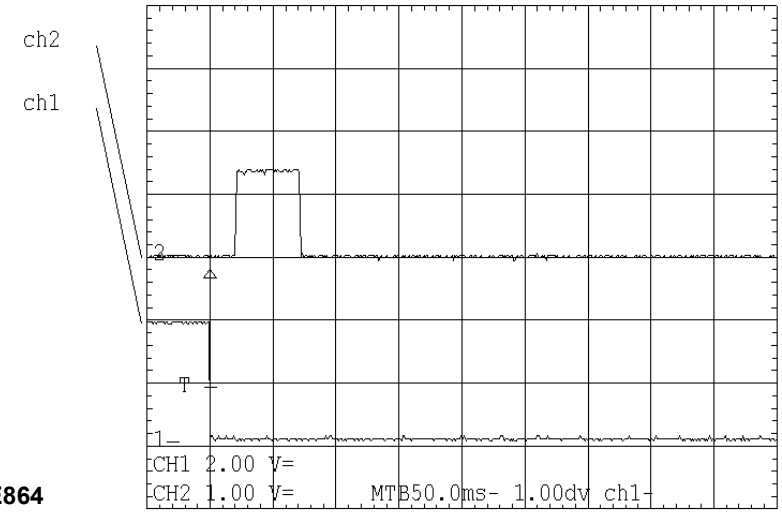
Ball	Signal	I/O	Function	Type	Input / output current	Default State	ON_OFF state	State during Reset	Note
C1	TGPIO_01	I/O	GPIO01 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
E6	TGPIO_02	I/O	GPIO02 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (JDR)
C2	TGPIO_03	I/O	GPIO03 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B3	TGPIO_04	I/O	GPIO04 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RF Transmission Control)
K8	TGPIO_05	I/O	GPIO05 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (RFTXMON)
B5	TGPIO_06	I/O	GPIO06 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	Pict 01	1	Alternate function (ALARM)
L9	TGPIO_07	I/O	GPIO07 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		Alternate function (BUZZER)
K11	TGPIO_08	I/O	GPIO08 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
C9	TGPIO_09	I/O	GPIO09 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H3	TGPIO_10	I/O	GPIO10 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
D1	TGPIO_11	I/O	GPIO11 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
G4	TGPIO_12	I/O	GPIO12 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
K10	TGPIO_13	I/O	GPIO13 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B4	TGPIO_14	I/O	GPIO14 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
F5	TGPIO_15	I/O	GPIO15 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H6	TGPIO_16	I/O	GPIO16 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
H5	TGPIO_17	I/O	GPIO17 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
K7	TGPIO_18	I/O	GPIO18 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
B1	TGPIO_19	I/O	GPIO19 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
C3	TGPIO_20	I/O	GPIO20 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	0		
L10	TGPIO_21	I/O	GPIO21 Configurable GPIO	CMOS 2.8V	1uA / 1mA	INPUT	1		
E8	TGPIO_22	I/O	GPIO22 Configurable GPIO	**CMOS 1.8V (not 2.8V !!)**	1uA / 1mA	INPUT	0		

Not all GPIO pads support all these three modes:

- GPIO2 supports all three modes and can be input, output, Jamming Detect Output (Alternate function)
- GPIO4 supports all three modes and can be input, output, RF Transmission Control (Alternate function)
- GPIO5 supports all three modes and can be input, output, RFTX monitor output (Alternate function)
- GPIO6 supports all three modes and can be input, output, alarm output (Alternate function)
- GPIO7 supports all three modes and can be input, output, buzzer output (Alternate function)

pict01

ch1: ON_OFF (2sec)
ch2: GPIO 06 [bis]



GE864

10.1 GPIO Logic levels

Where not specifically stated, all the interface circuits work at 2.8V CMOS logic levels.
The following table shows the logic level specifications used in the **GE864-QUAD/PY** interface circuits:

Absolute Maximum Ratings –Not Functional

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.0 V

Operating Range – Interface levels (2.8V CMOS)

Level	Min	Max
Input high level	2.1V	3.3V
Input low level	0V	0.5V
Output high level	2.2V	3.0V
Output low level	0V	0.35V

For 1.8V signals:

Operating Range – Interface levels (1.8V CMOS)

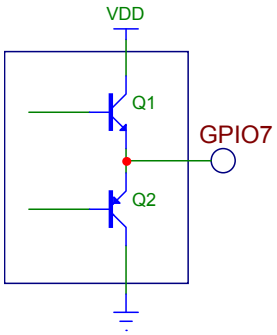
Level	Min	Max
Input high level	1.6V	3.3V
Input low level	0V	0.4V
Output high level	1,65V	2.2V
Output low level	0V	0.35V

10.2 Using a GPIO Pad as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 2.8V CMOS levels of the GPIO.
If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 2.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 2.8V.

10.3 Using a GPIO Pad as OUTPUT

The GPIO pads, when used as outputs, can drive 2.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.



Base circuit of a push-pull stage

10.4 Using the RF Transmission Control GPIO4

The GPIO4 pin, when configured as RF Transmission Control Input, permits to disable the Transmitter when the GPIO is set to Low by the application.
In the design is necessary to add a pull up resistor (47K to PWRMON).

10.5 Using the RFTXMON Output GPIO5

The GPIO5 pin, when configured as RFTXMON Output, is controlled by the GE864-QUAD / PY module and will rise when the transmitter is active and fall after the transmitter activity is completed.
For example, if a call is started, the line will be HIGH during all the conversation and it will be again LOW after hanged up.

The line rises up 300ms before first TX burst and will became again LOW from 500ms to 1sec after last TX burst.

10.6 Using the Alarm Output GPIO6

The GPIO6 pad, when configured as Alarm Output, is controlled by the GE864-QUAD / PY module and will rise when the alarm starts and fall after the issue of a dedicated AT command.
This output can be used to power up the GE864-QUAD / PY controlling micro controller or application at the alarm time, giving you the possibility to program a timely system wake-up to achieve some periodic actions and completely turn off either the application and the GE864-QUAD / PY during sleep periods, dramatically reducing the sleep consumption to few µA.
In battery-powered devices this feature will greatly improve the autonomy of the device.

NOTE: During RESET the line is set to HIGH logic level.

10.7 Using the Buzzer Output GPIO7

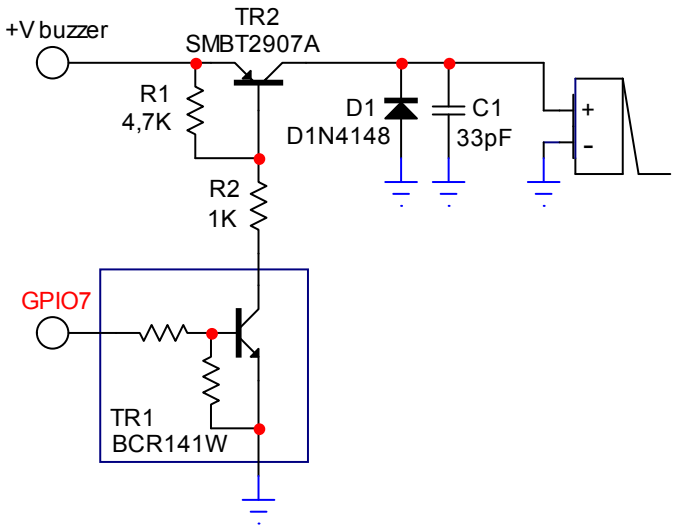
As *Alternate Function*, the GPIO7 is controlled by the firmware that depends on the function implemented internally.
This setup places always the GPIO7 pin in *OUTPUT* direction and the corresponding function must be activated properly by ***AT#SRP*** command (refer to *AT commands specification*).

Also in this case, the *dummy value* for the pin state can be both "***0***" or "***1***".

Send the command	AT#GPIO=7, 1, **2**<cr>:
Wait for response	OK
Send the command	AT#SRP=3

The GPIO7 pin will be set as *Alternate Function* pin with its dummy logic status set to *HIGH* value.

The "*Alternate function*" permits your application to easily implement ***Buzzer feature*** with some small hardware extension of your application as shown in the next sample figure.



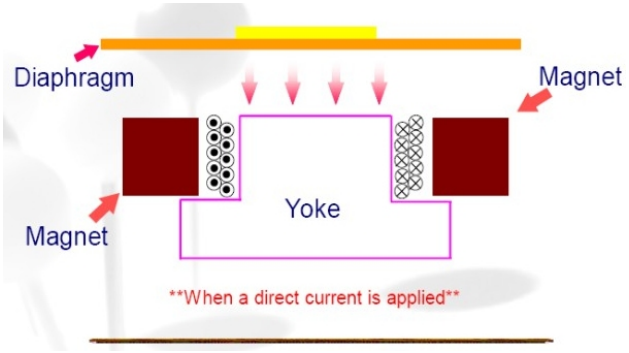
Example of Buzzer's driving circuit.

NOTE: To correctly drive a buzzer, a driver must be provided; its characteristics depend on the Buzzer and for them refer to your buzzer vendor.

10.8 Magnetic Buzzer Concepts

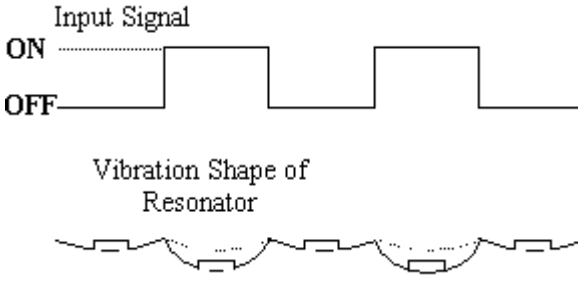
10.8.1 Short Description

A magnetic Buzzer is a sound-generating device with a coil located in the magnetic circuit consisting of a permanent magnet, an iron core, a high permeable metal disk, and a vibrating diaphragm.



Drawing of the Magnetic Buzzer

The disk and diaphragm are attracted to the core by the magnetic field. When an oscillating signal is moved through the coil, it produces a fluctuating magnetic field, which vibrates the diaphragm at a frequency of the drive signal. Thus the sound is produced relative to the frequency applied.



Diaphragm movement

10.8.2 Frequency Behaviour

The frequency behavior represents the effectiveness of the reproduction of the applied signals. Because its performance is related to a square driving waveform (whose amplitude varies from 0V to Vpp), if you modify the waveform (e.g. from square to sinus) the frequency response will change.

10.8.3 Power Supply Influence

Applying a signal whose amplitude is different from that suggested by manufacturer, the performance change following the rule "*if resonance frequency* f_o *increases, amplitude decreases*".

Because of resonance frequency depends from acoustic design, lowering the amplitude of the driving signal the response bandwidth tends to become narrow, and vice versa.

Summarizing: $Vpp \uparrow \rightarrow f_o \downarrow$ $Vpp \downarrow \rightarrow f_o \uparrow$

The risk is that the f_o could easily fall outside of new bandwidth; consequently the SPL could be much lower than the expected.

10.8.4 Warning

It is very important to respect the sense of the applied voltage: never apply to the *"-" pin* a voltage more positive than *"+" pin* : if this happens, the diaphragm vibrates in the opposite sense with a high probability to be expelled from its physical position , damaging the device forever .

10.8.5 Working Current Influence

In the component data sheet you will find the value of MAX CURRENT : this represents the maximum average current that can flow at nominal voltage without current limitation .
In other words it is not the peak current, which could be twice or three times higher.
If driving circuitry does not support these peak values , the SPL will never reach the declared level or the oscillations will stop.

10.9 Using the Temperature Monitor Function

10.9.1 Short Description

The Temperature Monitor is a function of the module that permits to control its internal temperature and if properly set (see the #TEMPMON command on AT Interface guide) it raise to High Logic level a GPIO when the maximum temperature is reached.

10.9.2 Allowed GPIO

The AT#TEMPMON set command could be used with one of the following GPIO:

Ball	Signal	Function	Type	Input / output current	Note
C1	TGPIO_01	GPIO01 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
C2	TGPIO_03	GPIO03 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
K11	TGPIO_08	GPIO08 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
C9	TGPIO_09	GPIO09 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
H3	TGPIO_10	GPIO10 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
D1	TGPIO_11	GPIO11 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
G4	TGPIO_12	GPIO12 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
K10	TGPIO_13	GPIO13 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
B4	TGPIO_14	GPIO14 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
F5	TGPIO_15	GPIO15 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
H6	TGPIO_16	GPIO16 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
H5	TGPIO_17	GPIO17 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
K7	TGPIO_18	GPIO18 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
B1	TGPIO_19	GPIO19 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
C3	TGPIO_20	GPIO20 Configurable GPIO	CMOS 2.8V	1uA / 1mA	
E8	TGPIO_22	GPIO22 Configurable GPIO	**CMOS 1.8V (not 2.8V !!)**	1uA / 1mA	

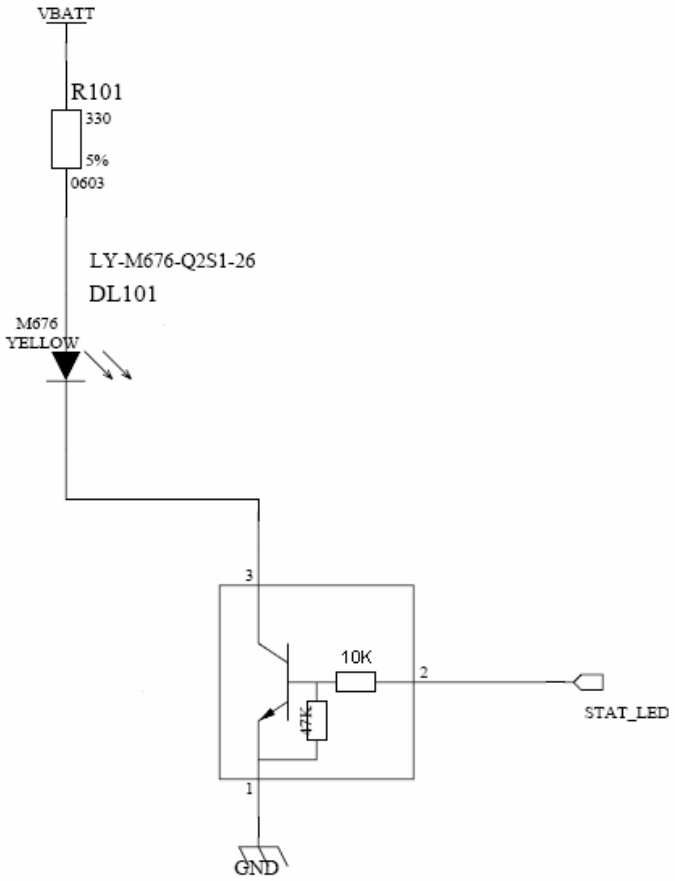
The set command could be used also with one of the following GPIO but in that case the alternate function is not usable:

Ball	Signal	Function	Type	Input / output current	Note
E6	TGPIO_02	GPIO02 Configurable GPIO	CMOS 2.8V	1uA / 1mA	Alternate function (JDR)
B3	TGPIO_04	GPIO04 Configurable GPIO	CMOS 2.8V	1uA / 1mA	Alternate function (RF Transmission Control)
K8	TGPIO_05	GPIO05 Configurable GPIO	CMOS 2.8V	1uA / 1mA	Alternate function (RFTXMON)
L9	TGPIO_07	GPIO07 Configurable GPIO	CMOS 2.8V	1uA / 1mA	Alternate function (BUZZER)

10.10 Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status.
In the GE864 modules, the STAT_LED usually needs an external transistor to drive an external LED.
Therefore, the status indicated in the following table is reversed with respect to the pin status.

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active



10.11 RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.
To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

10.12 VAUX1 power output

A regulated power supply output is provided in order to supply small devices from the module.
This output is active when the module is ON and goes OFF when the module is shut down.
The operating range characteristics of the supply are:

Operating Range – VAUX1 power supply

	Min	Typical	Max
Output voltage	2.75V	2.85V	2.95V
Output current			100mA
Output bypass capacitor (inside the module)			2.2µF

11 DAC and ADC section

11.1 DAC Converter

11.1.1 Description

The GE864-QUAD / PY module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on BGA Ball C7 of the GE864-QUAD / PY module and on pin 17 of PL102 on EVK2 Board (CS1152).
The on board DAC is a 10-bit converter, able to generate a analogue value based a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

	Min	Max	Units
Voltage range (filtered)	0	2,6	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = 2 * value / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

11.1.2 Enabling DAC

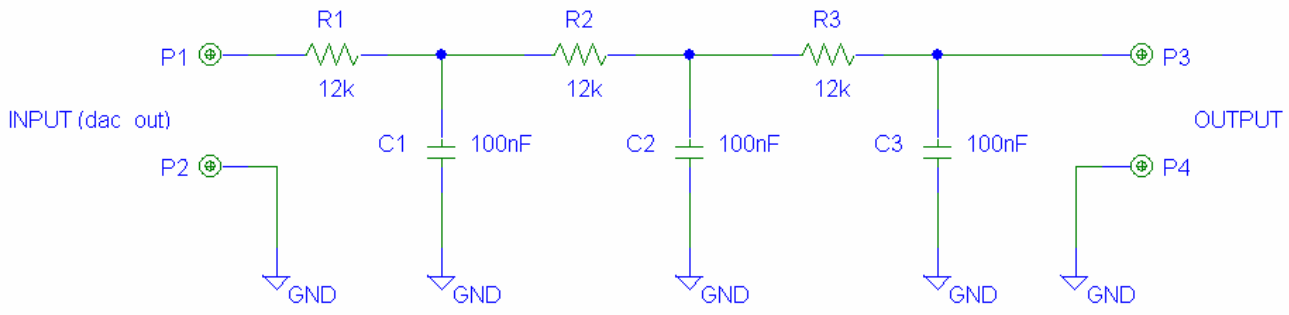
An AT command is available to use the DAC function.
The command is **AT#DAC[=<enable>[,<value>]]**

<value> - scale factor of the integrated output voltage (0..1023 – 10 bit precision)
it must be present if **<enable>=1**

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE: **The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.**

11.1.3 Low Pass Filter Example



11.2 ADC Converter

11.2.1 Description

The on board A/D are 11-bit converter. They are able to read a voltage level in the range of 0÷2 volts applied on the ADC pin input, store and convert it into 11 bit word.

	Min	Max	Units
Input Voltage range	0	2	Volt
AD conversion	-	11	bits
Resolution	-	< 1	mV

The GE864-QUAD / PY module provides 3 Analog to Digital Converters. The input lines are:

ADC_IN1 available on Ball J11 and Pin 19 of PL102 on EVK2 Board (CS1152).
ADC_IN2 available on Ball H11 and Pin 20 of PL102 on EVK2 Board (CS1152).
ADC_IN3 available on Ball G11 and Pin 21 of PL102 on EVK2 Board (CS1152).

11.2.2 Using ADC Converter

An AT command is available to use the ADC function.

The command is **AT#ADC=1,2**

The read value is expressed in mV

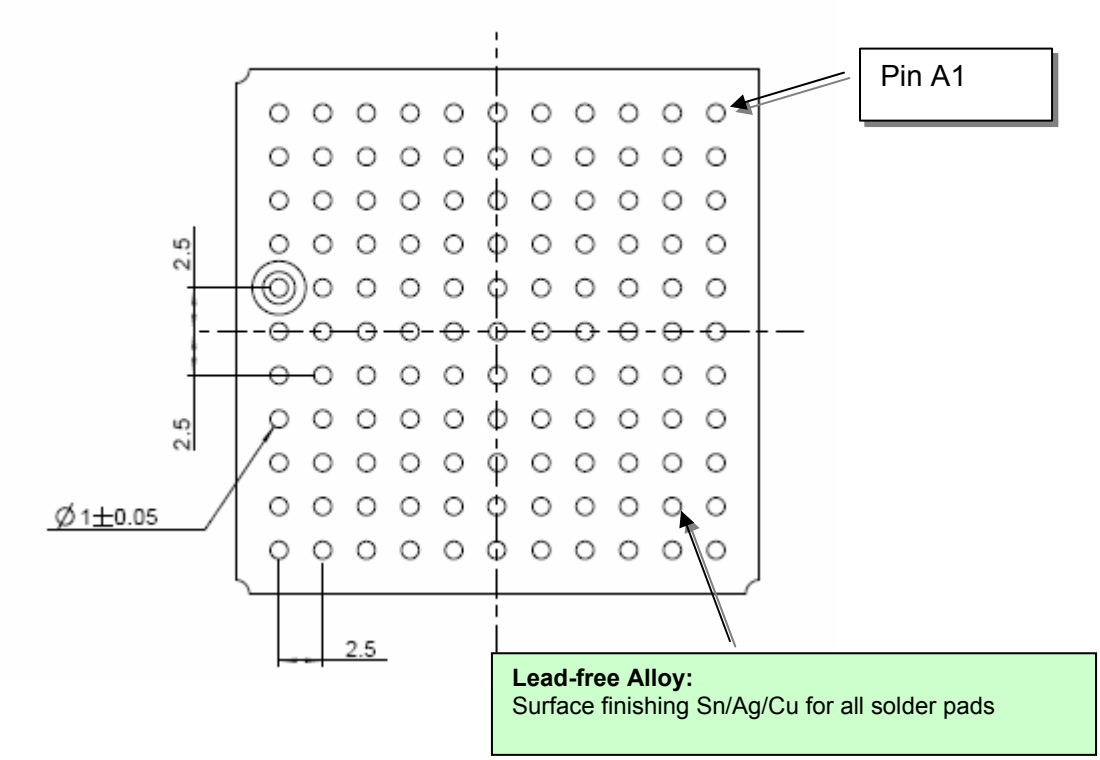
Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

12 Mounting the GE864 on your Board

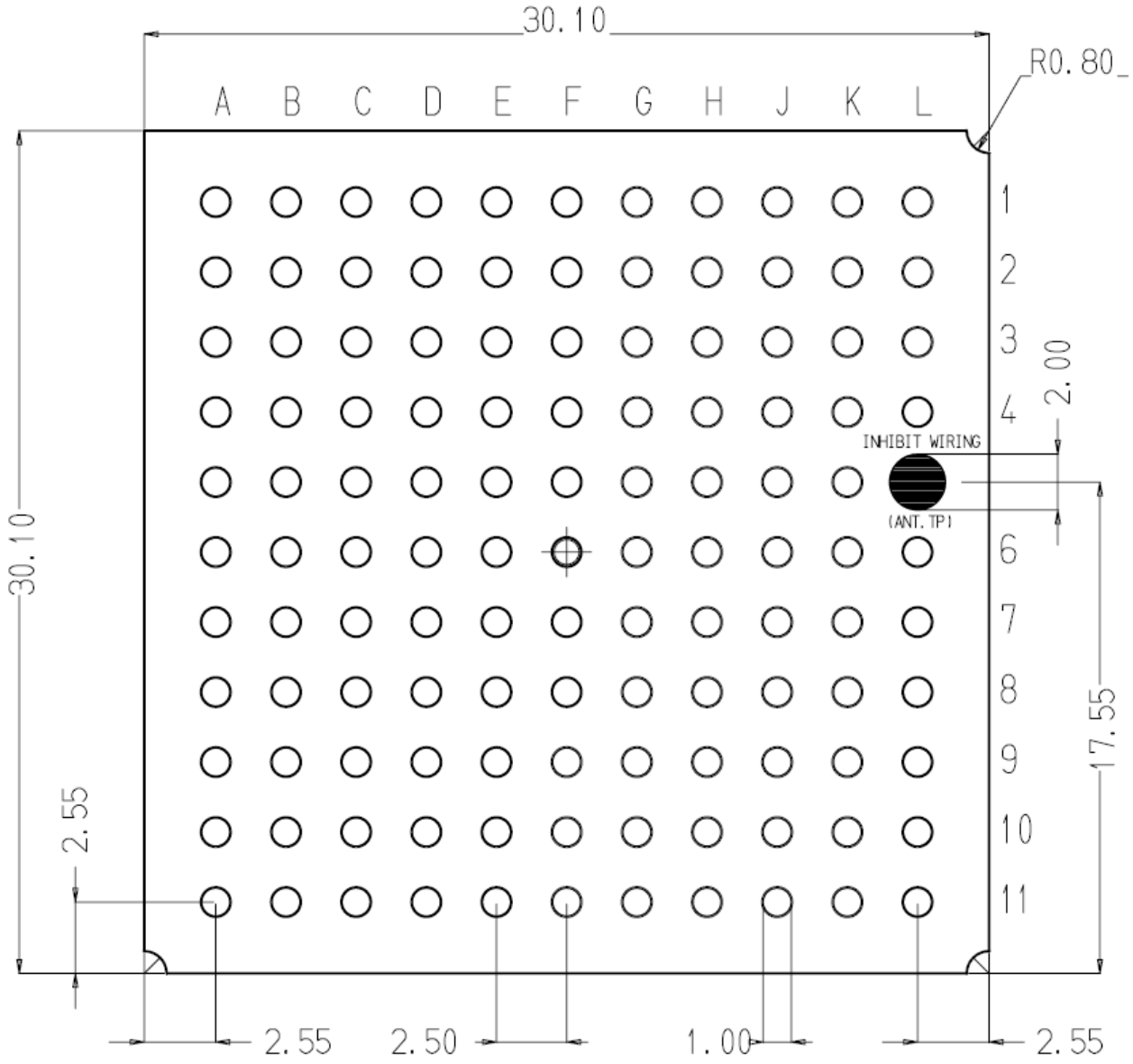
12.1 General

The **Telit GE864 modules** have been designed in order to be compliant with a standard lead-free SMT process.

12.1.1 Module finishing & dimensions



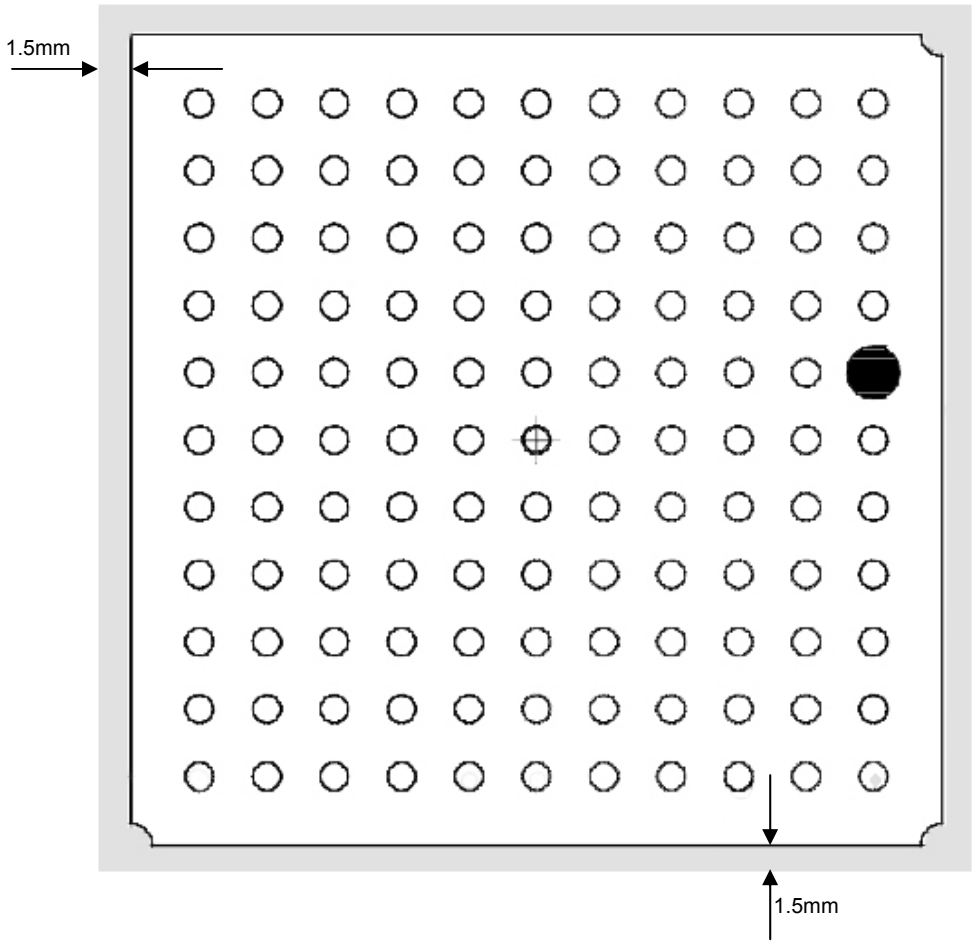
12.1.2 Recommended foot print for the application (GE864)



Top View

12.1.3 Suggested Inhibit Area

In order to easily rework the GE864 is suggested to consider on the application a 1.5mm Inhibit area around the module:



Top View

It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

12.1.4 Debug of the GE864 in production

To test and debug the mounting of the GE864, we strongly recommend to foreseen test pads on the host PCB, in order to check the connection between the GE864 itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

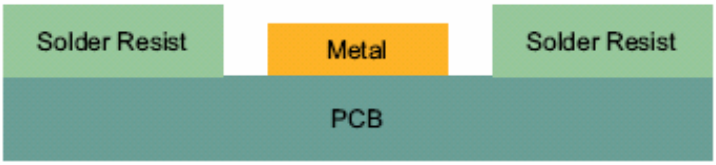
- TXD
- RXD
- ON/OFF
- RESET
- GND
- VBATT
- TX_TRACE
- RX_TRACE
- PWRMON

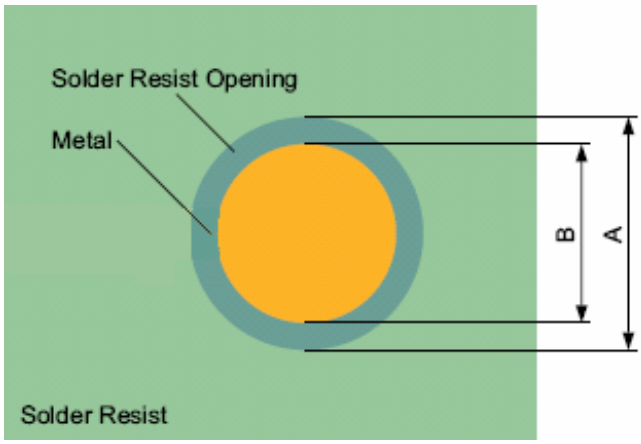
12.1.5 Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120µm.

12.1.6 PCB pad design

Non solder mask defined" (NSMD) type is recommended for the solder pads on the PCB.

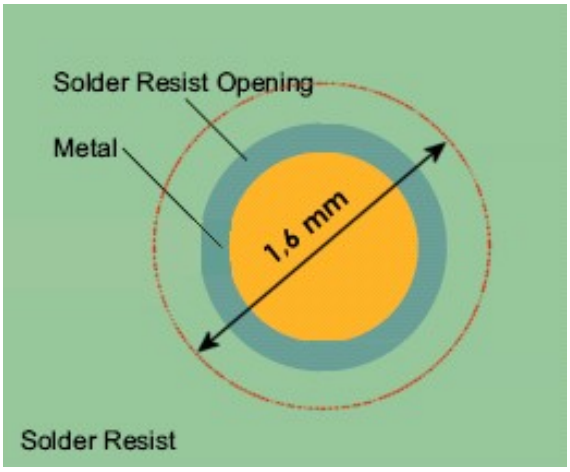




Recommendations for PCB pad dimensions

Ball pitch [mm]	2,5
Solder resist opening diameter A [mm]	1,150
Metal pad diameter B [mm]	1 ± 0.05

Placement of microvias not covered by solder resist is not recommended inside the "Solder resist opening", unless the microvia carry the same signal of the pad itself.



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

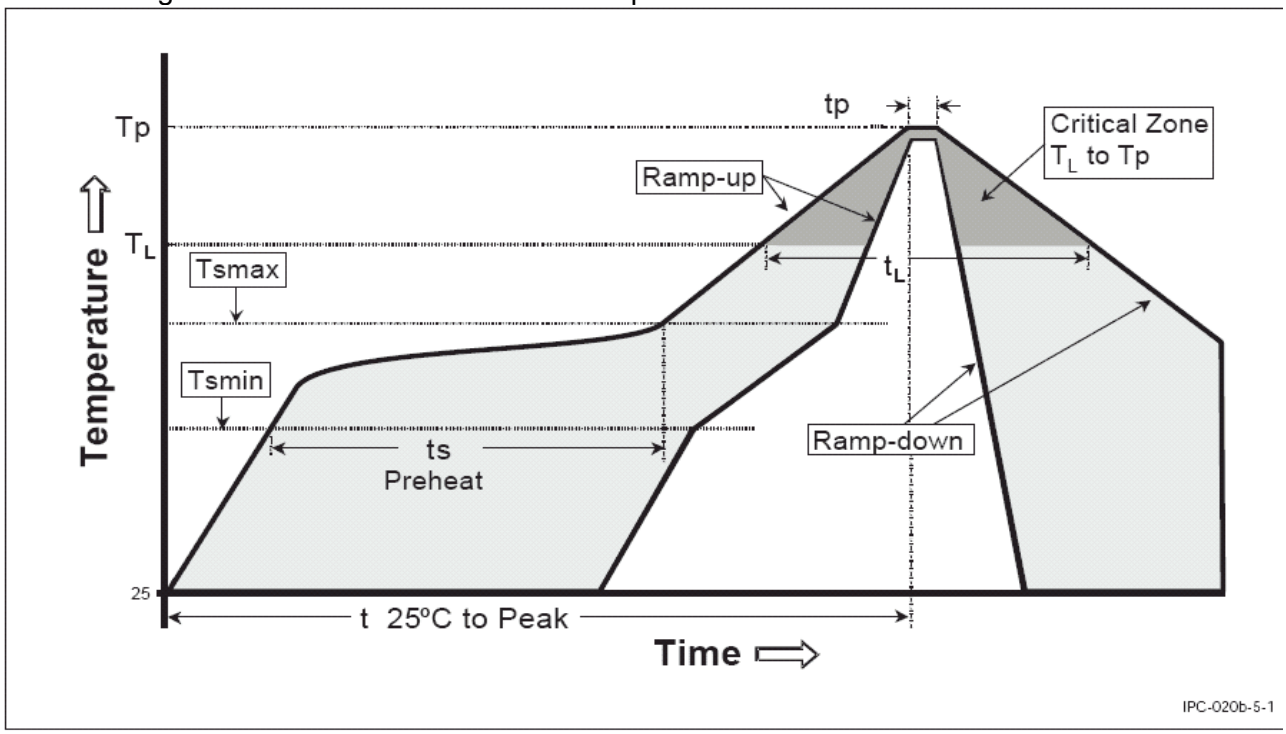
The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

12.1.7 Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

12.1.8 GE864 Solder reflow

The following is the recommended solder reflow profile



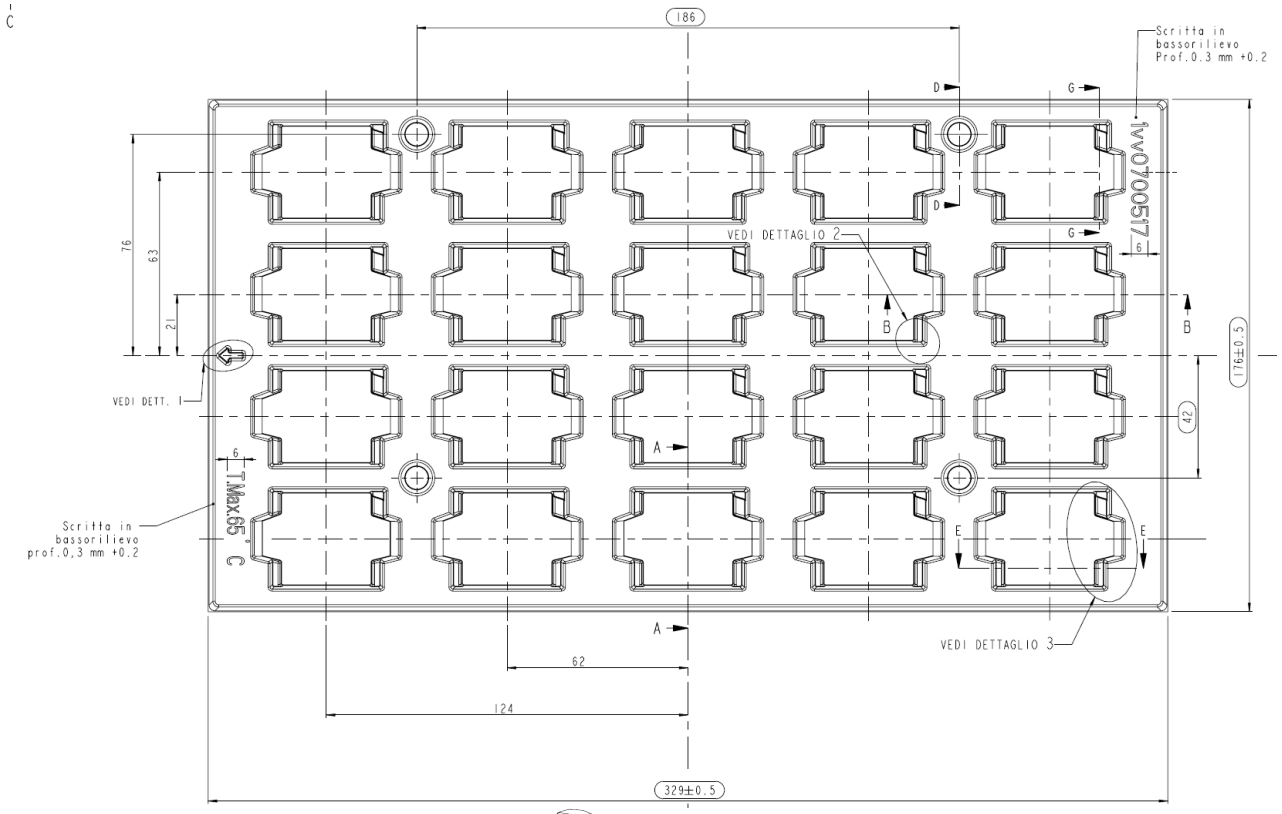
Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat 8 Temperature Min (Tsmin) 8 Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: 8 Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE: All temperatures refer to topside of the package, measured on the package body surface.

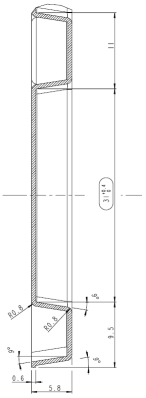
NOTE: GE864 module can accept only one reflow process

12.2 Packing system

The **Telit GE864 modules** are packaged on trays of 20 pieces each. This is especially suitable for the GE864 according to SMT processes for pick & place movement requirements.



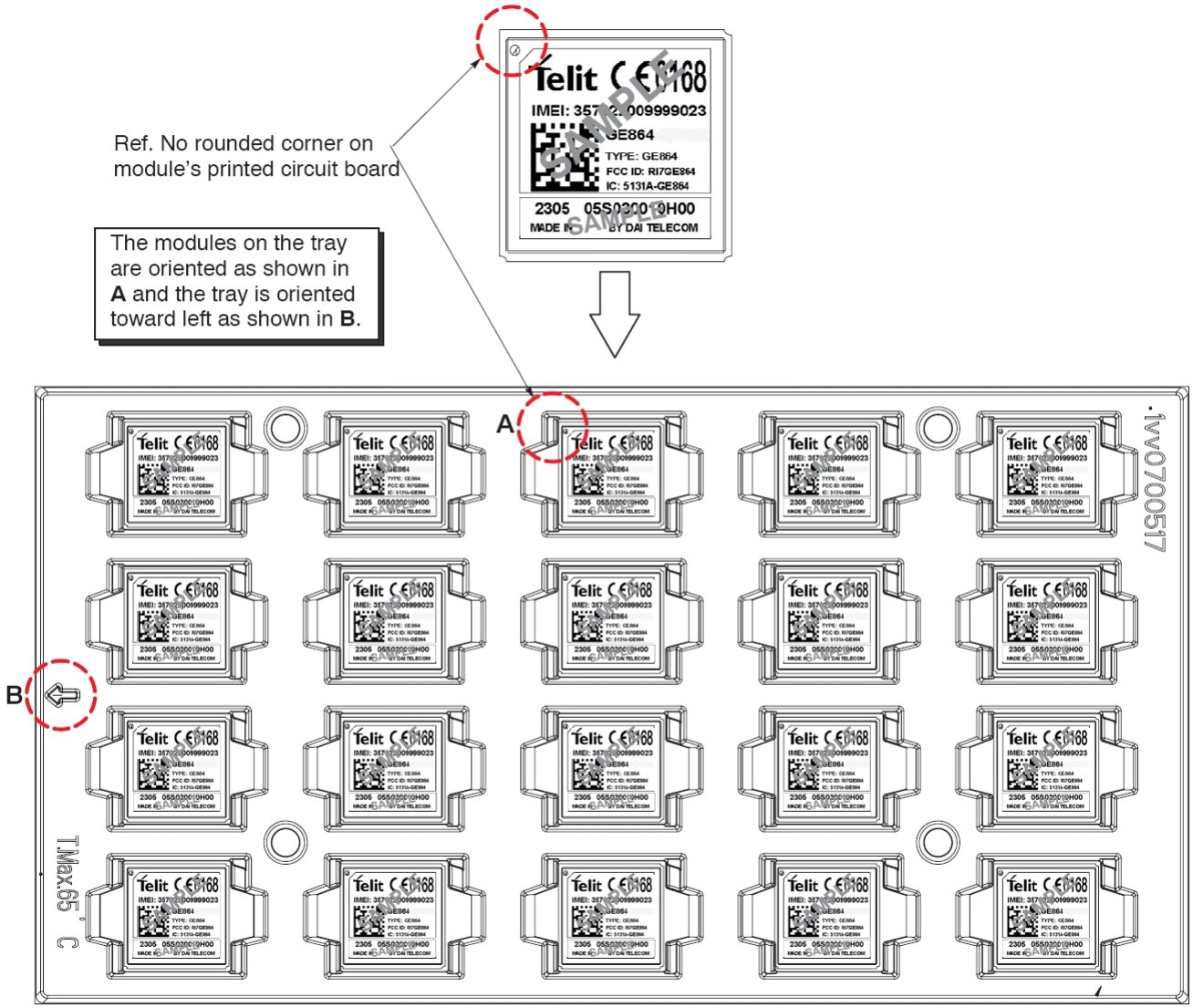
Section A-A



The size of the tray is: 329 x 176mm

NOTE: These trays can withstand at the maximum temperature of 65° C.

12.2.1 GE864 orientation on the tray



12.2.2 Moisture sensibility

The level of moisture sensibility of GE864 module is "3", in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

13 Conformity Assessment Issues

The GE864-QUAD / PY module is assessed to be conform to the R&TTE Directive as stand-alone products, so If the module is installed in conformance with Dai Telecom installation instructions require no further evaluation under Article 3.2 of the R&TTE Directive and do not require further involvement of a R&TTE Directive Notified Body for the final product.

In all other cases, or if the manufacturer of the final product is in doubt then the equipment integrating the radio module must be assessed against Article 3.2 of the R&TTE Directive**.**
In all cases assessment of the final product must be made against the Essential requirements of the R&TTE Directive Articles 3.1(a) and (b), safety and EMC respectively, and any relevant Article 3.3 requirements.

The GE864-QUAD / PY module is conform with the following European Union Directives:

- R&TTE Directive 1999/5/EC (Radio Equipment & Telecommunications Terminal Equipments)
- Low Voltage Directive 73/23/EEC and product safety
- Directive 89/336/EEC for conformity for EMC

  In order to satisfy the essential requisite of the R&TTE 99/5/EC directive, the GE864-QUAD / PY module is compliant with the following standards:
- GSM (Radio Spectrum). Standard: EN 301 511 and 3GPP 51.010-1
- EMC (Electromagnetic Compatibility). Standards: EN 301 489-1 and EN 301 489-7
- LVD (Low Voltage Directive) Standards: EN 60 950

In this document and the Hardware User Guide, Software User Guide all the information you may need for developing a product meeting the R&TTE Directive is included.

The GE864-QUAD / PY module is conform with the following US Directives:

- Use of RF Spectrum. Standards: FCC 47 Part 24 (GSM 1900)
- EMC (Electromagnetic Compatibility). Standards: FCC47 Part 15

To meet the FCC's RF exposure rules and regulations:

- The system antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all the persons and must not be co-located or operating in conjunction with any other antenna or transmitter.
- The system antenna(s) used for this module must not exceed 3 dBi for mobile and fixed or mobile operating configurations.
- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.

14 SAFETY RECOMMANDATIONS

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
- Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm

15 Document Change Log

Revision	Date	Changes
ISSUE#0	12/06/06	Release First ISSUE# 0
ISSUE #1	22/11/05	Added notice on page 4.
ISSUE #2	19/12/05	Added Paragr.10 Conformity Assessment Issues
ISSUE #3	07/02/06	Added products order codes table Added Disclaimer Added Safety Recommendations
ISSUE #4	07/09/06	Full Review of the manual Added ADC description Added DAC description Added Pin out and Process flow description Added Packaging
ISSUE #5	03/10/06	TGPIO23 now RESERVED; modified low pass filter example for DAC, 6.1 antenna characteristics
ISSUE #6	23/10/06	Updated “GE864 orientation on the tray” layout.
ISSUE #7	08/02/07	Pin out updated, Camera removed, Added Stat Led and GPIO5 description, added VAUX1, schematics updated for ON_OFF, reset, level adapter 5V, RS232 transceiver, Power supply. Modified Charger description.
ISSUE #8	07/06/07	Updated DISCLAIMER, Added note on charger (CFUN4 and ON_OFF), Added Power consumptions table, Added new table for GPIO status in Reset and Power on, added RFTXMON timing, Switching description modified in “+ 12V input Source Power Supply Design Guidelines”, Added Alternate Function for GPIO4, Added BGA balls mechanical drawing.
ISSUE #9	19/06/07	Modified absolute maximum ratings; added GPIO2 Alternate function description
ISSUE #10	10/06/08	Par 02: Updated Mechanical drawings Par 3.1: Removed nominal values on Audio, added DVI description Par 5.1: Added Supply Voltage Range Par 11.7: GPIO7 description; added section on Buzzer description Par 9: Audio section removed (a dedicated User guide on audio has been created) Par 5.2.1.4: added note on Charger Par 8.1: tip on RXD pull up added EVK chapter removed