HD74AC182

Carry Lookahead Generator

REJ03D0258–0200Z
(Previous ADE-205-378 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC182 is a high-speed carry lookahead generator. It is generally used with the HD74AC181 or HD74AC381 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

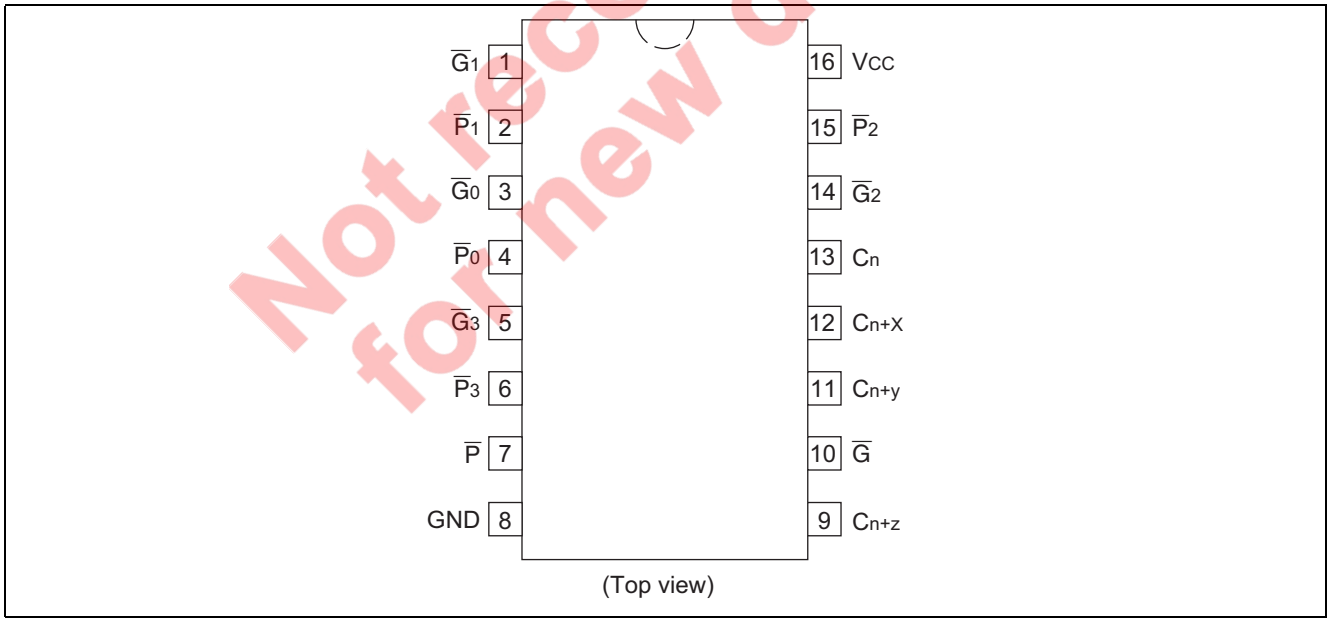
Features

- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC182FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC182RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

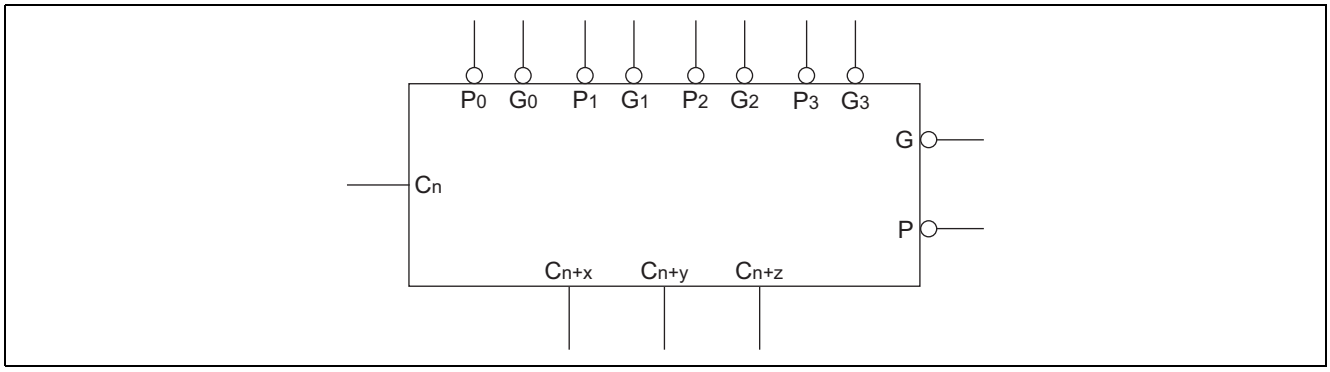
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



(Top view)

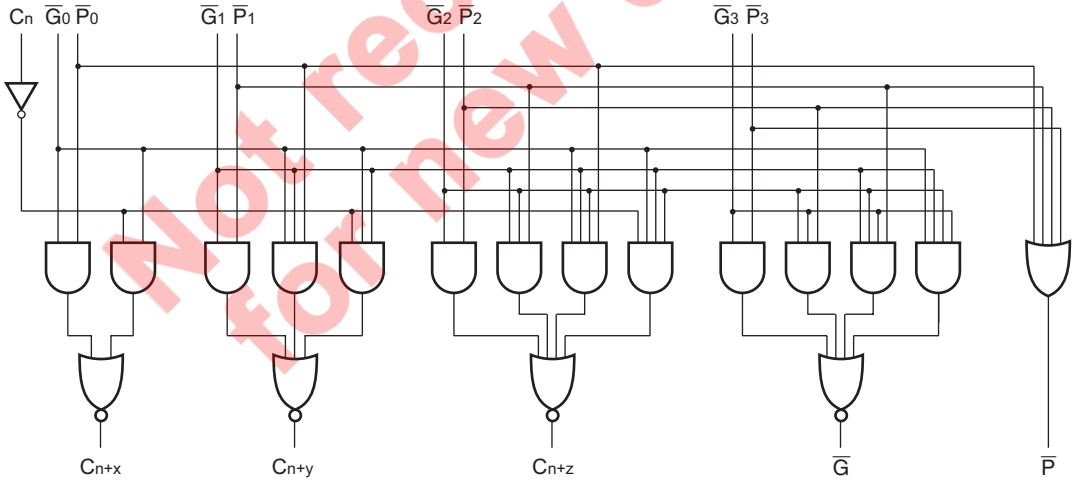
Logic Symbol



Pin Names

Cn	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active Low)
$\overline{G}_1$	Carry Generate Input (Active Low)
$\overline{G}_3$	Carry Generate Input (Active Low)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active Low)
$\overline{P}_2$	Carry Propagate Input (Active Low)
$\overline{P}_3$	Carry Propagate Input (Active Low)
C_{n+x} to C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active Low)
$\overline{P}$	Carry Propagate Output (Active Low)

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The HD74AC182/HD74ACT182 carry lookahead generator accepts up to four pairs of Active Low Carry Propagate ($\overline{P}_0$ to $\overline{P}_3$) and Carry Generate ($\overline{G}_0$ to $\overline{G}_3$) signals and an Active High Carry input (Cn) and provides anticipated Active High carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The HD74AC182/HD74ACT182 also has Active Low Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further level of lookahead. The logic equations provided at the outputs are:

$C_{n+x} = G_0 + P_0C_n$
$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$
$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$
$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$
$\overline{P} = \overline{P_3P_2P_1P_0}$

Also, the HD74AC182/HD74ACT182 can be used with binary ALUs in an active Low or active High input operand mode. The connections (Figure a) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last HD74AC182/HD74ACT182.

Truth Table

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H : High Voltage Level
L : Low Voltage Level
X : Immaterial

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay P_n to P	t_{PLH}	3.3	1.0	8.0	10.5	1.0	11.5	ns
		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay P_n to P	t_{PHL}	3.3	1.0	8.0	10.5	1.0	11.5	ns
		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay C_n to $C_{n+x, y, z}$	t_{PLH}	3.3	1.0	9.5	12.0	1.0	13.0	ns
		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay C_n to $C_{n+x, y, z}$	t_{PHL}	3.3	1.0	9.0	12.0	1.0	13.0	ns
		5.0	1.0	7.0	10.0	1.0	11.0	
Propagation delay P_n or G_n to $C_{n+x, y, z}$	t_{PLH}	3.3	1.0	10.5	13.0	1.0	14.0	ns
		5.0	1.0	8.0	10.5	1.0	11.5	
Propagation delay P_n or G_n to $C_{n+x, y, z}$	t_{PHL}	3.3	1.0	11.5	14.0	1.0	15.5	ns
		5.0	1.0	9.0	11.5	1.0	12.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

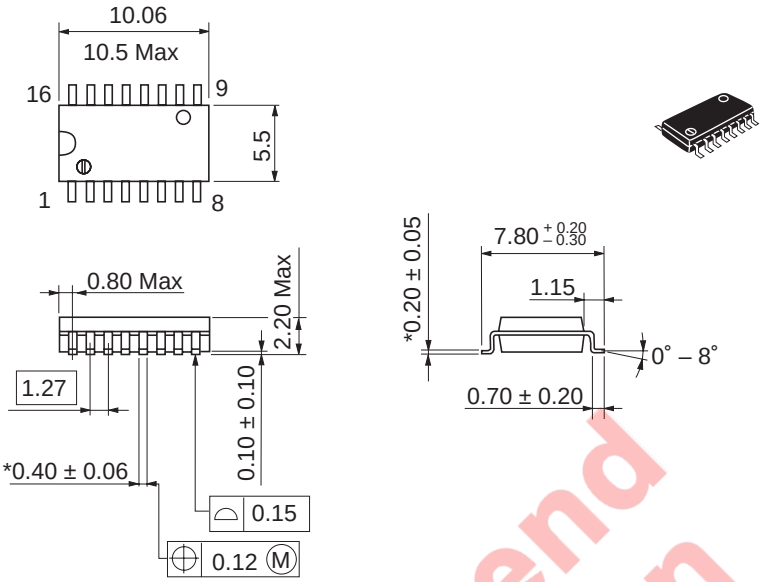
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	50.0	pF	V_{CC} = 5.0 V

Package Dimensions

As of January, 2003

Unit: mm

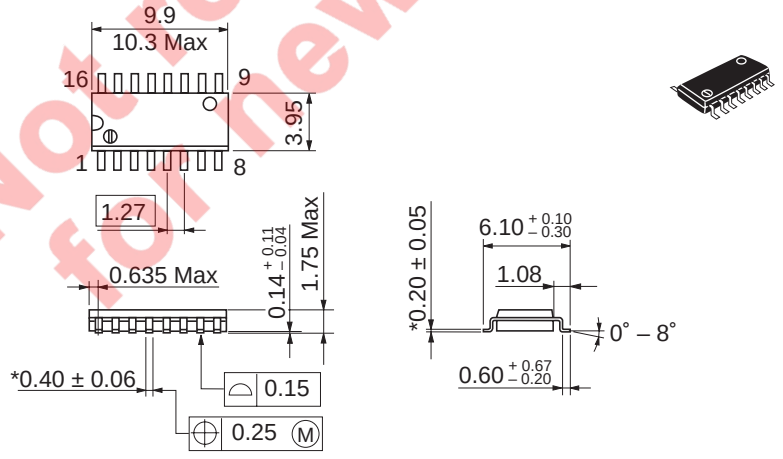


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

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